ABSTRACT

Title of Dissertation: DESIGN AND FABRICATION OF ON CHIP MICROWAVE PULSE POWER DETECTORS

Woochul Jeon, Doctor of Philosophy, 2005

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On-chip microwave pulse-power detectors are promising devices for many electrical systems of both military and commercial applications. Most research in microwave power detector design have been focused on thermal power detectors, such as thermistors or thermocouples, due to their wide dynamic range and high frequency operation. However, due to their slow thermal response time, it is impossible to detect microwave pulses with a few micro or sub-micro seconds of pulse width. Schottky diode power detectors are the best candidates for this purpose due to their fast pulse response time and small size.

We have developed a means for fabricating Schottky diodes as part of any Complementary-Metal-Oxide-Semiconductor (CMOS) process by modifying the layout file. CMOS Schottky diodes were added at pre-selected locations through a CMOS process. We have also developed a process for adding or deleting Schottky diodes on a CMOS fabricated chip by using Focused Ion Beam (FIB). FIB milling and ion induced deposition were used for adding or deleting Schottky diodes at any desired location on a CMOS-fabricated chip as a post-CMOS process. Spice models

of CMOS Schottky diodes were developed and used for designing the RF front end circuits in passive RF circuits. MOSFET based RF pulsed power detector circuits were also designed and fabricated.

Fabricated power detectors were tested under direct injection and radiation of microwave pulse signals. Measured results for fabricated CMOS Schottky diodes, FIB Schottky diodes and MOSFET half-wave and full-wave rectifier circuits are summarized in a table with the pulse response time, the dynamic range, the sensitivity, and the frequency response to determine which power detector is the best choice for detecting a specific source signal.

DESIGN AND FABRICATION OF ON CHIP MICROWAVE PULSE POWER DETECTORS

By

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Dissertation submitted to the Faculty of the Graduate School of the
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Preface

The thesis consists of eight chapters. Chapter 1 gives an introduction to the research. Chapter 2 presents basic operations of power detectors. Chapter 3 – 5 present the fabricated power detectors and measured results. Chapter 6 and 7 illustrate some applications of developed power detectors. Chapter 8 summarizes the thesis. Even though a number of details have been added in this thesis, the basic ideas presented in chapters 4 - 7 have been published earlier, which are in the following list.

Chapter 3 and Chapter 6.1:
W. Jeon, T. Firestone, J. Rodgers, and J. Melngailis, "Design and fabrication of Schottky diode, on-chip RF power detector", Proc., 2003 ISDRS, pp. 294-295, Washington DC, Dec. 2003
W. Jeon, T. Firestone, J. Rodgers, and J. Melngailis, "Design and fabrication of Schottky diode, on-chip RF power detector", Solid state electronics, Vol. 48, Iss. 10-11, pp. 2089-2093, Oct 2004

Chapter 4.2:
W. Jeon, T. Firestone, J. Rodgers, J. Melngailis, "On-chip RF pulse power detector using FIB as a post-CMOS fabrication process", Journal of Electromagnetics, in press

Chapter 4.2 and Chapter 6.2:
W. Jeon, T. Firestone, J. Rodgers, J. Melngailis, "CMOS/post-CMOS fabrication of on-chip Schottky diode microwave pulse power detectors", Proc., DET&E conference, Albuquerque, New Mexico, Aug. 2005

Chapter 5.1:
W. Jeon and J. Melngailis, "CMOS & Post CMOS Fabrication of on Chip Microwave Pulse Power Detectors", Proc., ISAP2005, Vol. 1, pp 221-224, Seoul, Korea, Aug. 2005

Chapter 5.2:
W. Jeon and J. Melngailis, "CMOS&post CMOS on-chip microwave pulse power detectors", 2005 ISDRS, Washington DC, Dec. 2005, Accepted

Chapter 7:
W. Jeon, J. Melngailis, and R. W. Newcomb, "CMOS passive RFID transponder with read-only memory for low cost fabrication", Proc., IEEE SOCC 05, pp. 181-184, Washington DC, Sept. 2005
W. Jeon, J. Melngailis, and R. W. Newcomb, "CMOS foundry Schottky diode microwave power detector fabrication, Spice modeling, and application", IEEE Intl. Work. Electronic Design, Test, & Applications (DELTA 2006), Jan. 2006, Accepted

Dedication

To my loving daughter Ellena, my wife Yonghyun, my parents-in-law,

and my parents.

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I also appreciate the Department of Defense MURI 2001 Program for supporting my research and my growing family. In addition I wish to thank Professor Victor Granatstein and Dr. John Rodgers for many useful discussions. I am also grateful to John Barry, Tony DeMarco, and Todd Firestone for being friends and helping me with fabrication and measurement.

My wife, Yonghyun Cho, my parents, Sangyong Jeon and Haeja Lee, and my parents-in-law, Gwanghee Cho and Byungsoon Lee, have been always supportive of me in everything I did. Without their love and never-ending support, I could not have finished my graduate studies. Special thanks to my daughter, Ellena, who makes me laugh at any given moment.

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Chapter 1: Introduction

Modern electronic systems are increasingly vulnerable to malfunction due to incident electromagnetic radiation, particularly since many integrated circuits operate at lower and lower voltages. The damaging RF radiation can be intentional, namely produced by high power microwave (HPM) weapons [1], or it can be due to ambient sources, such as lightning.

How, and at what level, microwaves penetrate equipment shielding and reach the vulnerable chips is of increasing interest. This motivates our project to build on-chip RF pulse power detectors both for measuring power at the chip level and at the board level and for developing strategies to mitigate its effects. Knowing the RF power levels in various chips and in various locations within chips is likely to be more useful than the "binary" information that a given external RF power level made the circuits fail.

Ideally the on-chip power detectors would have a wide dynamic range, and be fabricated in a standard CMOS process. For this purpose, several power detectors on silicon substrate have been reported, though most of them were not intended to be inserted directly on a chip. Power detectors usually used are thermistors, thermocouples, and diodes. The thermistor is used as a thermometric element and measures the temperature increase of a load, which is placed nearby and absorbs the injected RF power [2]. The thermocouples are based on the Seebeck effect, a voltage appears due to temperature gradient between two junctions in a closed circuit of two different metals, and used to measure the temperature increase of a load [2, 3]. Diodes are used to convert a high frequency signal to DC signal by rectifying the input signal.

Especially, Schottky diodes are known as fast rectifying devices and can be used as RF power detectors [4]. Because Schottky diodes have the fastest response time to a pulse input, Schottky diodes are exclusively used for RF pulse measurements. In the preliminary experiments, Schottky diodes for RF detection have been designed and built using both fabrication steps compatible with CMOS processes and post-fabrication focused ion beam (FIB) milling and deposition steps [5]. Because CMOS process is not specified for a Schottky contact, a modification of a CMOS process is required. As an alternate method, MOSFET diodes with bias circuit can be used for RF power detection for a low frequency range up to 5GHz. And, as a post-CMOS process, the use of FIB for fabricating Schottky diodes at any location of interest on a CMOS-fabricated chip is demonstrated. As an application of the suggested CMOS Schottky diodes, a charge pump circuit with CMOS Schottky diodes was designed and used in an RFID transponder.

The objectives of my thesis is design and fabrication of Schottky diode and MOSFET circuit on-chip microwave pulse power detectors by using both CMOS and post-CMOS process. We have developed a process for fabricating Schottky diodes in any CMOS process by modifying the layout file and a process for adding or deleting Schottky diodes on a CMOS-fabricated chip by using FIB. CMOS Schottky diodes are essential components for designing an RF passive integrated circuit. MOSFET based RF pulsed power detector circuits for detecting short microwave pulse with less than 100ns pulse width were designed and fabricated. Little work has been done on fabricating Schottky diode on silicon or on using MOSFET diodes for making on-chip power detectors. The use of FIB as a post-CMOS process to fabricate Schottky

diode power detectors has not been reported yet. The CMOS Schottky diodes were modelled by using Spice. The calculated I-V curves agreed with the measured DC I-V curves. The measured result and model of CMOS Schottky diodes would be helpful to reduce the effort for designing the RF front end circuits in passive RF circuits.

Chapter 2: Power detectors

Thermistors, Thermocouples, and Diodes are typically used as power detectors. Both thermistors and thermocouples use the fact that the incident microwave changes the characteristics of specific materials by increasing the temperature of the materials. Diodes directly rectify the incident microwave to a half-wave signal. By filtering the rectified signal with a low pass filter and measuring the DC output, the incident power level is measured. Since diodes are of the main interest in my thesis, other two methods will be examined briefly.

2.1 Thermistors

Thermistors are made from semiconductors, metallic oxides, or metals [6]. The electrical resistance of the thermistor varies with the incident power by the Joule

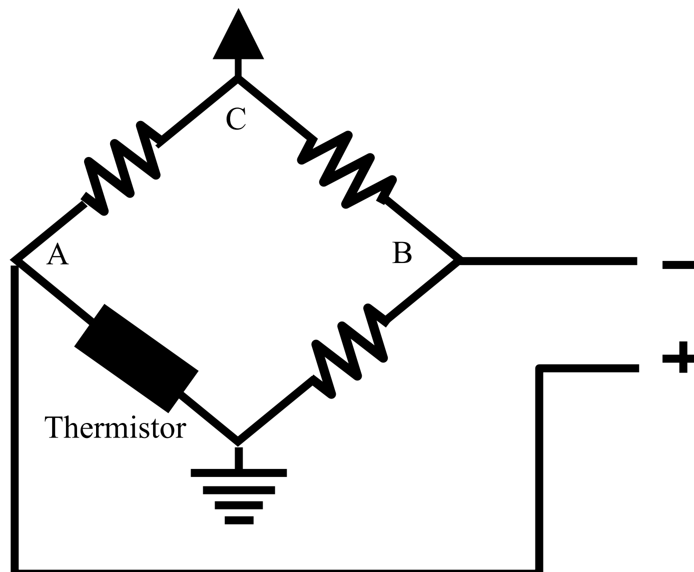


Figure 2.1: Power detector with a Balanced Wheatstone bridge consists of a thermistor and three identical resistors

effect. The Wheatstone bridge structure is used to measure the resistance change and hence the incident power. (Figure 2.1) Once RF power is injected to a thermistor, the resistance of the thermistor becomes lower and the voltage difference between the node A and the node B changes. A differential amplifier detects and amplifies the voltage difference and sends current to the node C for maintaining thermistor resistance to 50Ω for matching to RF source. By measuring the current output of a differential amplifier, the injected power level can be known. Typical operation range of thermistor power detector is between –20dBm and 10dBm [2]. Kopystynski et al. [6] fabricated and measured a wide band width (dc to 26GHz) power detector, which had a laser-trimmed 50Ω nichrome resistor as a thermal resistor. The dynamic range of their sensor was from -10dBm to 20dBm.

2.2 Thermocouples

Thermocouple power detectors are based on the fact that dissimilar metals generate a voltage due to temperature difference at a hot and cold junction of the two metals. The RF power injected to both hot junctions of thermocouples generates potential difference from hot and cold junctions. (Figure 2.2)

Various types of thermocouple power detectors on silicon or other substrate materials have been suggested. The input power levels of these thermocouple power detectors are between –30dBm to 20dBm and can be extended by using an attenuator [2]. Jaeggi et al [7] used CMOS polysilicon and aluminum junction as a thermocouple and their detector worked between –30dBm and 10dBm at the frequency of up to 400MHz. Haberli et al. [8] used CMOS compatible process to fabricate a power detector with an A/D converter, and its dynamic range was –30dBm to 10dBm.

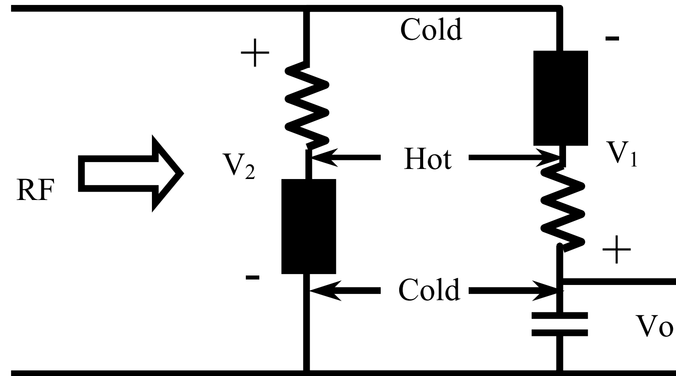


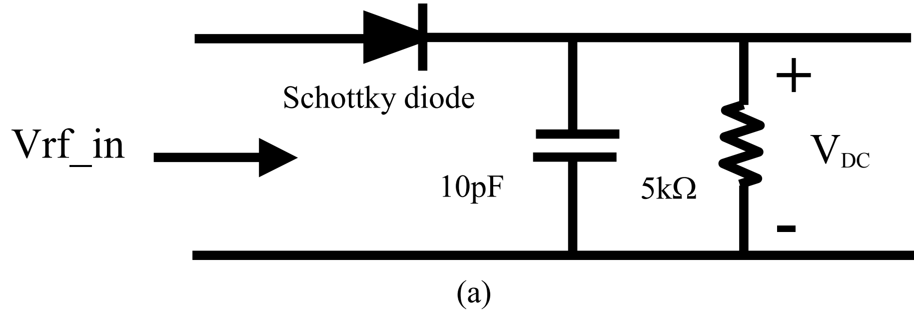
Figure 2.2: The Power detector with thermocouples. Vo = $V_1 + V_2$ Each thermo-couple consists of two different metals. (For example, Aluminum and poly silicon in CMOS process [13])

Kodato et al. [9] fabricated two thermal power sensors with Bi-Sb thermocouple. They operated in the power level of between –30dBm and15dBm and –20dBm and 20dBm at the frequency of up to 40GHz and 65GHz. The response time was 3ms and 40ms, respectively. Milanovic [10, 11, 12, 13] designed and tested a thermocouple microwave power detector fabricated through an n-well CMOS foundry with an additional etching process. They used polysilicon and metal as a thermocouple. Their detector detected the input power from –30dBm to 10dBm in the frequency range from 50MHz to 20GHz. And they improved their sensor to extend the frequency range up to 50GHz. [14, 15].

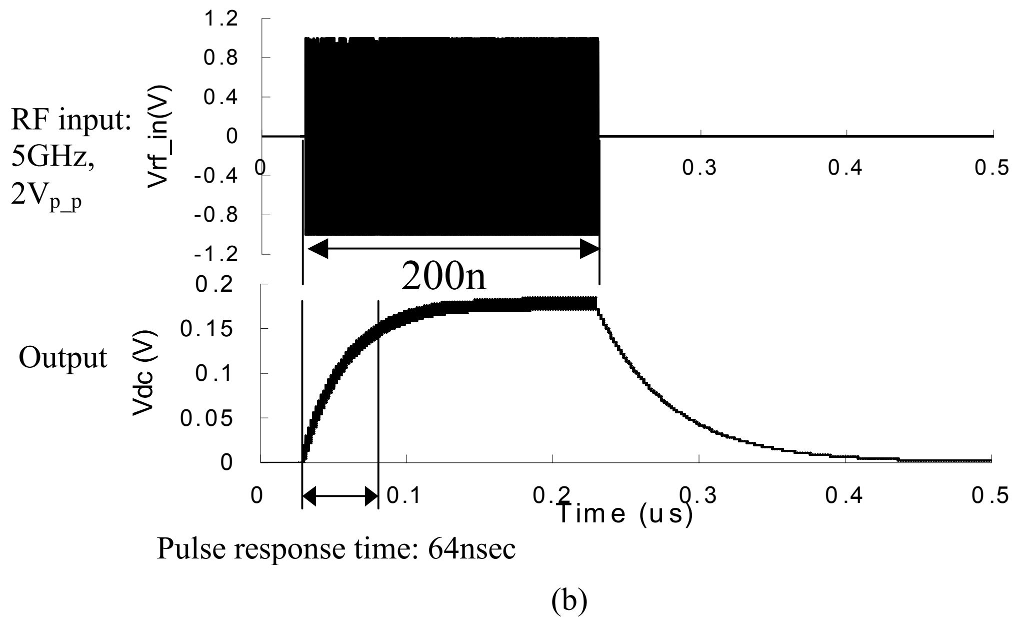
2.3 Diodes

Diodes, which have been used for signal level detection for a century, convert RF signals to DC signals by rectifying input signal. A diode rectifier circuit consists of a rectifying diode, a filter capacitor, and a resistor. (Figure 2.3) The diode rectifies the

incident RF signal, and the capacitor and the resistor produce a DC output by filtering out the high frequency part of the rectified signal.



(a)



(b)

Figure 2.3: (a) Power detector with a Schottky diode. RF input is rectified by the Schottky diode and stored in the capacitor. (b) RF pulse input is filtered to low frequency signal. (Schottky diode model: turn on voltage: 0.2V, series resistance: 214Ω, junction capacitance: 16fF)

For a small input voltage, the series resistance can be ignored because the junction resistance is much bigger than the series resistance. And, mathematically, if we assume the therminoic emission is dominant among the carrier transport mechanisms, a diode obeys the following diode equation.

$$I = I_s(e^{\frac{q}{nkT}V} - 1) \qquad (2.1)$$

This equation can be written as a power series for the better analysis of rectifying action.

$$I = Is\left(\frac{q}{nkT}V + \frac{\left(\frac{q}{nkT}V\right)^2}{2!} + \frac{\left(\frac{q}{nkT}V\right)^3}{3!} + ...\right) \qquad (2.2)$$

The second and other even-order terms of this series provide the rectification because negative voltage input becomes positive component in this series. The second order term is the most significant in a small signal operation and dc output is proportional to the square of power level, the diode is said to be operating in the square law region [2]. If the input signal becomes larger, the third term and higher terms become significant and the series resistance cannot be ignored, the diode is no longer in the square law operation region and moves into the linear region where the output voltage is proportional to the input voltage. (Figure 2.4) A typically biased Schottky diode has the square law region of between –70dBm to –20dBm, the transition region of between -20dBm to 0dBm, and the linear region of above 0dBm in a 50Ω matching

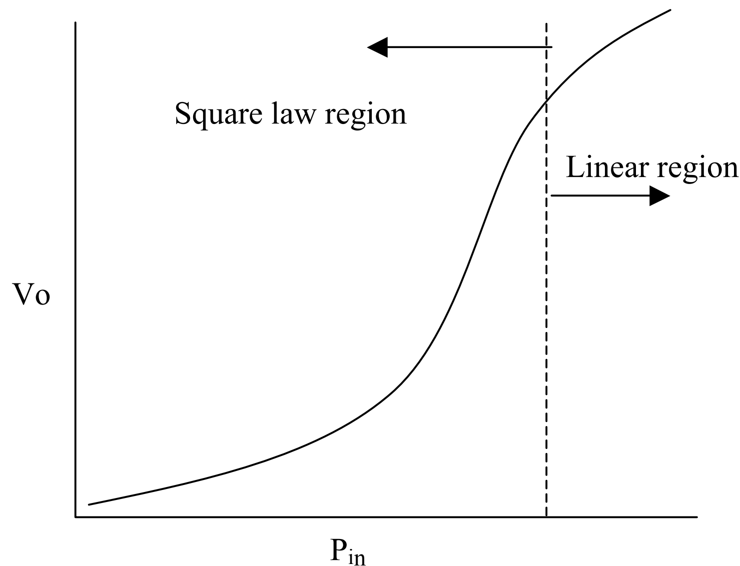


Figure 2.4: DC output vs. Power input curve of a diode.

system. The square law region can be extended up to 20dBm by using an attenuator, the linear compensation, molecular beam exptaxy (MBE), or Gallium-Arsenide (GaAs) semiconductor material technology [2]. Attenuators and calibrators are usually made by using digital signal processing circuitry.

Any type of diode can be used for power detection. The pn junction diode would be a sensitive RF detector. However, for the high frequency operation, minimizing the junction capacitance and the series resistance is required, and the bandwidth of the pn junction diode is limited due to the stored charge effects. Schottky diodes do not store charge in the junction and can be used for high frequency applications, and the low potential barrier across the junction increase the sensitivity of the Schottky diode power detector.

2.4 Microwave pulse power detectors

The most important parameters characterizing microwave pulse detectors in circuits are the pulse response time, operating frequency, and sensitivity. The frequency range of interest in HPM source is from 1GHz to 10GHz and the pulse durations are from 10’s to 100ns [16]. For detecting HPM source with 100ns of pulse width, the pulse response time of pulse power detector should be shorter than 100ns. Thermocouples, thermistors, and Schottky diodes, which can be fabricated on a standard CMOS process, have been used for RF power measurement due to their wide dynamic range [2]. Thermocouple power detectors have better performance than thermistors and due to their accuracy, broadband operation, and high dynamic range, they are usually used for power measuring instruments. Even though micron-size wires could have sub-microsecond thermal time constants, and superconducting

bolometers can be very fast, the fabrication would be expensive and it would be difficult to fabricate them directly on a silicon chip. Since both thermocouples and thermistors made by a typical fabrication process such as CMOS process have at least a few milliseconds of thermal time constant due to the heating and cooling of the sensing elements [2], they are not useful for RF pulse detection. Schottky diodes have much faster response, a few μs or less, and are the most promising devices for the RF pulse detection [4]. From the simulation result in Figure 2.3, the pulse response time of a Schottky diode is 64ns, which means any microwave pulse with more than 64ns of pulse width can be efficiently detected. Table 1.1 summarized the characteristics of three types of power detectors.

	Oprating frqeucncy	Dynamic Range	Pulse Response time
Thermistors	Almost no limit	-20dBm to 10dBm	1-10 ms
Thermocouple		-30dBm to 20dBm	1-10 ms
Diodes	Up to 100GHz	-70dBm to –20dBm	**0.1-10 μs**

Table 1.1. Comparison of three types of power detectors.

2.5 Schottky diode power detectors

In 1874 Karl Ferdinand Braun discovered one-way conduction in metal sulfide crystals and created the cat's whisker diode as the first step of Schottky diode [17]. L.O. Grondahl and P.H. Geiger found rectifying properties in a semiconducting copper oxide-copper junction in 1926 [18] and Dr. Walter Schottky published his diffusion theory of current transport in metal-semiconductor junctions in 1938 [19]. After his theoretical explanation, many researchers have used Schottky barrier diodes

for various applications and Siemens had begun commercially manufacturing Schottky diodes for microwave use.

Microwave power detection is one of the most popular microwave applications of Schottky diodes, since Schottky diodes are majority carrier devices and their junction capacitors can be small enough to be used for microwave rectification. Either GaAs [20] or Si [21, 22, 23] Schottky diodes are usually used for the RF power detection. GaAs Schottky diodes operating in THz region have been reported [20]. Ideally the chip power detectors would be fabricated in a standard CMOS process, and GaAs Schottky diodes do not fulfill to this purpose. Silicon Schottky diodes are known as fast rectifying devices and can be used as RF power detectors [4]. In special Molecular Beam Epitaxy (MBE) grown geometries, RF detection up to 100GHz has been reported [23, 24, 25]. However in CMOS-foundry-fabricated diodes detection of only up to 600MHz has been reported [23, 26].

To increase this cut off frequency, we needed to examine the key factors to limit high frequency region operation. From the equivalent lumped-element circuit model of a Schottky diode (Figure 2.5), a Schottky diode obeys the same expressions as a pn

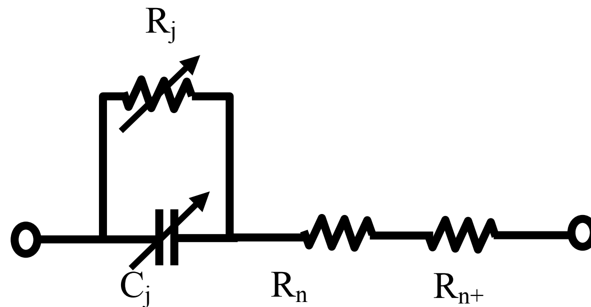


Figure 2.5: Equivalent lumped-element circuit of a Schottky diode. R_n is series resistance in n layer, R_j is the junction resistance, C_j is the junction capacitance, and R_{n+} is the series resistance in n+ layer. For low voltage input, R_j is much bigger than $(R_n + R_{n+})$. For high voltage region, the series resistance is dominant due to the small junction resistance.

junction diode. The junction capacitance, the junction resistance, and series resistances are given as [4] equation (2.3), (2.4), and (2.5).

$$C_j = A\sqrt{\frac{\varepsilon q N_d}{2(V_a + V_d)}} \qquad (2.3)$$

$$\frac{1}{R_j} = \frac{dI_x}{dV_a} = AI_s \frac{q}{nkT}\exp\left(\frac{qV_a}{nkT}\right) \qquad (2.4)$$

$$R_{series} = R_n + R_{n+} = R_o / A + R_1 / \sqrt{A} \qquad (2.5)$$

Where A is the contact area, Nd is the doping concentration, Va is an applied voltage, Vd is the built in voltage, R_o and R_1 is constant. Equation (2.5) is derived from the planar diode equation, which is introduced in the next section. Series resistance includes spreading resistance term due to the geometry of the buried layer, which is proportional to $1/\sqrt{A}$. From equations (2.3) and (2.5), the cut-off frequency, $1/(R_{series}+R_j)C$, of a Schottky diode is proportional to $1/\sqrt{A}$. To achieve a high cut off frequency, it is necessary to decrease the contact area and ultimately the resistance in the lightly doped n layer. To reduce the resistance in the lightly doped n layer, one method used is silicon molecular beam epitaxy (Si-MBE) [22, 25]. This process has been shown to reduce the n layer thickness to 0.3μm, which is near but not smaller than the depletion length of a Schottky diode. However, Si-MBE cannot be done in standard CMOS processes and another design compatible with the CMOS fabrication process is desired.

2.6 Planar Schottky diodes

The planar diode is designed for an easy integration into circuits, especially for on-chip microwave power detection. The conduction path should be as short as possible to achieve a low series resistance. The contact area also should be small to reduce the contact capacitance and increase the cut-off frequency. Figure 2.6 shows a cross-section view of a CMOS Schottky diode and its associated equivalent circuit elements. The diode consists of a Schottky contact between the metal and the lightly doped n-well (or p-well) layer and an ohmic contact between the metal and the highly doped n+ diffusion (or p+ diffusion) layer. The active layer under the Schottky contact of length L and width W is regarded as an R-C circuit, with the capacitance of

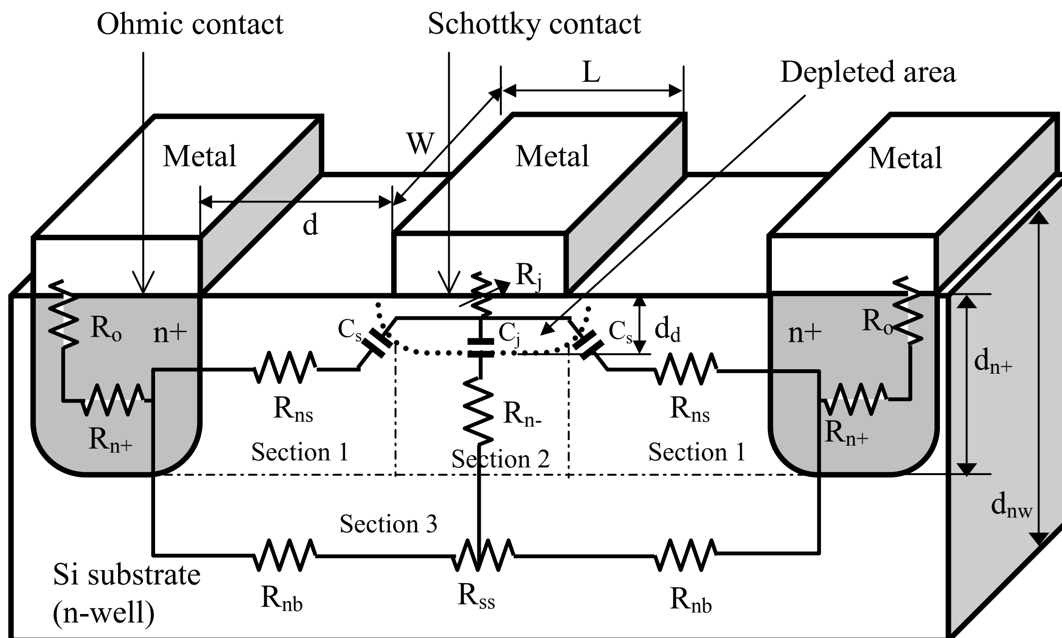


Figure 2.6: Cross-section view of a reverse-biased CMOS Schottky diode and its associated equivalent circuit elements. The conduction paths were divided by three different sections – the sidewall conduction (section 1), conduction under the Schottky contact (section 2), and the body conduction (section 3).

the depletion layer and the resistance of the conduction channel. The conduction channel is divided into three paths, the sidewall conduction, the conduction under the Schottky contact, and the body conduction. (section1, 2, and 3 in Figure 2.6) The bottom capacitance C_d can be calculated from the depletion depth, which is a function of the applied voltage. The depletion depth is given by the following equation.

$$d_d = \sqrt{\frac{2\varepsilon}{qN_D}\left(V_{bi} - V_{bias} - \frac{kT}{q}\right)} \tag{2.6}$$

Where V_{bi} is the built in voltage, V_{bias} is the bias voltage, N_D is the doping concentration of the n-well. The series resistance is the sum of the resistances in n-well and the resistances in the n+ region. The bottom capacitance can be determined by the following equation.

$$C_d = \varepsilon \frac{WL}{d_d} \tag{2.7}$$

The resistances of the n+ region and the ohmic contact resistance are much smaller than that of the n-well region and can be neglected. The sidewall capacitance can be calculated by the following equation.

$$C_s = C_d \frac{d_d 2(W+L)}{WL} = 2\varepsilon(W+L) \tag{2.8}$$

Since the depletion depth d_d is less than 1μm, Cs is small enough to be ignored. R_{ns} is the resistance between the sidewall and n+ region. R_{n-} in section 2 is the resistance under the Schottky contact, R_{nb} in section 3 is the resistance in the body of lightly doped layer. The following equations give the values of these resistors.

$$R_{ns} = \rho \frac{d}{W(d_{n+} - d_d)} \quad (2.9)$$

$$R_{n-} = \rho \frac{d_{n+} - d_d}{WL} \quad (2.10)$$

$$R_{nb} = \rho \frac{d}{W(d_{nw} - d_{n+})} \quad (2.11)$$

R_{ss} is the spreading resistance from section 2 to section 3. Figure 2.7 shows the distributed RC network for calculating the spreading resistance in section 3. From the R-C network, R_n can be ignored due to its small value, and the spreading resistance can be calculated the following equations [27, 28, 29].

$$R_{ss} = \frac{R_{sp}}{4\sqrt{\frac{\omega R_{sp} C_{jj}}{2}}} \frac{\sinh(\sqrt{\frac{\omega R_{sp} C_{jj}}{2}}) - \sin(\sqrt{\frac{\omega R_{sp} C_{jj}}{2}})}{\cosh(\sqrt{\frac{\omega R_{sp} C_{jj}}{2}}) - \cos(\sqrt{\frac{\omega R_{sp} C_{jj}}{2}})} \approx \frac{1}{12}\sqrt{\frac{1}{WL}} \frac{\rho}{(d_{nw} - d_{n+})} \quad (2.12)$$

If we assume that W is equal to L, the series resistance is given by the following

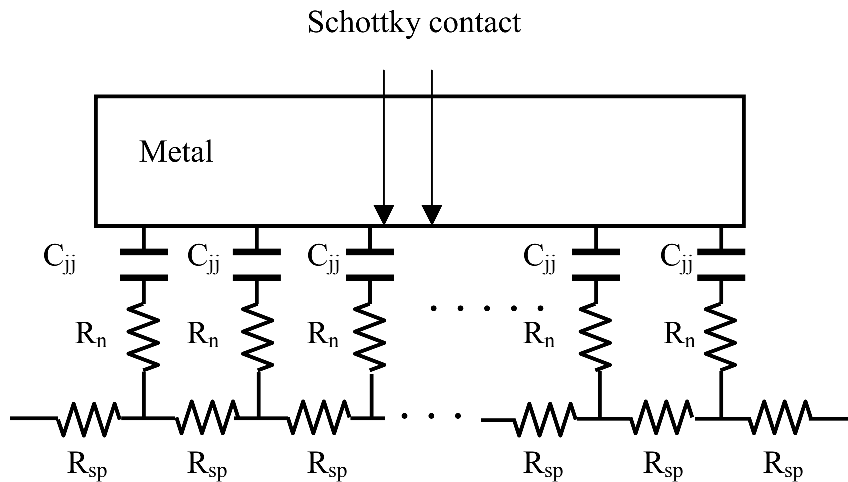


Figure 2.7: Distributed RC network of the Schottky contact for calculating the spreading resistance.

equation, which shows how equation (2.5) is derived.

$$R_{series} = R_{ns} \| \left(R_{nb} + R_{ss} + R_{n-} \right) \approx R_0 / A + R_1 / \sqrt{A} \tag{2.13}$$

Where A is the contact area of a Schottky diode. Finally, the cut-off frequency is given by

$$f_c = \frac{1}{2\pi C_j R_{series}} \propto \sqrt{1/A} \tag{2.14}$$

As we mentioned in the previous section, the cut-off frequency is proportional to $1/\sqrt{A}$.

Chapter 3: CMOS Schottky diode detectors

CMOS process is the most widely used process in integrated circuit fabrication. Schottky diodes for microwave power detector circuits have been made previously through the CMOS processes [23, 26]. However, the standard CMOS process is not specified for the Schottky contacts, and it is difficult to fabricate a Schottky diode by most standard CMOS processes. As a result, the reported Schottky diode fabrication methods highly depended on the process itself, and high frequency operation was not achieved. A modification of a CMOS process for fabricating Schottky diodes through any CMOS process has been developted and reported in the following sections.

3.1 Schottky diodes by a CMOS compatible process and FIB process

As a preliminary research project and before using a commercial CMOS process, CMOS compatible Schottky diodes were designed, fabricated, and tested in the Ion Beam Research and Applications Laboratory at the University of Maryland.

3.1.1 Fabrication

N-type Schottky diodes have been chosen because of the higher electron mobility in silicon. The basic structure (and current path) is metal-to-n-Si-to-n+Si-to-metal (Figure 3.1). To achieve a high cut-off frequency, the rectifying, metal-to-n-Si, contact area needs to be reduced and the conduction path in the n layer needs to be minimized. However, too small of a contact area limits the maximum power the device can detect before the diode burns out. In the case of MBE devices, which have an epitaxially grown n layer on top of an n+ layer, the series resistance was

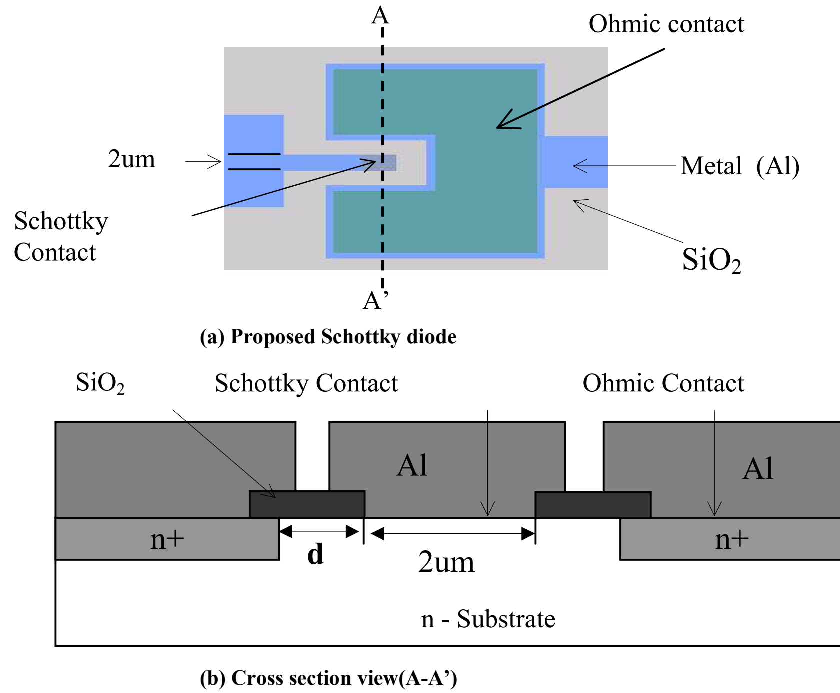


Figure 3.1: Fabricated Schottky diode with 2um x 2um contact area which is surrounded by n+ region (a) and cross section of a Schottky diode(b)

minimized simply by reducing the thickness of the n layer [21, 23]. However this cannot be done in standard CMOS processes and another design is required.

A mask set for fabricating Schottky diodes with reduced contact size and minimum series resistance between the n and the n+ regions (i.e. minimizing the distance d in Figure 3.1) was designed, and several Schottky diodes were fabricated. Since the current CMOS process has a definitive minimum distance between the n contact and n+ layer (eg. such as 1.2µm in AMI 0.5micron process), it is difficult to reduce this distance 'd' to 0.3µm as in the Si-MBE process. The 'd' was 3µm for the fabricated Shottky diodes in our lab. For testing under RF direct injection and irradiation, the mask set included ground-signal-ground (GSG) pad structures and antenna structures respectively, which were connected to Schottky diodes. The

processing steps used in the Schottky diode fabrication were the same steps used in standard CMOS processing: patterning of SiO_2, n+ activation by rapid thermal annealing, e-beam Al deposition, and Al patterning. To reduce the contact area and minimize the conduction path in a lightly doped n layer, which typically has a 10^{15} cm^{-3} doping concentration, a mask set was fabricated, which has several Schottky diode layouts starting with 2μm x 2μm contact area.

3.1.2 Measured result

After several fabrication steps, such as phosphorus diffusion to achieve the doping concentration of 10^{19} cm^{-3} or more and aluminum deposition for Schottky and ohmic contacts, several diodes were fabricated, and the DC I-V characteristics were measured. The DC I-V curve of the fabricated Schottky diode in figure 3.2 shows a

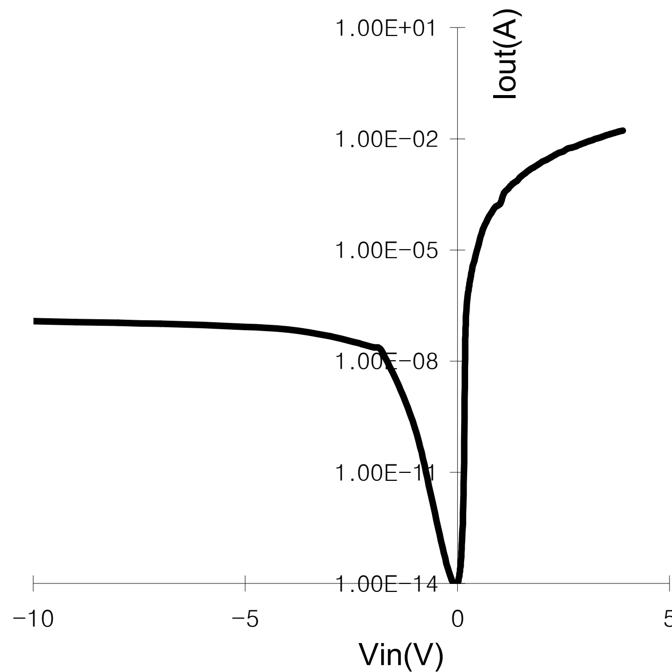


Figure 3.2: IV curve of a Schottky diode fabricated by the CMOS process (2umx2um contact area)

diode I-V curve with an 83Ω series resistance defined as the slope between 4V and 5V, where the series resistance is much bigger than the junction resistance. The RF power detecting characteristics of the Schottky diodes, which had a 2μm x 2μm contact area, were measured by directly injecting RF power through the GSG pads using a Cascade ACP-150 probe shown in Figure 3.3. Figure 3.4 shows the block diagram of the experiment setup. Agilent 83731B was used as an RF burst source. The injected RF signal had a pulse width of 1.5μs and a pulse repetition interval of 10ms and a frequency sweep from 1GHz to 10Ghz at an input power level 15dBm is shown in Figure 3.5. There was no apparent cutoff frequency in this frequency range. The measured result of a power sweep from 0dBm to 20dBm at 5GHz and 6GHz in Figure 3.6 shows a quadratic and a linear relationship between the input power and the detected voltage as expected. Figure 3.7 shows the measured pulse response for a 2GHz RF burst and a 20GHz RF burst input through the cascade probe. The pulse response times were 200ns and 1.2μs for 2GHz and 20GHz RF bursts, respectively.

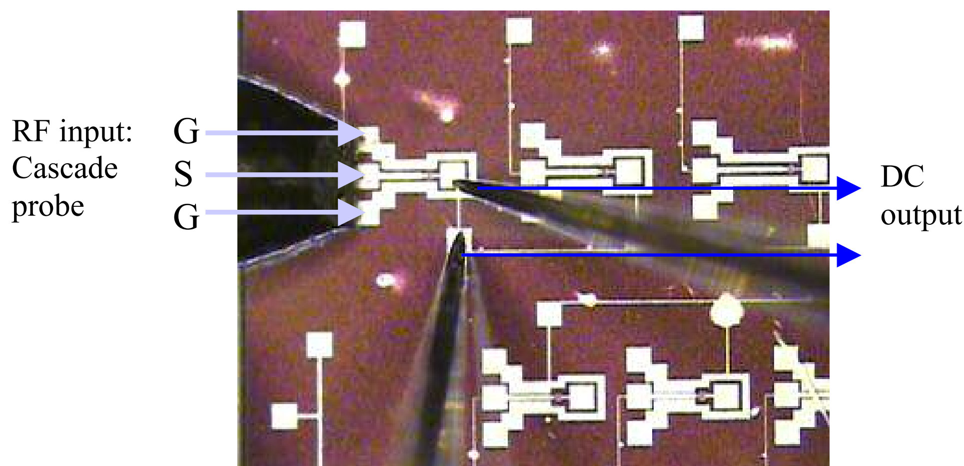


Figure 3.3: RF direct injection with Ground-Signal-Ground Cascade probe

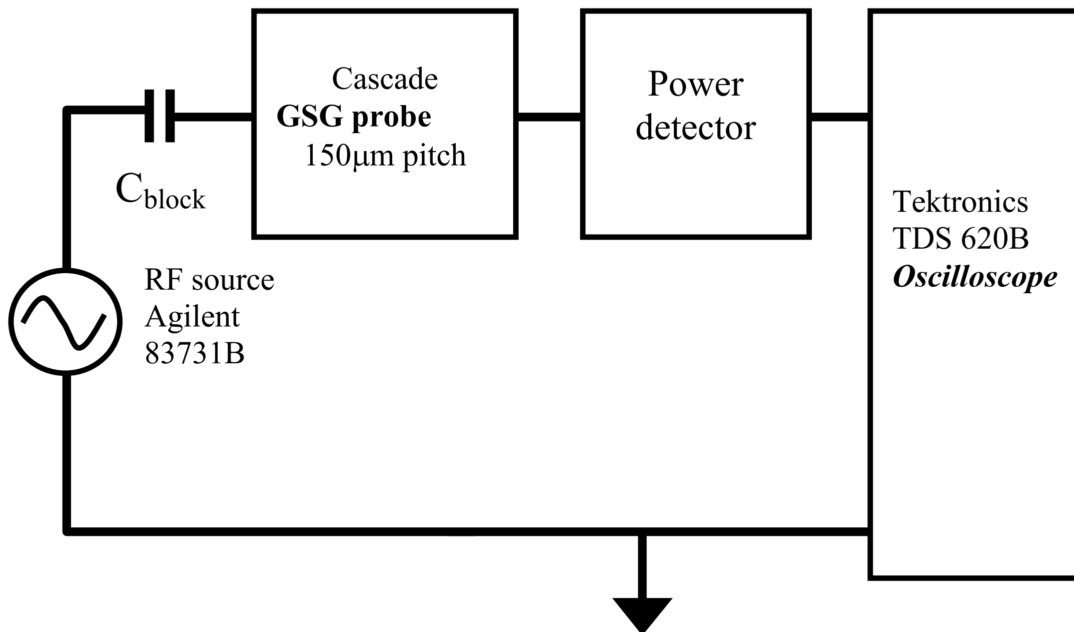


Figure 3.4: Experimental setup for RF burst direct injection with Cascade GSG probe.

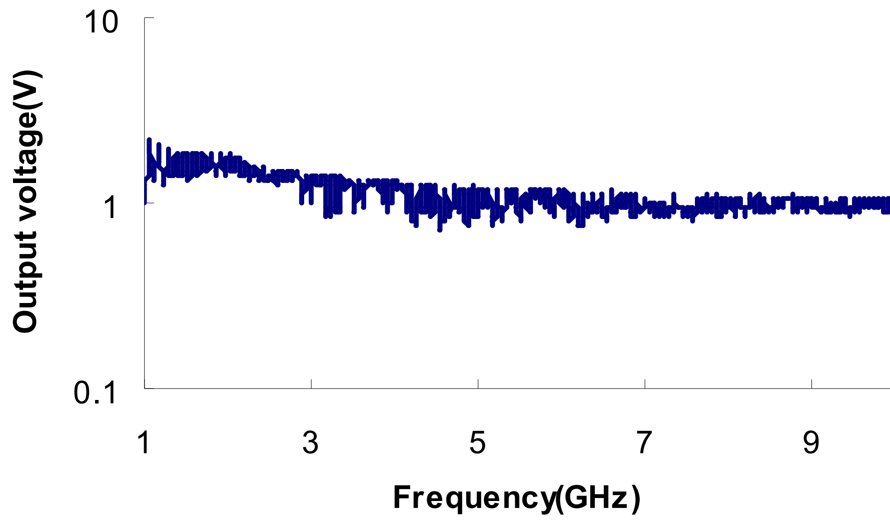


Figure 3.5: RF direct injection to 2μm x 2μm Schottky diode: Frequency (1GHz to 10GHz) sweep at 15dBm

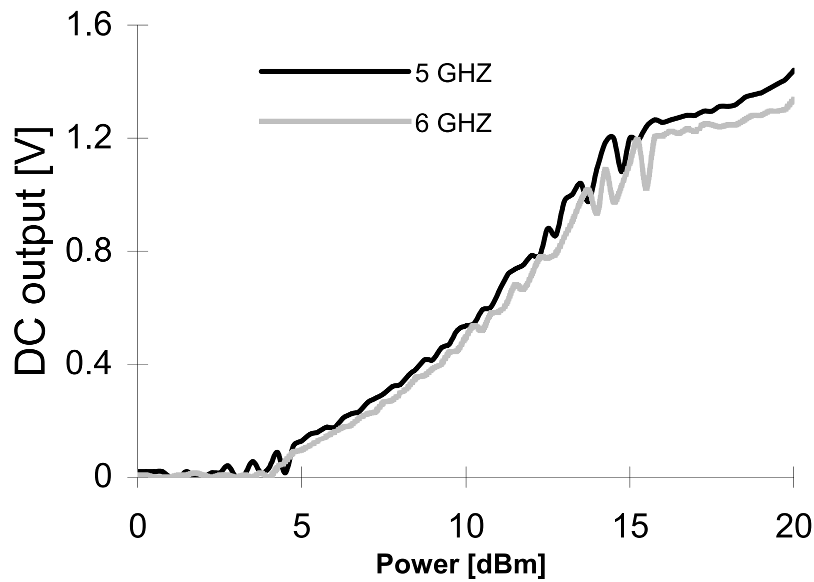


Figure 3.6 RF direct injection to 2μm x 2μm Schottky diode: Power (0dBm to 20 dBm) sweep at 5 and 6GHz

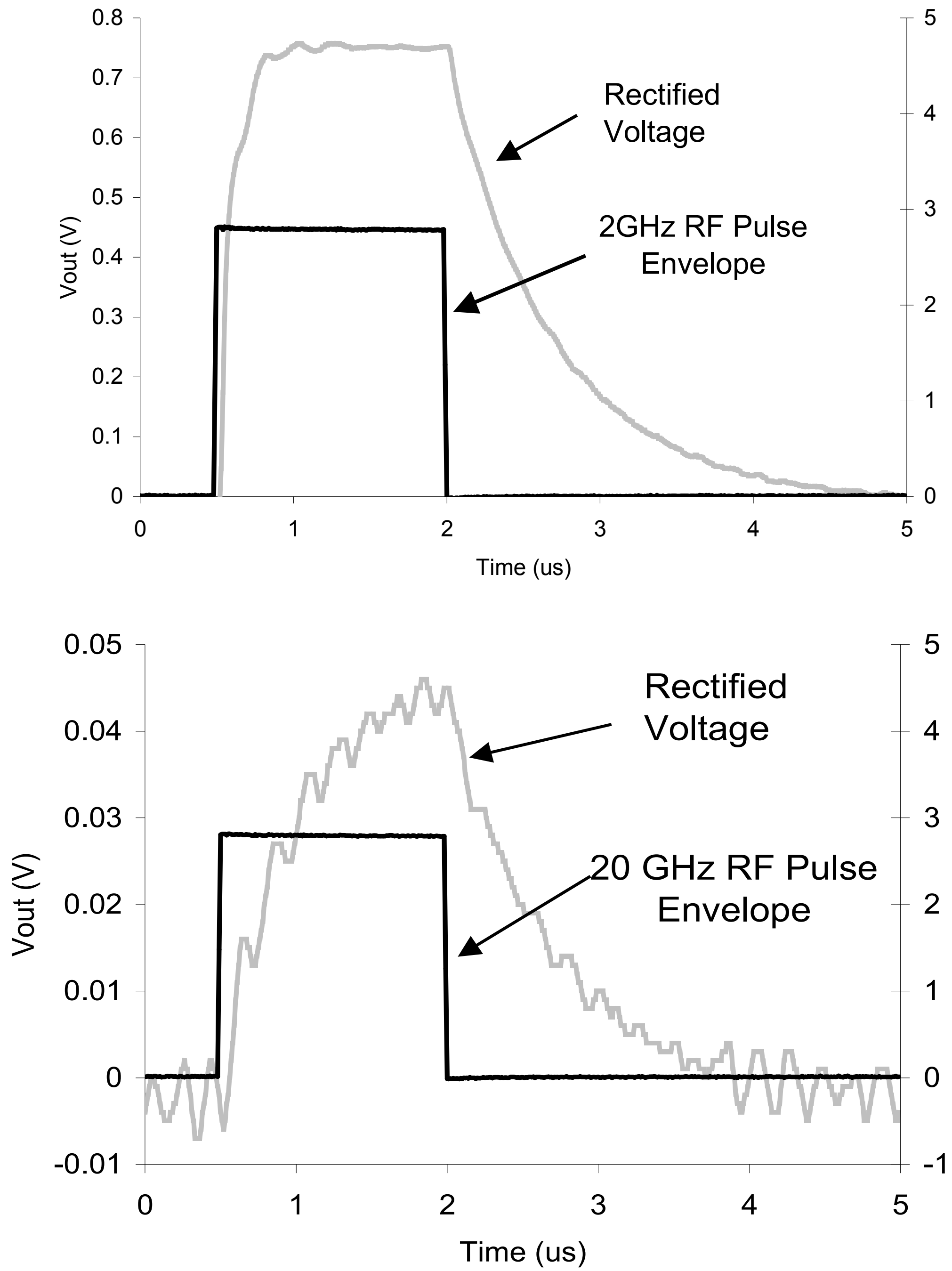


Figure 3.7: Output voltage pulse in response to 2GHz and 20 GHz RF burst

The pulse response time, witch is the rise time of the output pulse in response to a RF burst, can be calculated by the following lumped equivalent circuit of a diode with a load resistor and capacitor (Figure 3.8).

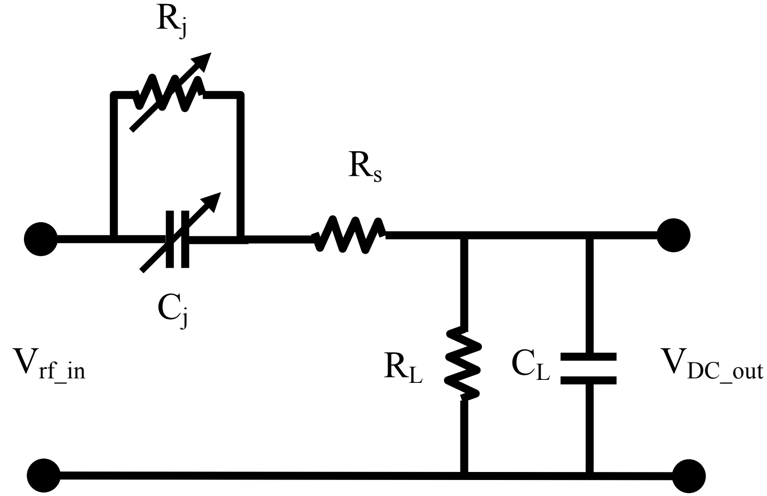


Figure 3.8: Equivalent lumped-element circuit of a Schottky diode with a load resistor and a capacitor. R_S is the series resistance, Rj is the junction resistance, Cj is the junction capacitance, R_L is the load resistance, 1MΩ, and C_L is the load capacitor, 1pF.

The output voltage is given by the following equations.

$$V_o = \frac{\dfrac{R_L}{1+sR_LC_L}}{\dfrac{R_j}{1+sC_j}+Rs+\dfrac{R_L}{1+sC_L}}$$

$$= \frac{R_L\left(1+sR_jC_j\right)}{R_j\left(1+sR_LC_L\right)+R_S\left(1+sR_jC_j\right)\left(1+sR_LC_L\right)+R_L\left(1+sR_jC_j\right)}$$

$$= \frac{R_L\left(1+sR_jC_j\right)}{R_j+R_S+R_L+s\left(R_SR_jC_j+R_SR_LC_L+R_jR_LC_L+R_LR_jC_j\right)+s^2R_SR_jR_L} \quad (3.1)$$

Since the series resistance is at least 10 times smaller than the 1MΩ load resistance, R_s is assumed to be zero. As a result the output voltage is given by the following equation.

$$V_o = \frac{R_L\left(1 + sR_jC_j\right)}{R_j + R_L + sR_jR_L\left(C_L + C_j\right)} \tag{3.2}$$

From equation (3.2), the rise time can be calculated as

$$T_r = \frac{2.2R_jR_L\left(C_L + C_j\right)}{R_j + R_L} \tag{3.3}$$

Where 2.2 term comes from the definition of the rise time, which is commonly expressed as the interval between the points of 10% and 90% amplitude ($T_r = 2.2\tau$, τ is the time constant). When the frequency of the input RF signal increases, the conversion loss becomes bigger, since the diode consumes more power due to the increased capacitance. In other words, because the diode is operating in a low voltage range, the junction resistance R_j becomes bigger. As a result, the pulse response time increases. For example, if the input RF has 2GHz frequency, the rise time would be

$$T_r = \frac{2.2R_jR_L\left(C_L + C_j\right)}{R_j + R_L}$$

$$= \frac{2.2 \times 91 \times 10^3 \times 10^6 (10^{-12} + 10^{-13})}{91 \times 10^3 + 10^6} = 204\ ns$$

where the junction resistance is assumed to be 91kΩ, and the junction capacitance is assumed to be 100fF. If the frequency of the input RF signal is 20GHz, the junction resistance is assumed to be increased 10 times to 910kΩ. From equation (3.3), the rise time is calculated to be 1.16μs, which agree to the measured result.

3.1.3 Schottky diodes by Focused Ion Beam process

Schottky diodes were fabricated using FIB techniques as a post-CMOS fabrication process on a chip fabricated through a CMOS compatible process. A FEI Dual beam 620 was used for FIB milling and FIB ion induced deposition for the final step in the Schottky diode fabrication process. The FIB process implants Ga ions during milling and deposition, but a Ohmic contact or a Schottky contact can be still made due to the small amount of Ga ions [30]. To achieve a high cut-off frequency, we designed the contact area to be 2μm x 3μm, and the distance between the Schottky contact and the ohmic contact as 3μm. The contacts were fabricated using FIB milling and FIB ion induced deposition techniques. After fabricating the highly doped n+ layer by a CMOS process, a 2μm x 3μm rectangular area was defined by FIB milling. Platinum was deposited by FIB ion induced deposition. SEM images and cross-section views for each step are shown in Figure 3.9. The series resistance was calculated to be 127Ω (Figure 3.10), which is larger than the device discussed in the previous section. The reverse leakage current was 140nA, the barrier height and the ideality factor were calculated to be 0.392eV and 1.96, respectively. The difference in the series resistance can be attributed to only one side of the diode conducting in FIB Schottky diode compared to the three sided conducting path in the CMOS process fabricated Schottky diode. Form the microwave pulse direct injection measurement with the same experimental setup as in Figure 3.4, the cut off frequency was 10GHz and junction capacitance was calculated to be 48fF (Fig. 3.11). Power sweep results show quadratic responses at 8GHz and 10GHz (Fig. 3.12). From the power sweep measurements, both CMOS compatible diode and FIB-fabricated diode operated at

5dBm of RF input or more. Since we assumed there is no bias circuit for our detectors, our detectors had low sensitivities. Typical diode detectors require bias circuits to achieve a high sensitivity.

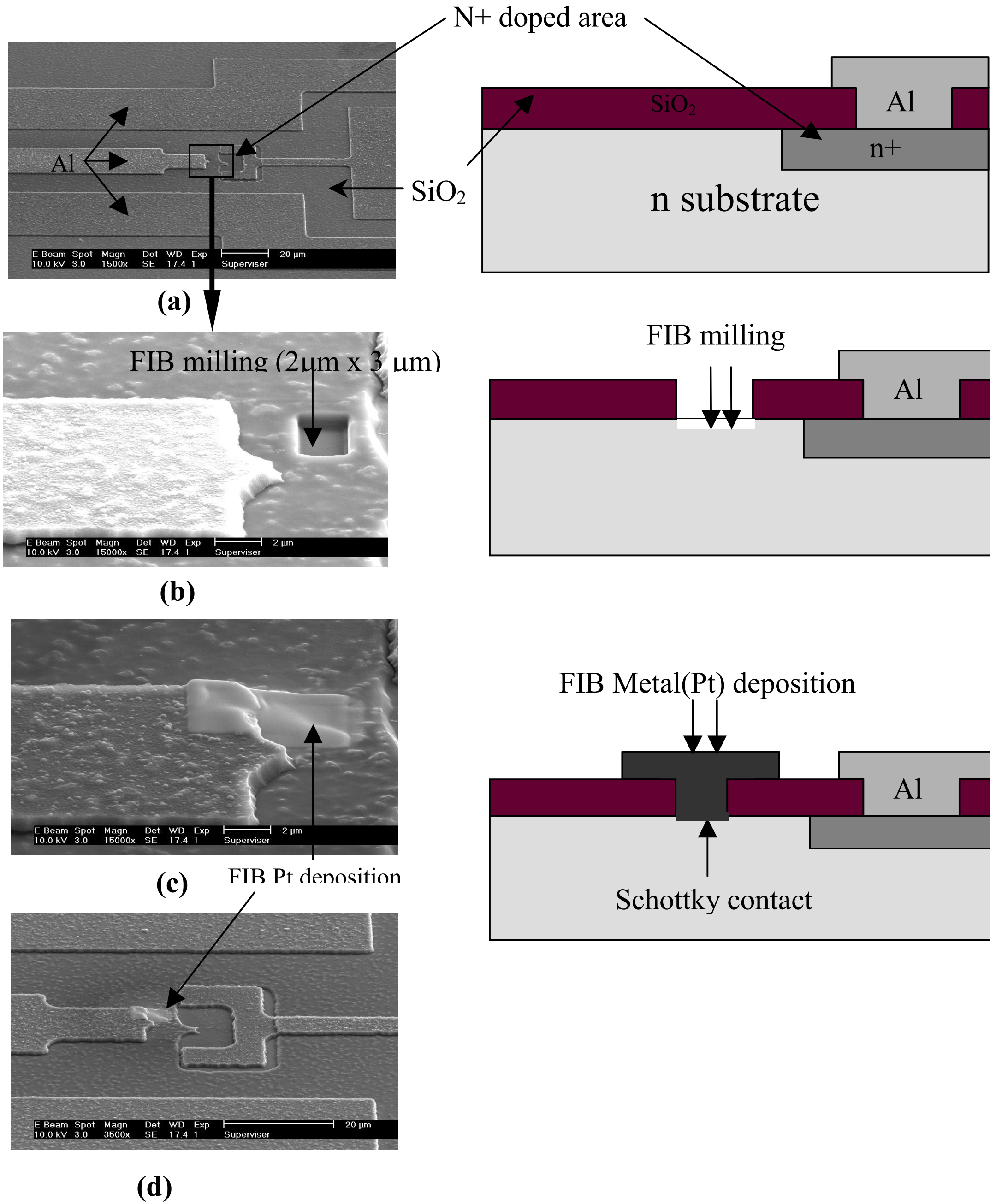


Figure 3.9: SEM images and cross-section views of fabricating steps by FIB. (a) CMOS processed device structure with only highly doped n area. (b) FIB milling of 2μm x 3μm rectangular area (c) Pt deposition (d) Fabricated Schottky diode structure

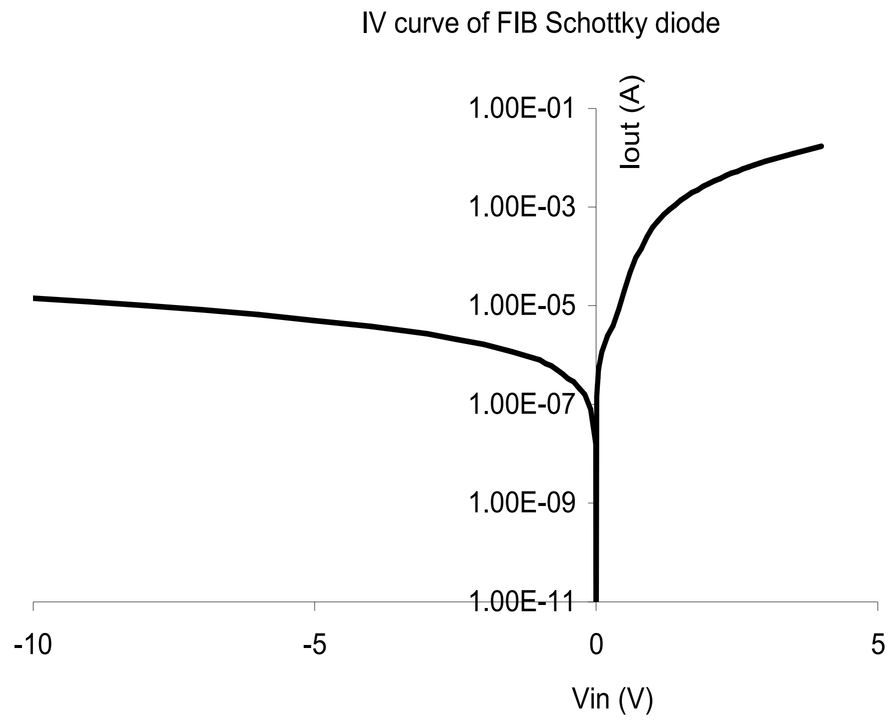


Figure 3.10: DC IV measured result of a Schottky diode by FIB

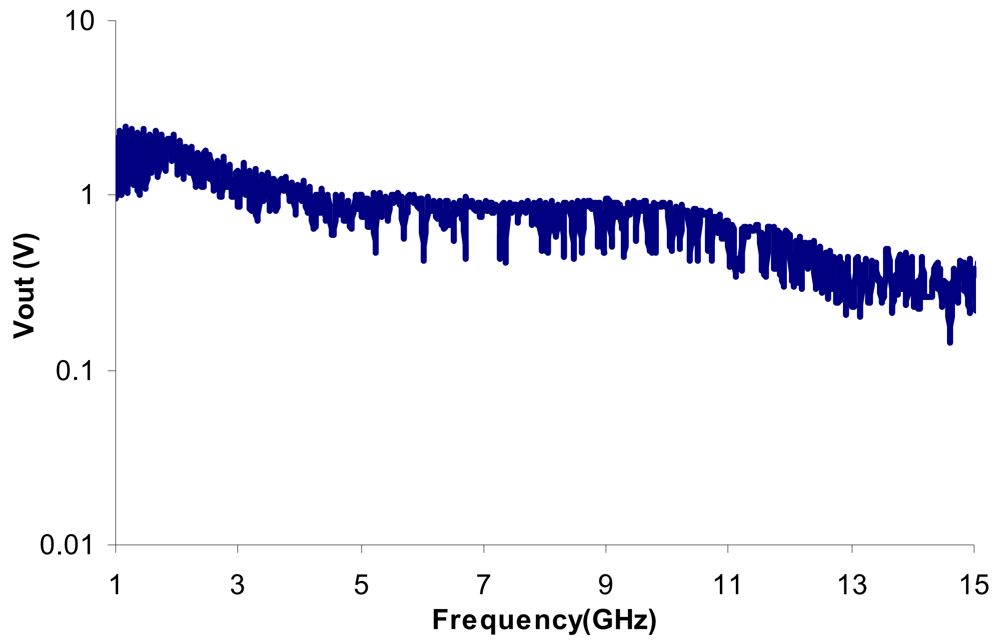


Figure 3.11: Measured result of the Schottky diode by FIB: Frequency sweep from 1 to 15GHz at 15dBm power injection

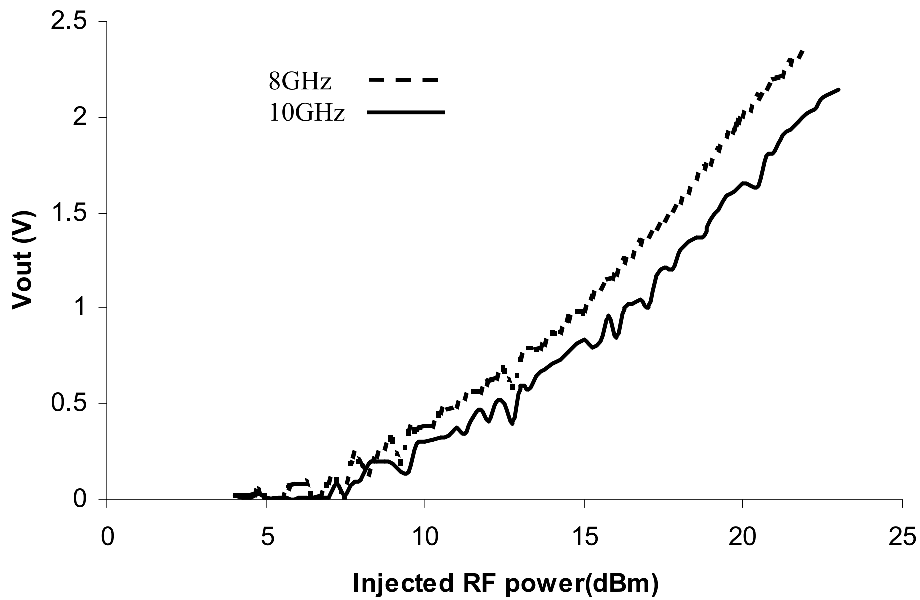


Figure 3.12: Measured result of the Schottky diode by FIB: Power sweep from 0 to 25dBm at 8 and 10GHz.

3.2 CMOS Schottky diodes

To fabricate power detectors through a commercial CMOS process, fabrication of CMOS Schottky diodes through three different CMOS processes (AMIS 1.5μ, 0.5μ, 0.35μ CMOS process) was tried. However, all failed to achieve Schottky contacts as expected. This was because the standard CMOS process is not specified for the Schottky contact, and a modification of a CMOS process was required.

3.2.1 Fabrication

In a standard CMOS design, when layouts for contacts to lightly doped substrate, such as Nwell or Pwell, are drawn, the layout editor automatically generates high impurity diffusion layers at the same locations to prevent Schottky contacts. By modifying the layout file to remove these impurity diffusion layers, Schottky contacts were achieved. Various Schottky contact areas from $2\mu m^2$ to $900\mu m^2$ were used. The fabrication steps of a CMOS Schottky diode are simple. First, a passivation layer was opened to diffuse n-type or p-type impurity. After diffusing impurities, another passivation layer is opened to expose the silicon surface without diffusing any impurities for a Schottky contact. Contact metals are deposited to make both ohmic contact and Schottky contact. Figure 3.13 shows the ground-signal-ground (GSG) pads for injecting an RF burst by using the Cascade probe and the cross section view of a Schottky diode fabricated through the 0.5μ CMOS process.

3.2.2 Measured result

Figure 3.14 shows the DC I-V measured result for CMOS Schottky diode power detectors fabricated and tested. The series resistances of the Schottky diodes with

$30x30\mu m^2$, $8x8\mu m^2$, $2x2\mu m^2$ contact areas were 100Ω, 494Ω, and 6.5kΩ, respectively. Figure 3.15 shows the RF pulse direct injection experiment with the same experimental setup as in Figure 3.4. An RF pulse was directly injected to the GSG pads as shown in Figure 3.13 by using the Cascade GSG probe. From the measured result, the CMOS-fabricated Schotty diode power detector with $2x2\mu m^2$ Schottky contact area had 820ns pulse response time, 28dBm dynamic range, and began to detect –13dBm input power level. The Schottky diode power detector with $30x30\mu m^2$ contact area had 35dBm dynamic range, 776ns pulse response time, and began to detect –20dBm input power level. From the frequency sweep measurement, smaller contact area Schottky diodes showed flatter frequency response. It was because the cut-off frequency of a Schottky diode is proportional to $1/\sqrt{A}$ from the equations (2.3) and (2.5).

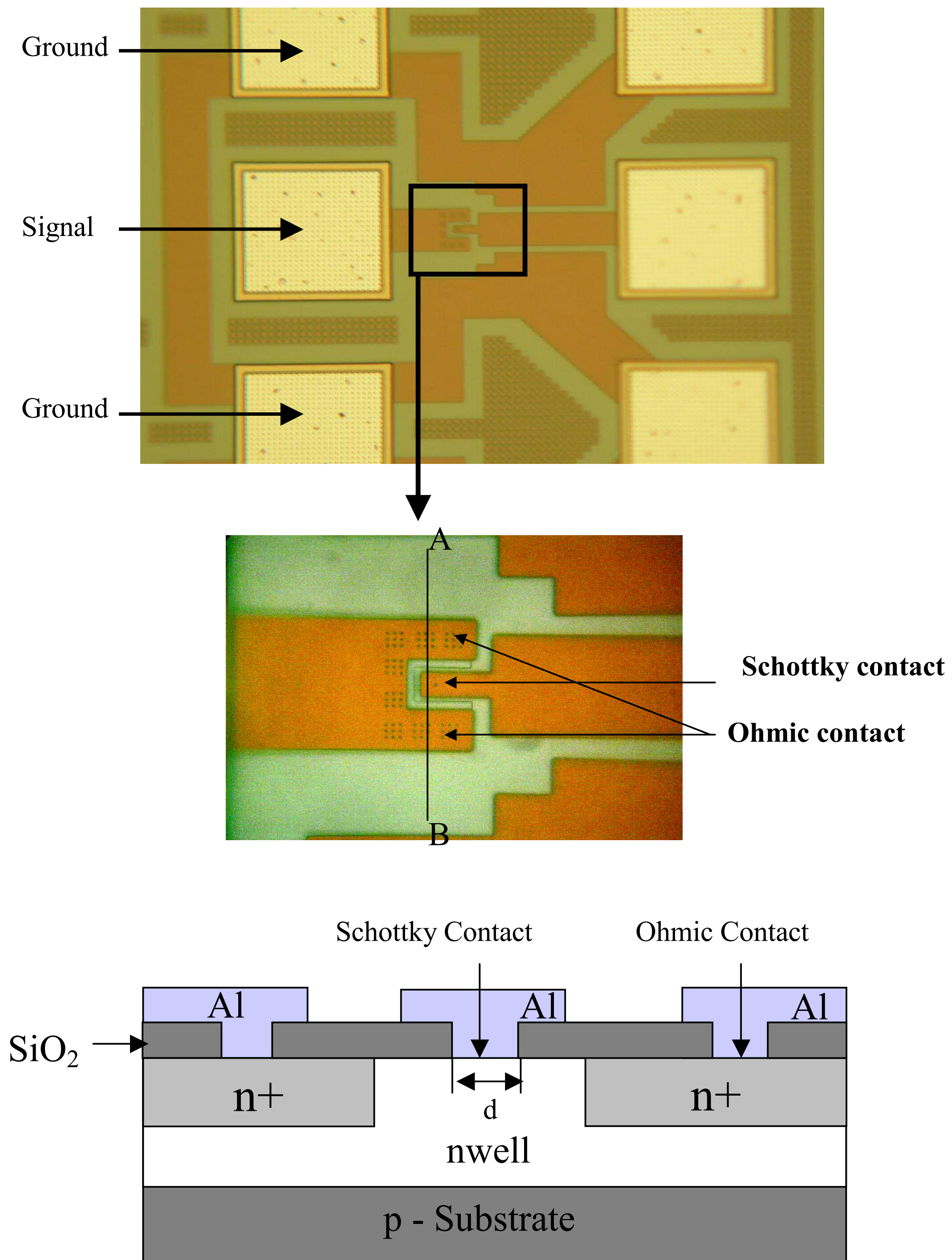


Figure 3.13: Ground-Signal-Ground pads for injecting RF pulse signal with Cascade probe. The magnified and the cross section view of a CMOS Schottky diode fabricated through 0.5µ CMOS process

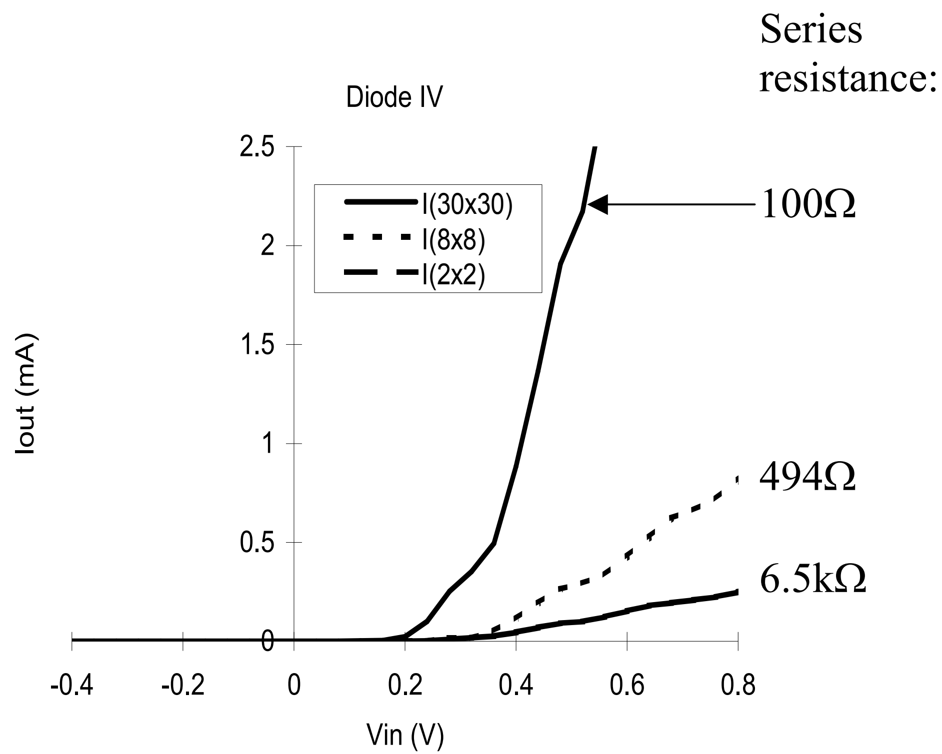


Figure 3.14: DC IV measured result. The bigger the contact area was, the lower the series resistance was.

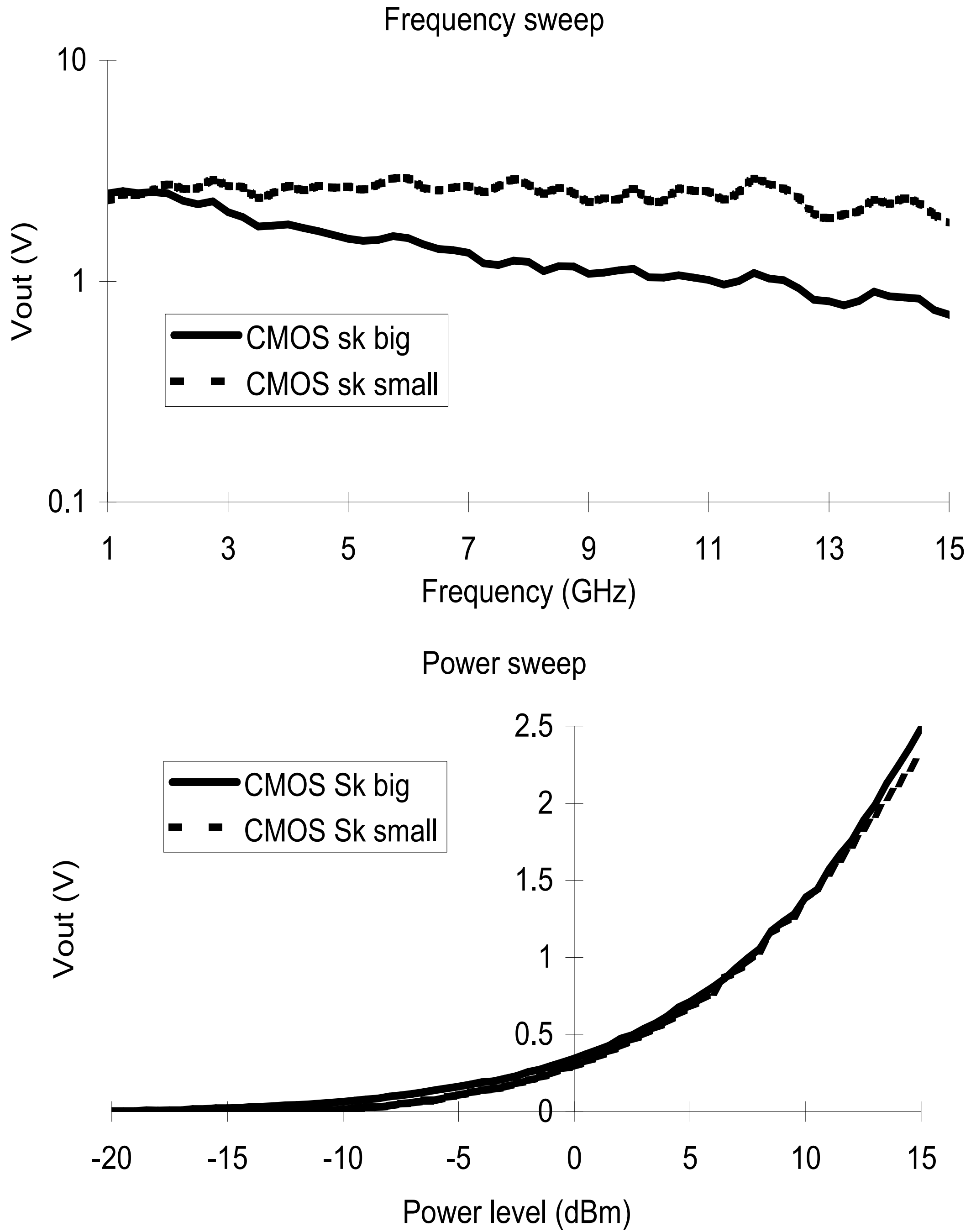


Figure 3.15: RF pulse direct injection measured result: Frequency sweep from 1GHz to 15GHz at 15dBm, Power sweep from –20 to 15dBm at 1GHz

Chapter 4: Post-CMOS Schottky diode power detectors

Focused Ion Beam (FIB) techniques have been used for ion implantation, creating localized damage, ion milling, ion induced deposition, lithography, and scanning-ion microscopy [31]. Its applications are IC device modification and failure analysis of fabricated chips by nano scale cutting and rewiring ability [32]. FIB ion induced deposition have been used for making Ohmic contacts on a silicon wafer [30], and we have used FIB milling and ion induced Pt deposition for fabricating Schottky diodes on a silicon wafer [5]. Although, as we will discuss in chapter 4, the CMOS process can be modified to fabricate Schottky diode detectors, the FIB process permits additional detectors to be fabricated in arbitrary locations. Once FIB fabrication steps are developed and if any space is available, any number of diodes can be added on a chip, since FIB is a quite reliable and repeatable process. Typical material removal and addition rate by FIB is in the 0.1 to 1μm^3 per second range. A typical Schottky diode site required two cuts and one deposition and was completed in 4 to 10 minutes. And, since FIB steps do not need any mask set, the fabrication cost can be also saved. The extra FIB steps do not harm the operation on CMOS chips since they are usually covered by thick oxide and nitride and only limited area will be exposed to ion beam. The post-CMOS-FIB fabrication, and the RF response of Schottky diodes are reported in Chapter 4.

4.1 Focused Ion beam system

The basic operation of FIB system is almost identical to SEM, except it uses an ion source rather than electron source. The main advantage of FIB system is a pattern can be milled or deposited at any location of interest without any mask. Figure 4.1 shows a schematic diagram of an Ion column of a FIB system.

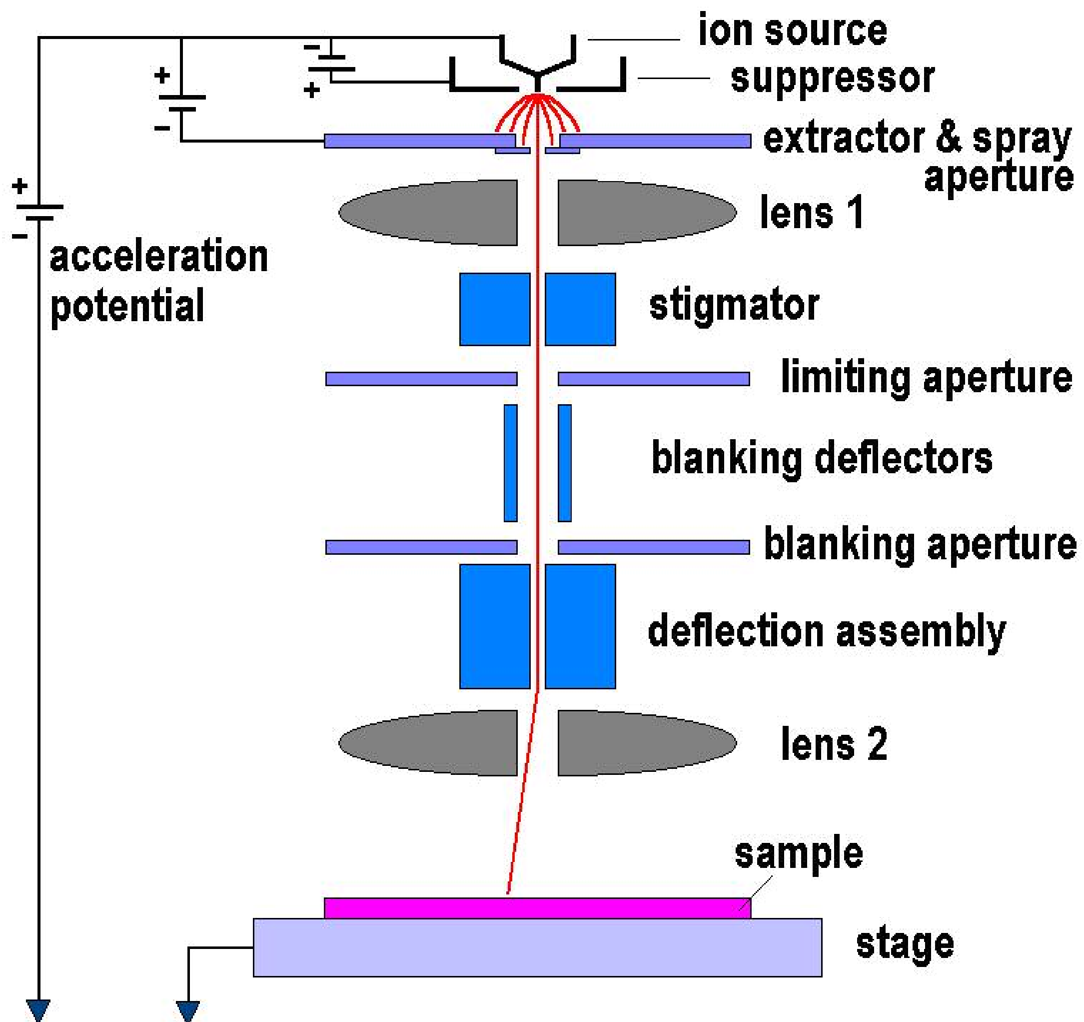


Figure 4.1: Ion column in a Focused Ion Beam system.

4.1.1 Liquid metal ion source

Liquid metal ion source (LMIS) such as Ga is used for the ion source, and the source is in a reservoir, which is in contact with a needle. (Figure 4.2) The liquid metal wets the needle and forms a round tip due to surface tension. When a high potential is applied between the tip and extractor, the liquid metal tip becomes sharper and sharper. The electric field is highest at the tip, and the sharper the tip is, the stronger the electric field is. Eventually, metal ions are emitted from the end of the tip. Ga is one of the best candidates as an LMIS due to its high surface tension and low vapor pressure at the melting point [31].

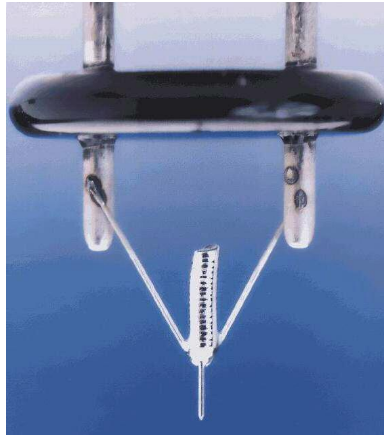


Figure 4.2: Liquid Metal Ion Source

4.1.2 Ion column

The ion column in Figure 4.1 focuses the ions to the target. The ion beam is generated from the LMIS by the extractor, which is typically hard at –10kV with respect to the LMIS. A typical ion emission current is set to 2.2μA in the FEI dual

beam 620 machine. The lens 1 condenses the ion beam and the stigmator adjusts the beam stigmatism. The limiting aperture sets the beam currents to between a few pA and tens of nA by changing variable apertures. The aperture size can be set to meet the desired current on the target. To write an arbitrary pattern, the blanker is used for turning the beam off in conjunction with the deflection assembly. The deflecting assembly uses raster scanning, and the lens 2 focuses the beam to a fine spot for the best resolution. The typical acceleration potential is from 10keV to 50keV.

4.1.3 FIB milling

The "local Ion milling" is a major advantage of the FIB applications. When Ga+ ions with a high current hit the target, the cascade collision process removes the target atoms from the surface, which is a physical sputtering of the target material (Figure

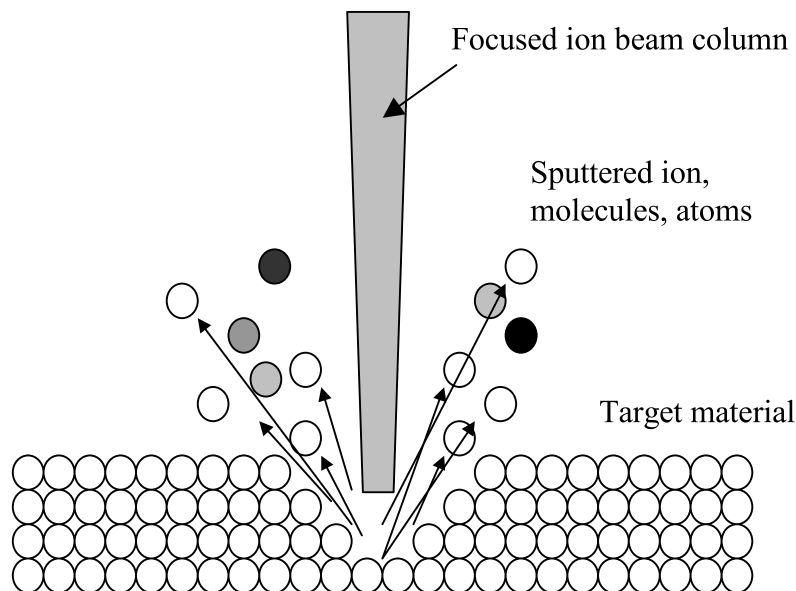


Figure 4.3: FIB milling: Ion column focused on the location to be milled. Atoms, electrons, and molecules are sputtered from the target material

4.3). Due to the size of the ion beam spot on the sample, the smallest pattern size can be a few tens of nanometers. By blanking and deflecting the beam, an arbitrary pattern can be fabricated. The yield, which is the number of ions removed per incident ion, depends on many variables and material properties, which are the sample density, the target atomic mass, the beam ion mass, and the incident angle. The reported yields are 2.6 atoms per ion with 30keV Ga+ ion for silicon [31], 2.0 molecules per ion with 68keV Ga+ ion for SiO_2, and 4.2 atoms per ion with Ga+ ion for Aluminum [32] To enhance the yield, small quantities of reactive gas can be introduced via gas needles that are positioned near the area being milled. In addition, gas assisted ion milling increases the selectivity of certain types of materials such as metals and insulators and minimizes the re-deposition of the milled material.

4.1.4 FIB ion induced deposition

A FIB system also enables the localized maskless deposition of both metals and insulator materials on to the surface by ion beam induced deposition. The deposition process is similar to the gas-assisted ion milling, except that a different precursor gas and the lower beam current are used. The precursor gases are sprayed on the surface by a fine needle. The ion beam decomposes the adsorbed precursor gases, and the desired metal remains on the surface as a thin film, while desorbed reaction products are removed through the vacuum system. (Figure 4.4) The smallest features that can be deposited are of the order of 100 nm. A typical application of FIB ion induced deposition is modifying or repairing an integrated circuit, since this technique can significantly reduce the time for debugging the circuit designs. Platinum is most widely used for this purpose, since it is inert and does not degrade due to exposure to

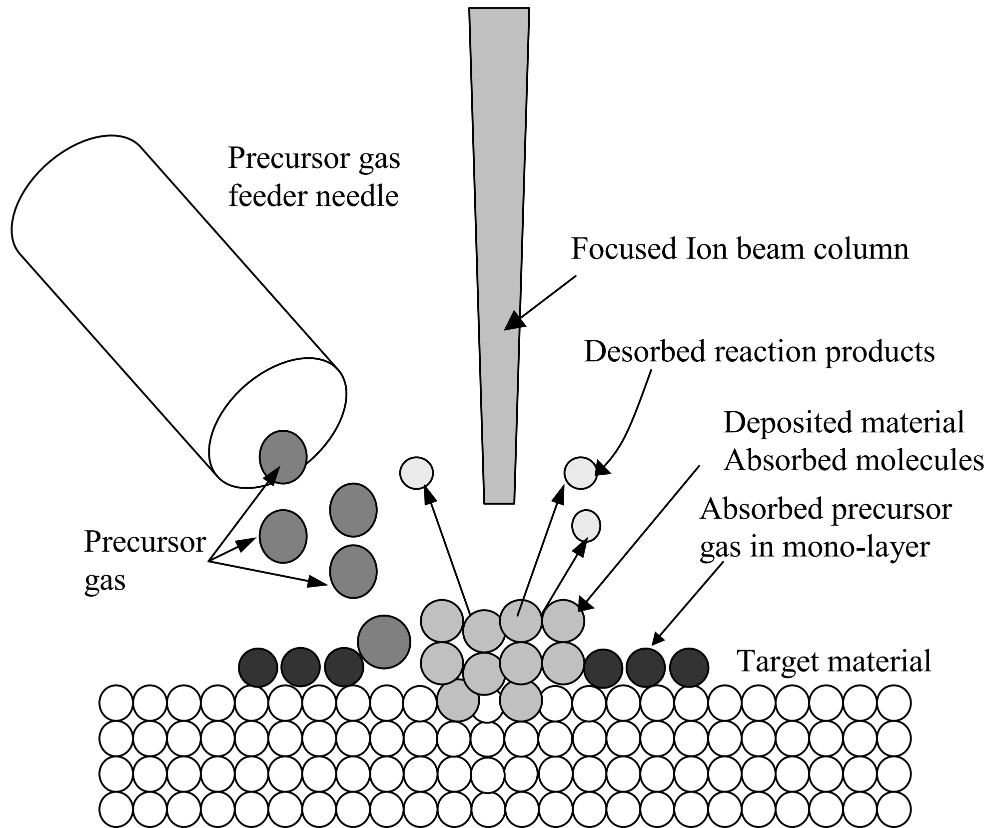
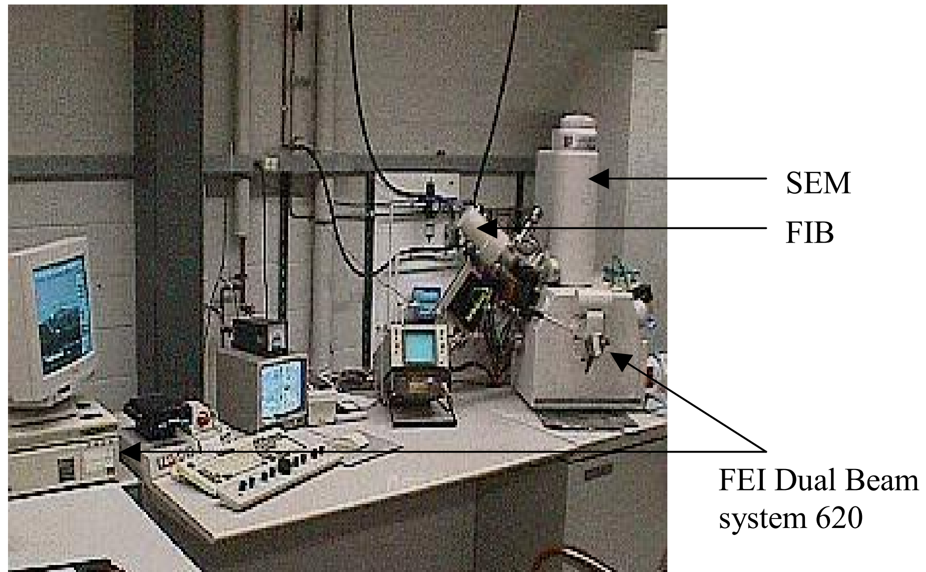


Figure 4.4: FIB ion induced deposition: Ion column focused on the location for deposition. Desorbed reaction products are removed through the vacuum system

air or to elevated temperatures or high current densities. Platinum also can be deposited directly on silicon [33]. An organometalic precursor gas, (trimethyl)-methlcyclopenta-dienylplatinum ($(((CH_3)_3(CH_3C_5H_4))Pt)$), which is heated to 39 °C to vaporize it into a gaseous state, is used for platinum deposition. Typical resistivity increases derived are between 70Ωcm and 1000Ωcm compared to 10μΩcm for bulk resistivity of pure platinum. The FIB deposited platinum film is contaminated by carbon, which is unwanted components of the precursor gas [33]. Even though the resistivity is elevated, the resistance can be low enough to give an electrical connection by increasing the thickness and the deposition area.

4.1.5 FEI Dual Beam system 620

The FIB system used for this research is Dual Beam system 620 made by FEI. Since the FEI Dual Beam system 620 has both a focused Ga+ ion beam column and a



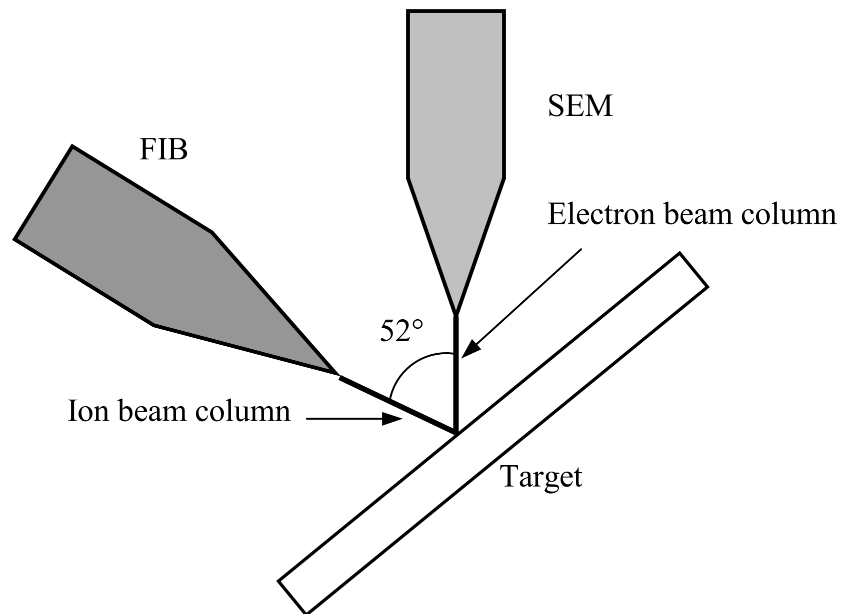


Figure 4.5: Dual Beam system, FIB is for imaging, milling, and deposition, SEM is for imaging.

field emission scanning electron column, this system has the ability to mill or deposit materials by ion beam and to image with upto 52° angle by electron beam at the same time. (Figure 4.5) Examining the cross-section view of a device is one of the advantages of the Dual Beam system due to the angle between two columns. Table 4.1 shows the detailed specification of ion and electron columns of the FEI Dual Beam System 620 [34].

Table 4.1

Ion Beam	Ion Source	Gallium LMIS
	Energy:	30keV
	Beam current	1pA - 11.5nA
	Resolution	16nm
Electron Beam	Electron Source	Field Emitter
	Energy:	1-30keV
	Resolution	5nm

4.2 FIB Schottky diodes on a CMOS chip

As a post-CMOS process, FIB milling and ion induced deposition can be used for fabricating Schottky diodes on a silicon chip, which was already fabricated by a standard CMOS process. Based on the design and measured result of the FIB Schottky diodes fabricated in our laboratory in Ch.3, CMOS Schottky diodes were designed and fabricated on a CMOS processed chip by 0.5µ CMOS process. Both n-type and p-type FIB Schottky diodes were fabricated and tested under the RF direct injection.

4.2.1 Design and fabrication

Both n-type and p-type FIB Schottky diodes on a CMOS chip fabricated by the AMIS 0.5μ CMOS process have been designed. Even though n-type Schottky diodes have higher electron mobility in silicon and better performance than p-type Schottky

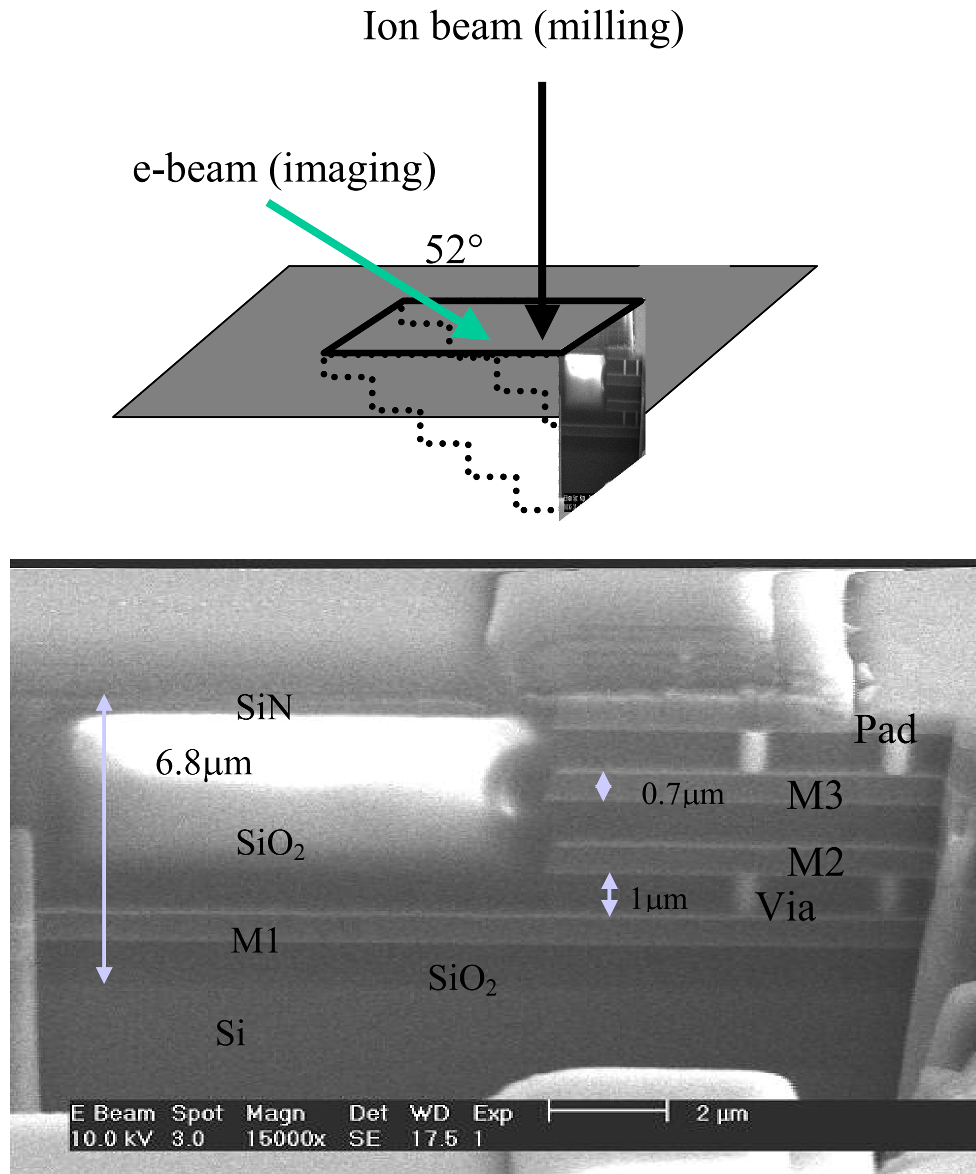


Figure 4.6: Cross-sectioning by FEI Dual Beam system 620 and the cross-section view of a CMOS chip. Due to the thick SiN and SiO_2 layers, RIE process was required.

diodes, p-type Schottky diodes are also useful, and it is easier to find a location for fabricating diodes since the most CMOS processes use p-type substrate. FIB milling and ion induced deposition were used as post-CMOS steps to build Schottky diodes in specially designed locations on the CMOS chips fabricated using 0.5μ CMOS process. Before the post-CMOS process, a CMOS chip was cross-sectioned to figure out the processing steps of the 0.5μ CMOS process. (Figure 4.6) From the cross-section view, we found the oxide and nitride layer was too thick (6.8μm) for FIB fabrication. Imaging the CMOS chip with a passivation layer was also difficult, since the current of the incident ions and electrons, which were emitted from the field emitter to the SiN layer, did not have a conduction path to the ground and charged up the surface of the SiN layer. Reactive Ion Etching (RIE) and chemical etching were used to remove the nitride and to make oxide layers thin enough to be processed by FIB. Two steps of FIB millings were used to expose the metal layer by milling the

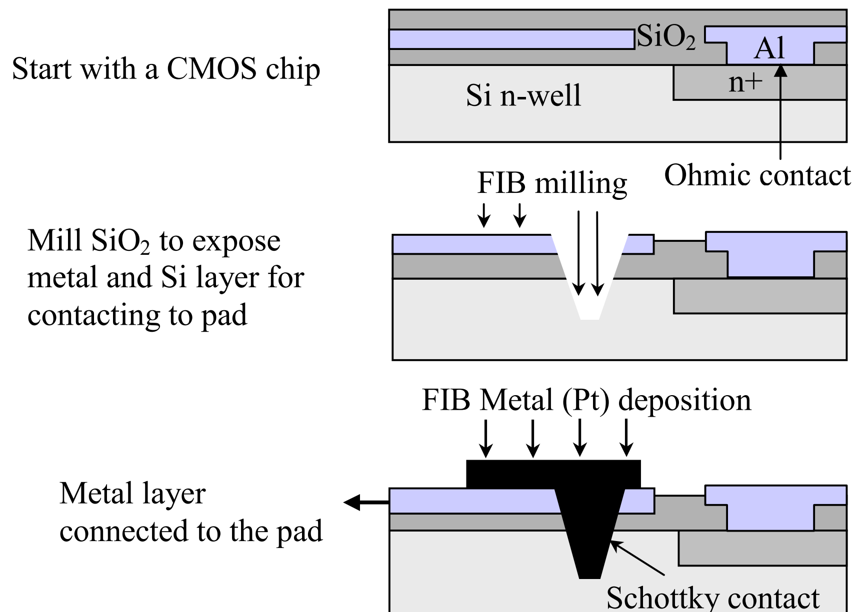


Figure 4.7: FIB Schottky diode fabrication, cross-section view of the fabrication steps.

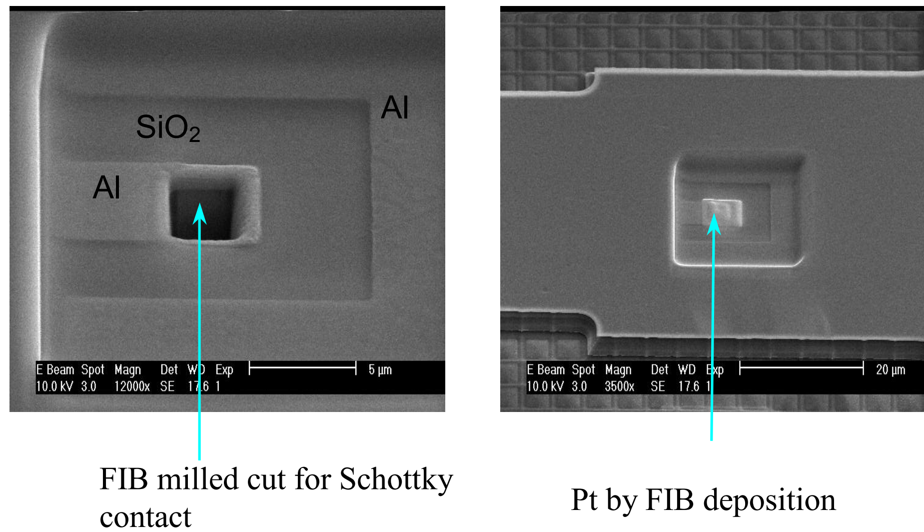


Figure 4.8: SEM pictures of the fabrication process for FIB Schottky diode. (after milling and after deposition)

thin oxide layer and to open a rectangular hole, which exposed the silicon substrate for Schottky contacts. As a final step, Platinum was deposited by FIB ion induced deposition. Figure 4.7 and 4.8 show the processing steps and SEM pictures for each step. An FEI Dual beam 620 was used for FIB milling and ion induced deposition. N-type Schottky diodes with contact areas of 8µm^2 (4µm x 2 µm) and 15µm^2 (2 contacts in parallel each 3µm x 2.5µm) on n-well and a p-type Schottky diode with contact area of 4µm^2 (2µm x 2µm) on p-substrate were fabricated.

To test cutting ohmic contacts and adding Schottky contacts on a CMOS chip, metal-to-nSi-to-n+Si-to-metal structures without any process modification, which was explained in chapter 3.2, was designed. Neither p-substrate nor n-well-to-metal contacts fabricated by these processes were Schottky diodes but rather ohmic contacts. The standard CMOS process does not allow any Schottky contact because either p-type or n-type are automatically implanted on any contact site. These

contacts are supposed to be ohmic to fabricate linear resisters on a chip. A contact site for the post fabrication of the Schottky diode was selected to cut the ohmic contact and to make a Schottky contact by FIB. FIB milling was used to cut the ohmic

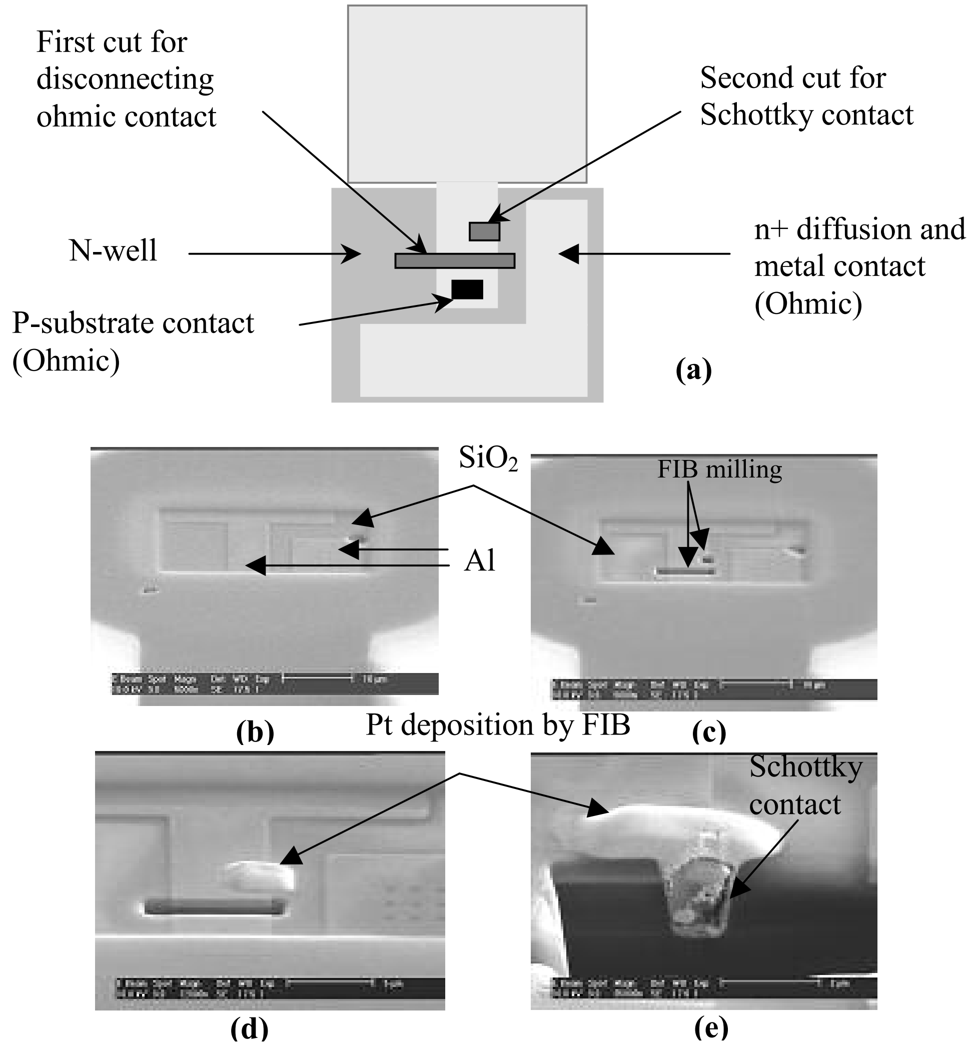


Figure 4.9: Layout and SEM image of an n-type Schottky diode fabrication steps by FIB. (a) FIB milling locations for cutting ohmic contact and milling for Schottky diode fabrication. (b) Etch Silicon Nitride and Silicon oxide to expose metal layer by RIE and FIB milling (c) Disconnect existing ohmic contact (long cut) and define 2µm x 2µm rectangular area by FIB milling (d) Deposit platinum by FIB ion induced deposition (e) Cross-section of a FIB-made contact (cross-sectioned after measurement and burned out) and the “U” shaped Pt filling the via made a Schottky contact to silicon substrate.

contact and to open a rectangular hole, which exposed the silicon substrate for a Schottky contact, and platinum was deposited. (Figure 4.9)

4.2.2 Measured result

The RF power detecting characteristics were measured by the direct injection of RF power through the Cascade ACP-150 probe. Figure 4.10 shows the block diagram of the experimental setup. As a signal source we used the Agilent 83731B RF signal generator, which can generate a signal in the frequency range of 1GHz to 20GHz and maximum power level of 15dBm. Figure 4.11 shows I-V curves of fabricated Schottky diodes. From these curves the series resistance of lightly doped n layer was calculated to be 227Ω defined as the slope between 4 and 5V, and the measured junction capacitance was 627fF at zero bias condition. For p-type diode, the series resistance was calculated to be 903Ω, which is bigger due to smaller contact area,

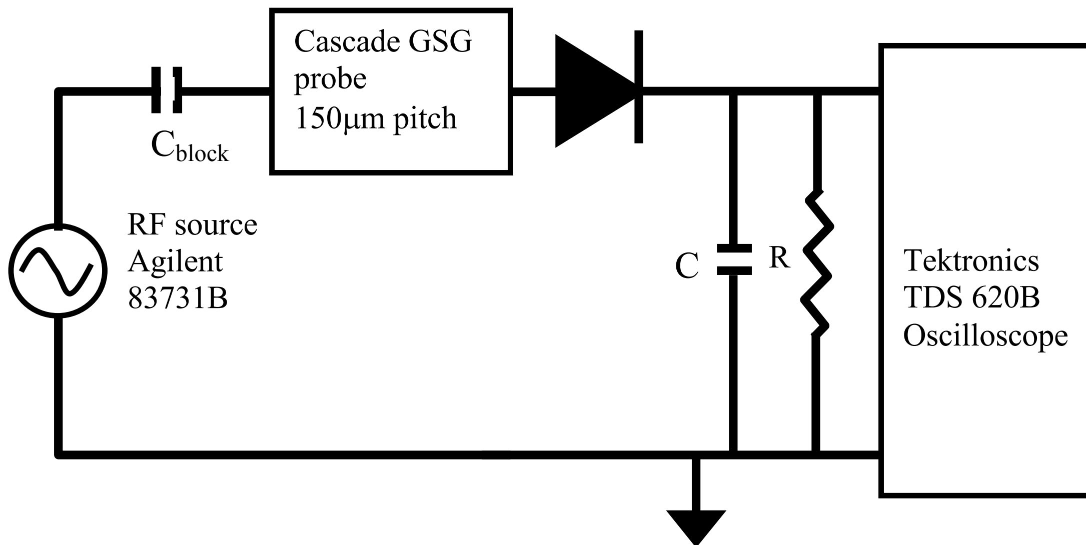


Figure 4.10: RF direct injection measurement setup: RF source generates a signal from 1GHz to 20GHz at a maximum power level of 15dBm. Cascade probe has 150μm pitch with Ground-Signal-Ground configuration. As a load, a 8pF and 10MΩ probe was used(C= 8pF, R =10MΩ). C_{block} is a DC blocking capacitor.

lower carrier mobility, and different barrier heights between n-type and p-type Schottky contact to platinum. Figure 4.12 and 4.13 show the measured result of the RF power direct injection to a Schottky diode through the ground-signal-ground (GSG) pads. Figure 4.12 shows the measured result of the power sweep for three diodes at the power level of –15dBm to 15dBm for the 15μm^2 n-type Schottky diode and 0dBm to 15dBm for the 6μm^2 n-type Schottky diode and the 4μm^2 p-type Schottky diode at 1GHz, 3GHz,

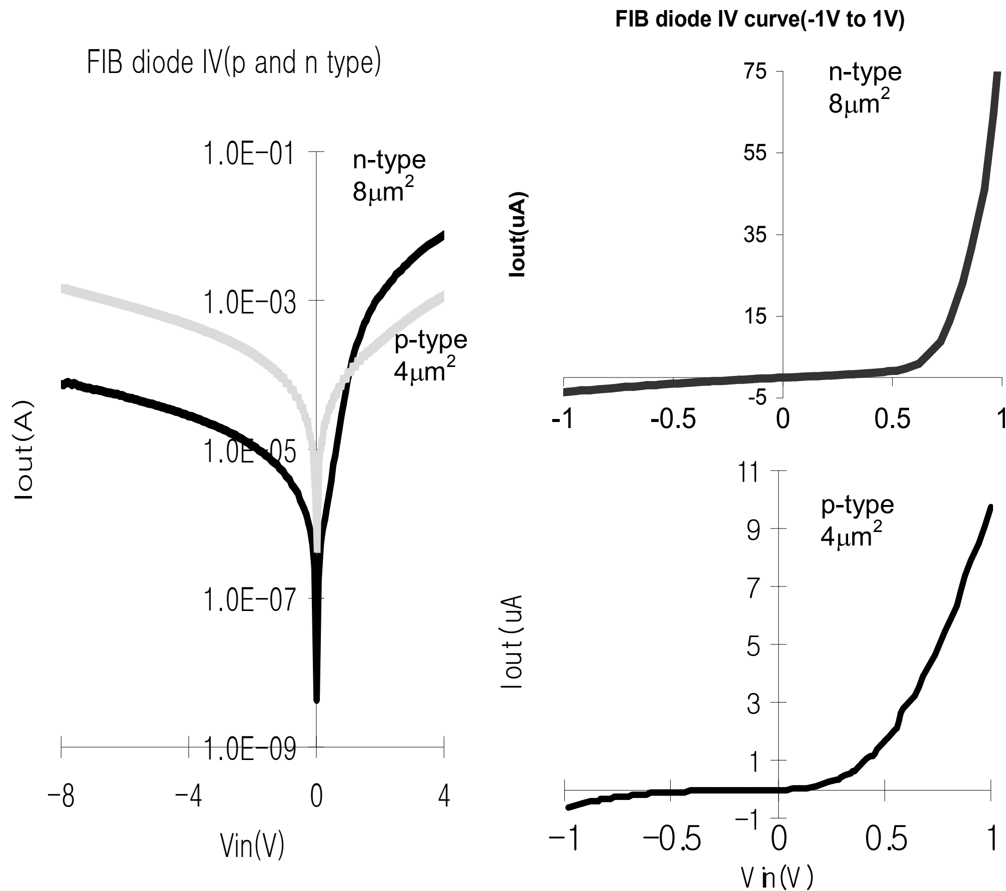
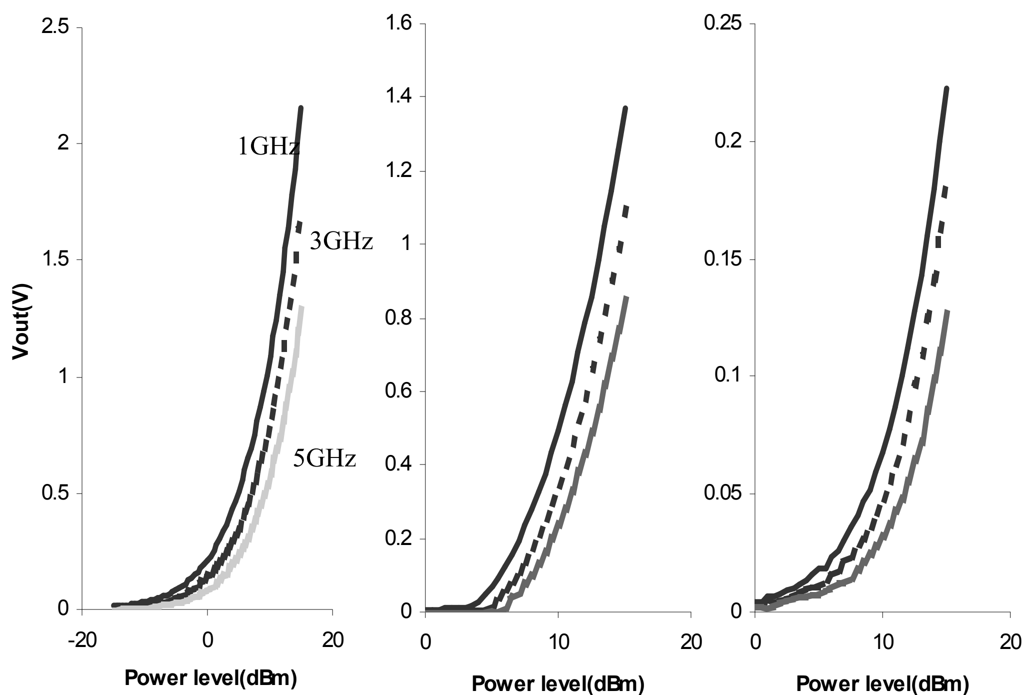
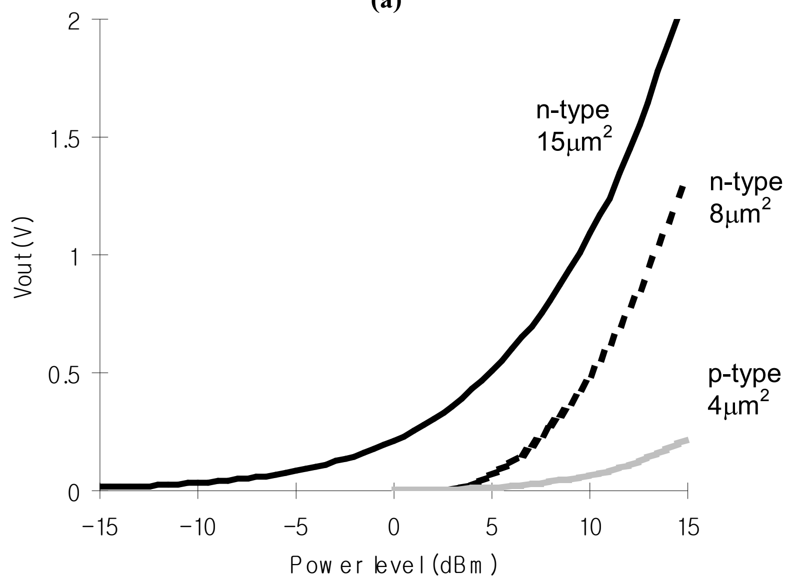


Figure 4.11: Measured result of FIB Schottky diodes: IV curves of the n-type Schottky diode with 8μm^2 contact area and p-type diode with 4μm^2 contact area. Due to tunneling at high reverse bias at p-type diode, reverse leakage current increased.



(a)



(b)

Figure 4.12: (a) Power sweep from –15dBm to 15dBm at 1GHz, 3GHz, and 5GHz for three diodes: n-type 15μm^2 diode, 6μm^2 diode, and p-type 4μm^2 Schottky diode, respectively. (b) Power sweep for three diodes at 1GHz

and 5GHz. This result shows quadratic curves and its dynamic range was 30dBm at zero bias condition. 30μs and 10μs pulse width and 10ms period RF pulses were injected for power sweep experiment. 30μs RF pulses were injected only to the 15μm^2 n-type Schottky diode due to its longer response time (i.e. the rise time of the rectified output pulse) of 6μs. Figure 4.13 shows the measured results of three frequency sweeps from 1GHz to 15GHz at an input power level of 15dBm. When the contact area decreased, the rectified output voltage decreased due to the increase of the junction resistance. Even though the smaller contact area Schottky diodes showed the lower rectified voltage, since this diode has much shorter pulse response time than that of bigger contact area Schottky diode, smaller diode has a better performance for detecting the RF pulse signal. The pulse response time at 1GHz 15dBm pulse input was 192 ns for the 4μm^2 p-type diode, 2.56 μs for the 8μm^2 n-type diode, and 6μs for

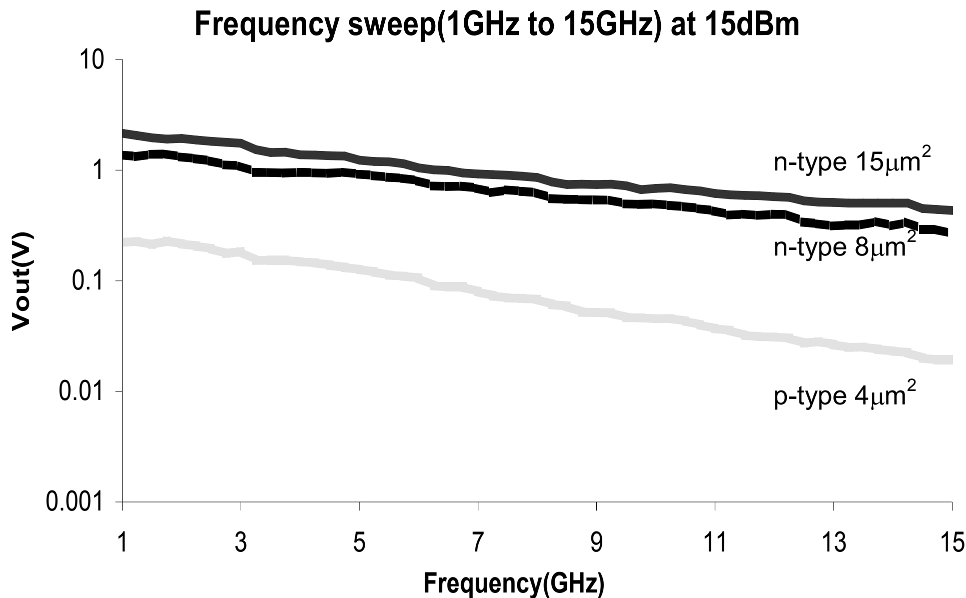


Figure 4.13: Frequency sweep from 1GHz to 15GHz at the power level of 15dBm

the 15 μm^2 n-type diode. This result shows the smaller area p-type Schottky diode power detector has better performance in the RF pulse detection, though its rectified voltage was about 10 times smaller than that of the 15μm^2 n-type diode. The smaller rectified voltage is, the shorter the pulse response time Schottky diode has. This fact indicates that even p-type Schottky diode has lower rectification due to higher junction and series resistance, if contact area is small enough, it can be used as a RF pulse power detector.

4.2.3 Bridge shaped FIB Schottky diode

A typical process for fabricating a Schottky diode for high frequency applications is using molecular beam epitaxy (MBE) for growing a very thin, 0.3μm, lightly doped

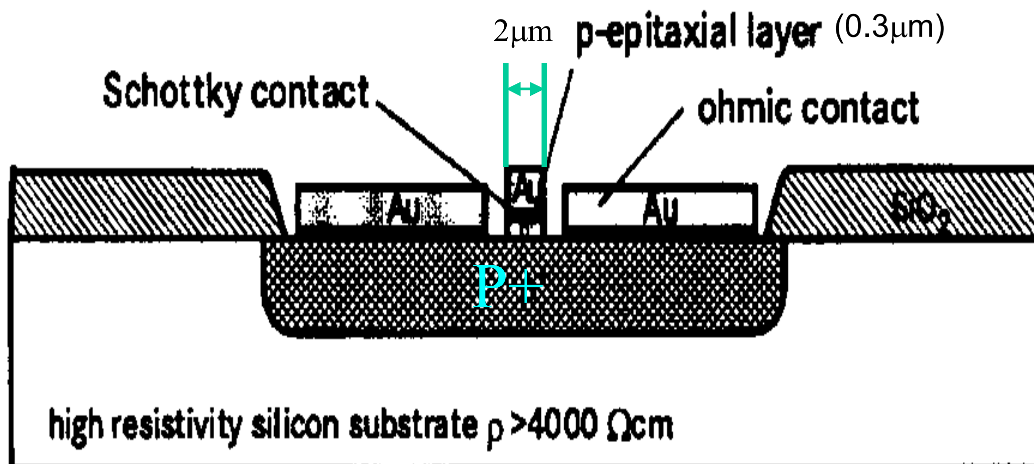


Figure 4.14: Coplanar Si-MBE Schottky diode developed for rectifying antennas by Strohm et al.

* Ref: K.M. Strohm, J. Buecher, & E. Kasper , Daimler Benz Research, Ulm, IEEE Trasn. MTT Vol.46, 669, (May, 1998)

layer on top of the highly doped layer. Strohm et al. have fabricated a Silicon Schottky diode by using Si-MBE process to make a Schottky contact, and the reported operating frequency was 93GHz (Figure 4.14) [35]. To make a similar structure as the reported Si-MBE Schottky diode, a bridge shaped FIB Schottky diode was designed and fabricated. Tilted FIB milling was used to make undercut triangular bridge shaped Schottky contacts on the fabricated n-type Schottky diode with 8μm^2 contact area described in the previous chapter. Figure 4.15 shows the processing steps and the SEM pictures of the fabricated bridge shapted Schottky diode. Contact area was measured to be 1μm^2. The measured result showed that the bridge shaped Schotty diode had 170ns pulse response time, (Figure 4.16) 25dBm dynamic range, and began to detect –10dBm input power level. Because of the increase of the junction resistance, the frequency response of the bridge shaped Schottky diode became worse than that of the Schottky diode without undercut. This is because the contact area is not large enough to ignore the reverse tunneling current. Even though the frequency response became worse than before, the pulse response time was significantly reduced from 2.6μs to 170ns due to the smaller contact capacitance.

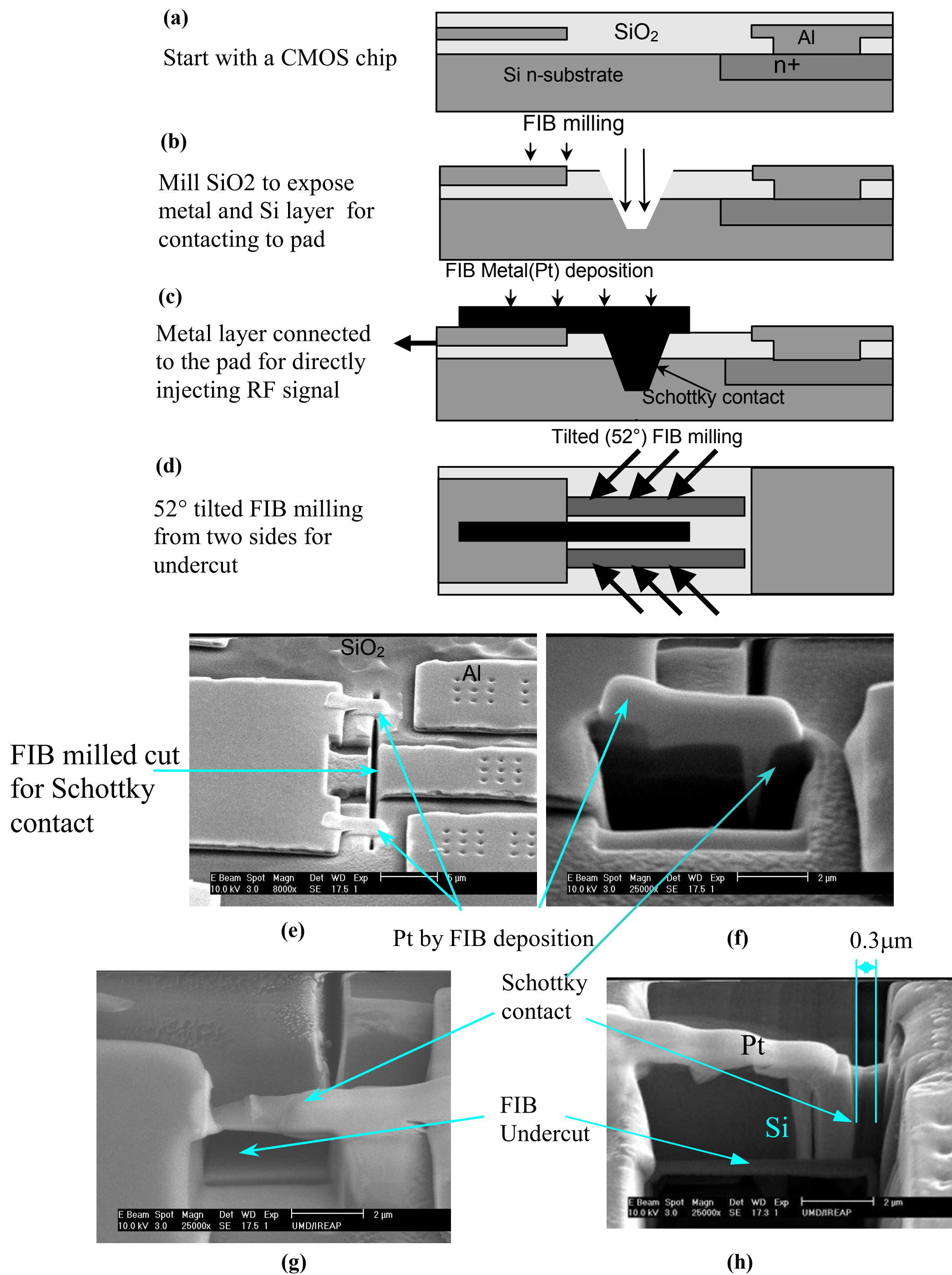


Figure 4.15: FIB Schottky diode fabrication, (a), (b), and (c): cross-section view (d): top view, and SEM images of a FIB processed bridge shaped diode, (e) Milling silicon and Platinum deposition, (f) Cross section of the fabricated device: refer (c), (g) Undercut by tilted FIB to minimize capacitance, (h) Another bridge shaped diode with 0.3um of lightly doped layer

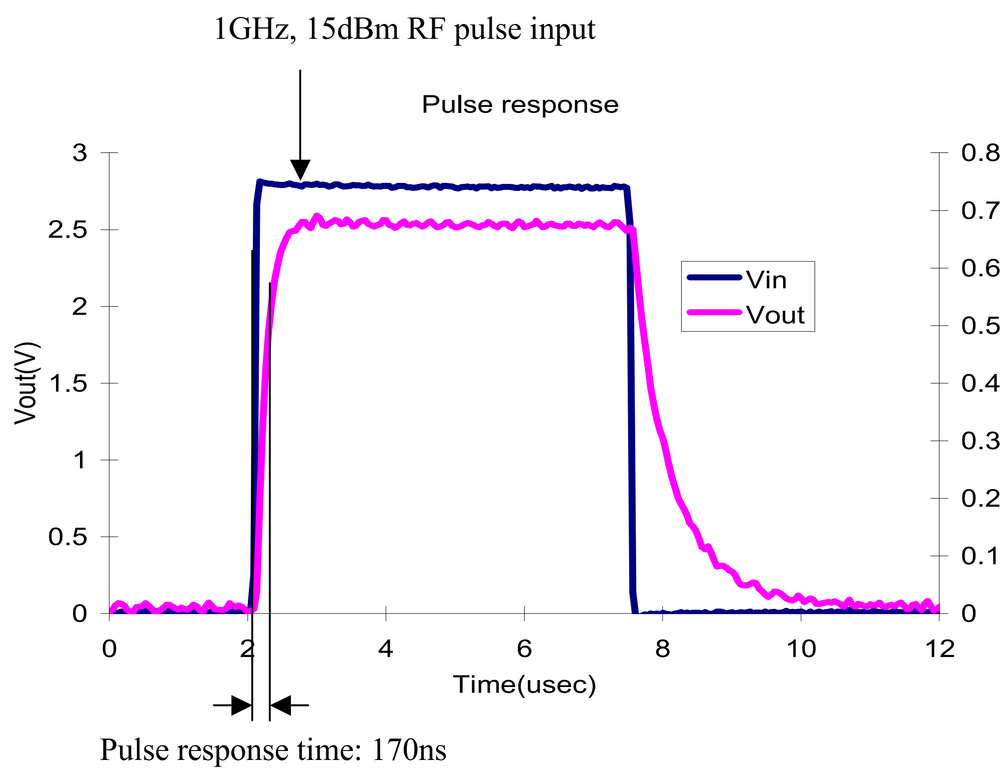


Figure 4.16: RF pulse response of Bridge shaped FIB Schottky diode, the pulse response time was 170ns

Chapter 5: MOSFET power detector circuits

A simple diode connected MOSFET can be used as a rectifier. However, its turn on voltage, usually 1V, is too high for small microwave signal detection and a bias circuit or a dc source is required to improve the sensitivity. Rantni et al. suggested a MOSFET power detector by adding dc sources to bias the gate of the MOSFET [36]. However, since their approach required a huge MOSFET, the pulse response time, which is the most important parameter for detecting RF pulses, was estimated to be 10's of μs. Their approach was also very sensitive to the variation of the bias voltage at the gate of the MOSFET. To minimize these problems, MOSFET power detector circuits were developed and fabricated through a 0.5μ CMOS process.

5.1 Diode connected MOSFET with a bias circuit

To increase the sensitivity of a simple diode connected (gate connected to drain) MOSFET, a bias circuit was added. Figure 5.1 shows the proposed circuit. M3 is diode connected nMOSFET and M1 supplies the bias current I_1.

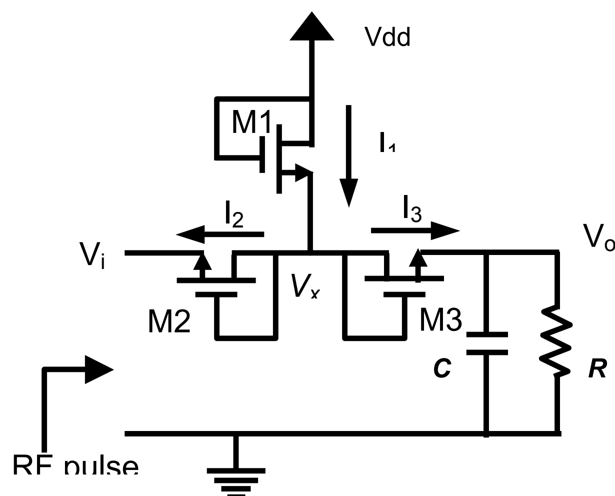


Figure 5.1: MOSFET power detector circuit: depends on the polarity of RF input, bias current I_1 flows to one of M_2 or M_3.

5.1.1 Operation

When the input voltage Vi is less than 0, and I_1 is equal to I_2, V_{xo} (V_x when V_i is equal to 0V) can be calculated and I_3 is small enough to be neglected by the following equations.

$$I_1 = K\frac{w_1}{l_1}(V_{dd} - V_{xo} - V_T)^2 \qquad I_2 = K\frac{w_2}{l_2}(V_x - V_T)^2$$

$$V_{xo} = \left(\frac{\sqrt{l_2 w_1}}{\sqrt{l_2 w_1} + \sqrt{l_1 w_2}}\right)V_{dd} + \left(\frac{\sqrt{l_2 w_1} - \sqrt{l_1 w_2}}{\sqrt{l_2 w_1} + \sqrt{l_1 w_2}}\right)V_T \tag{5.1}$$

$$V_o = I_{o3}(e^{\frac{q}{kT}(V_{xo} - V_o)} - 1)R \tag{5.2}$$

Where, K = $\mu C_{ox}q/2kT$, w is the width and *l* is the length of the channel. When Vi becomes bigger than 0V and I_3 is not negligible and the output voltage V_o begins to rise by the following equations.

$$I_2 = K\frac{w_2}{l_2}(V_x - V_i - V_T)^2 \tag{5.3}$$

$$I_3 = K\frac{w_3}{l_3}(V_x - V_o - V_T)^2 \tag{5.4}$$

$$I_1 = K\frac{w_1}{l_1}(V_{dd} - V_x - V_T)^2 = K\frac{w_2}{l_2}(V_x - V_i - V_T)^2 + K\frac{w_3}{l_3}(V_x - V_o - V_T)^2 \tag{5.5}$$

$$V_o = I_3 R \tag{5.6}$$

By solving (3)-(6), Vi and Vo are square functions of V_x.

$$V_o = aV_x^2 + bV_x + c \tag{5.7}$$

$$V_i = a'V_x^2 + b'V_x + c' \tag{5.8}$$

Where a,b,c,a',b', and c' are constants. As a result, the output voltage Vo has a linear dependence on the input voltage Vi by the following equation.

$$V_o = AV_i + B \tag{5.9}$$

Where A is a positive constant and B is a constant and near to 0 when Vi is equal to 0. When Vi is much bigger than 0V, almost all bias current flows to M3, I_1 is equal to I_3, and the output voltage becomes constant, I_3R.

5.1.2 Simulation and DC measured result

Figure 5.2 shows the DC simulation result and the DC measured result of the proposed MOSFET power detector. Both results are seen to agree. For the low input region, Vi is less than 0.7V, the circuit operates in the subthreshold mode, and smooth curve between Vi and Vo was observed.

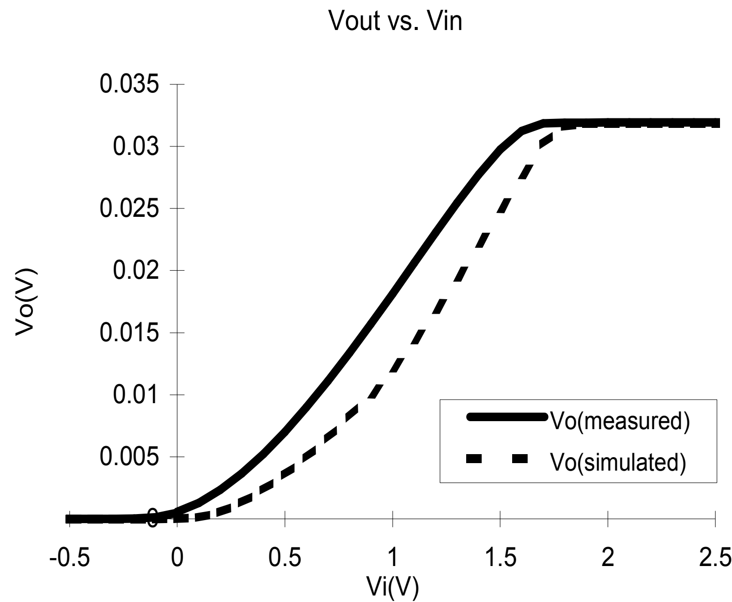


Figure 5.2: Simulated and measured dc curve of a MOSFET power detector. Measured result showed turn on voltage shift to –0.1V.

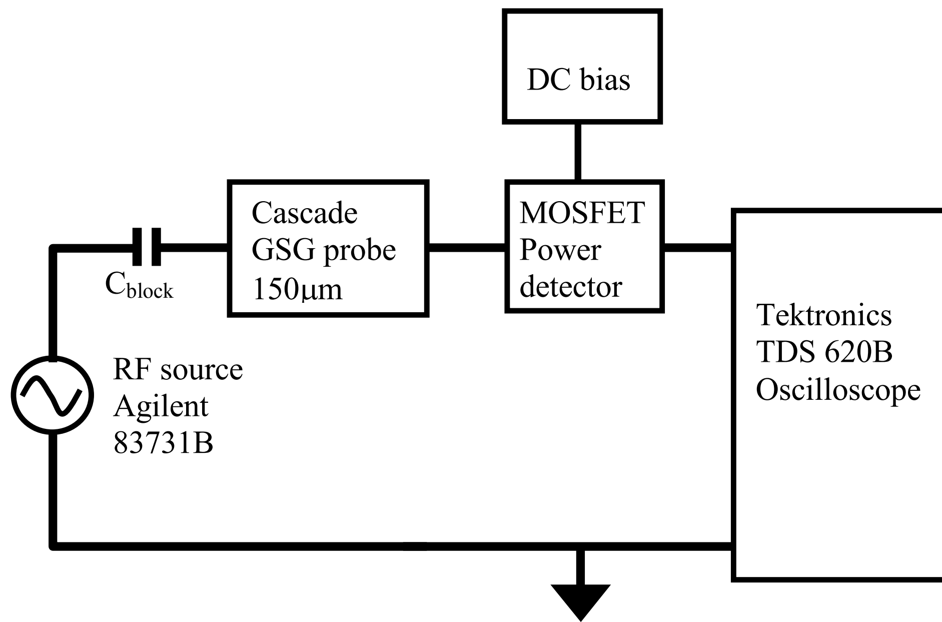


Figure 5.3: Experimental setup for RF burst direct injection with Cascade GSG probe.

5.1.3 Microwave pulse direct injection

The RF power detecting characteristics were measured by the direct injection of RF power through the Cascade ACP-150 probe. Figure 5.3 shows the block diagram of the experimental setup, which is similar to the Schottky diode measurement except an additional voltage source. We used the Agilent 83731B RF signal generator, which has a frequency range of 1GHz to 20GHz and maximum power level of 15dBm. Figure 5.4 and 5.5 show the measured result of the RF power direct injection to the fabricated MOSFET power detector through the ground-signal-ground (GSG) pads. Figure 5.4 shows the measured result of the power sweep from –15dBm to 15dBm for the MOSFET detector circuit with 100kΩ load and –10dBm to 15dBm for 1kΩ load at 1GHz. Both results showed curves of approximately quadratic shapes. RF pulse of

10μs width and 10ms period RF pulses were injected in power sweep experiment. For the MOSFET detector with a 100kΩ load, the dynamic range was 21dBm, and the

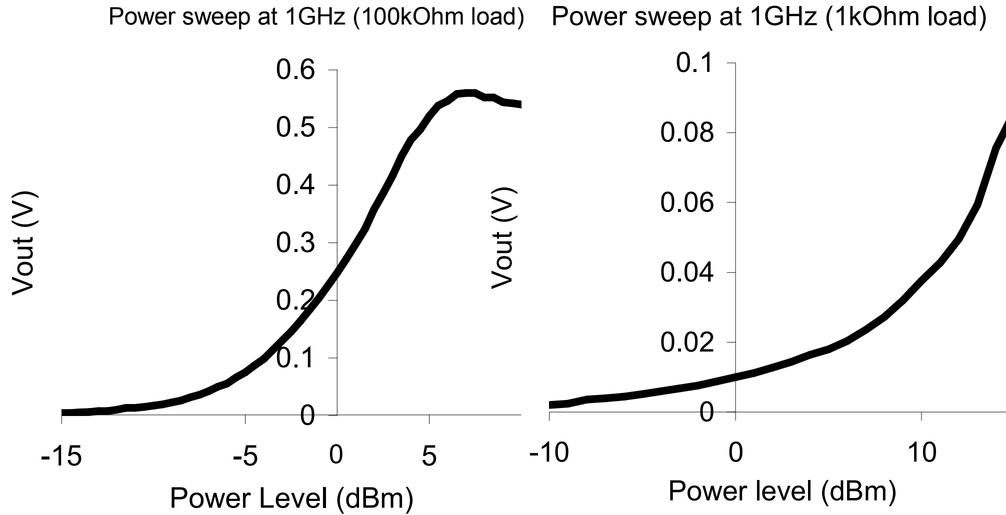


Figure 5.4: Power sweep at 1GHz, RF direct injection to two of the same MOSFET power detectors with a 100kΩ load and a 1kΩ load.

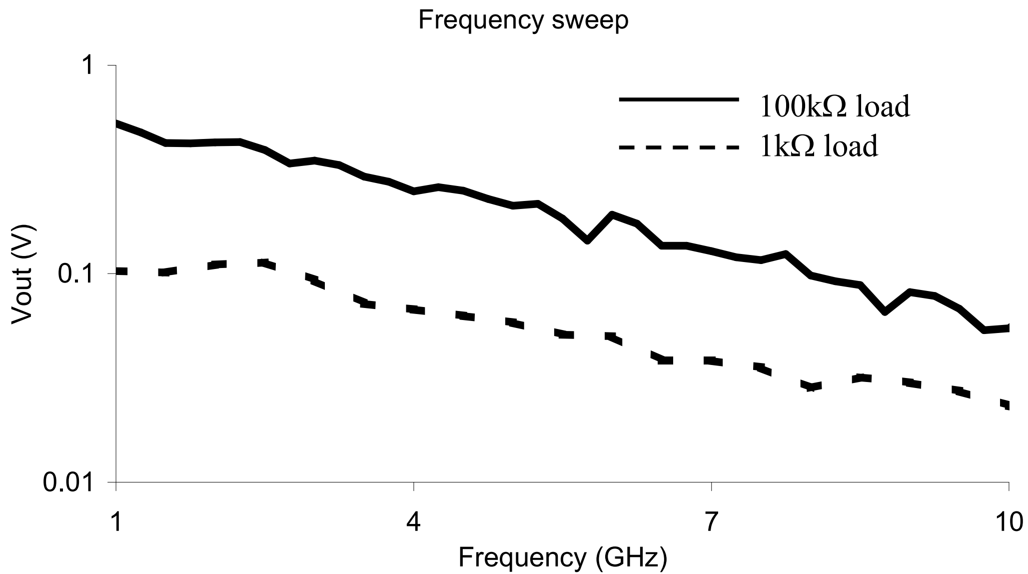


Figure 5.5: Frequency sweep at 5dBm for the MOSFET detector with a 100kΩ load and at 15dBm for the MOSFET detector with a 1kΩ load.

pulse response time was 200ns. Because the supply voltage was limited, the output voltage became saturated, when the input power level was over 6dBm. For the MOSFET detector with a 1kΩ load, the dynamic range was 25dBm, and the pulse response time was 52ns. Even though the output voltage was small due to the low power efficiency, the pulse response time was shorter and the dynamic range increased. Figure 5.5 shows the measured results of the frequency sweep from 1GHz to 10GHz at the input power level of 5dBm for the 100kΩ load MOSFET and 15dBm for the 1Ω load MOSFET. The MOSFET detector with a higher load resistance showed faster roll off.

5.2 Full-wave rectifier circuit

For more sensitive microwave detection and wide dynamic range, a full-wave rectifier circuit was developed and fabricated. Figure 5.6 shows the proposed

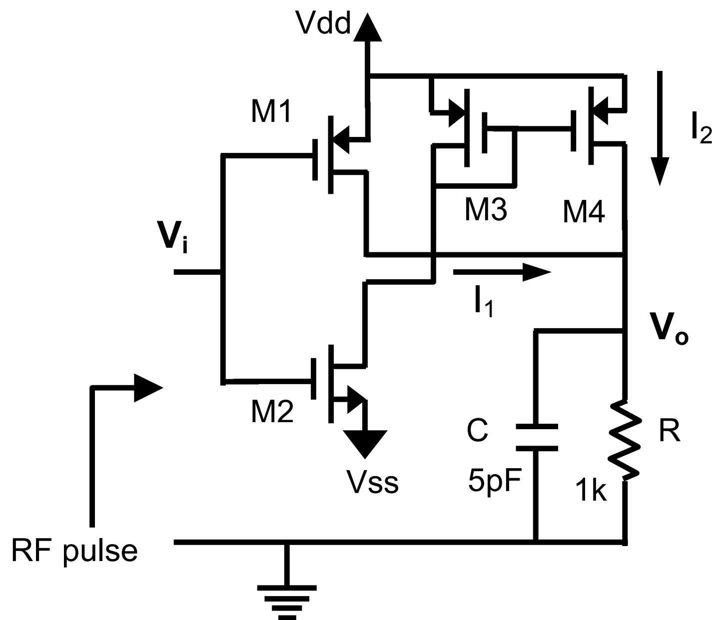


Figure 5.6: Full-wave rectifier circuit

MOSFET full-wave rectifier circuit. When an microwave input signal is applied to the gates of the pMOSFET, M_1, and the nMOSFET, M_2, the positive microwave part of the RF cycle turns on M_2, turns off M_1, and I_2 flows to the load, while the negative part of the RF turns on M_1, turns off M_2, and I_1 flows to the load. As a result, the load current always flows in one direction and is proportional to the absolute value of the microwave input.

5.2.1 Operation

The operation of the proposed full-wave MOSFET power detector circuit (Figure 5.6) can be divided by two parts. The first part is nfet with negative bias and p-type

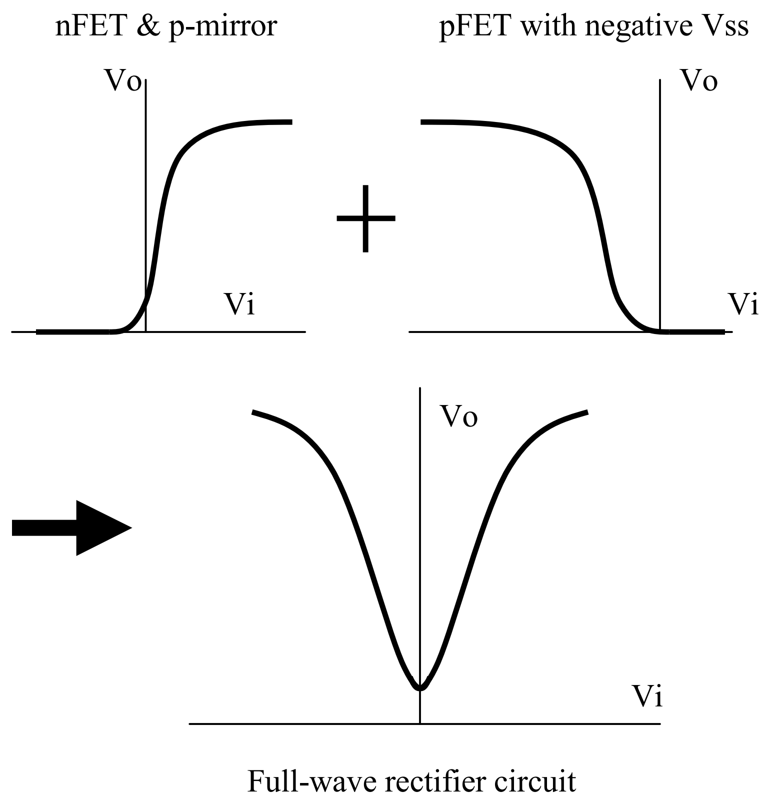


Figure 5.7: Full-wave rectifier DC curve consists of two DC curves of nFET & p-mirror and pFET with negative Vss.

current mirror and another is only one pfet. (Figure 5.7)

When the input is between Vss and Vss + V_{Tp}, M_2 is in the triode region. I_2 is given by the following equation.

$$I_2 = K_2\left(2\left(V_i - V_{ss} - V_{Tn}\right)\left(V_x - V_{ss}\right) - \left(V_x - V_{ss}\right)^2\right) \quad (5.10)$$

When M_2 is in the subthreshold region, the following equations apply to I_2.

$$I_2 = I_{o2} e^{\frac{qk}{kT}V_i} \left(e^{\frac{-q}{kT}V_x} - e^{\frac{q}{kT}V_{ss}}\right) \quad (5.11)$$

When M_1 is in the saturation region, the following equation applies to I_1.

$$I_1 = K_1 (V_i - V_{dd} - V_{Tp})^2 \quad (5.12)$$

The output voltage will be $Vo = (I_1 + I_2)R$, and I_1 is much bigger than I_2. As a result the output voltage depends on I_1, which linearly depends on the input voltage.

When Vi is bigger than Vss plus Vt, M2 is now in the saturation region and the following equations apply to I1 and I2.

$$I_1 = K_1 (V_i - V_{dd} - V_{Tp})^2 \quad (5.13)$$

$$I_2 = K_2 (V_i - V_{ss} - V_{Tn})^2 \quad (5.14)$$

Where, $K_1=K(w_1/l_1)$ and $K_2=K(w_1l_2w_3/l_1w_2l_3)$. The output voltage Vo is the load resistance times the sum of two currents and can be calculated by the following equations.

$$\begin{aligned} Vo &= (I_1 + I_2)R \\ &= \left(K_1 (V_i - V_{dd} - V_{Tp})^2 + K_2 (V_i - V_{ss} - V_{Tn})^2\right)R \quad (5.15) \\ &= \left((K_1 + K_2)V_i^2 - 2\left(K_1\left(V_{Tp} + V_{dd}\right) + K_2\left(V_{ss} + V_{Tn}\right)\right)V_i + K_1\left(V_{Tp} + V_{dd}\right)^2 + K_2\left(V_{ss} + V_{Tn}\right)^2\right)R \end{aligned}$$

Equation 5.15 can be rewritten as the following equation.

$$V_o = R(K_1 + K_2)\left(V_i - \frac{K_1(V_{Tp} + V_{dd}) + K_2(V_{ss} + V_{Tn})}{K_1 + K_2}\right)^2$$

$$+\left(K_1(V_{Tp} + V_{dd})^2 + K_2(V_{ss} + V_{Tn})^2 - \frac{1}{K_1 + K_2}\left(K_1(V_{Tp} + V_{dd}) + K_2(V_{ss} + V_{Tn})\right)^2\right)R$$

$$= R(K_1 + K_2)(V_i - A)^2 + B \tag{5.16}$$

By setting A to zero, the output is proportional to the square of the input plus offset, B. To make A to zero, the following equation is used.

$$\frac{K_1}{K_2} = \frac{-(V_{ss} + V_{Tn})}{V_{dd} + V_{Tp}} \tag{5.17}$$

If K_1 is equal to K_2, Vss is set to be Vdd + V_{Tp}-V_{Tn}.

When Vi is smaller than Vdd and bigger than Vdd-V_{Tn}, M_1 is operated in the triode region or in the subthreshold region and M_2 is in the saturation region. I_1 and I_2 are determined by the following equations.

$$I_1 = I_{o1} e^{\frac{qk}{kT}V_i}\left(e^{\frac{-q}{kT}V_o} - e^{\frac{q}{kT}V_{dd}}\right) \tag{5.18}$$

or

$$I_1 = K_1\left(2(V_i - V_{dd} - V_{Tp})(V_o - V_{dd}) - (V_o - V_{dd})^2\right) \tag{5.19}$$

$$I_2 = K_2(V_i - V_{ss} - V_{Tn})^2 \tag{5.20}$$

The output voltage will be $Vo = (I_1 + I_2)R \approx I_2 R$, since I_2 is much bigger than I_1. As a result the output voltage depends on only I_2, which linearly depends on the input voltage.

5.2.2 Simulation and measured result for DC curve

Figure 5.8 shows the DC simulation result and the DC measured result of the proposed full-wave rectifier power detector. The measured result showed 0.2V shift to positive x-axis due to the mismatch between the SPICE transistor models and the actual transistors.

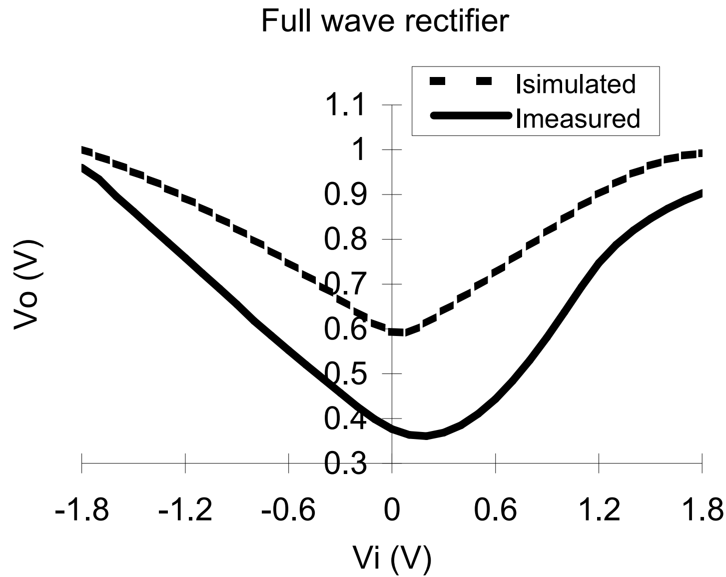


Figure 5.8: Simulated and measured DC curve (Vi vs. Vo)

5.2.3 Microwave pulse direct injection

The RF power detecting characteristics were measured by the direct injection of RF power through the Cascade ACP-150 probe. The same experimental setup as Figure 5.3 was used with an additional voltage source, Vss in Figure 5.6. Figure 5.9 and 5.10 show the measured result of the RF pulse direct injection to the fabricated MOSFET power detector through the ground-signal-ground (GSG) pads. Figure 5.9 shows the measured result of the power sweep at the power level of –15dBm to

15dBm for the full-wave rectifier circuit at 1GHz. 10μs pulse width and 10ms period RF pulses were injected for power sweep experiment. The measured result showed quadratic curves, the dynamic range was 22dBm, and the pulse response time was 101ns. Figure 5.10 shows the measured results of the frequency sweep from 1GHz to 10GHz at the input power level of 15dBm. The result showed much flatter frequency response than that of the previous MOSFET detectors in chapter 5.1.

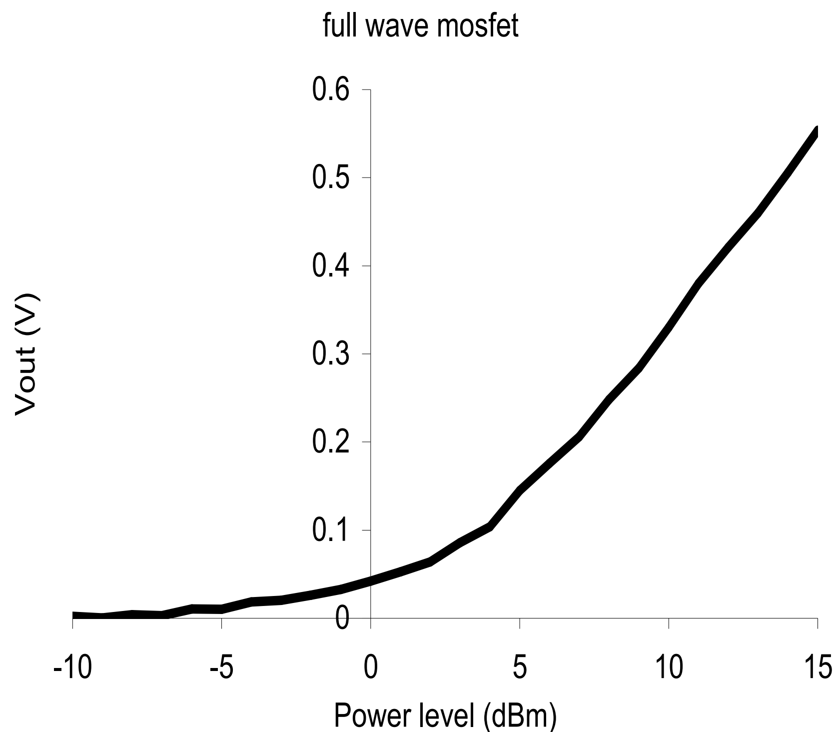


Figure 5.9: Power sweeps from –10dBm to 15dBm at 1GHz, RF direct injection to the full-wave rectifier circuit

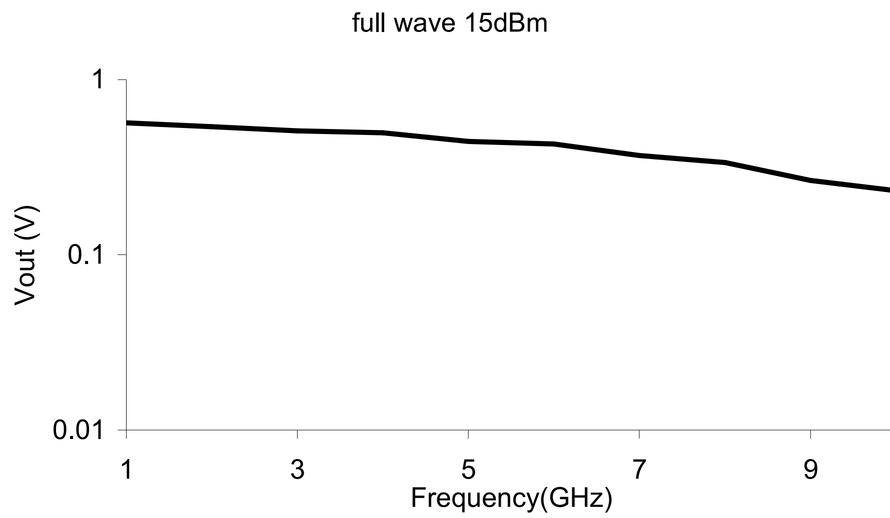


Figure 5.10: Frequency sweep from 1GHz to 10GHz at 15dBm for the full-wave rectifier circuit

Chapter 6: Microwave radiation measurement

To illustrate their applications for picking up RF signal, the fabricated detectors were connected to a patch antenna on a silicon surface and to a metal line on a circuit board. Microwave pulses were radiated on the chip with a horn antenna in a test metal box and on the board with a horn antenna in an anechoic chamber. From the measured results, the antenna gain was calculated.

6.1 RF radiation on a silicon wafer

A lab-made Schottky diode with 2μm x 2μm contact area was tested with RF irradiation under a horn antenna. A small patch antenna (750μm x 300μm) on a silicon wafer mounted in a big box structure (12cm x 10cm x 6cm) were used. (Figure 6.1) Due to the small size of the patch antenna structure, propagation loss, and coupling loss, we expected to need large RF power levels. The power level was high enough so that the patch antenna and the Schottky diode picked up the irradiated microwave signal. We were able to calculate the antenna gain by comparing the radiation result to the direct injection result.

6.1.1 Experiment

An x-band horn antenna was mounted on top of the metal box shown in Figure 6.1. The silicon wafer with the patch antenna, which has a 0.6μm oxide layer on top, was mounted at the bottom of the box. The Schottky diode was connected at the end of the patch antenna, and a 10pF capacitor was connected to the output of the Schotky diode. A coaxial cable was used to connect the output and the oscilloscope with 1pF and 1MΩ load. An RF signal was generated by the Agilent 83731B microwave signal

generator and amplified by an RF amplifier with 40dB gain. The power level of the RF radiation was between 25dBm and 45dBm, and the frequency of the RF signal was varied from 1GHz to 20GHz. Since the horn antenna was designed for x-band

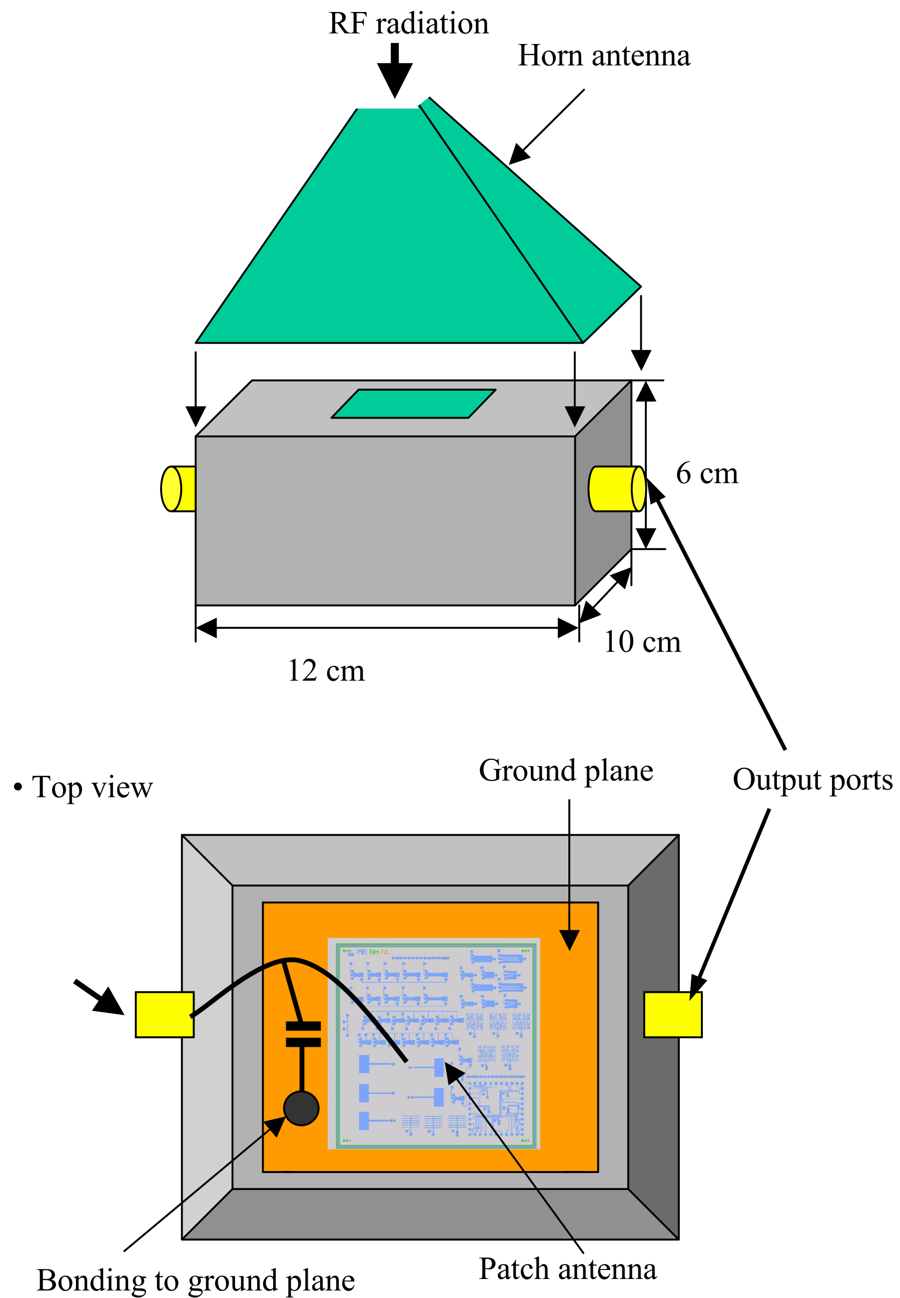


Figure 6.1: RF radiation test on a patch antenna structure on a silicon wafer

and was expected to be most efficient in the frequency range between 8GHz and 12.5GHz. The dc output was measured from the output ports as shown in Figure 6.1.

6.1.2 Measured result

Figure 6.2 shows the frequency sweep from 9.5GHz to 20GHz at 40dBm power level. There was no dc output under 9.5GHz. The measured result shows multiple peaks at several frequencies due to the mismatch, propagation loss, and coupling loss. Figure 6.3 shows the power sweep from 25dBm to 45dBm at 12GHz. The result shows quadratic curve, which means that the operating voltage of the diode is lower than the turn-on voltage. Since the power detector picked up the irradiated RF signal up to 12GHz, the cut-off frequency is assumed to be higher than 12GHz. After irradiating at 12GHz and 45dBm RF signal for 2 minutes, the metal line between the patch antenna and the Schottky diode melted down and no detection was observed. This fact supports that the patch antenna picked up the RF signal, and the RF signal coupled into the patch antenna was rectified by the Schottky diode power detector.

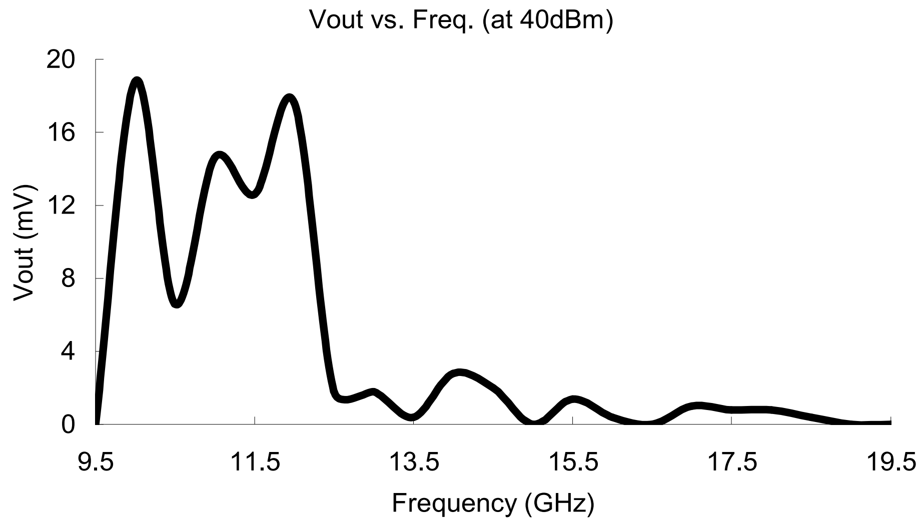


Figure 6.2: Measured result of irradiation test: Frequency sweep (9GHz to 19.5GHz) with a constant RF power level of 40dBm

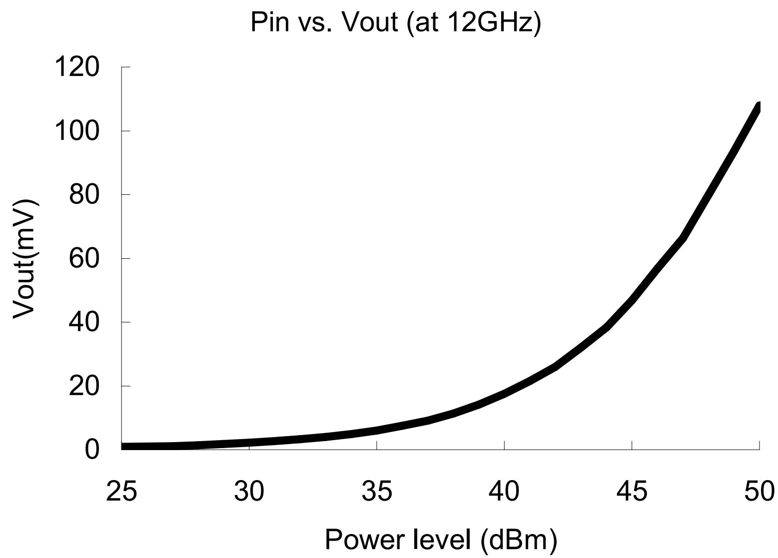


Figure 6.3: Measured result of irradiation test: Power sweep (25dBm to 55dBm) with a constant RF frequency of 12GHz

6.2 RF radiation on a board

To illustrate an application of the CMOS Schottky diode power detectors on a circuit board, a fabricated CMOS detector was connected to a metal line on a circuit board and an RF pulse was radiated on the board with a horn antenna in an anechoic chamber. (Figure 6.4)

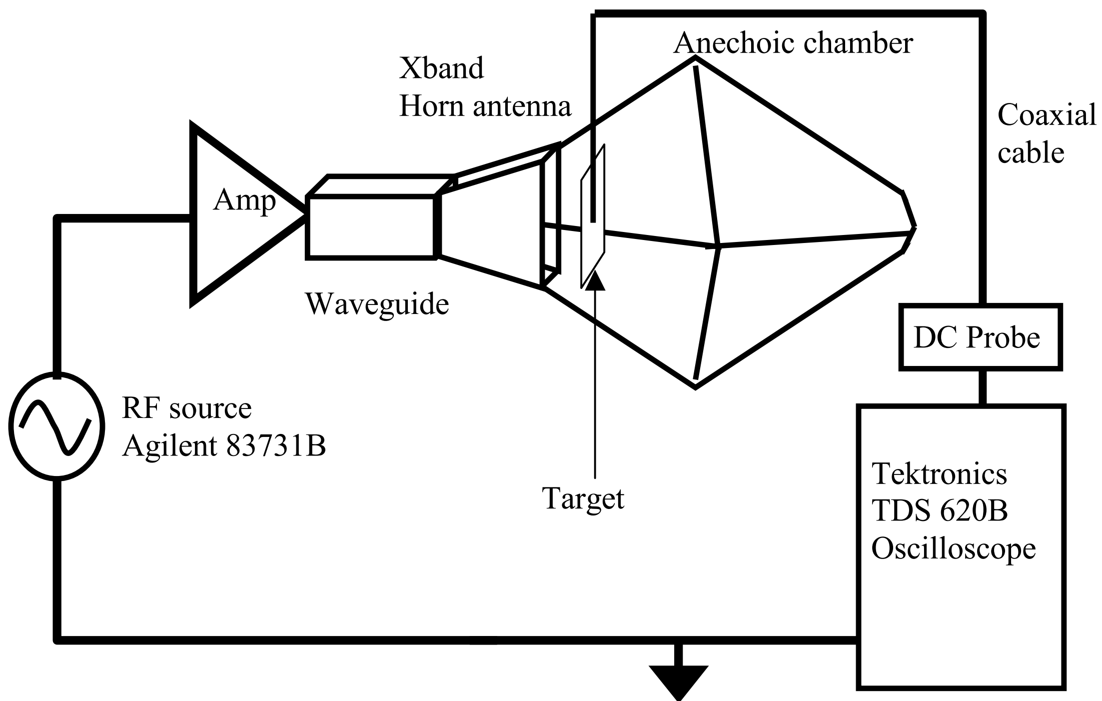


Figure 6.4: The experimental setup for RF radiation test. The target is a circuit board with power detector connected to a metal line on a board.

6.2.1 Experiment

An x-band horn antenna was mounted at the end of the anechoic chamber, and an amplified RF signal was irradiated to the circuit board. To minimize the free space transmission loss, the distance between the horn antenna and the circuit board was

1cm. The circuit board had several metal lines, and one of them was connected to the input of the Schottky diode power detector, which is packaged in a 40pin DIP package. Figure 6.5 shows the front-side view, where the RF signal is irradiated, and the back-side view of the circuit board. The Schottky diode was fabricated by a 0.5μm CMOS process and packaged in a 40pin package through the MOSIS service. To prevent the direct coupling of the irradiated power into the power detector, the

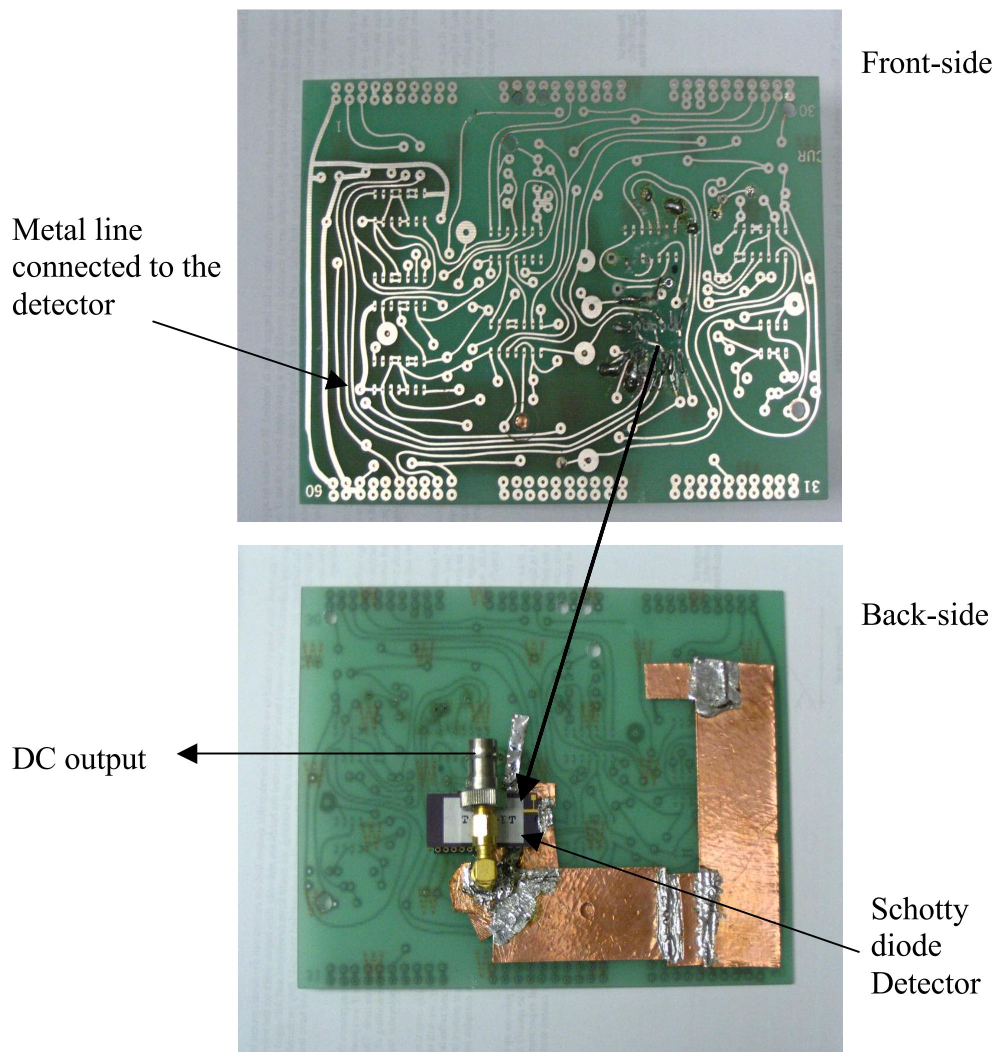


Figure 6.5: The circuit board for RF radiation test. The front-side view, where the RF signal is irradiated, and the back-side view of the circuit board.

detector was mounted on the back-side of the circuit board. After punching a hole between the detector and an end of the metal line, the metal line was soldered to connect the input pin of the power detector. As a ground plane was needed, a copper tape was attached to the back-side of the metal line and connected to the ground pin of the power detector. The output pin of the detector connected to the oscilloscope thorough an SMA adaptor and a coaxial cable. The RF signal was generated by the Agilent 83731B microwave signal generator and amplified by an RF amplifier with 40dB gain. The irradiated power level was from 18dBm to 30dBm and the frequency of the RF signal was from 1GHz to 20GHz. Since the horn antenna was designed for x-band and was expected to be most efficient in the frequency range between 8GHz and 12.5GHz.

6.2.2 Measured result

Figure 6.6 shows two frequency sweeps from 9.2GHz to 10.6GHz at 30dBm power level. There was no dc output under 9.5GHz and above 10.6GHz, since the horn antenna had a band pass filter with a frequency range between 9.5GHz to 10.5GHz. Since the metal line was not a designed antenna but an arbitrary shaped metal line, there were multiple peaks at several frequencies. After measuring, the metal line was cut and tested again to know if the actual power the metal line accepted. The solid line shows the measured result of the power detector connected to the metal line, and the broken line shows the measured result of the power detector without the metal line. The result shows that the connected metal line, which acts like an antenna, was tuned at 10.2GHz. Figure 6.7 shows two power sweeps from 18dBm to 30dBm at 10.2GHz. The result shows that at least 24.5dBm of irradiated power is

required to turn-on the diode connected to the metal line and to show an antenna-like behavior. The output with metal line was similar to a quadratic curve. Except for the frequency near 10.2GHz, we cannot assume the irradiated RF signal was coupled into the metal line, since the measured result for both detector with metal line and detector without metal line cases showed almost the same except at around 10.2GHz. The DC output voltage may come from other areas, such as the coaxial cable or ground plane.

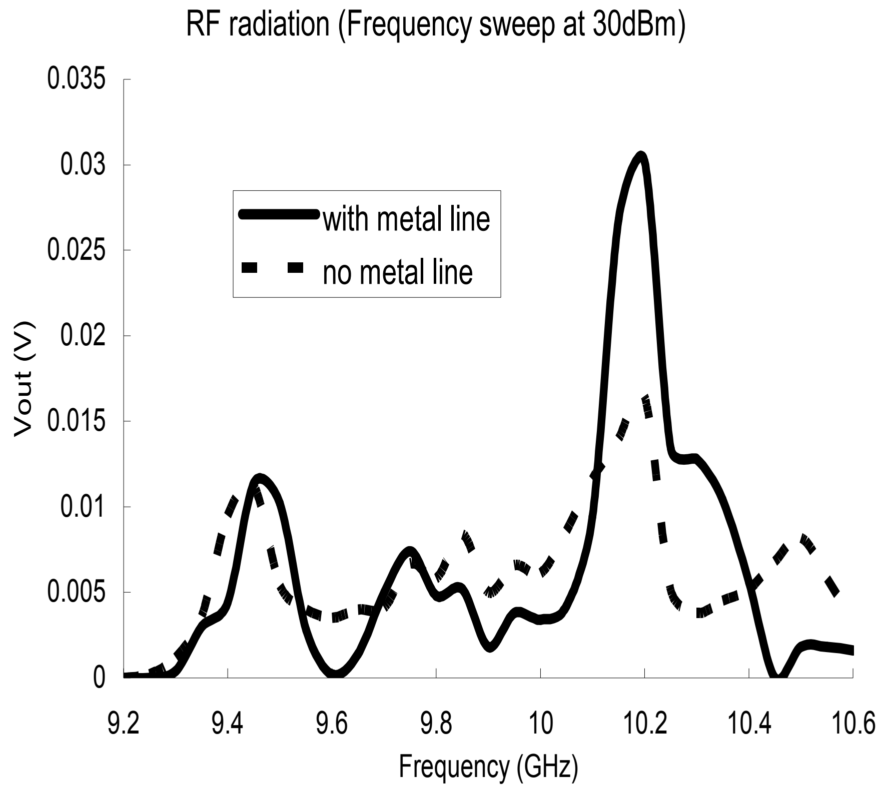


Figure 6.6: RF pulse radiation, two frequency sweeps from 9.2GHz to 10.6GHz at 30dBm. The solid line is for the detector with a metal line, and the broken line is for the detector without a metal line

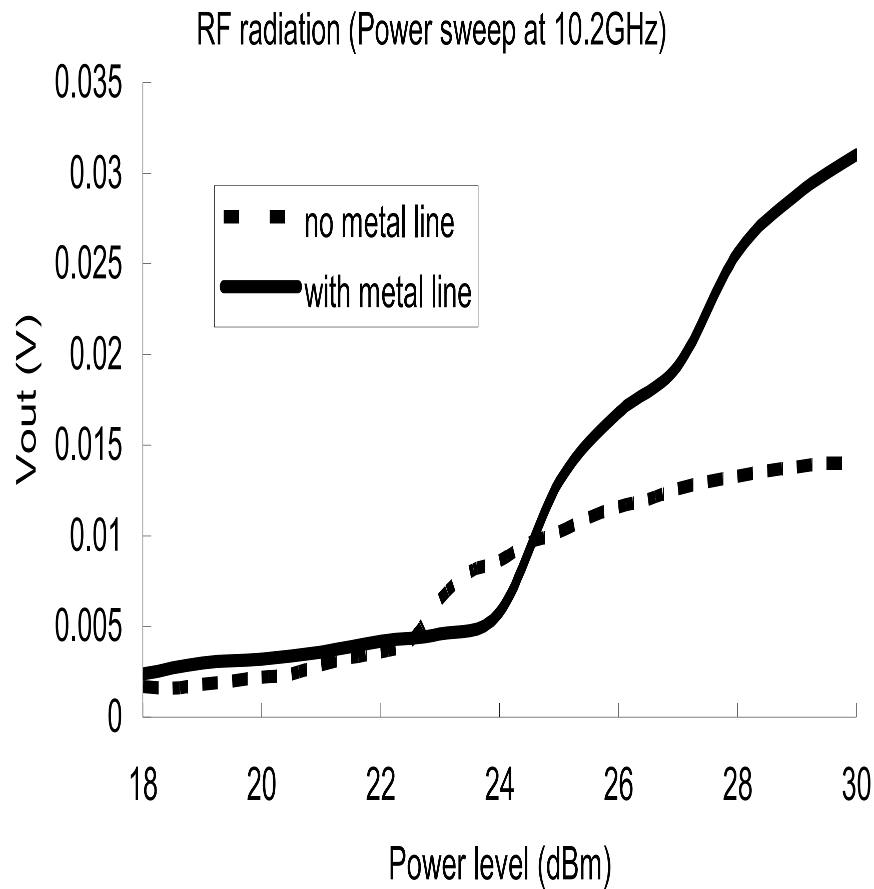


Figure 6.7: RF pulse radiation, two power sweeps from 18dBm to 30dBm at 10.2GHz. The solid line is for the detector with a metal line, and the broken line is for detector without a metal line

6.2.3 Antenna gain

By comparing the RF pulse radiation result with the RF pulse direct injection result, the antenna gain of the metal line can be calculated. Antenna gain is the ability to focus radio waves in a particular direction. The unit of antenna gain is dBi, decibels relative to isotropic. If an antenna with an isotropic radiation is assumed, the

antenna gain becomes 0dBi. Since the metal line was not designed for receiving an RF signal, the antenna gain of the metal line is expected to be very low.

The following Friis free space transmission equation [37] can be used to calculate the antenna gain of the metal line.

$$G_{Rx} = \frac{16 P_{Rx} \pi^2 d^2 L}{P_{Tx} G_{Tx} \lambda^2} \tag{6.1}$$

Where d is the distance between transmitter and transponder, P_{Tx} is the transmitted power, P_{Rx} is the received power, G_{Tx} is the transmitter gain, G_{Rx} is the receiver gain which is the antenna gain, λ is the wave length of the incident RF signal, and L is the system loss factor.

When the RF signal with 30dBm power level and 10.2GHz was incident, the measured output voltage was 0.0302V. From the RF direct injection measurement, 0.0302V dc output at 10.2GHz RF input can be achieved at –2.8dBm of the input power level, which is the received power, P_{Rx}, in the equation (6.1). The distance, d, was 1cm, the wave length, λ, was 2.94cm, and the radiated power, P_{TX} was 30dBm. The horn antenna gain can be calculated by the following equation.

$$D = 6.4 \frac{ab}{\lambda^2} \tag{6.2}$$

Where a and b is the width and height of the horn. (Figure 6.8) The width ‘a’ was 15cm and the height ‘b’ was 20cm. The antenna gain of the horn antenna in dB was calculated to be 23.47dB. As a result, the antenna gain of the metal line was –43.65dBi. Figure 6.9 explains the calculation steps.

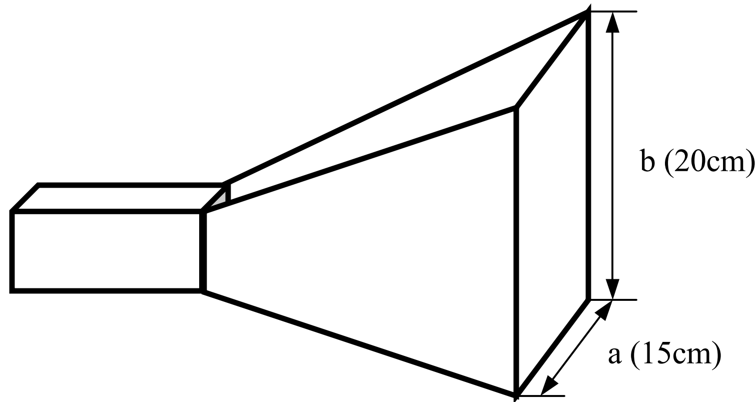


Figure 6.8: An x-band horn antenna, the gain of the horn antenna was calculated to be 23.47 dBi

$$G_{Rx} = \frac{16 P_{Rx} \pi^2 d^2 L}{P_{Tx} G_{Tx} \lambda^2}$$

d = 1cm (distance b/w antenna and target)
G_{Tx} = 23.47 dB (Horn antenna gain)
L = 1 (system loss factor, assumed)
λ = 2.94cm (wave length)

GRx = -43.65dBi

P_{Tx} = 30dBm (Radiated power)
P_{Rx} = -2.8dBm (Received

Radiation

Frequency	Power [dB	with antenı
10	30	0.0034
10.05	30	0.0042
10.1	30	0.0094
10.15	30	0.0268
10.2	30	0.0302
10.25	30	0.0134
10.3	30	0.0128
10.35	30	0.0104
10.4	30	0.0056
10.45	30	0
10.5	30	0.0018
10.55	30	0.0018
10.6	30	0.0016

Direct injection

Frequency	Power	Vout
10	-6	0.0048
10	-5.5	0.0052
10	-5	0.014
10	-4.5	0.0144
10	-4	0.0276
10	-3.5	0.016
10	-3	0.0208
10	-2.5	0.0436
10	-2	0.0524
10	-1.5	0.068
10	-1	0.0736
10	-0.5	0.0848
10	0	0.0992

30dBm radiation made the same output voltage as -2.8dBm direct injection

Figure 6.9: Antenna gain calculation by comparing the RF radiation result and the RF direct injection result, For 0.0302V output at 10.2GHz in RF radiation result, -2.8dBm direct injection needed

Chapter 7: CMOS Schottky diode modeling and applications

In passive microwave systems such as RFID the self-biasing circuit is a critical component and consists of broadband antennas and charge pump circuits. The DC operating voltage is generated by collecting, rectifying, and multiplying incident reading microwave signals. In addition, ambient signal harvesting has also been considered [38]. The charge pump consists of diodes and capacitors. Schottky diodes are the preferred candidates for better rectifying efficiency [39, 40]. One of the main issues of these RF CMOS system designs is integrating all components onto one chip for more compact, low power, and high frequency operation. Thus Schottky diodes also need to be integrated on a chip through the CMOS process. However, most CMOS processes are not specified for Schottky contacts, and modifications of a process is required to fabricate Schottky diodes [23]. And, for more precise circuit simulation, a SPICE model of a CMOS Schottky diode is required. In this work we addressed the fabrication and Spice modeling of CMOS Schottky diodes.

7.1 CMOS Schottky diodes

CMOS Schottky diodes have been fabricated by modifying the CMOS process and tested as described in chapter 3.2. To use the developed Schottky diode power detectors for more broad applications, more detailed examination is required. For better frequency response, the contact area of a Schottky diode should be reduced. However, too small contact area limits the power efficiency due to the high junction resistance and the series resistance. Depend on the applications, the tradeoff point can

be decided for the better performance. The following subchapters explain the measured result of Schottky diodes with various contact areas and geometries.

7.1.1 CMOS Schottky diode design

To figure out the relationship between the I-V curve and the contact area, Schottky diodes with various contact areas from 0.6μm x 0.6μm to 50μm x 50μm and different geometries were fabricated through a 0.35μ CMOS process and tested.

7.1.2 Measured result

DC measurements showed that the series resistance of the diodes is decided by not only the Schottky contact area but also the geometry of the conduction path. Figure 1(a) and 1(b) show two different layouts of Schottky diodes. Even though the contact area of the horseshoe shape contact (Fig. 1(b)) is 18 times smaller that that of rectangular shape contact (Fig. 1(a)), the two diodes showed very similar IV curves as

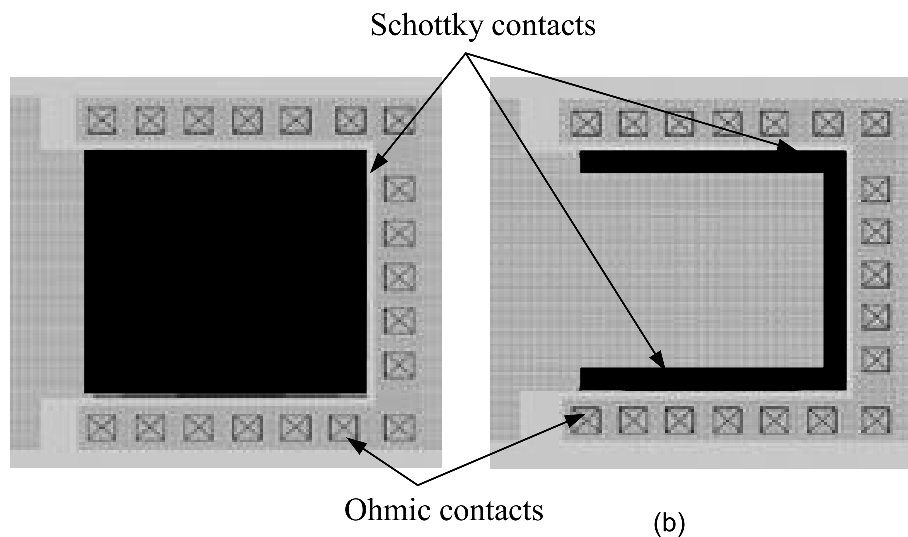


Figure 7.1: Layouts (a,b) of two Schottky diodes.

Contact area: (a) 343μm^2, (b) 19μm^2

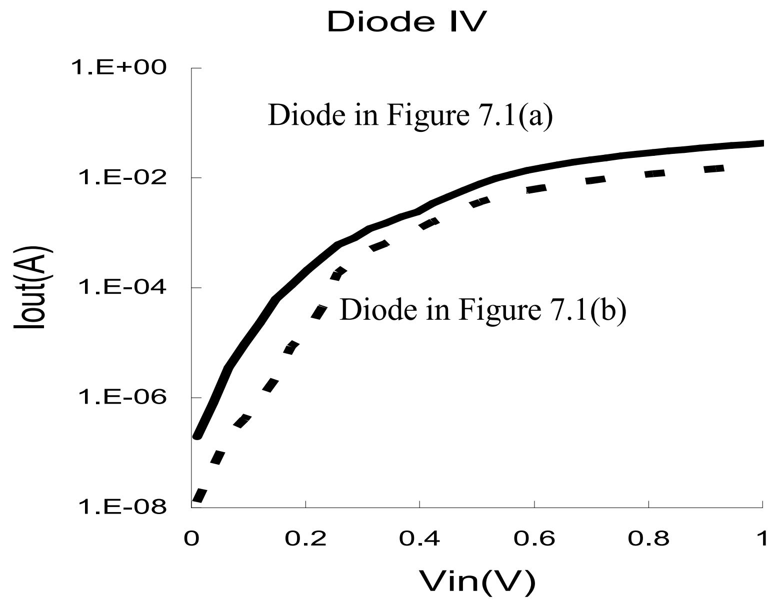


Figure 7.2: Measured result of two Schottky diodes. Even though Fig. 7.1(b) has 18 times smaller contact area, the measured series resistance was only 2.6 times bigger than that of Fig 7.1(a).

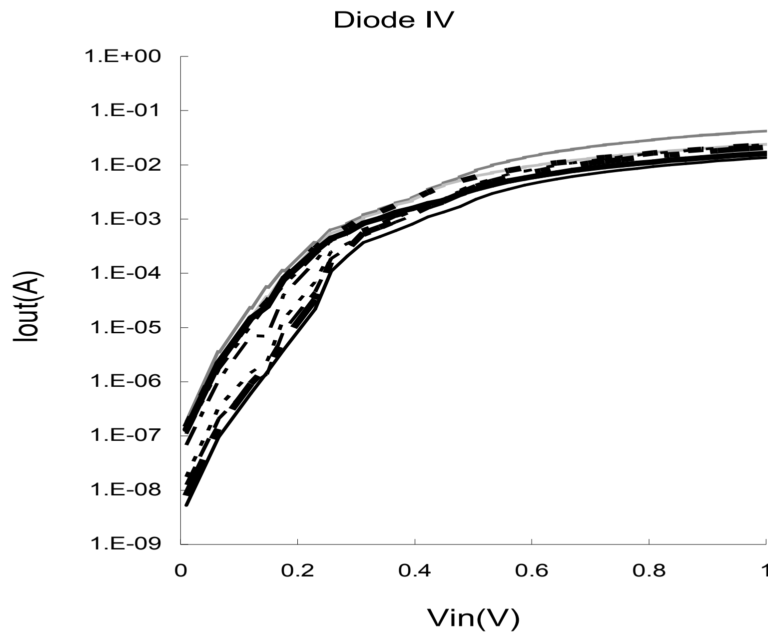


Figure 7.3: DC measured result of 10 n-type large Schottky diodes with different contact area with same conduction path geometry. The results were similar.

shown in Figure 7.2. The series resistances were 14Ω for diode (a) and 43Ω for diode (b). By using horseshoe shape geometry, the contact capacitance was reduced 18 times and the series resistance increased 3 times. As a result, we can assume that the cut off frequency increases 6 times. In other words, since the contact area should be small for the high frequency operation, as far as the design rule allows, a horseshoe shape contact rather than rectangular shape contact should be used. Figure 7.3 shows the DC measured result of 10 n-type Schottky diodes with different contact areas and similar conduction paths. The results were almost identical. Figure 7.4 shows the DC measured result of p-type Schottky diode with small contact areas from 0.16μm^2 to 8μm^2 with shortest possible conduction paths. The results were plotted on two different scales. The series resistance was from 74Ω to 1610Ω. The contact area in layout is not same as the fabricated contact area. When a contact rectangle is drown in the layout editor, the editor generates as many 0.6μm x 0.6μm rectangles as possible. It is because a 0.6μm x 0.6μm rectangle is the only contact pattern in the 0.35μm CMOS process. For example, when 10μm x 10μm contact is drown in a layout editor, the fabricated chip has 24 rectangles with 0.36μm^2 contact area. In other words, even though 100μm^2 contact area is drown in the layout editor, the actual contact area is only 8.64μm^2. Actual contact area were calculated and shown in Figure 7.4(b). From the DC measured result in Figure 7.4(b), the reverse breakdown voltage showed an interesting result. When the contact area decreases, the absolute value of the breakdown voltage increases due to high junction and series resistors. However, when the contact area decreases to smaller than 0.56μm^2, the absolute value of the reverse break down voltage decreases as shown in the dashed box in the Figure 7.4(b). This is

because the tunneling current begins to dominate the reverse leakage current, when the contact area becomes small enough.

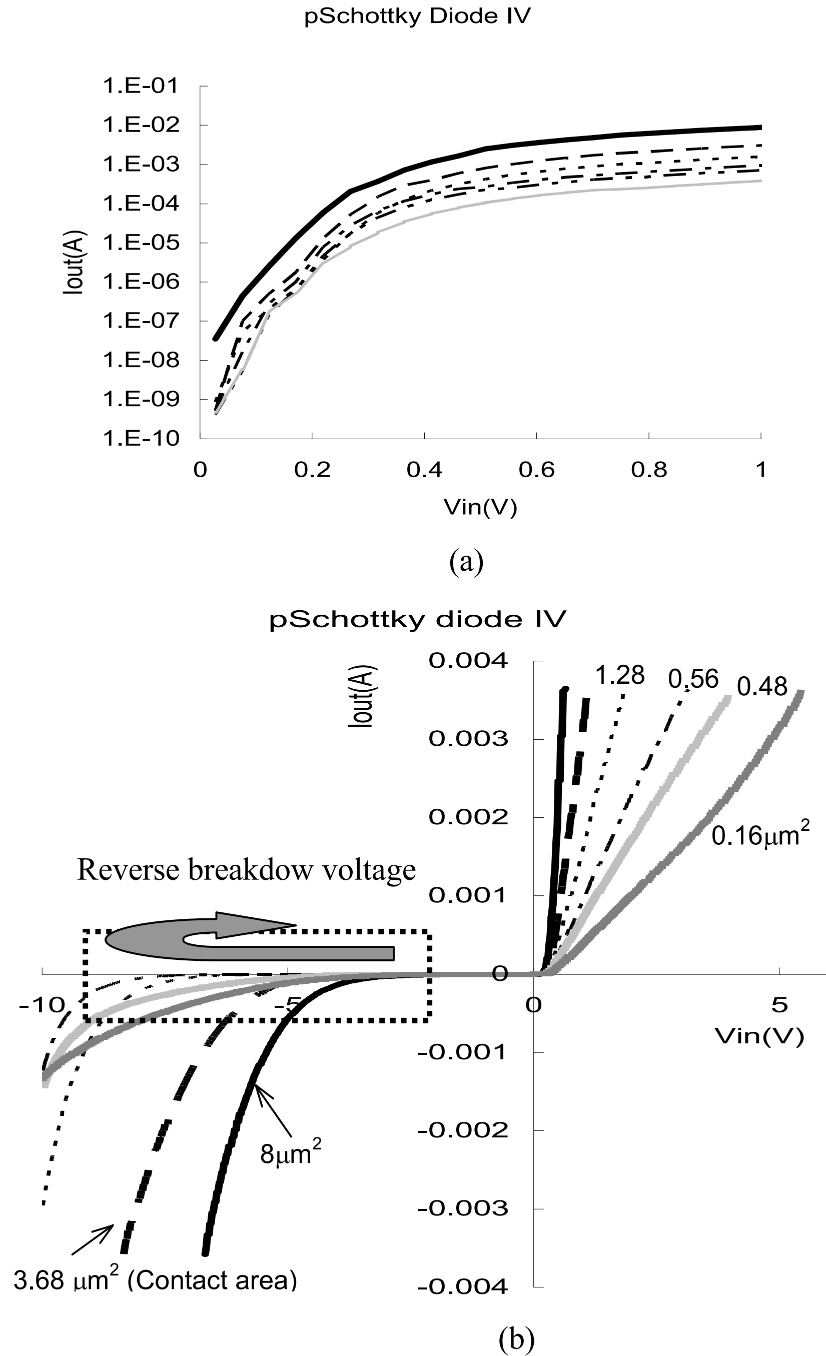


Figure 7.4: DC measured result of p-type Schottky diode with small contact area from $0.16\mu m^2$ to $8\mu m^2$. Plotted on log and linear scales. The series resistance varies from 74Ω to 1610Ω.

7.2 CMOS Schottky diode SPICE modeling

Currently available SPICE CMOS Schottky diode models for circuit simulation were insufficient for the actual CMOS circuit simulations. In the current SPICE Schottky diode models, forward bias currents for the high voltage region can be similar to the measured result by simply changing the series resistance value of a Schottky diode model. However, for the low forward voltage region where the junction resistance is bigger than the series resistance, a more precise model is required to solve the mismatch between the measured data and the simulation results mainly due to the generation-recombination effect, which is given by the following equation [4].

$$I_d = I_{te} + I_{rg}$$

$$= I_o \left[\exp(\frac{qV}{2kT}) - 1 \right] + I_{Ro} \left[\exp(\frac{qV}{2kT}) - 1 \right] \qquad (7.1)$$

Where I_{te} is the main diode current due to the thermionic emission and I_{rg} is the generation-recombination current.

7.2.1 SPICE modeling of a fabricated CMOS Schottky diode

Since it was difficult to create a new level of a diode model for SPICE simulation, currently available diode models were used for the simulation as shown in Figure 7.5. The first diode is for high voltage region and the second diode is for the low voltage region. A third diode can be added in the reverse direction for considering the tunneling effect when high reverse bias is applied.

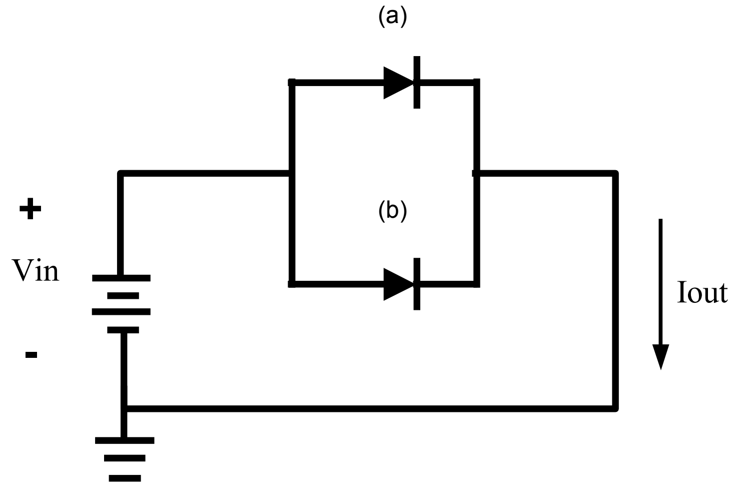


Figure 7.5: Schottky diode model for a Spice simulation: (a) is for high voltage range simulation, and (b) is low voltage region where the series resistance is smaller than the junction resistance. Parameters: (a) IS = 1E-14 RS = 40 N = 1 CJO = 160f XTI = 2 BV = 5.1 (b) IS = 5E-7 RS = 100 N = 1.5 CJO = 160f XTI = 2 BV = 45

7.2.2 Simulation and measured result

Figure 7.6 shows the comparison between the measured result and the simulated result. The dashed line shows the simulation result for one Schottky diode with the same series resistance. The solid line shows the measured result, and the gray line is the simulation result of the tow diode Spice model of eq. (1) and Fig. 6. Other two dashed lines are the simulation results of diode (a) only and diode (b) only. The simulated result is seen to agree with the measured result.

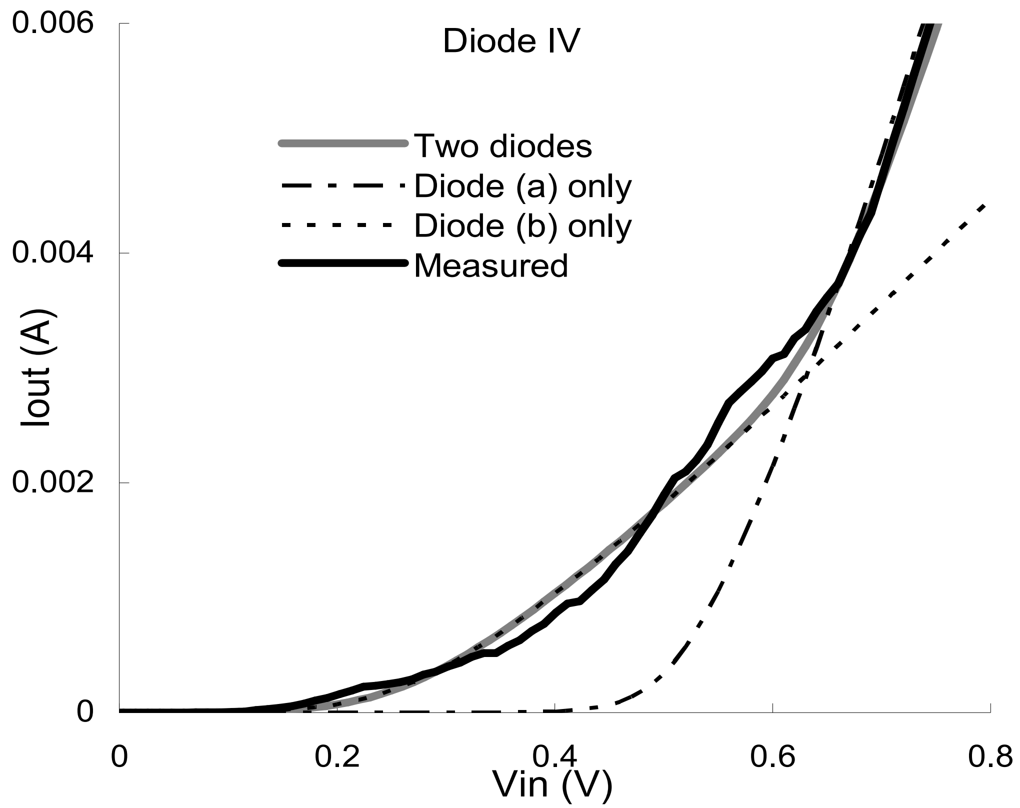


Figure 7.6: Measured and simulation result of the CMOS Schottky diode with 10x10μm^2 contact area. The simulation result of the modified diode model in Fig. 6 lays on the measured result

7.3 Applications

A passive integrated circuit for collecting ambient signals is a useful device both for studying hostile RF signals and for providing power for passive circuits such as RFID tags. CMOS Schottky diodes is a key component for these applications. As an example, a charge pump circuit, which uses arrays of diodes and capacitors to increase supply voltage in a circuit, was designed and fabricated. A voltage reference circuit with a Schottky diode was also considered.

7.3.1 Charge pump circuit

By using the suggested SPICE model, a charge pump circuit was designed, fabricated, and tested. (Figure 7.7) Schottky diodes with 10μm x 10μm contact areas were chosen for the proper current flow to charge up the load capacitors. The number of the stages needed, which in our example consists of two Schottky diodes and two

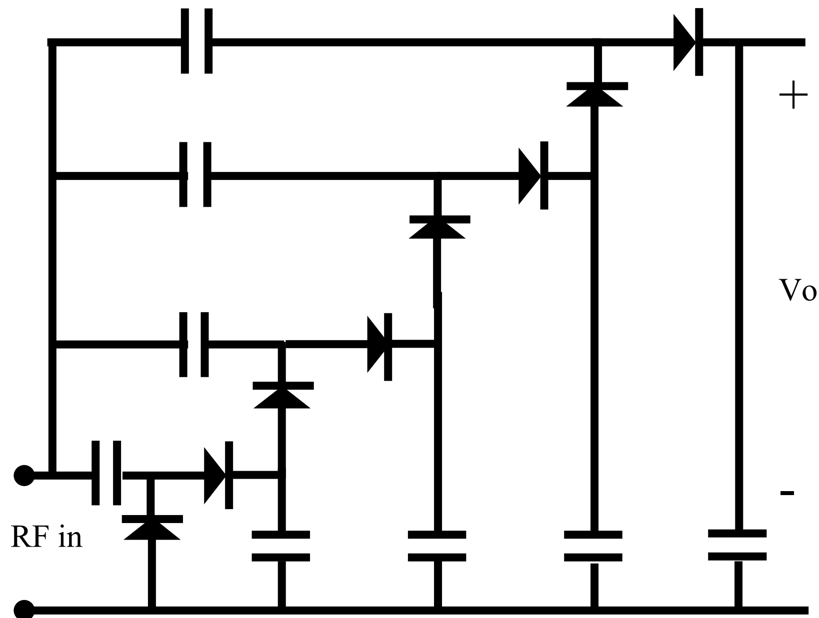


Figure 7.7: Fabricated 4-stage charge pump circuit with Schottky diodes

capacitors shown in Figure 7.7, is determined by the required efficiency and the required operating voltage. After simulating a 4-stage charge pump circuit with Schottky diodes and 2pF capacitors shown in Fig. 7.7, a CMOS circuit was fabricated and tested. The measured and simulated results in Fig. 7.8 are seen to agree. A 4-stage charge pump with diode connected MOSFET's as well as 2-stage and 13-stage charge pump circuits with Schottky diodes were also fabricated and tested for comparison. From the measured results, lower stage charge pump circuits showed a better performance to a low power input, and higher stage charge pump circuits showed better performance for high power input. This result shows that 6-stage or 7-stage charge pump circuits or a 4-stage charge pump circuit with larger contact area Schottky diodes may be useful for RFID applications and ambient microwave signal harvesting, though the number of stages strongly depends on the required operating voltage. More detailed relationship between the number of stages, the power efficiency, and the generated DC operating voltage is discussed in appendix.

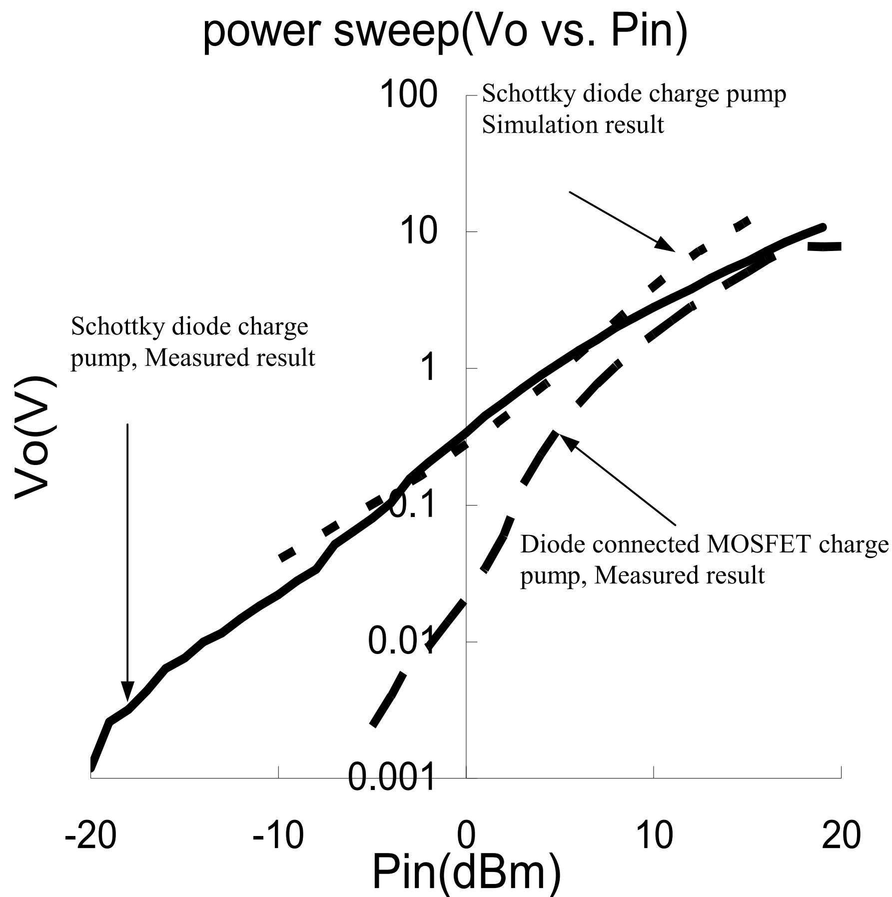


Figure 7.8: Measured and simulation result of the fabricated charge pump in Fig. 7.7 at 2.45GHz. The simulation result was similar to the measured result. Diode connected MOSFET showed less sensitive result as expected.

7.3.2 Voltage reference circuit with Shottky diodes

The operating voltage of a passive circuit using collected ambient signals should be constant and low, such as 1V or less. Since the operating voltage generated by a charge pump circuit is not a constant, a voltage regulator circuit is required. The voltage regulator circuit consists of a voltage reference circuit, which generates a supply independent reference voltage. The reference voltage usually refers to the turn-on voltage of a pn junction diode. However, since pn-junction diodes have high turn-on voltage, 0.8V or more, a lower voltage reference is impossible to be generated by referring the turn-on voltage of a pn junction diode. For more advanced CMOS technology, the operating voltage would be around 0.5V. Since we have developed a method of fabricating a Schottky diode for any CMOS process, a Schottky diode can

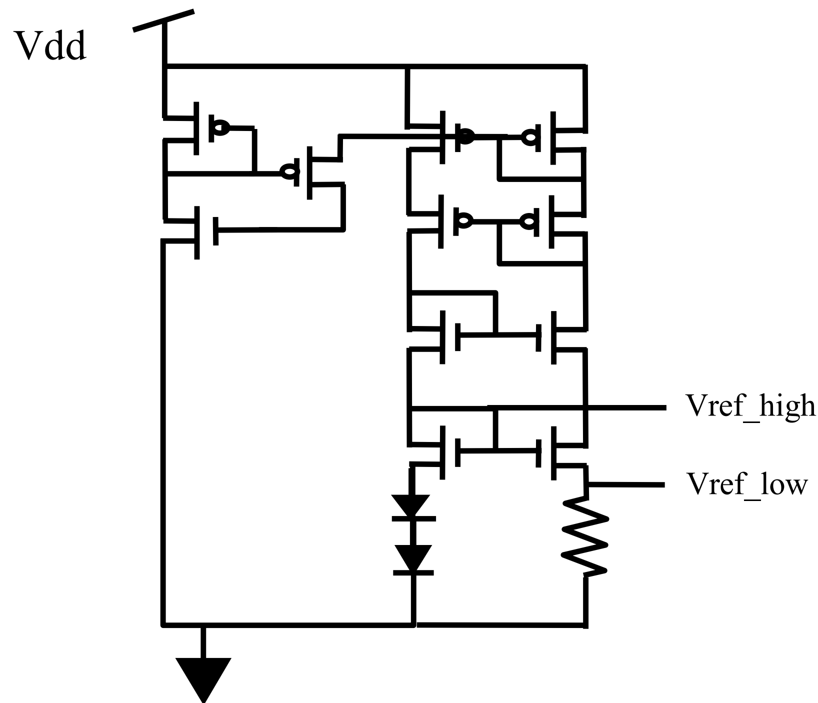


Figure 7.9: Voltage regulator circuit with two Schottky diodes, Vref_high = 1.05V, Vref_low = 0.42V

be used in a voltage reference circuit. By referring to the turn-on voltage of a Schottky diode in a voltage reference circuit, a lower reference voltage, such as 0.2V, can be achieved. By adding one more Schottky diode in series, the reference voltage can be 0.4V. Figure 7.9 shows the suggested voltage reference circuit, which is a well-known circuit [41], except for using two Schottky diodes. By using a feedback between two current mirrors, the output voltage becomes the turn-on voltage of the Schottky diode. Figure 7.10 shows the DC simulation result for Figure 7.9. The operating voltage is almost independent of the change in the supply voltage, Vdd. By referring to the Vref_high voltage, 1V of the reference voltage can be also generated.

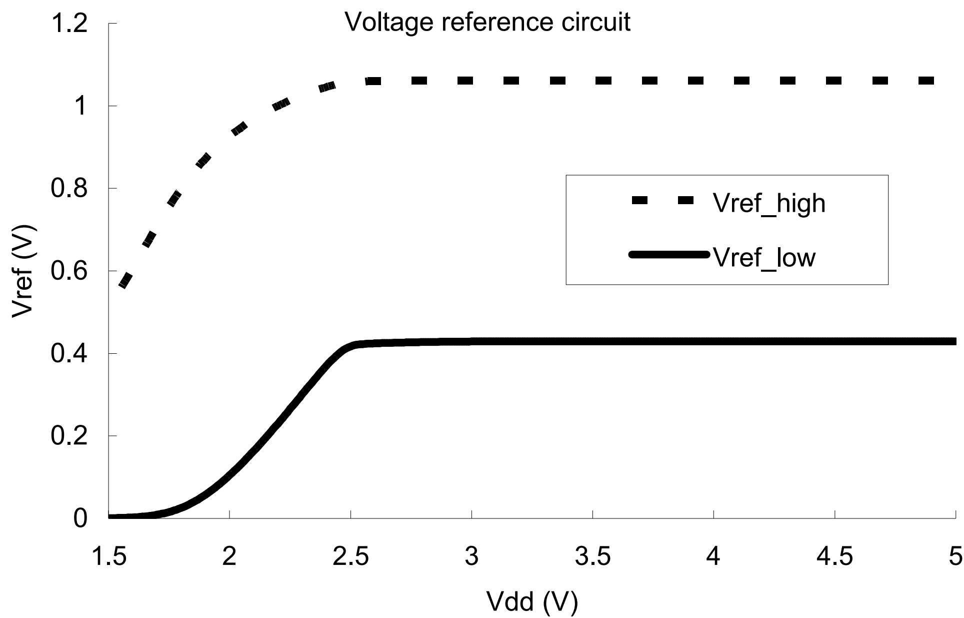


Figure 7.10: Simulation result of the voltage regulator circuit in Figure 7.9.

Chapter 8: Conclusions

This chapter consists of three sections. The first section compares the fabricated detectors, the second section conclude this dissertation, and the third section lists the contribution of this dissertation.

8.1 Comparison of the measured results

The power detectors we developed showed various characteristics. CMOS Schottky diodes and FIB Schottky diodes showed a wide dynamic range and a relatively flat frequency response. However, the output voltage, the frequency response, and the pulse response time strongly depend on the contact area. MOSFET power detectors showed the shortest pulse response time, though their frequency response and dynamic range were worse that that of the Schottky diode power detectors. Figure 8.1 and Figure 8.2 shows the measured results for all detectors fabricated and tested. Figure 8.1 shows the frequency response from 1GHz to 10GHz. Since an RF burst with the frequency range from 1GHz to 5GHz is expected to have the strongest effect on electrical systems, the power detectors were tested up to 10GHz. Figure 8.2 shows the power sweep from –21dBm to 15dBm. For the better comparison a pn junction diode and a diode connected MOSFET without a bias circuit were also fabricated and tested. Both the diode connected MOSFET and the pn-junction diode showed poor detections in terms of the sensitivity and the frequency response. Table 8.1 summarized the measured results for all detectors. The sensitivity in dBm is the input power level to generate 2mV DC output. The measured result of 2-stage, 4-stage, and 13-stage charge pump circuits were also included in table 8.1.

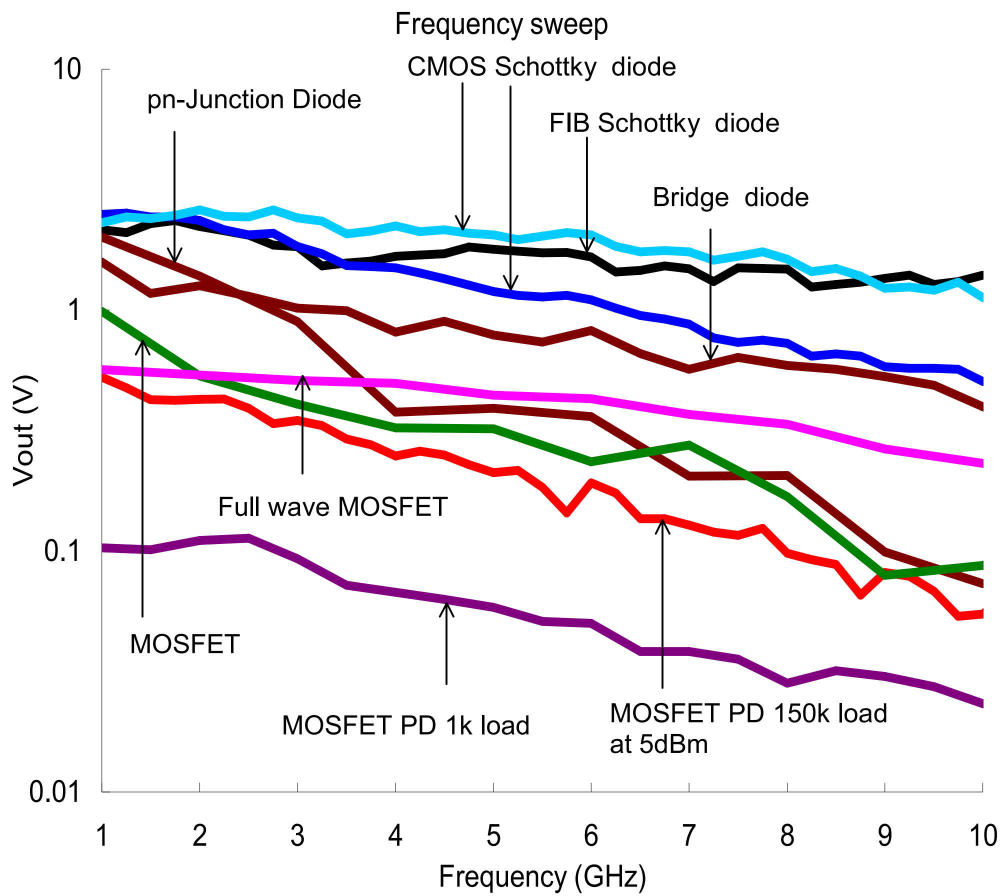


Figure 8.1: Frequency sweep (1GHz to 10GHz) for fabricated power detectors

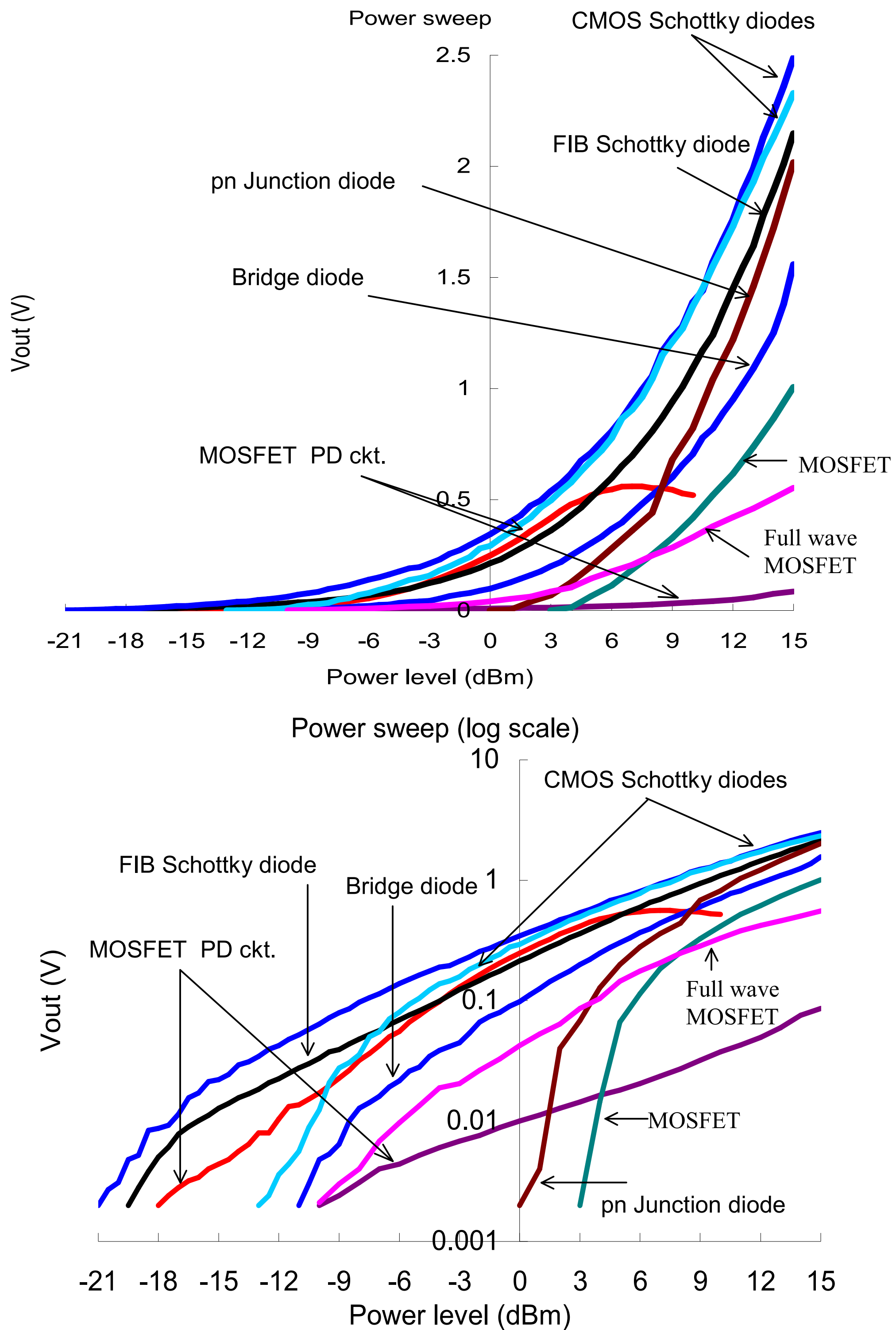


Figure 8.2: Power sweep (-15dBm to 15dBm) of fabricated power detectors at 1GHz

Table 8.1: Pulse response time, frequency response, dynamic range, and the lowest input power level to be detected.

		Pulse response time (sec) (1GHz, 10dBm)	Frequency response (Vo at 1GHz/Vo at 10GHz)	Dynamic range (dB)	Sensitivity (dBm) (1GHz)
CMOS Schottky diodes	n-type $92\mu m^2$	820n	4.93	**>36**	**-21**
	n-type $1.44\mu m^2$	776n	**2.05**	>34.5	-19.5
FIB Schottky diodes	n-type $15\mu m^2$	6µ	3.14	>35.5	-20
	n-type $8\mu m^2$	2.56µ	2.76	>17.5	-2
	p-type $4\mu m^2$	192n	4.91	>16.5	-1
	Bridge shaped	170n	3.97	>26	-11
MOSFET circuit	100kΩ Load	200n	9.59	23	-18
	1kΩLoad	**56n**	4.43	>25	-10
Full-wave MOSFET		101n	2.44	>25	-10
Diode connected MOSFET		1.2µ	11.33	>15	0
pn-junction diode		16µ	27.4	>12	3
Charge Pump	2-stage	76n	1.51	>33	-18
	4-stage	112n	2	>35	-20
	13-stage	630n	8.5	>15	0
	MOSFET	1.8µ	3.2	>21	-6

8.2 Conclusion

The main goal of this research is to design on-chip microwave pulse power detectors to measure the power level at any location of interest. The frequency range of interest in HPM source is from 1GHz to 10GHz and the pulse durations of interest are from 10's to 100ns. To detect HPM source with 100ns of pulse width, the pulse response time of pulse power detector should be shorter than 100ns. Therefore we have focused on reducing the pulse response time. Since thermal power detectors fabricated through the CMOS process showed a long pulse response time due to the thermal time constant, a few ms, Schottky diode power detectors and MOSFET power detector circuits were investigated as microwave pulse power detectors.

On-chip microwave pulse power detectors with CMOS Schottky diodes, FIB Schottky diodes on a CMOS chip, and MOSFET power detector circuits were designed, fabricated, and tested. The CMOS processes can be modified to fabricate Schottky diode on-chip detectors on pre-selected locations, and a post-CMOS process, FIB process, can be used to fabricate detectors in arbitrary locations or to remove the detectors fabricated in the CMOS run. FIB fabrication can also be used to alter the circuit in other ways to test the vulnerability to RF burst. Figures 8.1 and 8.2 summarize the measured result for power detectors fabricated for this research. From the measured results and the Table 8.1, a power detector can be selected depending on the pulse type. To detect a short pulse with shorter than 1μs pulse width, MOSFET detectors, small FIB diode, or bridge shaped diode power detectors can be used due to their fast pulse response time. To detect a long pulse with longer than 1μs pulse width, big FIB diodes, CMOS Schottky diodes are the best choice due to their flat

frequency response, wide dynamic range, and the high sensitivities. To illustrate an application of theses detectors a fabricated CMOS detector was connected to a metal line on a circuit board and a microwave pulse was radiated on the board with a horn antenna in an anechoic chamber. A SPICE model of a fabricated CMOS Schottky diodes was developed to meet the measured DC voltage I-V curve. By using the measured result and the SPICE model of the fabricated CMOS Schottky diodes, charge pump circuits were designed and fabricated, and a voltage regulator circuit with Schottky diodes was designed as a low voltage reference circuit.

8.3 Contribution

For my dissertation, I have presented the design and fabrication of various on-chip microwave pulse power detectors.

We have developed a method to fabricate Schottky diodes on any CMOS process by modifying the layout file. The developed Schottky diode is an essential component for designing an RF passive integrated circuit, such as RFID, since they are faster and more sensitive than pn-junction diodes due to the major carrier current transportation and a low, 0.4V, turn-on voltage.

We have also developed a method for adding or deleting Schottky diodes on a CMOS-fabricated chip by using FIB as a post-CMOS process. As far as we know the use of FIB as a post-CMOS process to fabricate Schottky diode power detectors has not been reported before.

We have also designed MOSFET power detector circuits for detecting short microwave pulse with less than 100ns pulse width. Even though a few researchers

have designed MOSFET power detector circuits, they were not useful for microwave pulse power detection due to the long pulse response time of a few ms.

By using the fabricated CMOS Schottky diodes, a CMOS Schottky diode Spice model was developed to meet the measured DC I-V result. The model was used to design charge pump circuits and an RFID transponder tag [40]. The measured result and model of the developed CMOS Schottky diodes may be helpful to reduce the effort for designing the RF front end circuits in passive RF circuits.

8.4 Challenge

Our work has led us into two new areas, testing the vulnerability of RFID tags and the "harvesting" of RF power for passive devices.

Testing the vulnerability of RFID tags is similar to the detection of hostile RF in chips. For this, an RFID transponder chip was designed and fabricated. After adding several FIB power detectors, this RFID tag will be tested under RF direct injection to know which power level and frequency would give the strongest effect on the RFID tag. This experiment would be an example of my research, since RFID tags are complete systems, which have standard electronic components, and may be one of the most vulnerable systems.

The “harvesting” of RF power for passive devices are receiving attentions in the wireless sensor network research. Wireless sensor networks is an emerging technology that has a wide range of potential applications, such as medical systems, environment monitoring, military applications, and other commercial areas. A wireless sensor network normally consists of a large number of distributed nodes, which are independent systems with sensors, embedded processors, low-power RF

circuits, and a power source [42]. One of the most important constraints on sensor nodes is the low power consumption requirement. Even though a battery can be used for the power source, energy harvesting would be the better approach to realize a permanent power source, since the size and cost of the nodes must decrease to achieve true ubiquitous system, and the power consumption of the nodes should become lower and lower due to the advanced fabrication methods and design. For low cost fabrication, CMOS process is the best candidate, and Schottky diodes are the key components for harvesting ambient RF energy. In other words, CMOS Schottky diodes may be helpful components for wireless sensor networks.

Appendices

Appendix A

Schottky diode transport mechanism

Due to the charge transportation from the semiconductor to the metal or from the metal to the semiconductor, the diode current flows in a Schottky diode. There are four different major mechanism of the carrier transportation. They are thermionic emission over the barrier, tunneling through the barrier, carrier recombination or generation in the depletion region, and minority carrier injection from the metal into

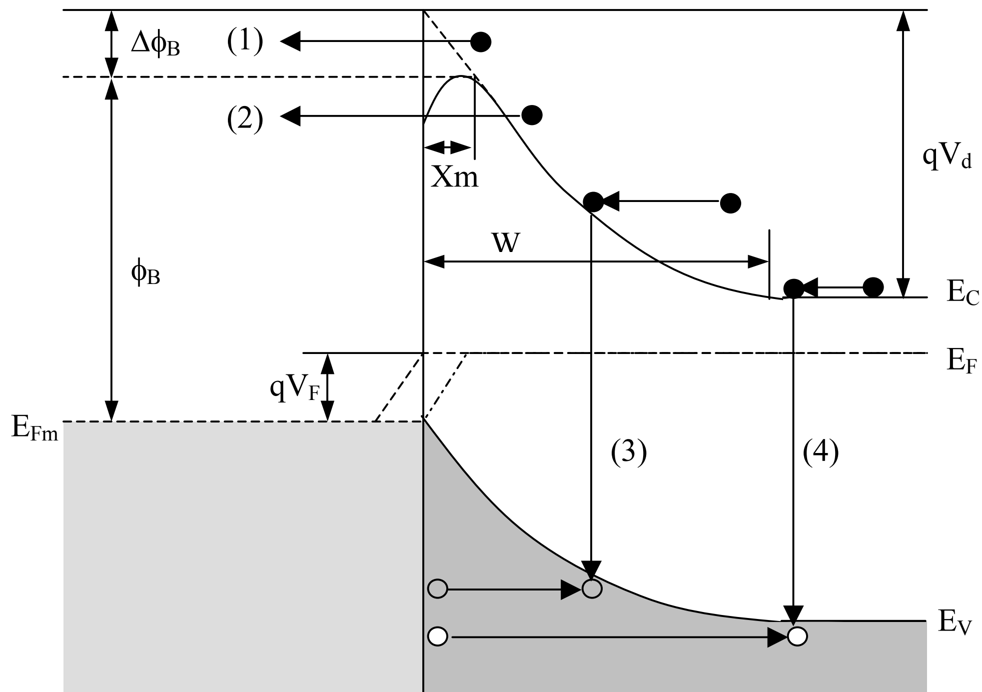


Figure B.1: Energy band diagram of a forward biased n-type Schottky diode with four different carrier transportation mechanism.
(1) Thermionic emission, (2) Tunneling through the barrier, (3) Carrier generation and recombination in the depletion region, and (4) hole injection from metal into the semiconductor (minority carrier injection)

the semiconductor. Figure A.1 illustrates four carrier mechanisms in an energy band diagram of a forward biased n-type Schottky diode. For the reverse bias, reverse processes occur. The thermionic emission is the dominant mechanism and the only charier transport mechanism for an ideal Schottky diode I-V curve. Other mechanisms cause departure from the ideal behavior.

A.1. Thermionic emission

The thermionic emission over the barrier and the diffusion and drift in the depletion region are effectively series, and the one which offers the higher resistance determines the current. The effect of drift and diffusion in the depletion region is assumed to be negligible in the thermionic emssion theory and the barrier height is assumed to be large compared to kT/q. If the electron collisions within the depletion region are neglected, the diode current equation can be derived as follow.

Assuming that the carriers have a Maxwellian distribution of velocities, the number of electrons n* per unit area which have sufficient energy to move over the barrier and given by the following equation.

$$n^{*} = n_0 \exp\left[\frac{-q(Vi - V)}{kT}\right] \quad (A.1)$$

$$n_0 = N_C \exp(-\phi_B / kT) \quad (A.2)$$

$$\phi_B = qVi + \phi_n \quad (A.3)$$

Where n_o is the electron concentration in the neutral semiconductor outside the depletion region, Vi is the built in voltage, and V is the applied voltage.

Finally, the number of electrons n* per unit area is given by the following equation.

$$n^{*} = N_C \exp\left[-\frac{(\phi_B - qV)}{kT}\right] \quad \text{(A.4)}$$

If the velocities of the carriers have an isotropic distribution and all the incident carriers cross over the barrier, the flux of carriers incident on the barrier is $n^{*}\bar{v}/4$. Where $\bar{v}$ is the average thermal velocity. The current from the semiconductor to the metal by these carriers is given by the following equation.

$$I_{SM} = \frac{qS\bar{v}}{4} N_C \exp\left[-\left(\frac{\phi_B - qV}{kT}\right)\right] \quad \text{(A.5)}$$

Under thermal equilibrium without applying the bias voltage, no net current can flow. To make the net current zero, the sum of the current from the metal to semiconductor, I_{MS}, and I_{SM} in equation (A.5) should be zero, and I_{MS} is given by the following equation.

$$I_{MS} = -\frac{qS\bar{v}}{4} N_C \exp\left(\frac{\phi_B}{kT}\right) \quad \text{(A.6)}$$

Under the bias condition, the barrier from the metal to semiconductor remains practically unchanged at ϕ_B, and I_{MS} can be considered as a constant, –Io. However, I_{SM} depends on the applied bias voltage, and, finally, by combining equation (A.5) and (A.6), the diode current equation can be obtained as the following equation.

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad \text{(A.7)}$$

For a Maxwellian distribution, $\bar{v} = \sqrt{8kT/\pi m^*}$. The carrier concentration is given by the following equation.

$$N_C = 2(2\pi m^* kT/h^2)^{3/2} \tag{A.8}$$

And the current Io can be written as

$$I_0 = SAT^2 \exp\left(\frac{-\phi_B}{kT}\right), \; A = \frac{4\pi m^* qk^2}{h^3} \tag{A.9}$$

where A is the Richardson constant, h is the Planck's constant, and S is the diode contact area. However, the carrier collision within the depletion region, which was assumed to be negligible, needs to be considered in the thermionic emission and the diffusion processes. Crowell and Sze considered these collision by adding the effect of image force barrier lowering and derived the current Io as [43]

$$I_0 = SA^* T^2 \exp\left(\frac{-\phi_B}{kT}\right), \; A^* = \frac{Af_p f_q}{1 + f_p f_q v_R / v_D} \tag{A.10}$$

where v_D is the effective diffusion velocity through the depletion region, f_p is the probability of an electron reaching the metal without scattering into the semiconductor, and f_q is the probability of its transmission through the barrier in the presence of quantum mechanical reflection and tunneling. At 300K, f_p and f_q is typically the order of 0.5 so that A* may be less than A by about 50%. The calculated values of A* at 300K are $112 Acm^{-2}K^{-2}$ for a n-type Silicon Schottky diode, $32 Acm^{-2}K^{-2}$ for a p-type Silicon Schottky diode, and $4.4 Acm^{-2}K^{-2}$ for a n-type GaAs Schottky diode. [4, 43]

A.2. Tunneling through the barrier

The carrier can also be transported across the barrier by quantum mechanical tunneling. Field Emission (FE) and Thermionic Field Emission (TFM) are the two ways in which the tunneling can occur in a Schottky junction. When the semiconductor is heavily doped, the depletion region becomes very thin and at low temperature the carriers with energy close to the Fermi level can tunnel through the thin barrier, which is called FE. At higher temperatures, a significant number of carriers are able to rise high above the Fermi level where they see a thinner and lower barrier, and these carriers can tunnel through the barrier, which is called TFM. The following equation is for calculating the tunneling current by estimating the probability of tunneling [44, 45].

$$I = SqV_R n\Theta \tag{A.11}$$

Where $V_R = \sqrt{\frac{kT}{2\pi m}}$ and Θ is the tunneling probability by WKB approximation derived from time independent Schrödinger equation, which is given by the following equation [44, 45].

$$\Theta = \exp\left(-\frac{4}{3} \frac{\sqrt{2qm^*}}{\hbar} \frac{\phi_B^{3/2}}{E} \right) \tag{A.12}$$

If tunneling dominates metal semiconductor contacts the ideality factor should appear in the reverse current term and the current voltage relation becomes [46, 47, 48]

$$I = I_0 \left\{ \exp\left(\frac{qV}{nkT} \right) - \exp\left[\left(\frac{1}{n} - 1 \right) \frac{qV}{kT} \right] \right\} \tag{A.13}$$

A.3. Carrier generation and recombination

Carrier can be generated, when a diode is reverse biased, or rccombinated, when a diode is forward biased, in the depletion region. The generation-recombination current is given by the following equation [4].

$$I_{rg} = I_{R0}\left[\exp(qV / 2kT) - 1\right] \tag{A.14}$$

Where $I_{R0} = \frac{qSn_iW}{2\tau_0}$, S is the contact area.

The generation-recombination current becomes significant only when a diode has a large barrier height, a low temperature, a lightly doped semiconductor with large depletion width, and low carrier lifetime.

A.4. Minority Carrier Injection

When the barrier height on an n-type semiconductor is substantially higher than half of the band gap of the semiconductor, the region where the semiconductor adjacent to the metal has a high concentration of holes and becomes p-type. Under a forward bias, minority carriers (hole on n-metal contact) diffuse into the semiconductor. The current by the minority carrier injection is given by the following equation [4].

$$I_{\min or} = \frac{qSD_p n_i^2}{N_d L_p}\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{A.15}$$

Where Dp is hole diffusion constant

Appendix B

Barrier height calculation

The barrier heights of the fabricated Schottky diodes can be calculated from current-voltage measurements. If we assume that the thermionic emission is a dominant carrier transport mechanism, from equations (A.7- A.10), the I-V curve of a Schottky diode is given by the following equation.

$$I = SA^{**}T^2 \exp\left(\frac{-q\phi_B}{kT}\right)\left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1\right] \tag{B.1}$$

Where S is the contact area, A** is the effective Richardson constant, n is the ideality factor, ϕ_B is the barrier height, and R_s is the series resistance of a diode. A^{**} is 96 A/(cm^2K^2) for Silicon Schottky diodes and 4.4 A/(cm^2K^2) for GaAs Schottky diodes. To fit the measured I-V curve with equation (B.1), three fitting parameters, R_s, n, and ϕ_B, should be extracted. If we assume all parameters are independent of the applied voltage, the series resistance calculated from the I-V curve in high voltage input region, such as the resistance between 4V and 5V. After obtaining the actual voltage applied to a diode by calculating the series resistance, the reverse leakage current, I_o, can be calculated from the intercept with y-axis of the ln(I)-versus-V_d curve, which is given by the following equation.

$$\ln(I) = \ln(I_s) + \frac{qV_d}{nkT} \tag{B.2}$$

Where Vd = V – IR_s. The barrier height is obtained from the following equation.

$$\phi_B = -nkT \ln\left(\frac{I_0}{SA^* T^2}\right) \quad \text{(B.3)}$$

The ideality factor is deduced from the slope of the curve. This technique is called standard method [49,50,51]. However, this method is only valid when the series resistance is small enough to make the curve straight within a voltage range of interest, and the barrier height and the ideality factor of a diode with a high series resistance cannot be calculated properly. Since some of fabricated Schottky diodes in our research have high series resistance, the standard method cannot be used [52]. To solve this problem, we used Lien plot, which was proposed by Lien et al. [53]. They have proposed an auxiliary function, which is based on plotting several Norde plots [54] and given by the following equation.

$$F_a(V, I) = \frac{V}{a} - \frac{1}{\beta} \ln\left(\frac{I}{SA^* T^2}\right) \quad \text{(B.4)}$$

Where β=q/kT and 'a' is an arbitrary parameter greater than the ideality factor. When 'a' is 2, equation (B.4) becomes the Norde plot, which assume the ideality factor is 1. From the graph of Fa versus I, we need to find a minimum point of each F_a for several a's, given range from the ideality factor to infinity. Since F_a-versus-I rather than F_a-versus-V is more convenient for calculating the series resistance, equation (B.4) is assumed to be $F_a(I)$. To find the minimum point of F_a, '$dF_a(I)/dI$' is derived and to be zero. The current, when '$dF_a(I)/dI = 0$', is noted as I_a, which is given by the following equation.

$$\frac{dF_a(I)}{dI_a} = \frac{1}{a}\frac{dV_a}{dI_a} - \frac{1}{\beta I_a} = 0 \quad \text{(B.5)}$$

The series resistance and the ideality factor are extracted by the following equation, which was derived from equation (B.1) and (B.5).

$$I_a = \frac{1}{R\beta} a - \frac{n}{R\beta} \tag{B.6}$$

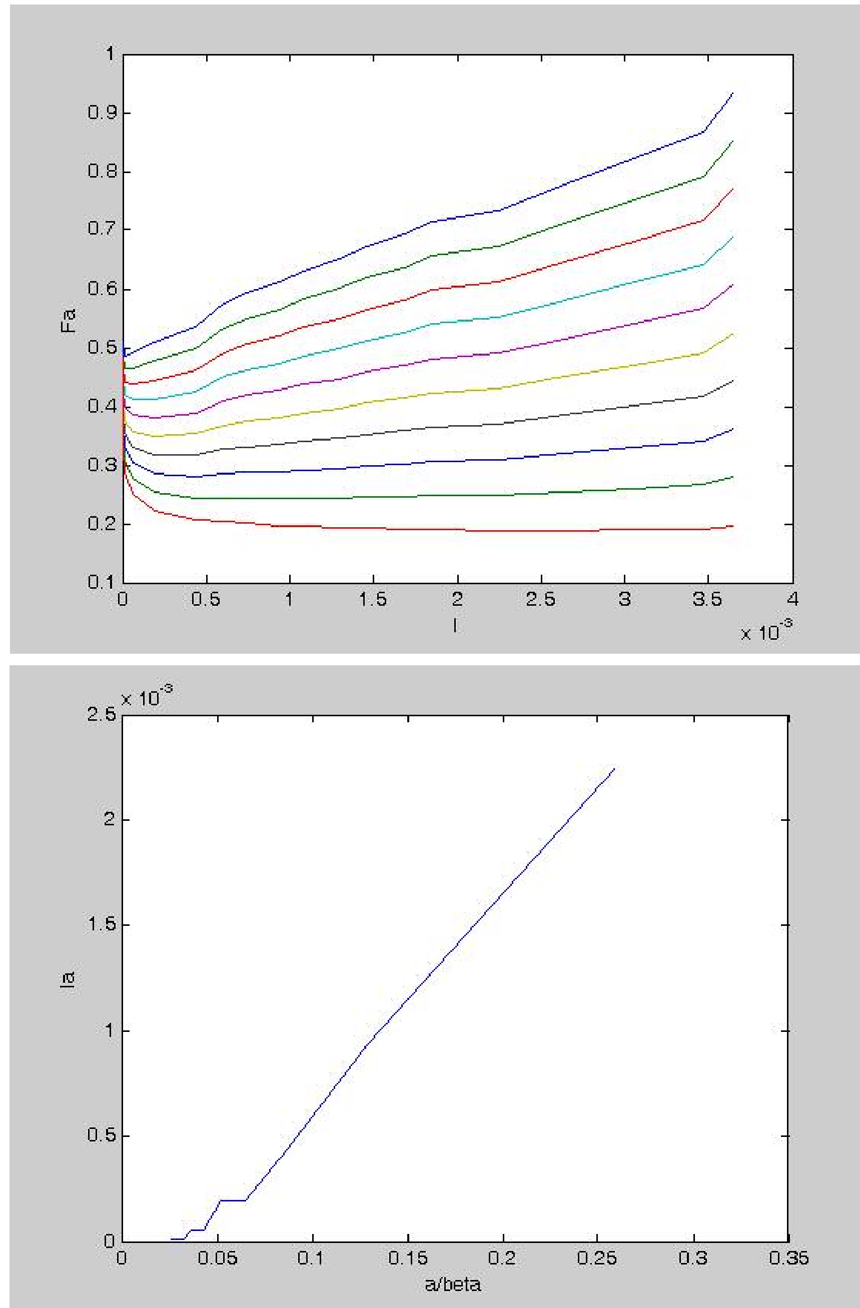


Figure B.1: Fa-versus-I graphs and Ia-versus-a/β graph

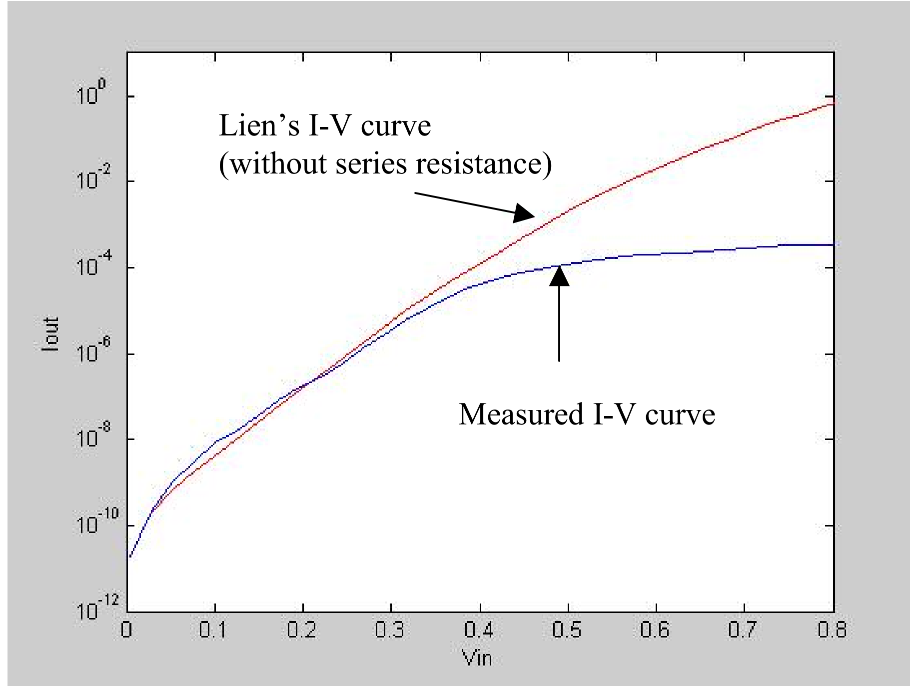


Figure B.2: Measured I-V curve and Lien's I-V curve by MATLAB

Figure B.1 shows F_a-versus-I graph and I_a-versus-a/beta graph. As shown in figure B.1, a plot of I_a-versus-'a' is a straight line whose slope determines the series resistance and whose extrapolated intercept at I_a=0 gives the ideality factor. The reverse leakage current, I_o, and the barrier height can be calculated from the standard method by using calculated R_s and 'n'. The MATLAB was used to calculate the barrier heights, the series resistances, and the ideality factors of the fabricate Schottky diodes. Figure B.2 shows the measured I-V and Lien's I-V curve derived by using MATLAB. Since the barrier height depends on the applied voltage, we also added the following equation [43, 55] to the MATLAB simulation.

$$\phi_B(V') = \phi_{B0} + \left(\frac{n-1}{n}\right)V' \tag{B.7}$$

From the calculated results in table B.1, FIB Schottky diodes were less ideal than CMOS Schottky diodes normally due to the damage on the silicon surface during the FIB milling process. The Barrier heights strongly depend on the contact areas of the Schottky diodes. The smaller the contact area is, the lower the barrier height is. In other words, smaller contact area Schottky diodes give better high frequency performances. [56]

Calculated parameters of fabricated Schottky diodes:

CMOS Schottky diodes:

Barrier heights (eV): 0.488 – 0.581

Ideality factors: 1.12 – 1.63

Series resistances (Ω) : 13 – 1044

Reverse leakage current (A): 7.95E-9 – 9.02E-11

FIB Schottky diodes:

Barrier heights (eV): 0.324 – 0.374

Ideality factors: 1.65 – 1.67

Series resistances (Ω): 637 – 3291

Reverse leakage current (A): 1.55E-7 – 2.29E-8

Diodes	Contact area (μm^2)	Barrier Height (eV)	Ideality factor	Series resistance (Ω)	Reverse leakage current(A)
CMOS Schottky diodes	343	0.571	1.637	13	7.95e-009
	124	0.555	1.363	27	5.30e-009
	55	0.551	1.561	37	5.11e-009
	30	0.548	1.388	46	2.44e-009
	8	0.529	1.119	200	1.44e-008
	0.56	0.512	1.292	558	2.84e-010
	0.48	0.504	1.254	779	1.43e-010
	0.16	0.46	1.035	1423	2.66e-010
FIB on CMOS chip	4	0.325	1.655	638	1.55e-007
FIB on lab-made CMOS chip	4	0.392	1.960	127	1.41e-007
FIB bridge diode	2	0.374	1.667	3291	2.29e-008

Table B.1: Calculated Barrier heights of the fabricated Schottky diodes

The following MATLAB code was used for obtaining the parameters.

```
% Loading measured I-V data from file 'IVme.txt'

% Calculating Rs, φB, and n of a fabricated CMOS Schottky diode with 1µm2 contact area.

load IVme.txt;

Vme = IVme(:,1);
```

```
Ime = IVme(:,2);

range = Vme(size(Vme,1));

beta = 1/0.0259;    % beta = q/kT, S: contact area, A: Richardson constant, T: temperature

S = 0.48E-8;

A = 96;

T = 300;

% Lien et al. method to calculate the series resistance (Rs)

flag = 0;

b = 1:-0.05:0.01;

a = 1./b;

for i = 1:size(b,2)

   Fa(:,i)=Vme/a(i)-1/beta*log(Ime/(S*A*T^2));

   gra(:,i) = gradient(Fa(:,i),Ime);

   for j = 1:size(Vme,1)-1

      if gra(j,i)*gra(j+1,i) < 0

         Ia(i)=Ime(j);

      end

      if (Vme(j) > 0.2)&(flag==0)

         k=j;

         flag=1;

      end

   end

end


for i = 1:size(Ia,2)

   afinal(i)=a(i)/beta;
```

```
end

Rsgr=gradient(afinal,Ia);
m = size(Ia,2);
slopforn = (Ia(round(2*m/3))-Ia(round(m/3)))/(afinal(round(2*m/3))-afinal(round(m/3)));
Rsfinal = 1/slopforn;
n = afinal(round(m/2))*beta-Rsfinal*beta*Ia(round(m/2));
Vd=Vme-Ime*Rsfinal;

% Barrier height and lnI vs. Vdiode curve calculation

slop = (log(Ime(round(k/2)))-log(Ime(round(k/3))))/(Vd(round(k/2))-Vd(round(k/3)));
Is = exp(log(Ime(round(k/2)))-slop*Vd(round(k/2)));
BHini = -1/beta*log(Is/(S*A*T^2));

% Voltage dependent Barrier height

c=0;
d=size(Vme,1);
V = [0:range/(size(Ime,1)-1):range];
for j=1:size(V,2)
    BH(j)=BHini+(n-1)/n*(V(j)-Ime(j)*Rsfinal);
    if Rsfinal/5 < S*A*T^2*exp(-beta*BH(j))*beta*exp(beta*V(j)/n)
         c=c+1;
 end
end
```

```
% I-Vd curve generation

for j=1:d
   if j<=c
      I(j)=S*A*T^2*exp(-beta*BH(j))*(exp(beta*(V(j))/n)-1);
   else
     I(j)=V(j)/Rsfinal*(j-c)^3/d^3+S*A*T^2*exp(-beta*BH(j))*(exp(beta*(V(j)*(d-
j+c)/d)/n)-1);
   end
end
   c=0;

% Plot I-V without considering Rs effect.
   semilogy (V,I,'r')
   hold on
end

% Print obtained values to the screen

fprintf('Rs = %f, n= %f, Is=%e, BH= %f\n', Rsfinal, n, Is, BHini)

% Plot measured I-V
semilogy (Vme, Ime)
xlabel('Vin');
ylabel('Iout');
```

hold off

Appendix C

Charge pump circuit

Passive microwave integrated circuits, which do not have their own on-board battery, are receiving more and more attention due to their widespread applications, especially for RFID and sensor network applications. In passive microwave systems such as RFID, the self-biasing circuit is a critical component and consists of broadband antennas and charge pump circuits. In the charge pump circuit design, the power conversion efficiency and the required operating voltage are the most important design specifications. The adjustable design parameters for designing a charge pump are the number of stages, the contact areas of the Schottky diodes, and the capacitors. To maximize the power efficiency, each Schottky diode should have low turn-on voltage and high current flow. Because a CMOS process has default metal, such as tungsten, to be contacted to the silicon surface, the turn-on voltage cannot be changed. The contact area is an adjustable parameter and needs to be large to increase the diode current. However, the contact area of the Schottky diodes used should be limited to make the cut-off frequency of the charge pump circuit to be higher than the frequency of the applied RF signal. Since each Schottky diode itself consumes the incident power, a smaller number of stages shows the better power efficiency. However, to generate a higher operating voltage with small RF signal input, two or more stages are required.

An N-stage charge pump circuit consists of Schottky diodes and capacitors. To calculate the power efficiency, a sinusoidal voltage V_i, which has a frequency f_i and an amplitude V_a, is assumed to be an RF input. ($v_i = V_a \cos(2\pi f_i t)$) The required operating charge pump output voltage is V_{dd}. For a DC equivalent circuit, all capacitors are assumed to be open, and the voltage drop across each diode is Vdd/N. For an AC equivalent circuit, all capacitors are assumed to be short, and all diodes appear to be in parallel or anti-parallel to the input. As a result, the voltage drop across each diode is given by the following equation.

$$V_d = \pm V_0 \cos(\omega_o t) - \frac{V_{dd}}{2N} \tag{C.1}$$

If the incident RF signal is small enough that the series resistances of Schottky diodes is much smaller than the junction resistance, the series resistance can be neglected, and the junction capacitance is small enough to be ignored. The diode current is given by the following equation.

$$I_d = I_S \left[\exp\left(\pm \frac{V_a}{V_T} \cos(\omega_0 t) \right) \exp\left(-\frac{V_{dd}}{2NV_T} \right) - 1 \right] \tag{C.2}$$

By using the modified Bessel function series expansion, the exponential of a cosinusoidal function can be expressed by the following equation [57, 58].

$$\exp(\pm x \cos(\omega t)) = B_o(\pm x) + 2\sum_{n=1}^{\infty} B_n(\pm x) \cos(n\omega t) \tag{C.3}$$

The DC operating current I_{dd} is therefore given by

$$I_{dd} = I_s \left[B_o\left(\frac{V_a}{V_T} \right) \exp\left(-\frac{V_{dd}}{2NV_T} \right) - 1 \right] \tag{C.4}$$

The diode reverse leakage current depends on the contact area. From equation (C.4), the DC operating current can be adjustable by changing the contact area and the number of stages (N). From the measured results as shown in Figure C.1, the Schottky diodes with the contact area of up to 20x20μm^2 can be used for UHF (910MHz) or microwave (2.45GHz or 5.8GHz) applications. A 5-stage or 6-stage charge pump with 10x10μm^2 or a 4-stage charge pump with 20x20μm^2 would be the best choice for generating 1V of DC operating voltage.

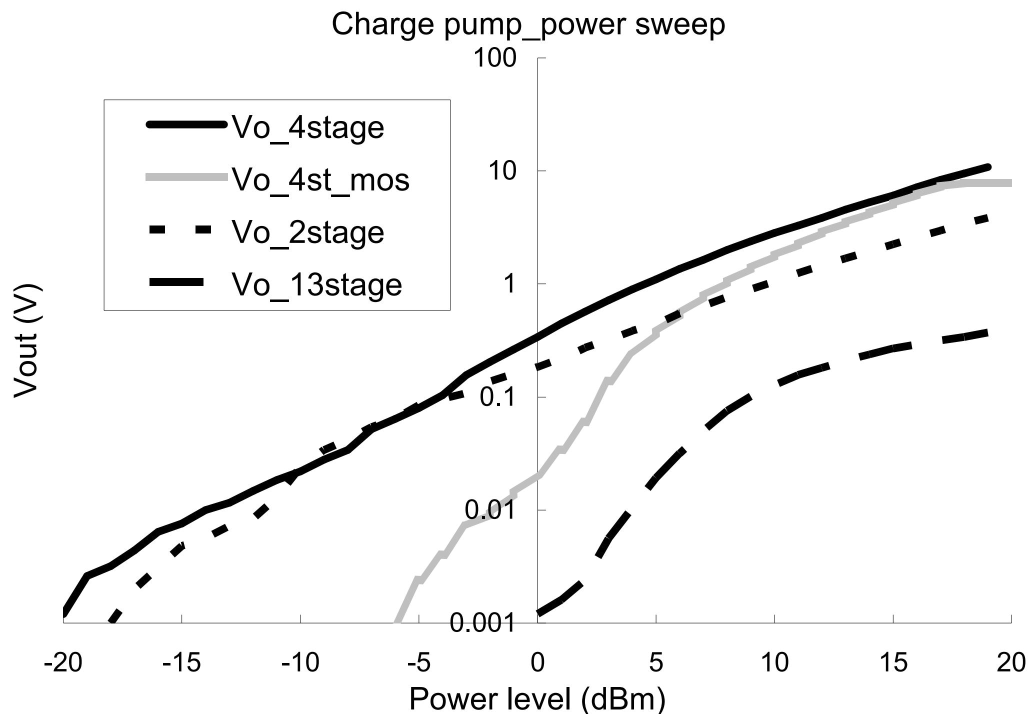


Figure C.1: Measured results of the fabricated charge pump circuits at 2.45GHz. The simulation result was similar to the measured result. Diode connected MOSFET showed less sensitive result as expected.

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