ABSTRACT

Title of Dissertation:	ANALOG SYSTEM-ON-A-CHIP WITH APPLICATION TO BIOSENSORS.
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This dissertation facilitates the design and fabrication of analog systems-on-a-chip (SoCs). In this work an analog SoC is developed with application to organic fluid analysis. The device contains a built-in self-test method for performing on-chip analysis of analog macros. The analog system-on-a-chip developed in this dissertation can be used to evaluate the properties of fluids for medical diagnoses. The research herein described covers the development of: analog SoC models, an improved set of chemical sensor arrays, a self-contained system-on-a-chip for the determination of fluid properties, and a method of performing on-chip testing of analog SoC sub-blocks.

ANALOG SYSTEM-ON-A-CHIP WITH APPLICATION TO BIOSENSORS

By

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Dedication

Jeremiah 29:11 For I know the thoughts I have for you says the Lord:
thoughts of PEACE (SHALOM) and not of evil
to give you an expected end. (KJV)

"For I know the plans I have for you," declares the LORD ,
"plans to prosper you and not to harm you,
plans to give you hope and a future." (NIV)

Lord Jesus,
I thank you for your thoughts, your peace, your mercy,
and your strength.

To Robert Spencer and Carolyn Van Hodge,
I couldn't imagine better parents.
Thank you, you are a blessing to us.

To Dr. Robert W. Newcomb,
Thank you for your help, and excellence in advising me.

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The author also acknowledges the MOSIS educational program which provided free fabrication of integrated circuits designed in this dissertation. This dissertation, therefore, acknowledges the organizations that jointly funded the MOSIS educational program: MOSIS, AMIS, and IBM.

The work in this dissertation began as a collaborative effort with The University of Maryland's Electrical Engineering Department, Microsystems Laboratory (Dr. Robert W. Newcomb and Angela Hodge), The George Washington University (Drs. Mona Zaghloul and Sharokh Ahmadi), and The United States Naval Academy (Dr. Louisa Sellami).

In 2000, through employment at the National Institute of Standards and Technology, Electronics and Electrical Engineering Laboratory, Semiconductor Electronics Division, Hodge expanded the research through the use of the division's microelectronics fabrication facility. Hodge wishes to thank Russell Hadjay for the numerous hours of processing facility training she received to further the efforts of

this dissertation. This dissertation also acknowledges the efforts of the student co-op from The George Washington University, Onur Tigli, in instituting some of the device layout.

This dissertation also acknowledges worked performed through employment and collaboration with the Naval Research Laboratory's (NRL): Code 6800, Electronics Science and Technology Division and Code 6900, Center for Biomolecular Science and Engineering. The work performed in this dissertation, relevant to these NRL entities includes the analysis of the gateless field effect transistor (macromolecular sensor). Particular acknowledgement is made to EOIR contractor, Stephanie Fertig, for training Hodge received in performing linker chemistry and for efforts made by Fertig and Dr. Leonard Tender to perform the surface chemistry through which DNA sensitivity was achieved. Additional acknowledgement is made to NRL employees, F. Keith Perkins and Martin Peckerar for the use and design of test equipment and procedures for macromolecular sensor testing and for the use of their fabricated macromolecular sensors.

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Chapter 1 Introduction

Section 1.1 Motivation for the Research

In a number of areas, it would be useful to have available smart sensors that can determine the properties of a fluid and from those make a reasoned decision. Among such areas of interest might be ecology, food processing, and health care [1]. For example, in ecology it is important to preserve the quality of water from which a number of parameters are of importance, including physical properties such as color, odor, and pH, as well as up to 40 inorganic chemical properties and numerous organic ones [2]. Therefore, in order to determine the quality of water it would be extremely useful if there were a single system on a chip which could be used in the field to measure the large number of parameters of importance and make a judgment as to the safety of the water. For such, a large number of sensors are needed as well as a means of coordinating the readouts of the single sensors into a user friendly output from which human decisions could be made. As another example, the food processing industry needs sensors to tell if various standards of safety are met. In this case it is important to measure the various properties of the food, for example the viscosity and thermal conductivity of cream or olive oil [3]. In biomedical engineering, biosensors are becoming of considerable importance as they have the potential to aid in medical diagnoses by providing a means of analyzing biological fluids for the existence of antibodies, which are proteins, commonly associated with diseases. There are a number of different types of biosensors including

electrochemical sensors, thermal sensors, mass flow sensors and optical sensors [4, 5, 6].

In the biomedical engineering field, methods for the selective determination of compounds in fluids are very important in clinical analysis. Present methods often require a long reaction time and involve complicated and delicate procedures. One valuable application in the health care area is that of the use of multiple sensors for maintaining in space astronaut health. In this arena, an array of eleven sensors is used to maintain the quality of recycled air although separate control and is effected by the use of an external computer. Therefore, the development of inexpensive and miniaturized sensors that are highly selective and sensitive and for which control and analysis is present all on one chip is very desirable.

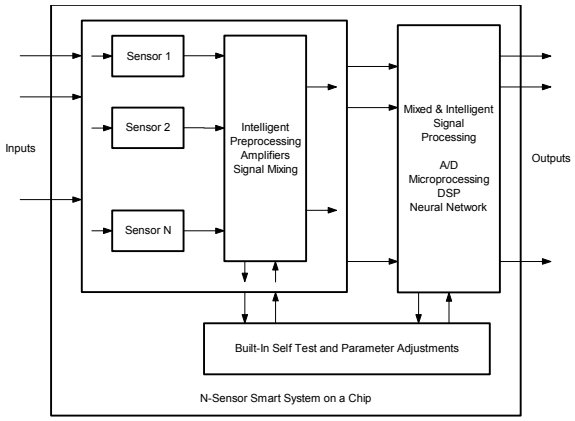


Figure 1.1 Architecture for N-Sensor Smart Sensor on a Chip

These types of sensors can be implemented on a semiconductor substrate with very large scale integration (VLSI) technology. Because the sensors are fabricated on a semiconductor substrate, additional signal processing circuitry can easily be integrated into the chip thereby readily providing functions such as multiplexing and

analog-to-digital conversion. In numerous other areas, one could find similar uses for a smart multi-sensor array from which measurements can be made easily with a small portable device.

The proposed architecture of these systems as shown in figure 1.1, can be configured with multiple inputs, sensors, and outputs. In addition to this is a series of smart signal processing elements called built-in self-test (BIST) devices, which are capable of evaluating each of the unique systems (sensors, analog-to-digital converters, etc) on the chip. In this system, there may be many classes of input signals (for example, material [as a fluid] and user [as an indicator of what to measure]). On each of these inputs, there may be many sensors (for example, one material may go to several sensors, each of which senses a different property [such as dielectric constant in one and resistivity in another]. The sensor signals are treated as an N-vector and combined as necessary to obtain the desired outputs, of which there may be many (such as an alarm for danger and indicators for different properties). For example, a patient with kidney disease may desire a system-on-a-chip (SoC) that gives an indication of when to report to the hospital. For this, the SoC would indicate a deviation of the dielectric constant from normal. In addition the spectral properties of peritoneal fluid may be sensed, with appropriate warning indicators for abnormal readings. These indicators could be combined to detect the presence and percentage of creatinine, a protein produced by the muscles and released in blood, in a fluid sample. A signal output for the system could indicate the percent of creatinine in the fluid with an appropriate warning alarm or indicator light when such percentages reach dangerous levels.

The underlying goal of this research is to develop biosensor devices capable of performing on-chip self-diagnostics. This work focuses on creating an on-chip built-in self-test (BIST) scheme for an array of biosensors and other system-on-a-chip related medical devices. This research will assist the medical industry by aiding in the early detection of faulty sensor devices used for the detection and treatment of disease. This research will aid health care providers in saving human lives, by providing an early warning system for the detection of faulty equipment and sensors.

In addition to developing a novel BIST method, this work will perfect the development of two unique multi-sensor systems. The first sensor system studied will be capable of detecting impurities in fluid. The principle behind the type of biosensor used in this research is that, by evaluating the effects of resistivity changes on the gain of a ChemFET, impurities can be detected in any liquid. The second sensor system studied will exploit the use of biosensors in performing matches and mismatches of antibody antigens and/or deoxyribonucleic acid (DNA) for the purpose of deciphering chemical compounds.

Section 1.2 Statement of Proposed Problem

The driving force in today's semiconductor industry is the need to maintain a rate of improvement in speed and size reduction of 2x every eighteen months in high-performance components. Currently, these improvements rely exclusively on advances made in semiconductor miniaturization technology. The 1999 International Technology roadmap for Semiconductors (ITRS) suggests that, "innovation in the techniques used in circuit and system design will be essential to maintain the

historical trends in performance improvement" [7]. Achievement of this advancement in circuit and system design techniques is increasingly becoming dependent on integrating multiple silicon technologies on the same chip. The devices that result from the aforementioned integration of multiple technologies are commonly referred to as System-on-a-Chip (SoC) devices.

Design is paramount for all categories of the ITRS roadmap. This is especially true for the SoC category where time-to-market for an Application Specific Integrated Circuit (ASIC) is a key attribute for new product delivery. Design is additionally important for SoC devices because of increasing system complexity. The growth of system complexity is due to the diversity of SoC design styles, integrated passive components, and the increased need to incorporate embedded software. Design for SoC devices will become increasingly difficult with the growing interaction among design levels, the difficulties associated with including multiple designs onto a single chip, design process predictability, and the growing size and dispersion of design teams.

These challenges are overcome with the use of block-based design approaches that emphasize design reuse. System blocks often contain a layout file that is used for the fabrication process and an Analog Hardware Description Language (AHDL) behavioral model used to describe the interaction of system components during the design process. Each system block should have features that allow for the implementation of on chip Built-in Self-Test (BIST). The emergence of the SoC paradigm imposes various metrology and standardization challenges. These include metrology for multi-technology process monitoring, BIST calibrations, validation of

behavioral model representations, and benchmarking simulation of system-on-a-chip systems interactions.

Another significant challenge involves ensuring the testability of a System-on-a-Chip of IC design. This is a formidable task, as testability within the context of mixed technology integrated circuits is not well defined. Testability is defined in this dissertation as controllability and observability of significant waveforms within a circuit. For most IC designers, significant waveforms are input/output signals that can be obtained at every stage of the circuit. The first stage of the circuit input is assumed to be controllable; while during the last stage, output is observable.

Some have proposed methods of assuring testability that involve the use of oscillatory BIST techniques [8, 9]. The BIST method using an oscillation-based test circuit has been shown to have the potential of overcoming common problems associated with conventional test methods. This BIST method has also been shown to be effective for any type of mixed analog/digital circuitry used as system blocks.

Section 1.3 Outline of the Methodology

Subsection 1.3.1 Multi-Sensor System Architecture

The architecture of the Multi-Sensor Smart System is given in figure 1, where there are multiple inputs, sensors, and outputs. A built-in self-test (BIST) element is included between each signal processing element. In this system, there may be many classes of input signals (for example, material [as a fluid] and user [as indicator of what to measure]). Each of the inputs may be directed to many sensors (for example,

one material may go to several sensors, each of which senses a different property [such as dielectric constant in one and resistivity in another]).

The sensor signals are treated as an N-vector and combined as necessary to obtain the desired outputs, of which there may be many (such as an alarm for danger and indicators for different properties). For example, a patient with kidney disease may desire a system on a chip that gives an indication of when to report to the hospital. In this case, an indication of deviation of dielectric constant from normal and spectral properties of peritoneal fluid may be sensed. Once combined, they indicate the presence of creatinine (a protein produced by the muscles and released in the blood) in the fluid. Here, the signal output is recognized as the percent of creatinine in the fluid and an alarm when at a dangerous level.

To design multi-technology SoCs such as in figure 1, block-based design approaches that emphasize design reuse are preferred, to reduce overall design time and cost of testing the new device. System blocks often contain a layout file that is used for the fabrication process an Analog Hardware Description Language (AHDL) behavioral model used to describe the interaction of system components during the design. To validate the interaction between various sensors, signal processing, and BIST sub-blocks, further development of a unique Testbench-on-a-Chip methodology.

Subsection 1.3.2 Testbench-on-a-Chip Methodology

The Testbench-on-a-Chip evaluates the interactions between key sub-blocks of the multi-sensor smart system. Figure 2 shows the block diagram of the Testbench-on-a-Chip. The most important aspect of the Testbench-on-a-Chip

methodology is to be able to multiplex input signals from different sensor system blocks or reference signals from different sensor system blocks or reference signals to different BIST system blocks. The outputs of the BIST system blocks are then multiplexed to the digital out of the TBOC. This enables the use of a computer controlled test system to select and analyze the interaction between different system blocks for a wide range of computer controlled test vectors.

The following sections describe the electronic circuitry used for my proposed Testbench-on-a-Chip in more detail. Included in this circuitry description are biosensors, ring oscillators, test op amps, and smart signal processing in the form of a MUX/DeMUX pair.

Subsection 1.3.3 Biosensor Systems

The class of biosensors studied in this work is designed to analyze physical properties of fluids. These sensors are capable of deciphering various characteristics associated with fluids including: pH, resistivity, and dielectric constant. The sensors can also discern inorganic and organic chemical properties. Such sensors are implemented using micro-electro-mechanical system (MEMES) technology. The sensor circuit can be fabricated on a semiconductor substrate that allows for the integration of additionally signal processing circuitry onto the chip. An array of such sensors can be used to determine multiple properties of a fluid, using a single chip.

Figure 3 is a schematic of the sensors studied for the detection of fluid properties. This example sensor circuit operates as a dielectric constant measurement device. This sensor can be provided as part of an integrated micro-system designed to determine the properties of a fluid. The fluid-sensing transistor in this sensor is a

VLSI adaptation of the CHEMFET. The sensor operates as a capacitive-type bridge such that a balance can be set for a normal dielectric constant. In the presence of a fluid, the unbalance that occurs within this sensor bridge is used to evaluate the fluid's dielectric constant.

The four CMOS transistors form the bridge: M1, M6, M7, and the fluid-sensing transistor comprised of transistors M2 through M5. The fluid-sensing transistor and transistor M1 the PMOS (p-type MOSFETs) transistors in the diode connected configuration (gate connected to drain). The lower two transistors, M6 and M7, are NMOS type (one diode connected and the other with a gate voltage control). The output, Vout, of the sensor circuit is taken between the junction of the fluid-sensing transistor and the diode-connected transistor, M7.

The transistors, M2 through M5, have openings in their gates to allow fluid to flow between the silicon substrate and the polysilicon gate where the gate oxide has been removed. This allows the fluid to behave as the gate dielectric for that transistor. Each of the transistors has a ratio of 10u/10u. The overall W/L ratio of the fluid-sensing transistor is therefore 40u/40u.

The fluid-sensing transistor is constructed out of four transistors with all terminals connected in parallel to increase the gain constant parameter KP that is proportional to the dielectric constant. Fabrication of the sensor is based on a sacrificial etch process, where the silicon dioxide gate dielectric in the fluid-sensing transistor is removed by chemical etch. This activity is accomplished by opening holes in protective layers using what is known as the, over-glass cut method available in the MOSIS-MEMS fabrication process.

The other sensor under study in this work is a biological macromolecular sensor for early detection of diseases. Over the course of this research, I will propose an analytic model for this sensor. The sensor, is a gateless depletion-mode field effect transistor (FET) having a source implant and a drain implant that are spatially arranged within a semiconductor structure. The source and drain are separated by an active channel, which is covered by a dielectric layer. The dielectric layer has a bottom surface, which is in contact with the active channel and a top surface, which is in contact with a sample solution. The top of surface of this gateless FET is modified with a receptor for detecting the presence of target antibody antigens and/or DNA strands. A reference electrode is attached externally to the sample solution. Figure 4, below shows the cross section of the device. The cilia-like structures or microchannels described also represent DNA and/or antibody antigen receptor sites.

The sensor detects the presence of target molecules in the sample solution by measuring the change in current between the source and drain. The change in current occurs via one of two methods. The first is due to the change in capacitance of the receptor-modified dielectric film/sample solution interface when target molecules bind to the molecular receptors. The second is the result of charged molecules binding to the receptor-modified dielectric film or sample solution interface.

The gateless field effect transistor will be evaluated for its ability to adequately detect matches in target, antibody antigen solutions. The sensors are active element devices capable of developing circuit gain. Such devices are known for their high input impedance, which makes them suitable for pre-amplifier application. Figure 5 below presents a schematic diagram of the gateless field effect

transistor. This provides the basis for the analytic model I will create, which will lend itself to development of chemical sensor simulations.

The gateless FET is small, easily mass-produced, and directly integrable in electronic systems. Large numbers of these devices can be packed into small areas, lending to the straightforward implementation of arras. One of the added advantages of the FET is that it can discriminate between charge and the thickness of a deposited film.

In spite of the many advances that have been made in the development of mixed signal technologies and biomedical devices, traditional methods of these implementations are limited by Moore's law. Moore's law suggests that, improvement in the development of semiconductor devices appears in the factor of 2X increase in device performance every 18 months. As system complexity becomes greater with time, there is a need to develop methods of maintaining this rate of improvement while decreasing time to market. The remainder of this work will address the issues associated with system-on-a-chip development of mixed signal technology. The example SoC developed in this work has application to the field of biomedical engineering as it serves as a means of testing biological and related fluids on a single chip.

Section 1.4 Dissertation Contributions

- **Design of an Analog System-on-a-Chip for testing fluidic properties including: DNA, Antibody Antigen, and Dielectric Constant**

  In chapter 3 of a novel system-on-a-chip (SoC) design is provided. The design encompasses the use of an array of biosensors to perform on-chip

measurements of a transistor's response to the dielectric constant of a fluid under test. The biosensors are analyzed and evaluated with hand calculations and SPICE simulations. Included in this analysis is the fabrication and evaluation of a gateless field effect transistor and a VLSI implementation of the ChemFET in chapter 4.

- **Models and Implementation of analog system-on-chip macros**

  Analog system-on-chip sub-blocks such as a chemical field effect transistor, macromolecular sensor, built-in self-test, voltage controlled oscillators, and level crossing detectors, are evaluated. Models of BIST sub-blocks and the responses of these sub-blocks to faults in a biosensor are transformed into equivalent system on a chip models. Hand calculations, system-level implementations, and SystemC source Code (SoC Model) implementations are provided for each device in chapter 3. In chapter 4, the SoC models are simulated and compared against equivalent SPICE simulations and hand calculations.

- **Design, implementation, and simulation of an analog SoC subblock testing procedure.**

  An oscillation based built in self test procedure is developed in chapter 3 to perform parametric and catastrophic testing of system-on-a-chip sub-blocks. The procedure involves the use of an oscillation based built-in self-test (BIST) method to detect potential system errors that may exist beyond a reasonable tolerance. The method developed is a modification of a previously developed oscillation test strategy and is novel in its application to sensor technologies. In chapter 4,

simulations of the oscillation based BIST components are provided. These simulations are generated by SPICE and through the analysis of hand calculations.

- **Design and evaluation of fabricated fluid analyzer sensors in the presence of antibody antigens (DNA), buffer, water, and air.**

  In chapter 3 the design of fluid analyzer sensors is presented. Included in the design are equations that model sensor performance and fabrication techniques. Chapter 3 also describes the process by which antibody antigens are attached to the sensors for substance evaluation. In Chapter 4 measurements of the gateless field effect transistor response to the presence of antibody antigens are presented. The response of the VLSI implementation of the ChemFET to various fluids is also shown in chapter 4.

Chapter 2 Background

Section 2.1 Overview

One of the challenges of developing systems-on-a-chip is making analog mixed-signal (AMS) intellectual property (IP) for off the shelf applications as ubiquitous as digital IP. This is largely due to the fact that the end user's design requirements preclude the "clean" reuse, seen when working with digital blocks [10]. This is because the performance of analog SoC designs is far more affected by system-level requirements such as technology, power, die size, and package type, than digital designs. Other variables that affect the feasibility of developing analog SoC sub-blocks include inherent performance sensitivity to designer specified variables such as: wirebond or flip-chip package, the desired I/O pitches, the number of metal layers in the technology process or whether the user wants to use a "low-voltage" or "generic" process. As such, digital SoC IP development has seen significantly more progress than the analog IP equivalents.

Analog designers, however, have made progress in a few areas. The first is the development of standards for AMS interfaces. The second is in the development of software tools for migrating analog circuits across similar process technologies.

In this chapter we discuss the current state of the art in system-on-chip development with application to biosensors. In section 2.2 information on SoC technology is provided. In section 2.3, built-in self-test (BIST), mainstream methods of performing SoC Test and verification are discussed. In section 2.4, the use of the

oscillation test strategy for BIST is analyzed. Section 2.5 offers a discussion of the current state of the art in system-on-chip modeling. While in section 2.6 a discussion of mainstream biosensor devices is provided. The contents of this chapter are summarized in section 2.7.

Section 2.2 System-on-a-Chip (SoC) Technology

For over a decade integrated circuit technology has seen significant changes beginning with the adoption of high-level description languages such as VHDL (very high-speed IC description language) and Verilog. The industry has also seen marked increase in manufacturing foundries. There has also been a shift in IC business away from vertically integrated semiconductor companies towards horizontally strong design companies [11]. This represents a shift from IC companies composed of large design teams, expensive manufacturing factories, and internal CAD tools development teams towards design houses. IC fabrication foundries have cornered the manufacturing market.

These changes reflect the never-ending increase of silicon capacity available to system and IC designers that has been predicted by Moore's Law. This now brings to the forefront, a cyclical crisis in design methodology and engineering productivity generating a ripple effect through the electronics industries [12]. The system-on-a-chip era, however, requires more than available silicon, it requires a new design methodology roadmap based on IP reuse needs.

There are now three industry leaders in the field of electronic-CAD tools development: Cadence Design Systems Inc., Synopsys Inc., and Mentor Graphics Corporation. Such commercial tools give IC design engineers the flexibility that is

needed to switch jobs easily; whereas, in-house tools that are specific to a given company's infrastructure are not as marketable to IC designers and today's manufacturing companies.

There has also been a trend over the past few years towards design services such as intellectual property (IP) providers, IC testing services, equipment-rental companies, etc. These companies provide a service to IC design practice as they facilitate the SoC design methodology, which has lead to new IC design business models and electronic-CAD tools development.

The starting point of any design project is writing the specifications. Such specifications, executable specifications, are typically written in C, C++ and/or HDL. Formal specifications are the characterization of the design, defined independently of any implementation. Once these specifications are identified, formal methods and tools can be used to check against the specifications. During this process decisions about timing and synthesis, functional design issues, physical design issues, verification strategies, and test strategies must be made.

The IC creation cycle can be broken up into four main steps: Concept, Design, Verification, and Implementation. For the Design to Verification step, there are certain industry wide acceptance ratios for specific tasks. These are identified by table 2.1 [13]. These ratios identify that the research effort most poignant to IC design revolves around verification. The verification process can be viewed in a hierarchical manner with reusable IP cores, SoC leave cells. Thus, the SoC design methodology can be divided into the following: identification of system requirements, writing preliminary specifications, developing high-level algorithmic

models, refining and testing algorithms, determining hardware/software requirements (characterizing the library of hardware/software macros & interface protocols), defining interfaces, partitioning device components into macros, and writing preliminary specifications for the macros.

Task	**Time Ratio (%)**
Verification	40
RTL + Synthesis	20
IC Layout	10
Test	10
System Integration	10
Other	10

Table 2-1 Shown are the catastrophic fault results on LCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 4x in their respective W/L ratio.

System-on-Chip (SoC) and mixed-signal devices in the marketplace will continue to increase rapidly as the semiconductor electronics industry enters the era of multimillion-gate chips. It has been predicted by some that within the next few years, state-of-the-art integrated circuits (ICs) will exceed 12 million gates and operate at speeds surpassing 600 MHz [14]. The IC industry has found that manufacturing costs for these devices are dominated by the direct and indirect costs associated with testing [15]. Involved in testing an IC are the direct costs associated

with procurement of test equipment and time to test and the indirect costs of developing test procedures. Moreover, the analog portion of mixed analog/digital circuitry although making up less than 10% of the overall chip area, has test procedures that tend to dominate the test time of mixed technology chips. This is due to the following:

1. Accurate analog signal sources must be fabricated onto the circuit under test (CUT).
2. Specialized equipment containing precision circuitry must be used to test Analog-to-Digital converters (ADCs) and Digital-to-Analog converters (DACs).
3. Current methods for testing ADCs and DACs require the use of expensive test equipment.
4. Cables that run from the CUT to the ADC's and DAC's of the tester often introduce parasitics that affect the performance of the chip [11].

Built-In Self-Test methods are expected to assist designers in avoiding many of these concerns. A necessary challenge to overcome involves ensuring the testability of an IC design. This is a formidable task as testability within the context of integrated circuits is not well defined. Testability is defined as controllability and observability of significant waveforms within a circuit structure [16]. For most IC designers, significant waveforms are input/output signals that can be obtained at every stage of a circuit design. The first stage of the circuit, input, is assumed to be controllable; while, the last stage, output, is observable.

Section 2.3 Built-In Self-Test

BIST methods will prove invaluable in assessing the real time accuracy and functionality of system-on-a-chip devices. Mixed signal BIST, in particular, will see increased usage in devices [17]. Despite the general consensus that suggests BIST as a relatively new technology, its principles have been used as part of high-performance analog design processes for several years [18]. Mixed signal BIST is used extensively in most auto-calibration techniques and feedback loops. However, to date no published approach performs on chip measurements of all key intellectual property (IP) device parameters (including analog-to-digital (ADC) and digital-to-analog (DAC) converters) while keeping time to test lower than conventional automatic test equipment (ATE) [19]. In general the field of mixed signal design and test has seen that simulations, silicon performance, and economic feasibility are continuously in competition with one another. For example, BIST circuit gate area is of economic importance because it increases IC area and because IP providers tend not to compare the BIST area to the overall IC circuit, but solely to the circuit-under-test (CUT) [20].

The problem with testing mixed-signal circuits arises from the fact that digital and analog fault models are inherently different. While digital fault models are understood to be stuck-at faults, analog fault models not quite as well defined or mature [21]. Moreover, analog signals are imprecise. Therefore, the accuracy of the measurement becomes a key concern. This represents a stark contrast to the logic '1' or '0' measurements of digital circuits. The many advantages of BIST cannot be fully exploited in mixed-signal circuits as long as the analog portions of mixed-signal technologies remain unsure. As such, in recent years, analog and mixed-signal

circuits have grown in importance and as a consequence several researchers have begun to address the problem of BIST for analog and mixed-signal circuits [9,10].

There are in general two categories of BIST techniques: functional and fault-based. Functional BIST apply traditional stimuli, such as sinusoidal or multi-tone waveforms, and measure the functional specifications of the circuit under test (CUT). Fault-based BIST techniques, however, are designed to detect faults using unconventional stimuli and signatures. Most of the BIST schemes test the analog blocks in a mixed-signal circuit using the digital-analog-digital path. This is unlike the analog-digital-analog path used by conventional external tests.

Several functional BIST schemes have been proposed for special classes of analog and mixed-signal circuits. Many of these schemes are based on on-chip functional testing of analog specifications including signal-to-noise ratio (SNR), frequency response and intermodulation distortion. Moreover, mixed-signal circuits with on-chip digital signal processing (DSP) cores may be used to perform DSP-based Fast Fourier Transform (FFT) testing. Here, the DSP core generates a 512-point sinusoidal input stimulus that is applied to the ADC via the DAC. An FFT analysis of the output response from the ADC is used to measure the combined performance of the DAC and ADC.

For circuits that do not contain a DSP core, the area overhead of performing an FFT analysis is extremely high. To counteract this, digital filtering techniques can be used. In these instances, on-chip sine or multi-tone test stimulus is generated using an over sampling based signal generator. Although, this generator is predominantly digital it includes an imprecise low pass filter. A narrow band digital filter is used to

measure the output performance of the circuit by separating the signal from noise power. As such the filter must be carefully designed to minimize the bias in test results.

Other BIST structures revolve around testing offset, gain, integral and differential linearity of DACs and successive approximation type ADCs. For these methods, a counter is used to generate the test stimulus and the output is sampled and compared with an appropriate reference voltage, which is selected by an analog multiplexer.

In contrast, fault-based tests are aimed at detecting manufacturing defects, which are modeled as faults, as opposed to measuring the functional specifications. In fact, several fault test schemes have been proposed that use different kinds of waveforms as test stimuli, which are easy to generate on-chip. These schemes typically compress the output response into various signatures. However, as a result of the imprecise nature of analog circuits and the absence of a direct mapping been the signatures and functional specifications, it is possible the test may result in a "fail" response for good circuits. As such, these BIST approaches for analog circuits must be evaluated not only on the basis of area overhead and fault coverage, but also yield coverage.

HBIST is a fault-based BIST scheme for mixed signal (hybrid) circuits. It allows the evaluation of analog test responses within a digital kernel system. Analog test stimuli, provided by the Hybrid Test Stimulus Generator (HTSG, an on-chip generator) are based on digital shift registers, which are used as signature analyzers. This digital BIST scheme has a very low area and performance impact. To overcome

the limitation of digital signatures, which inherently cannot accommodate tolerances in analog signals, a pattern manipulator is used to prevent the application of those input values that place the output response within the tolerance range of the comparator.

Another fault-based BIST method involves an analog signature analysis scheme that accommodates tolerances in analog signals. This method uses digital integration to accumulate the analog test response signature and computes the probabilities of aliasing and false rejection as a function of circuit tolerances and the signature register width. The absolute value of the signal is taken before integrating to reduce aliasing due to fault masking. The use of an analog integrator as a signature analyzer is also a feasible solution. Additionally, another on-chip test response measurement technique that takes into account the tolerance of signals uses special detectors, window comparators, for verifying whether or not the parameters converted to voltages are within an acceptable window.

A test technique for analog linear time-invariant (LTI) circuits embedded between DAC and ADC involves the linear transformation of the output sequence. This transformation of the input random process is analyzed by the first and second moments (mean, auto- and cross-correlations). These signatures are computed using digital arithmetic operations and have been compared with respect to fault coverage, hardware overhead and testing time. Correlations have better fault coverage than the mean. Autocorrelation requires less hardware and testing time compared to cross correlation. Further, research has shown that cross-correlation signatures are an approximation to a circuit's impulse response [22]. Another pseudorandom test

technique, the Fischer method, is used as a discrimination technique to define the boundaries of the signature space in order to maximize the fault and yield coverage and minimize the number of signatures required. Logistic discrimination analysis has also been used to select a minimal set of measure and tests consisting of DC and low frequency AC stimuli.

A concurrent test method for linear analog circuits, is one in which tests are based on continuous checksums. The checking circuit is implemented by a cascade of integrators and is virtually fixed regardless of the size of the original circuit. This scheme generates a non-zero signal in the case of fan error in the ac transfer function of the circuit. The method can be simplified for application to DC testing.

Another approach to fault-based testing involves self-checking analog circuits as presented by Vinnakota and Harjani [23]. In this work we see the way in which dual-rail code can be used to design self-checking fully differential analog circuits. The underlying methodology is geared towards the detection of transient faults.

A final style of BIST schemes involves low-cost vectorless BIST schemes that eliminate the need for test stimuli selection and application. These schemes convert the circuit into an oscillation mode during test. Faults cause the circuit to either stop oscillating or result in an oscillation frequency that differs beyond the tolerance range of the circuit's nominal value. The oscillation frequency can be evaluated using pure digital circuitry and interfaced to the boundary scan. The test method consists of portioning the complex circuit into functional building blocks such as operational amplifier, comparator, filter, PLL, etc., which are converted into circuits oscillate by adding additional circuitry or by cutting the damping loops and digitally

programming the filter coefficients. This process tends to achieve significant reduction in test times as compared to traditional testing methods. The oscillation test strategy is of particular interest and will be discussed in further detail in the following section.

Section 2.4 Built In Self Test with Oscillation Test Strategy

The oscillation test strategy (OTS) created by Arabi and Kaminska works by partitioning a complex analog circuit into functional building blocks such as: amplifier, operational amplifier (opamp), comparator, Schmitt trigger, filter, voltage reference, oscillator, phase lock loop (PLL), etc. or a combination of these blocks [24]. During the test mode, by adding some additional circuitry, each building block is converted to a circuit producing sustained oscillations. The oscillation frequency f_{osc} can be expressed either as a function of the CUT components or as a function of its important parameters. The building blocks that inherently generate a frequency such as oscillators do not need to be rearranged and their output frequency is directly evaluated. All operations are managed using control logic (CL).

Figure 2.1 below illustrates the application of the OTS method as a design for test (DFT) technique to improve the testability and ease the test problem. In the test mode, the CUT is partitioned into building blocks that are converted to oscillators using some additional circuitry. An analog multiplexer (AMUX) selects the output of the building block under test and its oscillation frequency is externally evaluated using test equipment. Before starting the test procedure the functionality of the test circuitry is verified by activating the test signal.

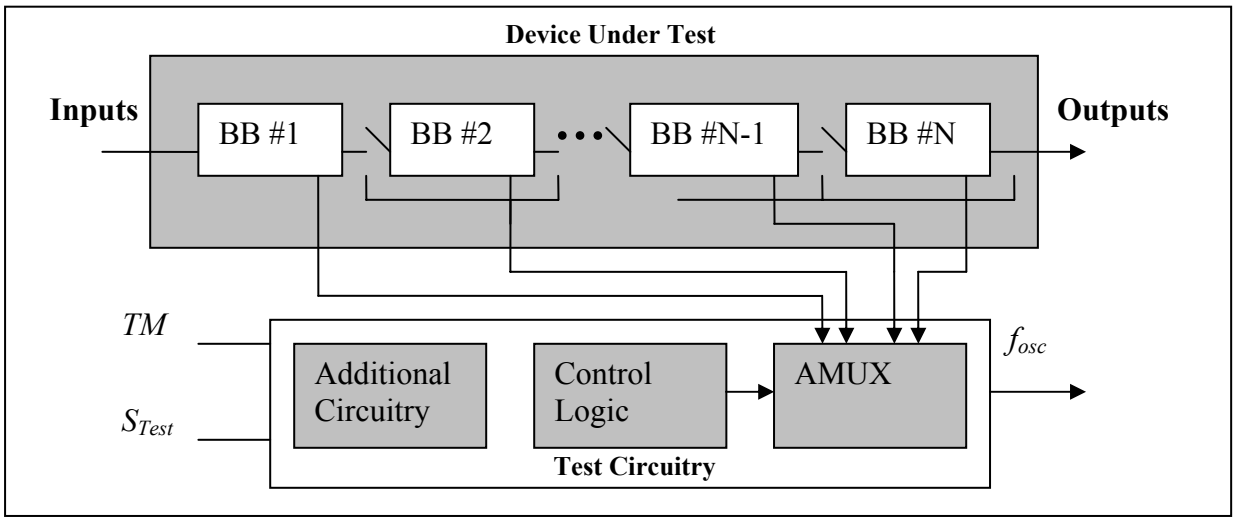


Figure 2.1 Simplified Test Structure of the Oscillation Test Strategy

The first step for this on-chip test method involves converting an analog building block to an oscillator with the use of appropriate feedback loops and adjustments to ensure sustainable oscillations. Depending on the CUT the feedback loop can be negative, positive or a combination of them.

Observability of a fault in a component C_i (or a parameter P_i) is defined through the sensitivity of the oscillation frequency f_{osc} with respect to the variations of the component C_i (or the parameter P_i). To increase the observability of a defect in a component (or a fault in a parameter), the sensitivity of the oscillation frequency with respect to that component (or parameter) should be increased. In other words, during the conversion process of the CUT to an oscillator, the oscillator architecture must be chosen to insure the maximum possible number of contributions for each of the CUT components to the resulting oscillation frequency. Existing faults in the

CUT related to components (or parameters that are involved in the oscillator structure manifest themselves as a deviation of the oscillation frequency. Therefore, the deviation of the oscillation frequency from its nominal value may be employed to testify to the existence of a fault. The tolerance band of f_{osc} for each CUT is determined using a Monte Carlo analysis taking into account the nominal tolerance of all important technology and design parameters. The accuracy necessary for additional circuitry is around the same accuracy provided for other CUT components.

The process of evaluating the OTS method involves understanding the fault modeling process. Analog fault modeling, for example, involves either parametric (soft) or catastrophic (hard) faults. Parametric faults, caused by statistical fluctuations in the manufacturing process, comprise the small deviation of CUT parameters from their tolerance band. Catastrophic faults are introduced by random defects and result in failures in various components. They are provoked, for example, by dust particles on a photolithographic mask which may cause either a short (open circuit), or large deviation of CUT parameters from their tolerance band such as width-to-length (W/L) ratio of a MOS transistor [25, 26].

Many studies have been devoted to determine the dominant fault type and to define the appropriate fault models. Research results denoted that 80-90 percent of observed analog faults were catastrophic faults consisting of shorts and opens in diodes, transistors, resistors and capacitances [27, 28]. It was also found that a test method which detects 100% of catastrophic faults did also find the majority of soft faults depending on the deviation value of the soft fault. The occurrence probability of faults has also been considered by Arabi and Kaminska. Their studies suggest that

catastrophic faults, and especially short faults, are dominant in both bipolar and CMOS processing technologies.

The catastrophic faults considered by Arabi and Kaminska in the evaluation of the OTS method comprise all possible shorts between circuit nodes and open faults at all circuit nodes excluding the transistor gates. An open fault was simulated by introducing a 10 M-ohm resistor. A short fault was modeled by a 10 ohm resistor.

A general method useful for converting an analog building block to an oscillator consists of adding a feedback loop to its structure and then adjusting the feedback elements to establish and sustain oscillation. Depending on the CUT the feedback loop can be negative, positive or a combination. The area overhead depends on the CUT and the chosen oscillator structure. In the case where a single oscillation frequency is not sufficient to cover all target faults, a suitable element of the feedback may be varied to produce different oscillation frequencies.

The OTS method was evaluated against a two stage CMOS operational amplifier (circuit under test) figure 2.2 below. This oscillator employs both positive and negative feedback. The op-amp is first converted to a limited-gain amplifier and then cascaded with a simple RC high-pass filter to construct a band-pass circuit. If the gain of the pass-band system is slightly greater than unity at its central frequency, connecting the output of the band-pass circuit to its input will result in sustained

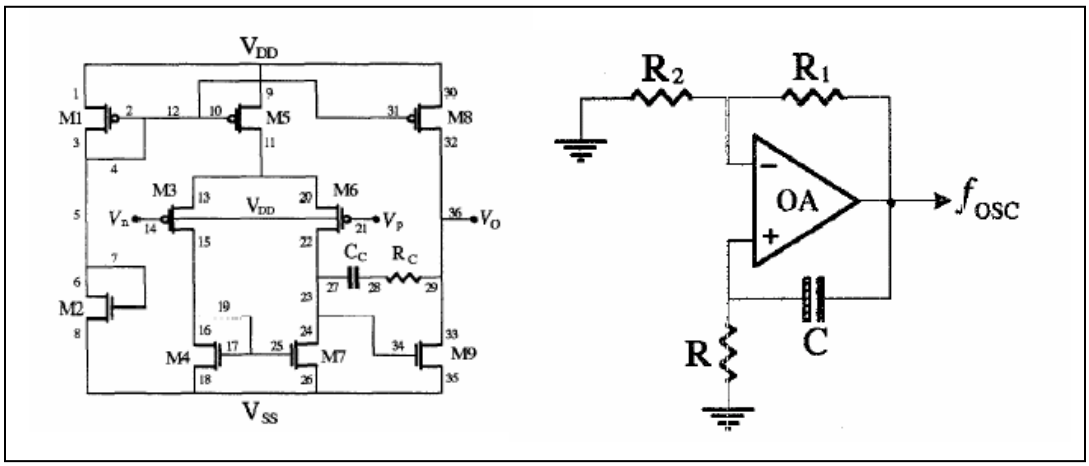


Figure 2.2 The schematic on the left is a 2-Stage CMOS Operational Amplifier Schematic. Circuit Under Test for OTS [9]. The schematic on the right represents the oscillation feedback system created with the additional resistors and capacitor.

oscillations at its central frequency. In reality noise at the input of the system is band-pass filtered, slightly amplified, and then fed back to the input, and the same action is repeated. Therefore, the system tends to oscillate at its central frequency. The amplitude of oscillations is limited by non-linear properties of the op-amp. The higher the quality-factor is of the band-pass system the purer the sinusoidal oscillation frequency. The equation model for the op-amp and oscillator follow.

The total amplifier dc open-loop gain is given by [29]

$$a_v = \frac{g_{m3} g_{m9}}{(g_{ds6} + g_{ds7})(g_{ds8} + g_{ds9})}, \quad (2.1)$$

where the channel conductances, g_m and g_{ds}, are defined as

$$g_m = \frac{\partial i_D}{\partial v_{GS}}\Big| I_D \cong \sqrt{(2\mu_o C_{ox} W/L)|I_D|}\ , \text{(2.2)}$$

$$g_{ds} = \frac{\partial i_D}{\partial v_{BS}}| I_D \cong I_D \lambda\ , \text{(2.3)}$$

in which μ_o is the channel surface mobility, C_{ox} is the capacitance per unit area of the gate oxide, W and L are effective channel width and length, respectively, and λ is the channel length modulation parameter of the transistor. The current I_D represents the quiescent current and is provided by M1, M2, and M5 transistors, assumed to operate in the saturation region.

The unity-gain bandwidth of the operational amplifier is calculated as follows

$$\omega_T = -a_v p_1 = g_{m1}/C\ . \quad (2.4)$$

As the operational amplifier is compensated, its transfer function can be given by a single pole transfer function

$$a_v(s) = \frac{a_v}{1 - s/p_1} \quad (2.5)$$

approximated by,

$$a_v(s) \approx \frac{-a_v p_1}{s} \quad (2.6)$$

in which p_1 represents its dominant pole.

The affects of adding the positive and negative feedback loops (to produce oscillation frequency, f_{osc}) are shown by the equations that follow. The positive feedback loop consists of an RC delay and the negative feedback comprises a voltage divider. To facilitate the mathematical analysis the combination of feedback loop is presented by a singe negative feedback block in which the positive feedback appears as a term with negative sign. The feedback block converts the operational amplifier under test to a second order system which has the potential of oscillation. The new transfer function is derived as follows

$$A_v(s) = \frac{a_v(s)}{1 + a_v(s) f(s)} \quad (2.7)$$

where,

$$f(s) = G - \left(\frac{-s/p_2}{1 - s/p_2} \right) (2.8)$$

By substituting $a_v(s)$ and $f(s)$ in $A_v(s)$ we obtain

$$A_v(s) = \frac{a_v p_1 (p_2 - s)}{s^2 + ((1 - G) a_v p_1 - (p_1 + p_2))s + (G a_v p_1 p_2 + p_1 p_2)}. \quad (2.9)$$

The system poles are obtained by equating the denominator of the new transfer function to zero. In order to construct an oscillator from this new transfer function,

its poles must be placed on the imaginary axis in the s- domain by forcing the coefficient of the term s to zero which is realized by proper selection of the value of G as follows

$$G = 1 - \frac{p_1 + p_2}{a_v p_1} \text{ (2.10).}$$

The conversion of the circuit under test's analog signal to an oscillating frequency signal is modeled by the following equations. The natural oscillation frequency for the new system is given by

$$\omega_{osc}^2 = G a_v p_1 p_2 + p_1 p_2 = a_v p_1 p_2 - p_2^2. \text{ (2.11)}$$

In which the oscillation frequency, f_{osc}, is $\omega_{osc} / 2\pi$. This oscillation frequency strongly depends on important characteristics of the operational amplifier (or circuit) under test which, are determined by all components of the device. Existing faults in the device under test will show a deviation in device characteristics from their nominal value. This can be monitored as above by observing the oscillation frequency. With the development of the oscillating signal comes the need for conversion with a frequency to number converter (FNC) as shown by figure 2.3.

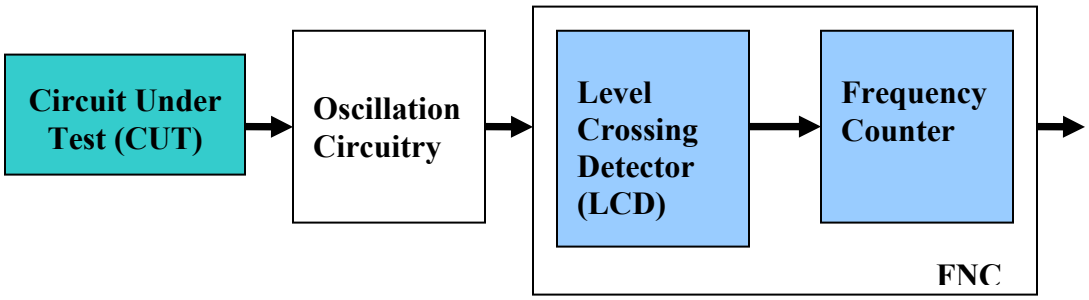


Figure 2.3 Block Based Design of Signal Conversion Process

In order to evaluate the oscillation frequency coming from a building block in the test mode, the frequency is first converted to a corresponding number. The figure above shows the block diagram of the frequency to number converter (FNC). The FNC is comprised of a level crossing detector and a frequency counter. It uses a simple and fully digital circuit which converts each frequency to a related number. The oscillation frequency f_{osc} of the selected building block is first passed through a level-crossing detector (LCD) to obtain a rectangular waveform compatible with logic levels and is then applied to a counter. The counter is enabled by the high level of reference frequency (f_{REF}), therefore during the high state of the reference frequency the counter counts, and during its low state the center is disabled and stops counting. The output value of the counter contains a number which is related to its input frequency, coming from the building block under test, and can be evaluated by the control logic (CL) during the low-state of f_{REF} . The CL resets the counter after evaluating its output number. Therefore, an accurate frequency-to-number conversion is obtained. The accuracy of the system is determined by the reference

frequency and the bit number of the counter M. The digital output value is given by $B = \frac{f_{osc}}{2f_{REF}}$.

This technique provides reasonable accuracy and satisfies the requirements of the application. A schematic representation of the LCD implemented in CMOS is shown in the figure 2.4 below. The LCD is designed using a CMOS current source inverter which acts as a comparator. The current source is a common gate configuration using a p-channel transistor with the gate tied to a dc bias voltage. The bias voltage has been adjusted to obtain a trip voltage V_{TRP} = 1V. The trip voltage is given by the input voltage required to make the current of the transistor M1 equal to the bias current I_B. The gain of the comparator is given as

$$\frac{V_{OUT}}{V_{IN}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2}} = \left(\frac{2K_N' W_1}{L_1 I_B}\right)^{1/2} \left(\frac{-1}{\lambda_1 + \lambda_2}\right), \quad (2.12)$$

where W_1 and L_1 are the effective channel width and length, $K_N' = \mu C_{ox}/2$ is the transconductance parameter and λ is the channel length modulation parameter of the transistor M1.

Whereas a great deal of progress continues to be made in the area of built-in self-test for mixed signal technologies, the problem is far from being solved. This is due to the fact that issues such as area and performance overhead, fault model/coverage, the DFT/BIST automation process and interface to digital tools need to be resolved first. Today very complex mixed-signal multi-chip modules (MCMs) are being designed and in the future, such MCMs will contain buried passives, optoelectronic interconnections, RF components and very closely coupled digital and

analog parts. Therefore, the problem of design for testability (DFT) and built-in self-test will continue to be of great concern to researchers in the semiconductor industry. The research discussed in chapters 3 and 4, address many of the concerns surrounding the development of a robust method of performing on-chip test of multiple types of mixed signal IP.

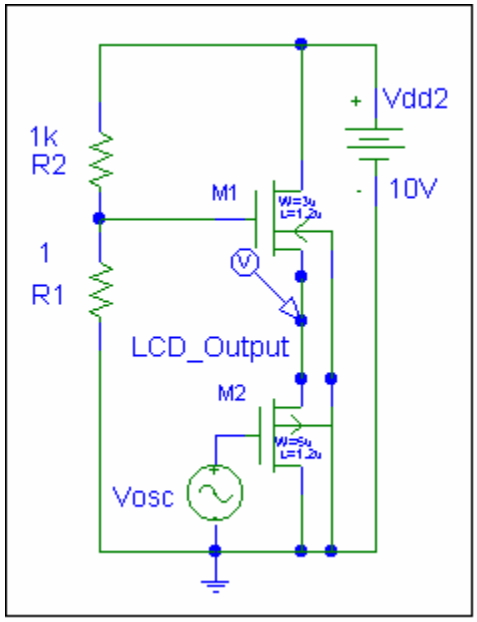


Figure 2.4 Level Crossing Detector

Section 2.5 SystemC and System-on-a-Chip Modeling

Essential to today's semiconductor industry is rapid delivery SoCs. As such, early and accurate modeling of an entire system is essential for lowering the time-to-market of complex embedded devices. Modeling SoCs requires the development of system-level design specifications that define both the hardware and embedded software contained within SoCs [30]. Full system modeling of sensors and related

SoC devices typically involves the analysis of circuit equations that describe the functionality of the system.

Much of today's analog modeling is limited to computer-aided electrical circuit analysis software such as SPICE and VHDL-AMS (Very High Speed Hardware Description Language – Analog Mixed Signal). VHDL-AMS is a standard, which serves to unify hardware description languages while making the libraries of elements that could be accessible by other users or designers. While SPICE is a design tool that falls into the category of general purpose analog circuit simulators.

SPICE is used for initial design development, debugging and performing system diagnostics. With SPICE simulation, circuit blocks may be represented as behavioral elements and simulated in a functional form. Behavioral elements allow designers to test circuit theory without the time involved in developing transistor and component-level descriptions of each circuit function. System on a Chip models differ from previous work [31, 32] in that they are developed to be system modules that can be applied to System-C library and Malab/Simulink environments.

SystemC and other hardware description languages (HDLs) make it easy to combine multiple IP blocks into a single simulation. As such, SoC models of mixed signal technologies are developed from high-level descriptions of circuit operations. The approach to module development (system level design) of biosensors and mixed signal technologies involves creating the full model of the device and capturing the inputs and outputs between each stage of the system. The output of the systems modules are then compared against simulated outputs of electrical equivalent circuits.

The system module development scheme used for systems-on-a-chip augment traditional methods of developing models of biosensor devices and facilitates the incorporation of these sensors in SoC designs.

The semiconductor industry will soon see software and hardware design streamlined into a single flow process. The increasing complexity of SoCs has introduced the need for abstract executable specifications that cover both hardware and embedded software. Hardware description languages (HDLs) like SystemC ameliorate the development of such specifications (models).

SystemC Background

SystemC is like a standard design and verification language that spans from concept to implementation in hardware and software. Prior to 1999 there were many proprietary C or C++ based SoC design environments that did not have an open standard. As such their usefulness was limited since model availability from IP vendors did not exist. SystemC was developed by the Open SystemC Initiative (OSCI), a consortium of major EDA and IP companies that contributes to and governs SystemC development and distribution. It has now become the de facto standard for system level design. As such, IP vendors are beginning to provide SystemC compatible models of their IP.

SystemC is based on C++. One of the objectives of the language is to improve overall productivity for designers of electronic systems. In many cases, today's systems contain application-specific hardware and software. Additionally, the hardware and software are usually co-developed on a tight schedule, the systems

have tight real-time performance constraints, and thorough functional verification is required to avoid expensive and sometimes catastrophic failures.

SystemC allows engineers to design both the hardware and software components together as these components would exist on the final system, but at a high level of abstraction. This higher level of abstraction gives the design team a fundamental understanding early in the design process of the intricacies and interactions of the entire system and enables better system trade offs, better and earlier verification, and overall productivity gains through reuse of early system models as executable specifications.

As with most design languages, SystemC has evolved. SystemC is the result of the evolution of many concepts in the research and commercial EDA communities. Many research groups and EDA companies have contributed to the language. The language began as a very restrictive cycle-based simulator, essentially an RTL language. It is now evolving into a true system design language that includes both software and hardware concepts. Although SystemC does not specifically support analog hardware or mechanical components, there is no reason why these aspects of a system cannot be modeled with SystemC constructs or with co-simulation techniques.

SystemC is not a traditional programming language, it is a class library within a well established language, C++. SystemC is not a panacea that will solve every design productivity issue. However, when SystemC is coupled with the SystemC Verification Library, it does provide in one language many of the characteristics relevant to system design and modeling tasks that are missing or scattered among the

other languages. Additionally, SystemC provides a common language for software and hardware, C++.

The SystemC Verification (SCV) library is a methodology-specific library. It is the most significant of the potential libraries used by SystemC. This library adds support for modern high-level verification language concepts such as constrained randomization, introspection, and transaction recording. The first release of the SCV library occurred in December of 2003 after over a year of Beta testing.

Design Methods

Design methods surrounding SystemC are currently maturing and vary widely. In the next few years, these methods will settle into a cohesive design methodology (with a few variants among certain industry segments). The resulting methodology will feel similar to the methodologies in use today, but at higher levels of abstraction. To some, the concept of using one unified language for hardware and software development appears revolutionary, but this concept is clearly an evolutionary path for those who frequently work in both domains.

Although tools and language constructs exist in SystemC to support register-transfer-level (RTL) modeling and synthesis, a major reason for using the language is to work at higher abstraction levels than RTL. SystemC's ability to model RTL designs enables support of design blocks generated by higher level (behavioral or graphical entry) synthesis tools or to support legacy design blocks.

Benefits of SystemC

The primary motivation for using SystemC is to attain the productivity increases required to design modern electronic systems with their ever increasing complexity. Without productivity advances, many new system concepts will be impractical. In the next sections, we will examine system complexity, methods for attacking this complexity, and SystemC-enabled solutions.

The primary driver leading to the need for a new system design language is the same that previously lead to the need for the current design languages: increasing design complexity. Modern electronic systems consist of many sub-systems and components that include hardware, software, and algorithms. Each of these disciplines has become more complex in modern systems. Additionally, the interaction between them has become increasingly complex.

Interactions imply that trade offs between the domains are becoming more important for meeting customer requirements. System development teams find themselves asking questions like, "Should this function be implemented in hardware, software, or with a better algorithm?" Systems are so complex, just deriving specifications from customer requirements has become a daunting task.

SystemC and complexity

Today's design community uses several approaches for attacking the complexity issues that come with complex system design:

- Abstraction
- Design Reuse
- Team Discipline

- Project Reuse
- Automation

SystemC supports several techniques for addressing these complexity issues because it leverages C++. One of SystemC's greatest strengths is its ability to provide higher levels of abstraction for all components of a design. In the following sub-section an example of a SoC model is discussed.

SystemC SoC Modeling Model Example

SoC modeling begins with an evaluation of the timing issues associated with circuits being evaluated. To translate timing between operations into an SoC model,

```
sc_set_time_resolution(10, sc_ps);

sc_time t2(3.1416, sc_ns);
```

Figure 2.5 Example of modeling Time for SoC applications. Shown is the method of changing the default time resolution and of setting a new time variable.

integer-valued time models are used. These models are described using a "sc_time" type. For example the figure 2.5 above shows "sc_time t2(3.1416, sc_ns)". This model of time creates a time object t2, which represents 3142 picoseconds. The default time resolution for SystemC models of SoC devices is 1 picosecond. Changing time resolution to 10 picoseconds or some other factor results from using

the sc_set_time_resolution ( ) command. Such changes are useful for modeling a waiting period between design processes.

In addition to modeling time it is necessary to understand the conditions under which various actions are taken during device operation. Such conditions are called events. Events are equivalent to conditional statements that when true institute processes or procedures. Events determine whether and when a process's execution should be triggered or continued. Event finders are objects associated with specific lines of communication (ports and methods). They operate as conduits in that they return an event object when invoked through an interface. An example of the model associated with event and event finer conditions is shown in the figure 2.6 below.

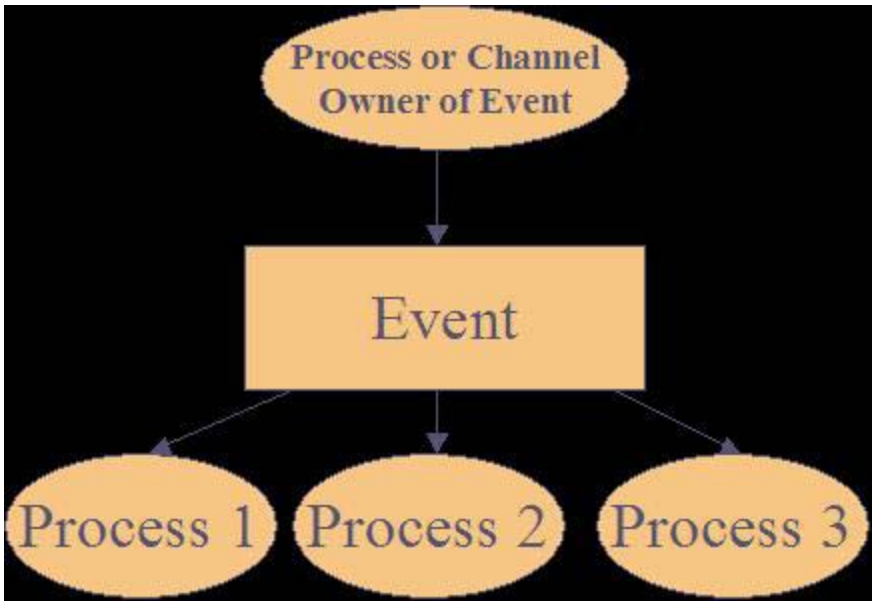


Figure 2.6 Model showing events and event finders.

A third component of SoC modeling involves the development of modules, or system sub blocks. Modules are the basic building blocks for portioning a design. They allow designers to break complex systems into smaller pieces and hide internal

data representations and algorithms from other modules. Modules typically contain ports, processes, internal data, channels, and hierarchically other modules. An example of a module is shown in figure 2.7 below.

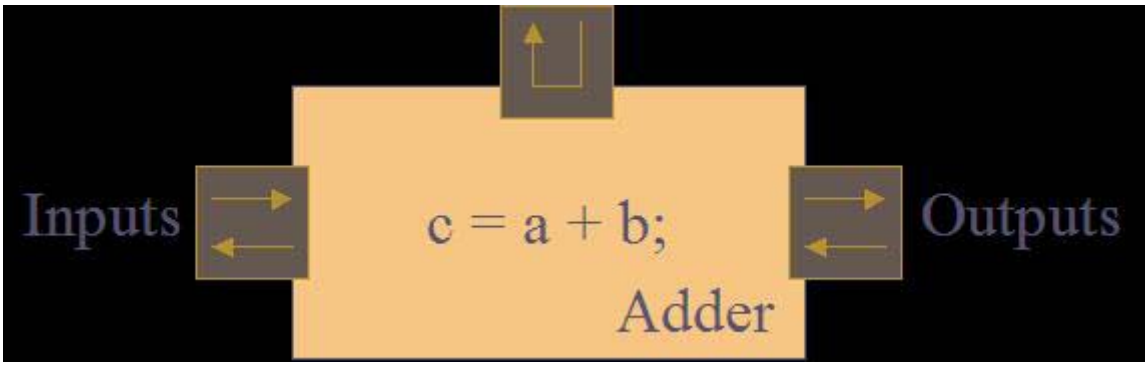


Figure 2.7 SoC Module

In figure 2.7, we see a simple example of a SoC implementation of a bit adder. The inputs (shown on the left of the above figure) to this sample module are the values "a" and "b". The output is "c". The process involves summing "a" and "b" and assigning the resulting value to "c". The input and output symbols on the left and right of the module are ports. These ports allow modules to connect to and communicate with their surroundings. SoC models of ports are boxes with two arrows pointing in opposite directions. Ports take in external inputs and distribute internal outputs. At the top of this module is a SoC block containing a u-shaped arrow; this represents an interface. Interfaces consist of a set of operations in which an operation's name, parameters, and return values are specified. Good examples of interface usage includes read and write statements in which data is read in from a module or written to another module.

Figure 2.8 SoC Channel

Channels are also included in SoC models. Channels carry out operations initiated through interfaces. These are traditionally represented as a thick wire-like line as shown in figure 2.8 above.

The process component of a SoC is the basic unit of functionality that provides a mechanism for simulating concurrent behavior. A sample process for the adder example follows in figure 2.9:

```
SC_MODULE(Adder){
  sc_in<int>   a;
  sc_in<int>   b;
  sc_out<int> c;
void compute() {
   c = a + b;
}
  SC_CTOR(Adder) {
  SC_METHOD(compute);
  Sensitive << a << b;
  }
};
```

Figure 2.9 SystemC Based Adder Module Code

A complete process is created with a member function and an additional statement calling the member function. In the above example, the member function compute() taken in conjunction with the statement sc_method(compute) creates a complete process. Here we see that the member function compute() assigns the sum of the inputs “a” and “b” to the output “c”. While this appears to complete the action associated with the module, it does not create a process. Inside the module’s constructor, delineated by sc_ctor(adder), resides the statement sc_method(compute). This sc_method statement maps the member function, compute, to a method process by registering it with the scheduler. As with the C++ programming language, “void compute( )” indicates that compute( ) is a function or subroutine.

When a method process is affected by an event on another port, it is said to be sensitive, to the event. In the preceding figure 2.9, the statement following sc_method(compute) specifies that this process is sensitive to changes in the values of hardware signals that will be connected to the input ports. Thus for every change in “a” or “b”, the method process compute() is evoked and the value of “c” is updated.

Complete SoC Model of the Adder

In this subsection a complete model of the SoC 4-bit adder is presented, and simulated with SystemC. Here the development of a SoC model of a 4-bit binary adder from a bit binary adder is shown. We begin by discussing the SoC model components of a bit adder.

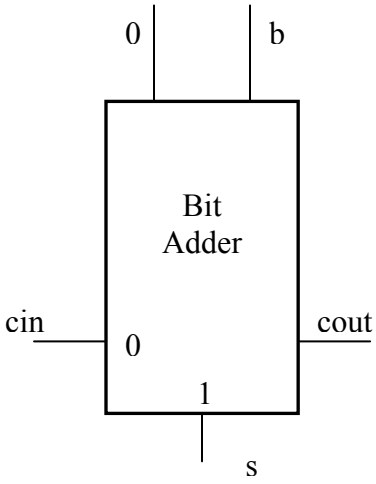


Figure 2.10 Bit-Adder Symbol

The bit binary adder is comprised from two half-adder circuits plus two and-gates and an or-gate to design a 1 bit binary adder circuit. The circuit has 3 inputs and 2 outputs. The inputs are a carry input, "cin", and two binary digits, "a" and "b". The outputs are the carry output, "cout", and the sum, "s". The bit adder is typically modeled as follows:

```
(define bit-adder
(lambda (a b cin)
(let* ((t (bit-half-adder a b))
(g (bit-and a b))
(p (bit-and t cin)))
(list (bit-or g p)
(bit-half-adder t cin)))))
```

Table 2-2 SystemC Based Bit Adder Module

The bit-adder has the characteristics outlined in the following:

(bit-adder 0 0 0) ==> (0 0)
(bit-adder 0 1 0) ==> (0 1)
(bit-adder 1 0 0) ==> (0 1)
(bit-adder 1 1 0) ==> (1 0)
(bit-adder 0 0 1) ==> (0 1)
(bit-adder 0 1 1) ==> (1 0)
(bit-adder 1 0 1) ==> (1 0)
(bit-adder 1 1 1) ==> (1 1)

Table 2-3 Bit Adder Testbench

The bit-adder symbol, shown below, indicates the adder circuit inputs and outputs The 4-bit adder is constructed from 4, bit-adders as depicted by figure 2.11 below.

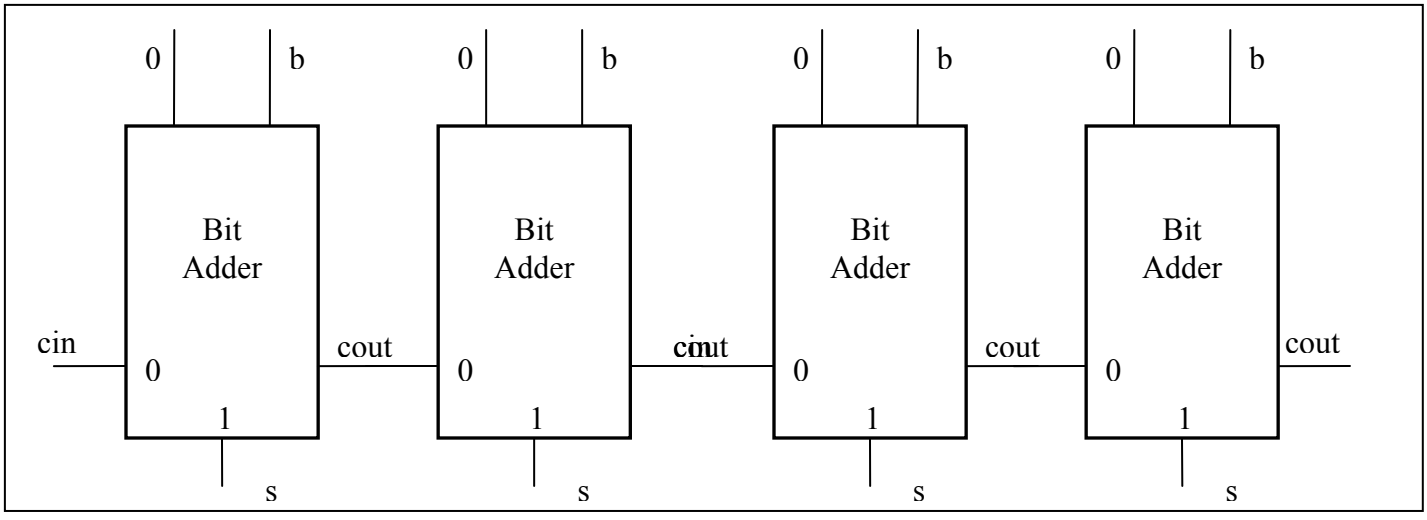


Figure 2.11 4-Bit Adder Symbol

The 4-bit adder model is defined as follows:

```
(define 4-bit-adder
(lambda (a3  a2  a1  a0  b3  b2  b1  b0)
(let* ((t0  (bit-adder  a0  b0  0))
(t1 (bit-adder a1  b1  (wire-output  0  t0)))
(t2 (bit-adder  a1  b1  (wire-output  0  t1)))
(t2  (bit-adder  a3  b3  (wire-output  0  t2))))
(list  (wire-output  0  t3)
(wire-output  1  t3)
(wire-output  1  t2)
(wire-output  1  t1)
(wire-output  1  t0)))))
```

Table 2-4 4-Bit Adder Model

The following table provides typical characteristic responses for the 4-bit adder.

a_input	b_input	cin	sum	cout
0000	0000	0	0000	0
0000	0000	1	0001	0
0010	0011	0	0101	0
0011	0100	0	0111	0
0011	0000	1	0100	0
0011	1000	1	1100	0

Table 2-5 Characteristic responses for a 4-bit adder. These responses are used as the testbench for the SoC model of the adder.

Here, we introduce the SoC model implementation of the 4-bit adder as well as output results after the model has been evaluated by SystemC. The main program for the SystemC model implementation of the 4-bit adder follows.

```
#include "add1.cpp"
#include "add4_tst.cpp"
#include "vector.cpp"

int sc_main(int argc, char* argv[])
{
        sc_signal<sc_lv<4> > A_s,B_s,SUM_s;
        sc_signal<sc_logic> A3,A2,A1,A0,B3,B2,B1,B0,S3,S2,S1,S0;
        sc_signal<sc_logic> CIN_s,cout1,cout2,cout3,COUT_s;
        vectorIn vector2bits1("Vector_2_BITS1");
        vector2bits1 << A_s << A3 << A2 << A1 << A0;
        vectorIn vector2bits2("Vector_2_BITS2");
        vector2bits2 << B_s << B3 << B2 << B1 << B0;
        BIT_ADDER adder1("BitAdder1");
        adder1 << A0 << B0 << CIN_s << S0 << cout1;
        BIT_ADDER adder2("BitAdder2");
        adder2 << A1 << B1 << cout1 << S1 << cout2;

        BIT_ADDER adder3("BitAdder3");
        adder3 << A2 << B2 << cout2 << S2 << cout3;
        BIT_ADDER adder4("BitAdder4");
        adder4 << A3 << B3 << cout3 << S3  << COUT_s;
        vectorOut bits2vector("bits2vector");
        bits2vector << S3 << S2 << S1 << S0 << SUM_s;
        testbench test1("TestBench1");
        test1  << A_s << B_s << CIN_s << SUM_s << COUT_s;
        sc_start(200,SC_NS);
        return(0);
}
```

The adder was evaluated using the characteristic responses shown in table 2.2 above. The following “testbench” program was created to model the characteristic responses.

```
#include "systemc.h"

SC_MODULE (testbench)
{
        sc_out<sc_lv<4> > A_p,B_p;
        sc_out<sc_logic>  CIN_p;
        sc_in<sc_lv<4> >  SUM_p;
        sc_in<sc_logic>   COUT_p;
        SC_CTOR (testbench)
        {
                SC_THREAD (process);
        }
        void process()
        {
                        //Case 1
                        A_p = "0000";
                        B_p = "0000";
                        CIN_p = SC_LOGIC_0;
                        wait (5, SC_NS);
                        assert ( SUM_p.read() == "0000" );
                        assert ( COUT_p.read() == SC_LOGIC_0 );
                        wait (10, SC_NS);
                        print();

                        //Case 2
                        A_p = "0000";
                        B_p = "0000";
                        CIN_p = SC_LOGIC_1;
                        wait (5, SC_NS);
                        assert ( SUM_p.read() == "0001"  );
                        assert ( COUT_p.read() == SC_LOGIC_0 );
                        wait (10, SC_NS);
                        print();

                        //Case 3
                        A_p = "0010";
                        B_p = "0011";
                        CIN_p = SC_LOGIC_0;
                        wait (5, SC_NS);                        //Allow signals to set
```

```
                assert ( SUM_p.read() == "0101" );          //The assert signal
                assert ( COUT_p.read() == SC_LOGIC_0 );    //checks output
                wait (10, SC_NS);
                print();


                //Case 4
                A_p = "0011";
                B_p = "0100";
                CIN_p = SC_LOGIC_0;
                wait (5, SC_NS);                           //Allow signals to set
                assert ( SUM_p.read() == "0111" );          //The assert signal
                assert ( COUT_p.read() == SC_LOGIC_0 );    //checks output
                wait (10, SC_NS);
                print();


                //Case 5
                A_p = "0011";
                B_p = "0000";
                CIN_p = SC_LOGIC_1;
                wait (5, SC_NS);                           //Allow signals to set
                assert ( SUM_p.read() == "0100" );   //The assert signal
                assert ( COUT_p.read() == SC_LOGIC_0 );    //checks output
                wait (10, SC_NS);
                print();


                //Case 6
                A_p = "0011";
                B_p = "1000";
                CIN_p = SC_LOGIC_1;
                wait (5, SC_NS);                           //Allow signals to set
                assert ( SUM_p.read() == "1100" );   //The assert signal
                assert ( COUT_p.read() == SC_LOGIC_0 );    //checks output
                wait (10, SC_NS);
                print();


                sc_stop();
//End Simulation
}
void print()
{
cout << "At time " << sc_time_stamp() << "::";
cout << "(a,b,carry_in): ";
```

```
        cout << A_p.read() << B_p.read() << CIN_p.read();
        cout << "  (sum,carry_out): " << SUM_p.read() << COUT_p.read() << endl;
        }
};
```

The SystemC output for the 4-bit adder SoC model follows in table 2.6. As shown the output for the SoC model implementation of the adder corresponds with the expected 4-bit adder output shown in table 2.5.

```
SystemC 2.0.1 --- Mar 30 2005 16:43:53
Copyright (c) 1996-2002 by all Contributors
ALL RIGHTS RESERVED
At time 15 ns::(a,b,carry_in): 000000000  (sum,carry_out): 00000
At time 30 ns::(a,b,carry_in): 000000001  (sum,carry_out): 00010
At time 45 ns::(a,b,carry_in): 001000110  (sum,carry_out): 01010
At time 60 ns::(a,b,carry_in): 001101000  (sum,carry_out): 01110
At time 75 ns::(a,b,carry_in): 001100001  (sum,carry_out): 01000
At time 90 ns::(a,b,carry_in): 001110001  (sum,carry_out): 11000
```

Table 2-6 SystemC output for 4-bit adder.

Following this discussion of SoC model development, is an overview of biosensors.

Section 2.6 Chemical Field Effect Transistor Biosensors

Interest in biosensors has increased rapidly in the past few years due to the many potential advantages offered by these devices. Among these are: small size, speed of processing, and specificity.[33] The term “biosensor” in the broad sense describes any device or apparatus which detects biological signals for the purpose of diagnosis, monitoring, imaging or sensing the state of the biological organism. This

includes the more narrow definition – that of a biosensor as a continuous, reversible monitor of some physiological parameter.

Recently, the biosensor field has entered a phase which stresses practicality, miniaturization and reliability [34]. Devices which have shown promise in the laboratory are being scrutinized from the viewpoint of price and performance and are being closely compared to existing techniques. To lower costs through quantity production savings, integrated circuit or integrated optics techniques are often adopted. The chemically sensitive field-effect transistor (CHEMFET), for example, is designed to perfect a practical, miniaturized electrochemical sensor capable of measurements in biological fluids.

Background on the Chemical Field Effect Transistor

One of the first ChemFETs developed was the palladium gate design investigated by Lundstrom [35]. This device uses nickel (Pd) metal as the gate conductor. Hydrogen (H) is catalytically dissociated at the metal surface then diffuses to the metal/insulator interface where the H atom polarizes to induce modulations in the gate field effect. Many modern ChemFET structures utilize conducting polymers such as polypyrrole or polyaniline as the gate conductors [36] and are used as vapor sensors.

The basic CHEMFET is a miniaturization of the Kelvin Probe (vibrating capacitor). The heart of a basic CHEMFET is the gate capacitor in which silicon forms one plate while the chemically selective layer forms the other. When the two chemically different plates are electronically connected, the equalization of Fermi levels leads to formation of electric field in the dielectric. This field is proportional to

the difference of work function of the two plate materials [37]. A remarkable property of the silicon-based devices is that silicon is hermetically sealed by silicon dioxide (and silicon nitride). Therefore, the work function of silicon does not change over the entire operating range of temperatures and thus serves as a stable reference electrode. This aspect of conventional silicon electronics is normally taken for granted and generally overlooked, but it is a tremendous advantage to perform Kelvin probe miniaturization for application to integrated CHEMFET structures.

Direct translation of the Kelvin probe leads to the suspended gate field-effect transistor (SGFET) [38]. The SGFET shown in the figure 2.12 below is a form of CHEMFET where the conductive gate is suspended above the insulator layer so that solution or vapor can directly interact with both gate and insulator layer to produce a change in work function of the device.

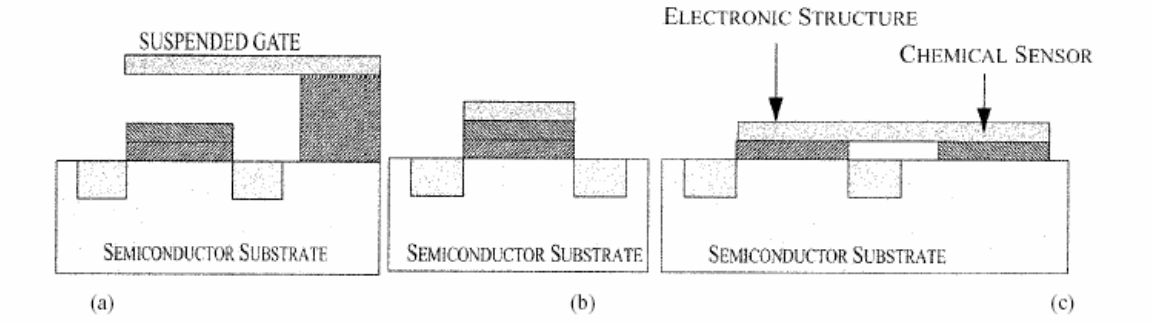


Figure 2.12 Common implementations of the basic CHEMFET [97].

The (a) suspended gate field effect transistor (SGFET) is the most straightforward miniaturization of the Kelvin Probe and consists of a regular MOSFET structure, with the gate suspended over the insulator layer so that both chemically sensitive gate and insulator are exposed to the sensing environment. Other common structures include the (b) ordinary CHEMFET which is identical to

the MOSFET structure except the gate is chemically sensitive and the (c) extended gate FET (EGFET) where the electronic gate and most of the FET are housed in a location that is relatively remote from the chemically sensitive area where signal transduction occurs.

The main motivation for fabricating this type of transistor is that it is possible to modify electrochemically the suspended gate and thus change its selectivity for gasses of interest. The second advantage of this sensor is that the gate can be operated at different temperatures, thus achieving a certain additional selectivity [39]. The SGFET and other common basic CHEMFET structures which are modifications of this direct miniaturization of the Kelvin probe are also depicted in figure 2.12 above.

The terms CHEMFET and potentiometric sensor have come to be used interchangeably in the applications of miniaturized solid-state chemical sensors. As the name implies, potentiometric sensors derive their useful (analytical) information from an explicit relationship between the potential of the indicator electrode and concentration in the analyte (vapor or liquid). Because the potential of a single phase cannot be measured, a second or reference electrode is introduced to enable a voltage (or potential difference) to be measured between the indicator or measurement electrode and the reference electrode. The need for a reference electrode is similar to the need for a ground (floating, signal or earth) in any electrical circuit and as in electrical circuits, may be constructed to reference the signal of interest at the measurement electrode in a variety of ways. The use of a reference electrode to enable a voltage measurement that is representative of changes in charge distribution

on the measurement electrode comes about from established sensing principles. For example, reference and measurement electrodes are used in a variety of potentiometric ion-selective electrodes for both aqueous (liquid-phase) and vapor (gas-phase) measurements and macroscale ion-selective electrodes now represent the largest group among all chemical sensors in commercial use today.

The chemiresistor, however, is a simple type of chemical sensor that relies on the change in conductivity of an organic or inorganic material in response to an analyte. Like potentiometric sensors, chemiresistors can be made to be highly sensitive to small concentrations of organic solvent vapors in ambient air.

The benefit of potentiometric sensors is that they can be miniaturized into a FET-based architecture, and are particularly suitable for miniaturization because the integrity of the transduced signal that carries chemical information does not depend on the sensing area. Noise and signal to noise ratio do not degrade significantly with miniaturization. The trade-off to a chemiresistor, however, is that the miniaturized potentiometric sensor is often larger than its chemiresistor counterpart and requires more complex measurement overhead. This increase in size can be partially compensated by the noise advantages of this type of device. Another disadvantage of the miniaturized potentiometric sensor is that the power of the measured signal containing relevant analyte information is very small and its measurement requires significant amplification at high input impedance before the signal can be further processed for concentration and discrimination information. Embedding the analyte-sensitive electrode into the field-effect transistor (FET) structure is an attractive solution to the amplification problem. FETs of course, can be fabricated in standard

CMOS and other microfabrication processes in which conversion of the electronic FET to an effective chemical sensor requires in theory, only replacement of the gate with a suitable chemically sensitive material. The impact of the environment, materials compatibility, and other fabrication issues, however, make the integration of the CHEMFET with standard FET architectures significantly more complicated than the theory and has generated a broad range of CHEMFET architectures and design methodologies directed at solving practical, portable chemical sensing problems. Because of the convenience and compatibility of the FET structure with standard micro-fabrication processes, miniaturized potentiometric sensors (microsensors) have become synonymous with chemically sensitive field-effect transistors and continue to be pursued as a viable solution to chemical sensing problems requiring portability and real-time operation.

A different approach has been introduced by using conducting polymers dissolved in and cast from organic solvents for the chemically sensitive material in the basic CHEMFET. A typical example of such a polymer is polyaniline (PANI) which can be prepared chemically or electrochemically and then dissolved and cast from such compounds as formic acid. This technique makes it possible to deposit the chemically sensitive and electroactive gate materials and to pattern them photo- litho-graphically directly on top of the gate dielectric [40]. Subsequent chemical or electrochemical modification of this material can then be performed [41] which opens a possibility for construction of a wide range of chemical sensors for detection of electrically neutral species in non-conducting samples, such as gases or dielectric liquids.

Although less prevalent than in chemiresistor development, research efforts in the CHEMFET area have also been committed to the development of suitable packaging, chemical sensing electronics, and integration levels for the construction of portable systems. Efforts to integrate all signal processing into a microcontroller-based system have been reported [42] as have efforts to develop circuit models of CHEMFET structures in Spice [43] for future chemical sensing microsystem and electronic developments. These efforts are gaining momentum as the demand to turn the vast amount of research attention onto the CHEMFET structure and materials into viable systems continues to increase.

CHEMFET sensors have now been studied for nearly three decades. Much of the pioneering work was done by Jiri Janata at the University of Utah [44]. Janata defines a chemical sensor as "a device that provides continuous information about its [chemical] environment. Unlike imaging (visual sensing) technologies where only one type of light (e.g., infrared or visible range) is detected and sound (auditory sensing) technologies where only one type of pressure wave is detected, chemical sensors must transduce a variety of input stimuli using a variety of transduction mechanisms or reactions.

ChemFET Transduction

Transduction is the process of translating a change in a given chemical environment into electrical signals. The broad range of stimuli and transduction mechanisms is a result of both an inherent characteristic of most chemical sensor technologies and an engineered characteristic that is used to produce a signal

representing the stimulus of interest significantly stronger than those of interfering stimuli.

Sensor transduction principles fall into four main categories: thermal, mass electrochemical (applicable to biological, DNA, blood cell, fluid analysis), and optical. Within each category, devices which fit the general definition of chemical sensor range widely in size and operational parameters. The transduction principle for the modern ChemFET is a chemical modulation of the electron work function of the conducting polymer gate material [45]. The device threshold voltage, VT, is dependant on the difference between the work function of the polymer, Φ_{poly} and that of silicon, Φ_{Si}.

$$V_T \propto \Phi_{Si} - \Phi_{Poly}, \quad (2.13)$$

The threshold voltage is determined from the drain current, I_{DS} versus gate voltage, V_G relationship for non-degenerate, n-channel devices in saturation:

$$I_{DS} = Const(V_G - V_T)^2, \quad (2.14)$$

Where *Const* is a constant governed by the fabrication parameters [46]. Figure 2.17 gives an example of a measurement circuit for measuring changes in the threshold voltage of the gate conductor.

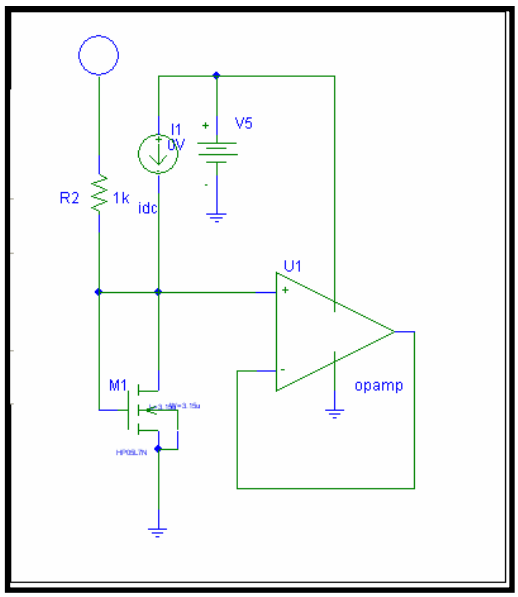


Figure 2.13 Measurement circuit for ChemFET work function.

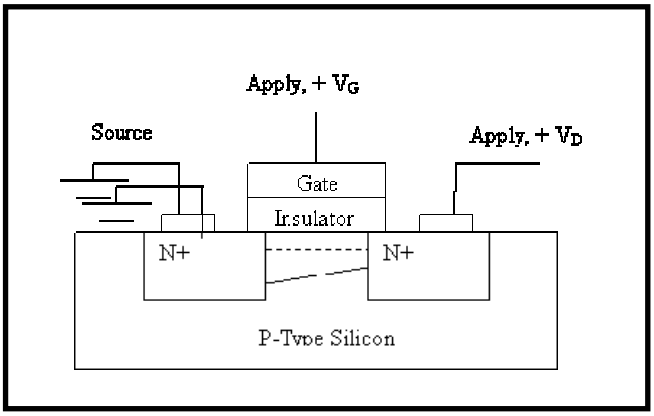


Figure 2.14 Idealized ChemFET cross section schematic.

CHEMFET STRUCTURE

An idealized schematic cross section of a ChemFET is shown in Figure 2.18. Unlike a conventional MOSFET, the threshold voltage of the CHEMFET can be chemically modulated. The nature of this modulation has been reviewed in detail [47, 48] and it defines three major types of devices in the chemical family.

- ISFET (ion selective FET): the ion sensitive field effect transistor (ISFET), which is a direct miniature equivalent of the ion selective electrode, is a CHEMFET structure without a conductive gate; the ion selective layer is placed on top of the insulator layer of the FET structure.
- ENFET (enzyme FET): enzymatically selective field effect transistor, which is equivalent to a potentiometric enzyme electrode, is another CHEMFET structure without a conductive gate; the chemically sensitive enzyme layer forms part or all, of the entire insulator layer of the FET structure.
- Basic or "work function" CHEMFET: this field effect transistor has its macroscopic counterpart in the Kelvin probe [49] and is a FET structure with a conductive gate; the conductive gate is the chemically selective area layer. The insulator can be a traditional material such as SiO_2, a special layer chosen for its chemically selective interaction with the gas in generating a work function change, or a sandwich of custom and traditional insulator layers.

The primary disadvantage of the ENFET and ISFET structure is the inescapable need for a large reference electrode which somewhat diminishes the practical appeal of individual small indicator devices. Potentiometric enzyme electrodes have only limited usefulness due to their vulnerability to experimental

artifacts originating from the composition of the matrix of the sample [50, 51, 52]. The same limitation applies to the ENFETs or miniaturizations of the potentiometric enzyme electrode which until now remain only a laboratory curiosity. The ISFET, on the other hand, despite its need for a reference point or electrode, has met with substantial progress in the past decade, in part due to the fact that its macroscale counterpart, the ion selective electrode, has already matured into a variety of commercial products. The situation is substantially better with the work function CHEMFET than with both the ENFET and ISFET in terms of compatibility with miniaturization for portable instrument development.

The CHEMFET is essentially a large feature size insulated gate field-effect transistor. The gate length is typically roughly 20 microns. The large feature size is dictated by the need to have a minimum amount of chemically active material in order to obtain sufficient signal. The essential difference between a ChemFET and a typical FET for electronic applications is that the gate conductor material is chosen such that its properties can be modulated by an external chemical stimulant. For example, a FET that can be used for detection of hydronium ion (i.e. PH) is one with a base insulator [53]. For this FET, ions will partition into the gate insulator and modulate current flow between source and drain. This configuration, however, requires an external reference electrode.

ChemFETs are built with a chemically sensitive gate material (generally a heavily-doped conducting polymer) applied on the gate oxide. When a chemical is applied to which the gate material is sensitive, the Fermi level at the gate shifts causing a change in the work function of the metal via bulk and surface modulation

thereby causing the threshold voltage of the FET to change in a measurable way [54, 55]. Although research continues to acquire a more precise definition, at this time the input-output relationship of a diode-connected ChemFET in the saturation region of operation with a constant drain-source current applied can be modeled as:

$$V_o = x_o \ln(a[C]) + x_1 + \sqrt{\frac{2I_D}{K'\left(W/L\right)}}, \quad (2.15)$$

In the above equation x_o and x_1 are constants that depend on physical device parameters associated with the materials used to build the ChemFET and the geometry of the device as well. They do not change in a meaningful way in response to an applied analyte and can be determined empirically. "α" is a scaling factor. "[C]"is the concentration of the analyte I_D is the drain current through the ChemFET. It is generally set to some constant value. K' is another physical parameter. "W" and "L" are the width and length of the FET channel. The nature of the input-output equation is therefore logarithmic. However, this formula is only valid for moderate concentration ranges [56].

Design

The FET design used in [57] uses a metallization layout designed to allow simultaneous detection of work function and impedance changes. For testing, potentials are applied at a single gold lead which contacts both the drain and the gate. Thus, the device is hard-wired in the source-follower configuration. The source and substrate are grounded. I_{DS}, is kept constant and gate voltage is monitored. A

symmetrical lead on top of but not connected to the source provides a contact point for monitoring the impedance of the chemically active layer.

Fabrication

Fabrication of ChemFETs requires slightly different processing steps than a standard n-channel FET. One major difference is that noble metals must be used for contact leads to ensure chemical inertness. Another difference is that the gate requires a low stress silicon nitride insulator. This is deposited in a high temperature chemical vapor deposition process and reduces the chance for pin-hole defects. One last difference is that the surfaces of the devices must be isolated from each other with a tall, inert polymeric material. These wells are filled with solution during gate conductor casting and electrochemical modification.

Advantage of ChemFETs for Microsystems

The ChemFET for detection of chemical vapors may be compared with the competing technologies of surface acoustic wave (SAW) devices and chemiresistors, both of which have utilized polymer active materials [58, 59, 60]. SAW devices are mass sensor transducers that monitor the change in frequency and phase angle of an acoustic wave moving across the surface of a piezoelectric substrate. Active materials are coated over the device surface and the acoustic signature changes as the layer adsorbs vapors and increases in mass. Chemiresistors are very simple devices in which active materials are coated onto inter-digitated electrodes. The resistance between the digits is monitored. The resistance of the loaded polymer is modulated by the swelling of the polymer as it absorbs gases.

Different sensor technologies may be compared with a number of parameters including size, sensitivity, noise, stability, and cost. Some factors are greatly influenced by the choice of chemically active material while others tend to be a function of the transducer.

ChemFETs are inherently compatible with silicon electronics. This suggests the possibility for greater system integration by fabricating both interfacing and support circuits with the sensor on the same substrate. Such integration could lead to further gains in size and power needs.

CHEMFET Sensitivity

Sensitivity is a term often used to refer either to the lowest level of chemical concentration that can be detected or to the smallest increment of concentration that can be detected in the sensing environment. In typical laboratory applications for chemical sensing, it is necessary to know exactly how much of each chemical component is present in a complex mixture across a wide dynamic range. In many portable chemical sensing applications, however, such as landmine detection, environmental (ground water and air pollution) monitoring, and toxic chemical agent detection, it is necessary only to know when the concentration of a single or small number of chemicals has exceeded certain alarm levels. This change in focus from complex composition analysis to alarm level detection changes the requirements of the sensing system. In the laboratory applications both the sensitivity associated with dynamic range and resolution as well as sensitivity associated with the lower detection limit are important. In medical applications involving ascertaining

creatinine levels in kidney dialysis patience, for example, alarm level sensitivity would be useful.

ChemFET sensitivity is a logarithmic function of vapor concentration [61]. This means a much broader dynamic range than that of SAW devices or chemiresistors, both of which have linear response curves [62]. Detection limits for some ChemFET systems in parts per billion (ppb) range have been reported; well below the limit chemical sensors [63]

Alternative CHEMFET Sensor Technology

CHEMFET technology relies on the presence of a chemically sensitive membrane, which upon interacting with the species in solution or gas changes the gate potential of the FET. During the last few years, another type of sensor has been constructed and tested. This sensor, which does not require cumbersome membrane deposition steps, is based on modulation of the electron work function and is dedicated for gas applications (it is the microscopic equivalent to the so-called Kelvin probe or vibrating capacitor). The sensor is composed of a field-effect transistor, in which the metal gate forms a suspended bridge that is separated from the solid insulator by a narrow gap. In figure 2.15 below, we show a schematic diagram of the suspended beam cross section area. It can operate in an ambient gas or in a vacuum, and the active area of the probe can be locally heated.

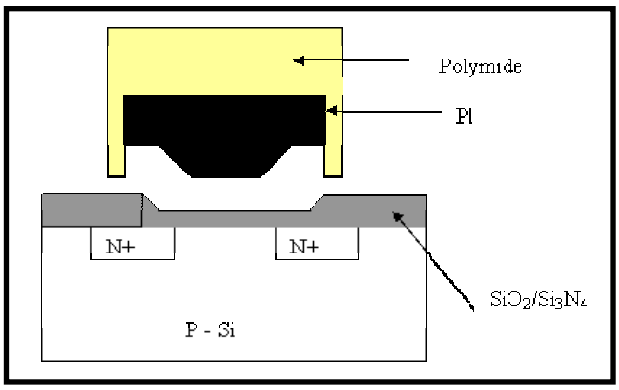


Figure 2.15 Schematic Diagram of the suspended beam cross section area.

There is no practical limit on the lifetime of bare CHEMFET chips. This is important from the point of view of fabrication and storage of the unfinished devices. The in-use lifetime of the average CHEMFET depends on the type of chemically sensitive layer. For example, it can be years for a bare silicon nitride pH ISFETs, or months for membrane ISFETs and days for Enzyme FETs (ENFETs). Lifetime data for various gas FETs are not yet available. As such, an open problem suggested in chapter 5, involves determining the lifetime of gas FETs.

ADVANTAGES OF AN ARRAY

There is no such thing as perfect selectivity for a single sensor/analyte system. Even if perfect selectivity were possible, then a single device could only provide information about a single analyte, and would not guarantee a broad dynamic range. Because real world samples are mixtures, it is necessary to use an array of sensors to increase selectivity and dynamic range, and the number of simultaneous analytes. A simple illustration of array utility is the pH test strip. Single component acid-base indicators typically can only respond to pH changes over 1 or 2 pH units. In contrast,

the test strip, with many indicators on a single sampling tool can resolve pH to within one unit or better. This is possible by analyzing the pattern of colors generated. In fact, much of the current development of sensor array technology comes from improving pattern recognition algorithms [64].

Arrays can improve signal to noise by averaging response from many sensors. The optimum number of sensors has been investigated; the number ranges from 6 to 10.

An array of ChemFETs in addition to additional mixed signal technologies for processing will result in a system-on-a-chip (SoC) design that is tailored to the medical community. These would be useful to the medical community.

On chip medical technology devices for therapeutic or long term monitoring of organism functions, encompasses some of the most challenging and technically demanding of designs. As a result, some have considered medical technology to be the principle cause of the high cost of health care. Yet others believe that this is an unjustified criticism and that medical technology can provide immediate advances in the productivity of health care services, thereby reducing health care costs while increasing the quantity of services [*65*]. The use of microelectronics, analog systems-on-a-chip, and integrated circuit (IC) devices will aide in improving health care costs due to the speed with which they can be mass produced and the low costs of manufacturing such devices for testing biological fluids.

Section 2.7 Summary

In this chapter a discussion of analog systems on a chip with built in self test and application to biosensors is provided. Included in this discussion is an overview of SoC technology, a detailed analysis of the oscillation test strategy, and an overview of biosensor devices with special attention given to the CHEMFET. While much work has been conducted in the area of digital system-on-chip design, very little emphasis has been placed on analog SoC designs, leaving analog SoC development far behind its digital counterpart. As such, it would be beneficial to devote research to the development of analog SoC devices and device models that are suitable for the design reuse needs of the SoC industry.

In addition, the area of development of on-chip self diagnostic for both analog and digital system sub-blocks requires further study. The most promising of the techniques reviewed involves the use of the oscillation test strategy (OTS). This method is flawed, however, because it relies on developing oscillations from a set of feedback loops placed around the circuit under test. This method inherently proves problematic as oscillations are produced from a device that may not be functioning properly within the circuit. Moreover, the oscillations are produced for CMOS amplifier circuits containing internal capacitors and resistors, which take up a large amount of area on the SoC die. Other problems with the OTS method involve resistors and capacitors that are used in feedback loops and level crossing detectors, which take up a large amount of space on the die area. A final area of interest is in the development of an improved set of fluid analyzer biosensor arrays suitable for the SoC environment.

Solutions to these issues will be discussed at length in chapter 3 with verifiable results presented in chapter 4.

Chapter 3 Novel Development of an Analog System-on-a-Chip with Built-In Self-Test

Section 3.1 Overview

Analog intellectual property (IP) re-use for the system-on-chip (SoC) environment is a challenging endeavor as most analog circuitry is difficult to standardize, especially across technologies. This is due in part to varied definitions of end-user design requirements and the inherent complexity of analog circuitry. Much thought and preparation, therefore, is needed for the successful integration of analog IP into the SoC domain. Included in this is a need for the development of analog SoC models. Such models can be developed in SystemC through the use of floating-point representations and the declaration of appropriate device behavior. In many cases, however, analog IP SoC fails to meet the desired specifications for end-user use and as such requires significant modifications prior to use in given SoC designs. As such, there is a significant lag in analog system-on-chip IP development in comparison to digital SoC intellectual property.

In addition to the need for advancement in the field of analog SoC IP, there is a need to develop on chip SoC test methods capable of discerning faults in analog devices, while limiting the cost of BIST area overhead. Therefore, improved methods of performing on-chip testing of SoC macros, in which said methods limit the die area covered by traditional BIST techniques, is also necessary. Moreover, there is a need for

the development of on-chip devices capable of evaluating fluids for potential medical applications.

This chapter presents solutions to the above open problems through the development of a fluid analyzer system-on-chip capable of performing on-chip self-diagnostics and distinguishing various fluid properties. Here, the description and the development of analog IP SoC macros and models specific to these devices are provided. Included in this are the novel biosensors, smart signal processing devices, and built-in self-test circuits used in the SoC design. The resulting SoC design is referred to as a Testbench-on-a-chip (TBOC) [66]. Figure 3.1, originally shown in chapter 1 as figure 1.1, presents a high level view of the fluid analyzer SoC developed and evaluated in this work.

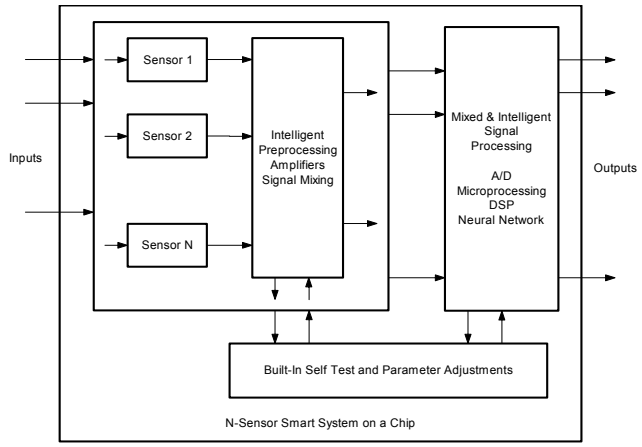


Figure 3.1 High Level View of fluid analyzer system interactions.

Specific details about the fluid analyzer SoC are provided in section 3.2. The proposed analog devices appear in sections 3.3, "Analysis and Design of Biosensors for Fluid Testing", and 3.4, "Oscillation Based Built-In Self-Test (OBIST)". The OBIST

method developed in this dissertation is an improvement upon the Oscillation Test Strategy (OTS) discussed in chapter 2. These improvements are discussed in detail in section 3.4. Analog SoC models of the devices under study are provided in section 3.5. The chapter concludes (section 3.6) with a summary of the dissertation' contributions to novel ideas in analog SoC design, modeling, and evaluation.

Section 3.2 Fluid Analyzer SoC

The fluid analyzer SoC is comprised of three macros: a biosensor/preprocessing macro, a built-in self-test macro with parameter adjustment, and an intelligent signal processing macro. The elements of the intelligent signal processing macro (top right sub-block in figure 3.1) were not fabricated and are left as open problems. This dissertation focuses on the development of the first two macros: the biosensor/preprocessing macro and the built-in self-test/parameter adjustment macro, as the elements of these macros were fabricated and tested. Each of these is made up of multiple devices. The fluid analyzer SoC was fabricated with devices contained in the first two processing elements: biosensors, a mux/de-mux pair, an on chip signal generator, amplifiers, voltage controlled oscillators, and additional biosensor specific transistors for parameter adjustments.

The biosensor/preprocessing macro filters input signals through biosensors and directs the outputs of those sensors through the BIST circuitry or through intelligent processing devices for signal analysis and target identification. This macro appears in the top left of figure 3.1. It contains an array of biosensors, intelligent preprocessing, amplifiers, and devices for signal mixing.

Biosensor sub-blocks are used to perform the fluid analysis aspect of this work. Each biosensor can be developed to be sensitive to fluidic properties such as dielectric

constant, DNA, other antibody antigens, and protein. One class of biosensors studied in this work is based on VLSI implementations of the CHEMFET and has been published in [67]. This class of biosensors is presented in section 3.3.1, VLSI Implementation of Chemical Field Effect Transistor. Another class of biosensors studied and published in [68, 69] is the gateless field effect transistor. This class of biosensors is described in section 3.3.2, "A Gateless Field Effect Transistor".

The intelligent pre-processing exists in the use of on-chip signal generators and a multiplexer/de-multiplexer pair. Please note the interaction between the input signal, the system sub-blocks, and the output signal. Here we see one of the more important aspects of this SoC, its ability to multiplex input signals to different system blocks. This multiplexing system allows for smart signal processing in the selection of biosensors, the oscillation based BIST, or other internal circuits.

The second macro is used for built-in self test and parameter adjustment. This macro is used to identify the existence of faults within each of the devices in the SoC. Once faults are identified in sensors, for example, parameter adjustments can be made. Included in the parameter adjustment and BIST sub-block is a set of additional sensor specific transistors that can be accessed by the sensors in sub-block 1 through the use of the mux/de-mux pair. When faults are identified in biosensor transistors, the mux/de-mux pair selects fault-free transistors in the BIST/parameter adjustment macro as replacements for the transistors.

The third processing element for the fluid analyzer system contains: mixed and intelligent signal processing, analog-to-digital converters, microprocessing elements, and neural networks. Ideally these devices would be used to identify the properties (DNA,

dielectric constant, resistivity, color, etc.) of fluids under test based on biosensor output responses to the fluid being analyzed.

A view of the internal macros that make up the aforementioned sub-blocks is provided below in figure 3.2. The biosensor sub-block can be made up of an array of biosensors including the VLSI implementation of the ChemFET and the gateless field effect transistor. The fabricated SoC contains VLSI ChemFET biosensors only. The BIST sub-block is made up of a set of voltage controlled ring oscillators, operational amplifiers, and counters. The smart signal processing sub-block is created by the mux/demux pair, a test operational amplifier, and an on-chip voltage source.

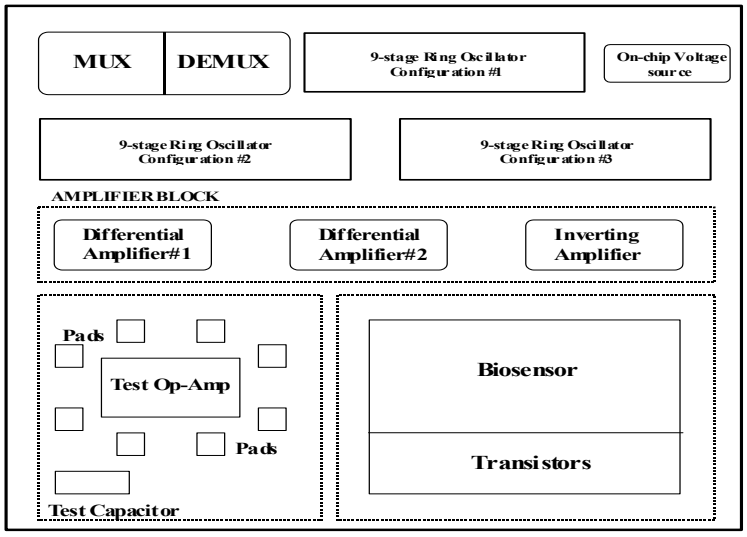


Figure 3.2 Block Diagram of Testbench-on-a-chip (TBOC)

In the following section an analysis and design discussion of the biosensors evaluated in this research is provided.

Section 3.3 Analysis and Design of Biosensors for Fluid Testing

The classes of biosensors studied in this work are designed to analyze physical properties of fluids. Such sensors are capable of distinguishing various characteristics associated with fluids including: dielectric constant, antibody antigens (DNA), fluid flow, protein concentration, and resistivity. Such sensors can discern inorganic and organic chemical properties. The sensors developed in this work can be implemented using standard very large scale integration (VLSI) fabrication procedures. In fact, the sensor circuits developed here can be fabricated on a semiconductor substrate that allows for the integration of additional signal processing circuitry onto the chip. The semiconductor substrates are amenable to application of the organic surface chemistries (for sensor sensitivity to DNA and other antibody antigens) which are discussed later in this section. An array of such sensors can be used to determine multiple properties of a fluid, using a single chip. The following subsections provide a discussion of the VLSI implementation of the ChemFET and the gateless field effect transistor studied in this work.

SubSection 3.3.1 VLSI Implementation of Chemical Field Effect Transistor

A schematic for the VLSI implementation of the chemical field effect transistor (ChemFET) sensor is shown in figure 3.3. This sensor is of interest because of its ability to detect fluid properties. This circuit operates as a dielectric constant measurement device and, as such, can be provided as part of an integrated micro-system designed to determine the properties of a fluid. The fluid-sensing transistor in this sensor is a diode connected transistor and is comprised of transistors M2 – M5, forming the VLSI

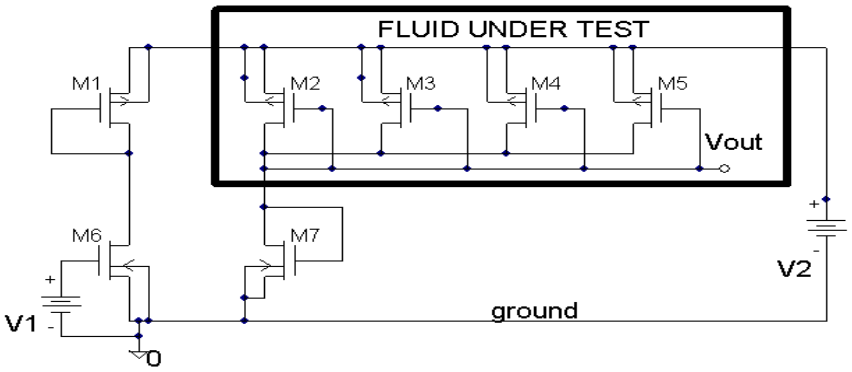


Figure 3.3 VLSI Adaptation of a Chemical Field Effect Transistor

adaptation of the CHEMFET. The sensor operates as a capacitive-type bridge such that a balance can be set for a normal dielectric constant. In the presence of a fluid, the unbalance that occurs within this sensor bridge is used to evaluate the fluid's dielectric constant.

Four CMOS transistors form the bridge: M1, M6, M7, and the fluid-sensing transistor (transistors M2 through M5). The fluid-sensing transistor and transistor M1 are PMOS (p-type MOSFETs) transistors in the diode connected configuration (gate connected to drain). The lower two transistors, M6 and M7, are NMOS type (one diode connected and the other with a gate voltage control). The output, Vout, of the sensor circuit is taken between the drains of M6 and M7.

The parallel connected transistors, M2 through M5, have openings in their gates to allow fluid to flow between the silicon substrate and the polysilicon gate where the gate oxide has been removed. This allows the fluid to behave as the gate dielectric for that transistor. Each of the transistors has a W/L ratio in our design of 10u/10u. The overall W/L ratio of the fluid-sensing transistor is therefore 40u/10u.

The fluid-sensing transistor is constructed out of four transistors with all terminals connected in parallel to increase the gain by the effective width with the constant parameter K_P. The sensing occurs because the K_P parameter is proportional to the dielectric constant. This proportionality is described in further detail in the following subsection, 3.3.1.1, Hand Calculations for the CHEMFET. In Spice the K_P parameter is described by the following:

$$K_P = \frac{\varepsilon_{ox} \times \mu_n}{t_{ox}}, \quad (3.1)$$

Fabrication of the sensor is based on a sacrificial etch process, where the silicon dioxide gate dielectric in the fluid-sensing transistor is removed by chemical etch. This activity is accomplished by opening holes in protective layers using the over-glass cut method available in the MOSIS-MEMS fabrication process. Two layers of metal over the polysilicon are used to prevent gate collapse.

Subsection 3.3.1.1 Hand Calculations for the CHEMFET

The first step towards developing an understanding of the ChemFET's ability to detect dielectric constant involves creating characteristic equations for the device. In this section SPICE implementations of the biosensor are studied and compared against the developed characteristic equations. This work serves as the initial step towards developing and evaluating SoC models for the fluid analyzer SoC sub-blocks (macros).

The characteristic equations are performed on figure 3.4 below. This figure produces the same output as figure 3.3 and it is redrawn here, as a SPICE model, for simplicity. For example, in lieu of 4 diode connected transistors representing the fluid under test, a single diode connected fluid under test transistor whose W/L ratio is 4 times

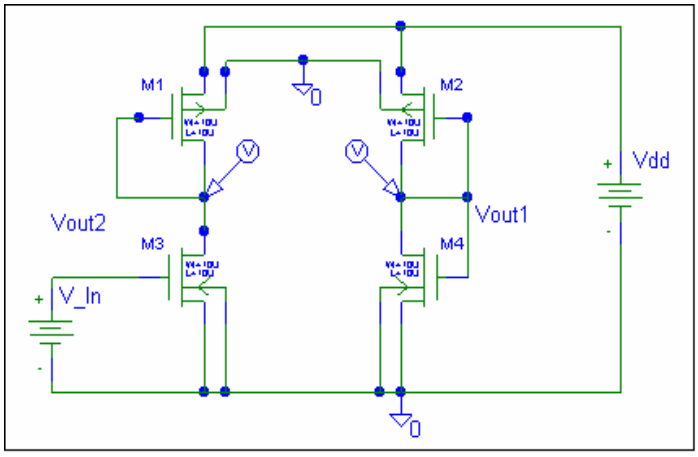


Figure 3.4 Simplified VLSI Implementation of Chemical Field Effect Transistor. V_In in this figure equals Vin in the hand calculations describing this sensor.

larger in equivalent width than the remaining system transistors, is shown. Characteristic equation analysis begins by defining the current and voltage relationships among each of the elements within the system. We begin with a model of the VLSI implementation of the Left Hand Side (LHS) of the CHEMFET (stage 1). The LHS of the CHEMFET is represented by transistors M1 and M3 as well as by input voltage V_In (V_{in}) and output voltage Vout2, measured with respect to ground. Using $K = \frac{KP}{2}\frac{W}{L}$, indexed for each transistor,

$$-V_{DS1} = |V_{TR1}| + \sqrt{\frac{-I_{D1}}{K_1}}\ , (3.2)$$

also, assuming M3 in saturation,

$$I_{D3} = K_3 (V_{in} - V_{TR3})^2 , (3.3)$$

$$V_{OUT2} = V_{dd} - |V_{DS1}| , (3.4)$$

$$V_{OUT2} = V_{dd} - \left(|V_{TR1}| + \sqrt{\frac{-I_{D1}}{K_1}} \right), (3.5)$$

$$I_{D1} = -I_{D3} , (3.6)$$

$$V_{OUT2} = V_{dd} - \left[|V_{TR1}| + \sqrt{\frac{K_3}{K_1}(V_{in} - V_{TR3})^2} \right], (3.7)$$

$$V_{OUT2} = V_{dd} - |V_{TR1}| - \sqrt{\frac{K_3}{K_1}}(V_{in} - V_{TR3}), (3.8)$$

Modeling the right hand side (RHS, stage 2) of the CHEMFET is similarly presented below. The RHS is comprised of transistor M2, transistor M4, and voltage, Vout1.

$$-I_{D2} = K_2\left(V_{dd} - V_{OUT1} - \left|V_{TR2}\right|\right)^2, \quad (3.9)$$

$$= I_{D4} = K_4\left(V_{OUT1} - V_{TR4}\right)^2, \quad (3.10)$$

or

$$\left(\sqrt{\frac{K_4}{K_2}} + 1\right)V_{out1} = V_{dd} - \left|V_{TR2}\right| + \sqrt{\frac{K_2}{K_4}}V_{TR4}, \quad (3.11)$$

therefore,

$$V_{out1} = \frac{V_{dd} - \left|V_{TR2}\right| + \sqrt{\frac{K_2}{K_4}}V_{TR4}}{1 + \sqrt{\frac{K_2}{K_4}}}, \quad (3.12)$$

A balance is set in the VLSI implementation of the CHEMFET when $V_{OUT1} = V_{OUT2}$. The question that this circuit posses is for a fluid specified dielectric constant, $\in$,

affecting $K_2 = \eta \in \big/ \left(2t_{fluid}\right)$ what input voltage, V_{in}, produces the desired balance. In the preceding, t_{fluid}, is the thickness of the dielectric fluid. As $V_{OUT1} = V_{OUT2}$ for a balance, (3.8) = (3.12) gives:

$$V_{out1} = V_{out2} = V_{dd} - \left|V_{TR1}\right| - \sqrt{\frac{K_3}{K_1}}\left(V_{in} - V_{TR3}\right), \text{ (3.13)}$$

solving for V_{in} equation 3.14 shows:

$$V_{in} = V_{TR3} + \sqrt{\frac{K_1}{K_3}}\left(V_{dd} - \left|V_{TR1}\right| - \left[\frac{V_{dd} - \left|V_{TR2}\right| + \sqrt{K_2 \big/ K_4}\, V_{TR4}}{1 + \sqrt{K_4 \big/ K_2}}\right]\right). \text{ (3.14)}$$

In the above, the ratio of $\frac{K_4}{K_2}$ is defined by the following:

$$\frac{K_4}{K_2} = \frac{\eta \in_{si} \big/ 2t_4}{\eta \in_{fluid} \big/ 2t_{fluid}}. \text{ (3.15)}$$

With $t_4 = t_{fluid}$, equation (3.15) becomes:

$$\frac{K_4}{K_2} = \frac{\in_{si}}{\in_{fluid}} . \quad (3.16)$$

Substituting equation (3.16) into (3.14) gives:

$$V_{in} = V_{TR3} + \sqrt{\frac{K_1}{K_3}} \left[V_{dd} - |V_{TR1}| - \left(\frac{V_{dd} - |V_{TR2}| + \sqrt{\frac{\in_{Si}}{\in_{fluid}}} V_{TR4}}{1 + \sqrt{\frac{\in_{Si}}{\in_{fluid}}}} \right) \right] . \quad (3.17)$$

Thus the V_{in} needed to balance is dependent on the dielectric constant, and solving equation 3.17, for $\in_{fluid}$ as a function of V_{in}:

$$\in_{fluid} = \in_{Si} \left[\frac{\sqrt{\frac{K_3}{K_1}} (V_{in} - V_{TR3}) - V_{dd} + |V_{TR1}| + V_{TR4}}{\sqrt{\frac{K_3}{K_1}} (V_{in} - V_{TR3}) + |V_{TR1}| - |V_{TR4}|} \right]^2 . \quad (3.18)$$

Figure 3.5 shows a Spice simulation of the biosensor, V_{out2} versus V_{in} showing that there is sufficient range of adjustment to give a balance for a very wide range of fluids. In figure 3.6 we see the effect of contrasting K_P values to simulate a fluid under test and mimic expected changes in output voltage with respect to the entrance of a dielectric altering substance. The new K_P value introduced is 50% less than the old K_P

value. As expected by equation 3.14, the resulting input voltage, V_{in} that is used to balance the device is lower than the normal K-value input voltage as the intersection of V_{out1} & V_{out2} is shifted to the left. In Spice the K_P parameter is defined in equation 3.1 and repeated here: $K_p = \frac{\varepsilon_{ox} \times \mu_n}{t_{ox}}$.

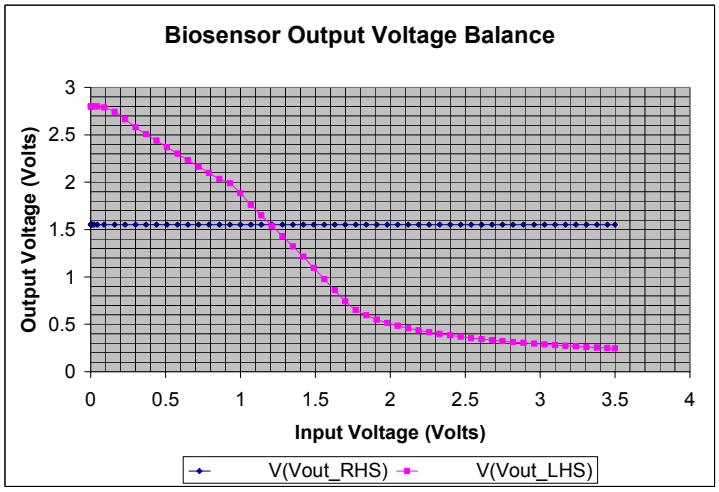


Figure 3.5. Biosensor output comparison versus input voltage, the KP value for this example is 2.048e-05, where KP = $\mu C_{ox}/2$.

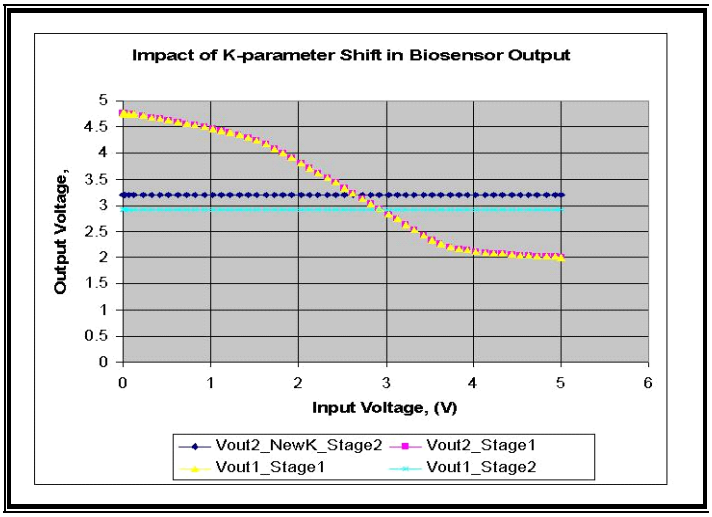


Figure 3.6. Biosensor output comparison with contrasting KP parameter values versus input voltage. The KP values shown are for KP = 2.048e-05 (normal KP) and KP = 1.024 e-05 (new KP).

It is noted that a more accurate model of the above equations, would include a voltage shift characteristic of charge-trapping instabilities. The trapped surface charge would impact the threshold voltage of the transistor(s) exposed to fluids under test. For the case of figure 3.4 above, transistor M2 (the fluid under test transistor) would be affected by this trapped charge.

Charge-trapping instabilities are common during device operation and/or characterization of thin-film transistors. It is typically associated with hot-carrier induced oxide damage which results in device degradation (voltage shift, transconductance reduction, drain current degradation, etc.) and has long plagued researchers interested in MOSFET reliability[70]. For the case of the biosensors studied in this work, charge trapping results from charges induced on the surface of the transistors directly from fluids under test. In the following evaluation of charge trapping effects on threshold voltage, we limit the discussion to the physical affects of fluid on the biosensor. A detailed description of hot-carrier induced (traditional) charge trapping appears in Appendix A.

Threshold voltage shifts in transistor-based biosensors due to charge trapping are generally the result of stresses induced on the gate of the transistors through which fluids are evaluated. The trapped charge (Q_{ox}) results in localized build up of interface states (N_{SS}) and is modeled in the following.

Beginning with the basic equation for drain-source current,

$$I_{DS} = \frac{\mu C_{ox} W}{2L}\left(V_{gs} - V_{TH}\right)^2 , \quad (3.19)$$

A change in drain-source current, due to trapped charge would therefore be expressed as,

$$\Delta I_{DS} = \frac{\Delta\varepsilon}{d_{ox}}\mu\left(\frac{W}{L}\right)\left(V_{gs} - V_{TH}\right)^2 , \text{(3.20)}$$

in which,

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta\varepsilon}{\varepsilon} , \text{(3.21)}$$

Thus, the resulting threshold voltage V_{TR} for transistor M2, inclusive of trapped surface charge effects, is expressed as:

$$V_{TR} = 2\phi_b + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s qN_d\, 2\phi_{bi}} + \frac{1}{C_{ox}}qN_{SS} , \text{(3.22)}$$

where,

$$C_{ox} = \frac{\varepsilon_s}{d_{ox}} . \text{(3.23)}$$

In the above, we see for fluids containing positive charge, an increase in threshold voltage and for fluids containing a negative charge we see a decrease in threshold voltage.

Subsection 3.3.2 A Gateless Field Effect Transistor*

The other sensor under study in this work is a biological macromolecular sensor for early detection of diseases. The device was patented and developed by members of the Naval Research Laboratory as listed by the endnote below. The publications that came about from the macromolecular sensor analysis performed in this dissertation, can be found in [68, 69]. In this dissertation, in addition to a discussion of the sensor analysis, a SystemC implemented model for the macromolecular sensor, is created and evaluated. This model is a software implementation of the macromolecular sensor and relies on the analytical model of the device.

The macromolecular sensor, is a gateless depletion-mode field effect transistor (FET) having a source implant and a drain implant that are spatially arranged within a semiconductor structure. The source and drain are separated by an active channel, which is covered by a dielectric layer. The dielectric layer has a bottom surface, which is in contact with the active channel and a top surface, which is in contact with a sample solution. The top surface of this gateless FET is modified with a receptor for detecting the presence of target antibody antigens and/or DNA strands as shown in figure 3.7. A reference electrode is attached externally to the sample solution. The cilia-like structures or micro-channels shown in this figure, and introduced to the biological macromolecular sensor, represent DNA and/or antibody antigen receptor sites.

The sensor detects the presence of target molecules in the sample solution by measuring the change in current between the source and drain. The change in current occurs via one of two methods. The first is due to the change in capacitance of the

* US Patent No. 6482639, "Microelectronic device and method for label-free detection and quantification of biological and chemical molecules", E.S. Snow, M. Peckerar, L.M. Tender, S.J. Fertig, and F.K Perkins, The United States of America as represented by the Secretary of the Navy, Filed June 22, 2001.

receptor-modified dielectric film/sample solution interface when target molecules bind to the molecular receptors. The second is the result of charged molecules binding to the receptor-modified dielectric film or sample solution interface.

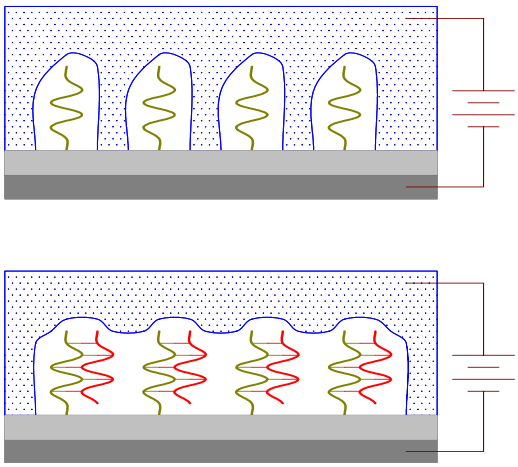


Figure 3.7 Antibody/Antigen attachments to gateless Field Effect Transistor.

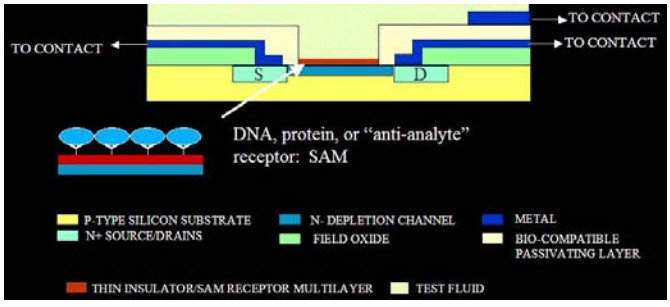


Figure 3.8 Cross Section of Gateless Field Effect Transistor .

The gateless field effect transistor is evaluated for its ability to adequately detect matches in target, antibody antigen solutions. This sensor is an active element device

capable of developing circuit gain. Such devices are known for their high input impedance, which makes them suitable for pre-amplifier application. Figure 3.8 presents a cross section of the gateless field effect transistor. This provides the basis for the analytic model created in this work.

Subsection 3.3.2.1 Hand Calculations for Gateless FET

We now show the development of an analytic model of the self assembled monolayer (SAM) treated, gateless FET [71]. The macromolecular sensor is a depletion-mode FET in which a SAM treatment is applied locally. Appendix B provides detailed references for chemistries associated with SAM treatment applications.

The advantage of using the FET as a biosensor is that it can discriminate between charge and the thickness of a deposited film. The basic equation of this (depletion-mode) FET operating in saturation is [71]:

$$I_{DS} = \frac{1}{2}\mu C_{ins}\frac{W}{L}\left(V_{th}^2 - V_{gs}^2\right), \qquad (3.24)$$

where C_{in} is the insulator capacitance per unit area, μ is the channel charge mobility, V_{th} is the threshold voltage, V_{gs} is the voltage drop between the gate and the source, and W and L are the width and length of the channel. The device threshold voltage V_{TH} depends on gate charge and on the thickness of the gate insulator C_{ins}, as shown in the expression below:

$$V_{TH} = \frac{1}{C_{ins}}\left(qN_d x_d + Q_{ins}\right), \qquad (3.25)$$

rewriting equation (3.19) we obtain,

$$V_{TH} = 2\phi_b + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s qN_d 2\phi_{bi}} \quad . (3.26)$$

Here, q is the absolute value of charge on the electron, N_d is the doping density of the substrate under the channel and Q_{ins}, is the charge per unit area in the gate insulator. For the gateless operation envisioned, increases in insulator thickness above the active silicon channel decreases C_{ins}. Mobility (μ) is also influenced by charge but as a second-order effect. As with the threshold voltage associated with the VLSI adaptation of the chemical field effect transistor, the threshold voltage in 3.26, would be shifted due to charge trapping. The shift in equation 3.26 is as expressed by, the shift in equation 3.22, $\frac{1}{C_{ox}} qN_{SS}$.

The macromolecular sensor's ability to extract threshold voltage and gate capacitance is a major advantage over the standard ChemFETs discussed in chapter 2. Normally, in traditional ChemFETs like those described in chapter 2, the materials used to immobilize the analyte were too thick to fully exploit the capacitance signal effectively. In addition, advances in SAM technology replaced chelating resins as materials of choice for sensor technologies. These SAMs can be locally applied, and different head groups can be applied to different sensors in an array through "microspotting" machines available today. Thus, multi-analyte arrays are possible.

The studied structure was assembled as an array of gateless field effect transistors in which each device on the wafer has a separate drain contact. The configuration studied

uses 288 devices per chip arranged in groups (or cells) of four on a 6.5 mm pitch. Each device has a separate and independent drain contact. There is also one gated test structure adjacent to every dozen sensors. Finally, a reference electrode is on each cell and is included to establish the solution potential. For the studied structure, the starting material was a p-type <100> Si wafer. The channel region was $6\mu m$ x $30\mu m$ (LxW) and phosphorous (P) was implanted at 60 keV to a dose of 6 x 10^{11} cm^{-2}. The source and drain contacts were formed by a P implant at 80 keV to an area density of 10^{15} cm^{-2}. A 63 nm thermal oxide layer was followed by a 30 nm LPCVD Si_3N_4 layer (thicknesses determined by ellipsometry). Following a Cr/Au contact metallization, a 600 nm LPCVD oxide layer was formed over all.

Section 3.4 Oscillation Based Built-In Self-Test (OBIST)

As discussed in chapter 2, the BIST method using the oscillation test strategy (OTS) has been shown to have the potential of overcoming common problems associated with conventional test methods. This BIST method was also shown to be effective for any type of mixed analog/digital circuitry used as system blocks. The OTS contains several resistors, internal capacitors, and depended upon an external positive and negative feedback loop to produce oscillations in the circuit under test.

The inherent problems with this method are as follows: the use of external resistors and capacitors reduce the amount of die area for non-test circuitry on the chip and the development of oscillations based on the circuit under test (a CMOS amplifier) could continually propagate internal system errors making fault detection and on-chip correction unwieldy. Another inherent problem with the OTS method is the fact that it uses an external level-crossing detector comprised of two resistors to produce clock-like

signals. The resistors in and of themselves further exacerbate the space issue raised by the OTS method.

As such, a novel oscillation based built in self test (OBIST) method is developed and evaluated in this dissertation. The published results of the OBIST method can be found in [72]. The evaluation of this built-in self-test is comprised of Spice simulation and SystemC based SoC modeling and simulation. This evaluation begins by looking at the analog to digital conversion process of the OBIST method.

Analog to Digital Converter (ADC), a key component of BIST circuitry, is used to interface mixed signal devices. The specific focus of the ADC evaluation used here is on the use of oscillation-based digital circuits for mixed signal testing including the production line technique of using standard ring oscillator properties. It is expected that this work will lead to establishing the test metrology necessary for developing BIST methods that incorporate the use of analog-to-digital system blocks.

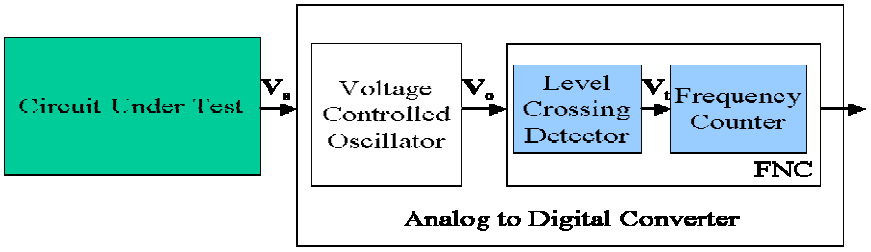


Figure 3.9 Block Diagram of ADC Conversion Process

Converting the output of the analog CUT into a digital signal involves transferring the signal through an ADC comprised of a voltage controlled oscillator (VCO), level crossing detector (LCD), and frequency counter (FC). The LCD and FC make up the frequency-to-number converter (FNC), which passes a number to a frequency counter for

processing. A block diagram of this ADC conversion process was presented in figure 2.3 and is repeated in figure 3.9. The frequency counter output that appears at the output of this diagram can be expressed as a function of the CUT's components or parameters.

Changes in various component characteristics (i.e., transistor W/L ratios) will give rise to deviations in the CUT's expected output. The test for an out of range component is therefore denoted by any deviation of an acquired oscillation frequency from its expected nominal value.

Many questions arise from this testing methodology. The first involves how best to develop a method to transform the CUT signal into an oscillating signal. The second asks how best to test for deviations in actual output and expected output. The third involves developing a means to feed the expected output values into an analog SoC that may contain systems with faults.

In answering the first question, this work proposes to create oscillations from a steady-state voltage output with the aid of a voltage controlled ring oscillator (VCO), an example of the VCO used here is provided in figure 3.10. While the OTS method uses negative feedback through an op-amp to produce the required oscillations, the method used in this dissertation, feeds the analog output of the circuit under test directly into the input of the VCO. The use of this method for producing oscillation frequency eliminates the size and fault propagation error issues raised by the OTS. The answer to the second question raised above requires the development of a SoC model of a counter to count the digital, clock-like, outputs generated by the VCO-LCD pair. Answering the third question involves the use of test vectors generated by the end-user and processed through

the system with the aide of test programs like, National Instruments' Lab View. In this dissertation we focus on the first two concerns.

To develop a steady-state voltage output, oscillations are created with the aide of the voltage controlled ring oscillator shown in figure 3.10, below. This VCO is a structure made up of three unique parts including a control input stage, a propagation delay controlled ring oscillator, and an output buffer. The input control voltage (Vin) that originates from the circuit under test controls the overall oscillation frequency of the VCO. This voltage is capable of "current starving" the inverter stages of the ring oscillator and thus changing the propagation delay. The input sets the current in the current source transistors labeled M56 and VCO_Input, which in turn sets the current in the delay control elements. The ON resistance of the pull-up (upper transistors of the ring oscillator) and pull-down (lower transistors of ring oscillator) transistors is modulated according to the input voltage, Vin. These variable resistances control the current available to charge and discharge the load capacitance of each inverter stage in the ring oscillator. When the control voltage is large, a large current will flow, producing a small resistance and thus a small propagation delay.

Each of the inverters appearing in the VCO ring oscillator consists of two complimentary transistors (an NMOS and a PMOS). A ring oscillator consists of an odd number of inverters. The output of the last inverter is connected to the input of the first. The minimum number of inverters needed to produce oscillations is three. The oscillation frequency (f_{osc}) is inversely proportional to the gate propagated delay time and the number of gates n.

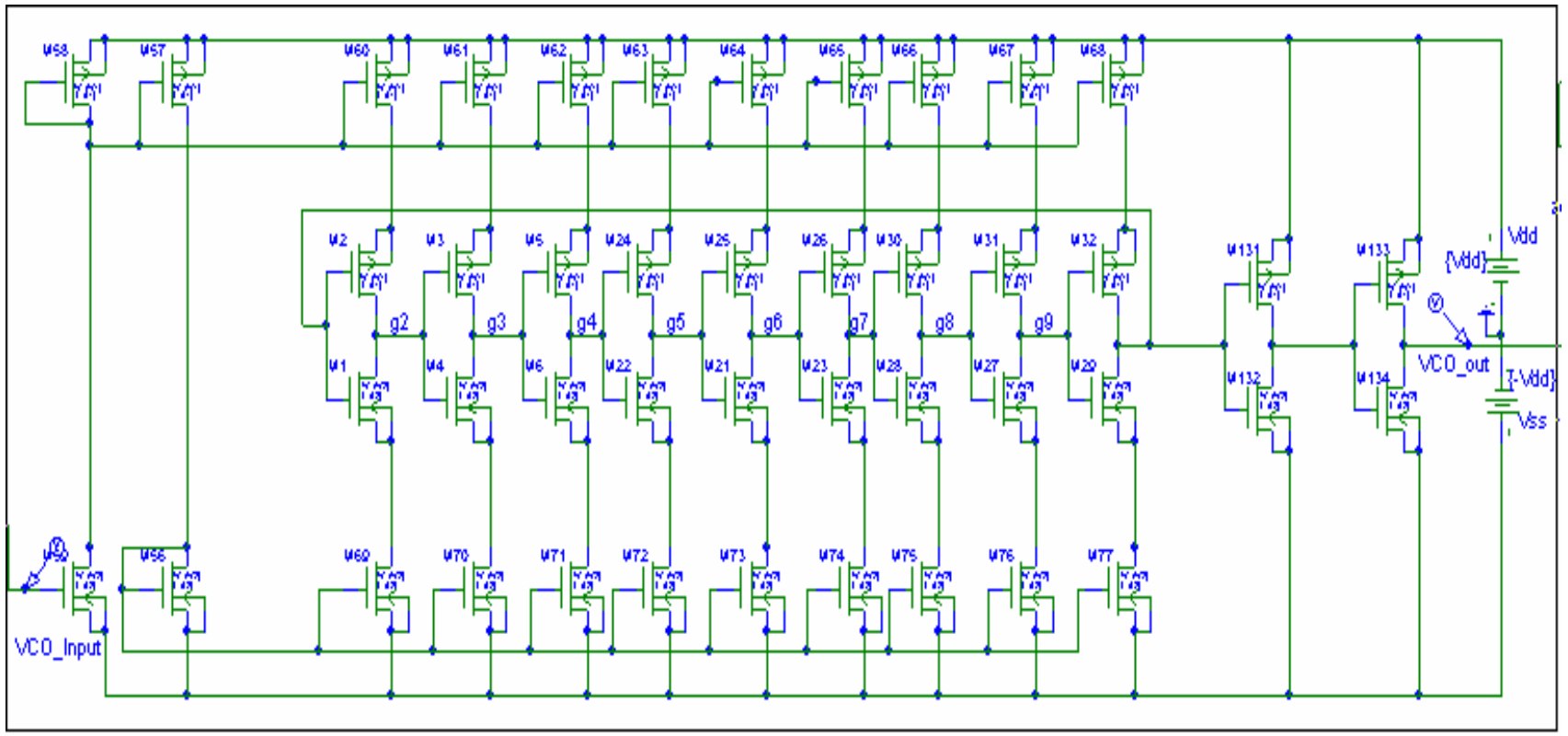


Figure 3.10: Voltage Controlled Ring Oscillator. This figure depicts a multistage voltage controlled ring oscillator made up of solely transistors. * full page picture (landscape) and verify your explanation for 9 ring oscillator is discussed later *

In this analysis several VCO configurations are considered. The key variables in the design study were those that affected the ring oscillator stage. A number of inverters and drain voltages were considered prior to selecting the configuration for the BIST method studied here. A selection of a 9-inverter ring oscillator was chosen based on the frequency of oscillation for a 20 ms Spice simulation. The 9-inverter ring oscillator oscillates more rapidly than the 3-, 5-, and 7-inverter ring oscillators evaluated. Additional details about the oscillations appear later in this section when discussions of delay time in the CMOS inverter occur. The 9-inverter ring oscillator with a drain (source) voltage of 0.25V (-0.25V) was chosen as most suitable for the BIST ADC under Spice transient analysis evaluation. The circuit was evaluated for 20ms at steps of 20μs.

THE OSCILLATION FREQUENCY AND VCO TIME DELAY

In this section the switching performance and the delay time of the inverters comprising a "n-ring" oscillator are analyzed (where n is the number of inverters included in the oscillator). To produce oscillations we require an odd number of inverters. The output of an inverter generally drives a capacitance load, since the gate of a following MOS transistor stage is an almost perfect insulator. An illustration of cascade connected CMOS inverters can be seen in the ring oscillator stage of figure 3.10. The effective capacitance at the output of the first inverter results from contributions of interconnections, overlap areas, and transistor gates. In most designs the nonlinear gate capacitance is dominating. Since, the transistor equations are nonlinear, an accurate switching performance prediction of a circuit is only time

effective with the aid of a circuit simulation program. The following equations for load capacitance estimation and oscillation frequency are approximations and useful for aiding in understanding the uniqueness of the modified oscillation frequency module developed in this work.

Load Capacitance Estimation

The input voltage of the inverter is switched from a low (L), to a high (H), state and the effective capacitances of the n-channel transistor are considered first. Here "H" and "L" mean the voltage levels Vcc and –Vcc, where Vcc = Vdd – Vsd of the voltage control transistors [upper ones of figure 3.10]. To ease the derivation and in order to come up with a worst-case estimate, it is assumed that the transistor remains in the resistive region during switching. Under this condition the gate capacitance can be divided into source and drain contributions of 50% each. At time t = 0 the n-channel transistor is cut off, its gate source capacitance $C_{gs} = \frac{C_{ox}}{2} WL$ is charged to 0V and its gate drain capacitance $C_{gd} = \frac{C_{ox}}{2} WL$ to $V_{GD} = - V_{CC}$ via the p-channel transistor. If the n-channel transistor is turned on this causes the C_{gs} capacitance to be charged from 0V to V_{CC}; while, the C_{gd} capacitance is charged to a different polarity from $-V_{CC}$ to $+V_{CC}$. The resulting charging currents are for C_{gs}

$$I_S(t) = \frac{C_{ox}WL}{2}\frac{dV_{GS}}{dt} \approx \frac{C_{ox}WL}{2}\frac{V_{CC}}{\Delta t}, \qquad (3.27)$$

and for C_{gd}

$$I_{DS} = \frac{C_{ox}WL}{2}\left(\frac{dV_{GS}}{dt} - \frac{dV_{DS}}{dt}\right) \approx \frac{C_{ox}WL}{2}\left[\frac{V_{CC}}{\Delta t} - \left(-\frac{V_{CC}}{\Delta t}\right)\right], \qquad (3.28)$$

$$\approx C_{ox}WL\frac{V_{CC}}{\Delta t}, \qquad (3.29)$$

This leads to a total charging current at the gate of

$$I_G(t) = I_S(t) + I_{DS}(t) \approx \frac{3}{2}C_{ox}\frac{V_{CC}}{\Delta t}. \qquad (3.30)$$

This results in an equivalent capacitance model of the n-channel transistor. In this model, used for the cascade-connected CMOS inverters, a loading situation results where the effective loading is

$$C_L \approx \frac{5}{2}\left(C_{ox,n} + C_{ox,p}\right)\cdot WL, \qquad (3.31)$$

If the p-channel transistor geometry is chosen to be twice as large as that of the n-channel transistor the capacitance loading shown in equation 3.23 results.

$$C_L \approx 7.5C_{ox}\cdot WL, \qquad (3.32)$$

Switching performance of the CMOS inverter

The switching behavior is described as follows. If the input signal V_{in} changes abruptly from 0V to V_{CC}, this causes the p-channel transistor to be cut off and the n-channel transistor to be conducting, discharging capacitance C_L. At a value of $0.1\,V_{CC}$ it can be assumed that the following stage interprets this value as an L signal. Up to a voltage of $V_{DS} = V_{CC} - V_{tn}$, the n-channel transistor is in the saturation region and subsequently in the resistive region. Because of these two operation conditions the fall time t_f has to be divided into two time intervals. With the current of the n-channel transistor I_{DS} being equal to that discharging the capacitance I_C, the first time interval

$$I_C = -I_{DS}\,.$$

$$C_L \frac{dV_Q}{dt} = -\frac{\beta_n}{2}\left(V_{CC} - V_{tn}\right)^2$$

$$\int_0^{t_{f1}} dt = \int_{Vcc}^{V_{CC}-V_{tn}} \frac{2C_L}{-\beta_n\left(V_{CC} - V_{tn}\right)^2} dV_Q \,, \quad (3.33)$$

$$t_{f1} = \frac{2C_L V_{tn}}{\beta_n\left(V_{CC} - V_{tn}\right)^2}$$

can be found in (3.24). A similar derivation yields the second time interval

$$C_L \frac{dV_Q}{dt} = -\beta_n\left[\left(V_{CC} - V_{tn}\right)V_Q - \frac{V_Q^2}{2}\right]. \quad (3.34)$$

$$\int_0^{t_{f1}} dt = -\frac{C_L}{\beta_n}\int_{V_{cc}-V_{tn}}^{0.1V_{CC}} \frac{1}{(V_{CC}-V_{tn})V_Q - \frac{V_Q^2}{2}} dV_Q \text{, (3.35)}$$

$$t_{f2} = \frac{C_L}{\beta_n}\frac{1}{V_{CC}-V_{tn}}\ln\frac{1.9V_{CC}-2V_{tn}}{0.1V_{CC}}$$

Adding the two, a total fall time of

$$t_f = t_{f1} + t_{f2} = \frac{C_L}{\beta_n}\frac{1}{V_{CC}-V_{tn}}\left(\frac{2V_{tn}}{V_{CC}-V_{tn}} + \ln\frac{1.9V_{CC}-2V_{tn}}{0.1V_{CC}}\right). \text{ (3.36)}$$

In analogy to this derivation, the rise time determined by the p-channel transistor can be derived

$$t_r = t_{r1} + t_{r2} = \frac{C_L}{\beta_p}\frac{1}{V_{CC}+V_{Tp}}\left(\frac{-2V_{Tp}}{V_{CC}+V_{Tp}} + \ln\frac{1.9V_{CC}+2V_{Tp}}{0.1V_{CC}}\right) \text{(3.37).}$$

These equations state that the rise and fall times are proportional to the capacitance loading, given by (3.23), and that these times can be reduced by increasing the gain factors of the transistors.

Delay time of the CMOS inverter

The input of an inverter is usually driven by a signal which behaves similarly to that considered at the output. The delay between input and output signal can be approximated for the charging and discharging case by $t_{dr} \approx t_r / 2$ and $t_{df} \approx t_f / 2$. This leads to the following average delay time of the CMOS inverter which is useful for first hand estimations.

$$t_d \approx \frac{1}{2}\left(t_{dr} + t_{df}\right) \approx \frac{1}{4}\left(t_r + t_f\right), \quad (3.38)$$

Buffer stages are used in integrated circuits to drive relatively large parasitic on-chip capacitances, which are present in conjunction with clock and data lines or output stages. The buffers or drivers which are analyzed can be divided into super buffers and bootstrap ones. The CMOS inverter can be used to drive a large load capacitance, C_L. This results in a substantial delay time of the circuit, which might not be acceptable from a system point of view. Increasing the current gain of the transistors by making the geometry ratios $\left(W/l\ L\right)_n$ and $\left(W/L\right)_p$ larger, may not necessarily lead to the required reduction in the delay time, since the input capacitance of the inverter increases also. In the extreme case the value of the input capacitance may even be of the same order as the load capacitance. Cascaded CMOS inverters with staggered geometry ratios, called super buffers, are a solution. The first inverter has a relatively small input capacitance of C_1, which corresponds to the geometry dimensions of the input transistors. This inverter drives a second one with

a $\left(W/L\right)$ ratio of the transistors α times larger than that of the first inerter. This results in an increased input capacitance $C_2 = \alpha \cdot C_1$. The second inverter in turn drives a third one with also an α times larger geometry ratio and larger input capacitance of $C_3 = \alpha \cdot C_2 = \alpha^2 \cdot C_1$, and so on until the nth inverter drives the load capacitance C_L. The question arises as to how many inverters are needed and what capacitance ratio

$$\alpha = \frac{C_{N+1}}{C_N}, \quad (3.39)$$

is required in order to achieve a minimum delay time. If identical inverters are cascaded, each inverter has an identical time delay of t_d. If staggered geometry ratios are used, the delay of each inverter increases to

$$t_d^{'} = \alpha t_d . \quad (3.40)$$

This results in a total inverter chain delay time of

$$T_d = nt_d^{'} = n\alpha t_d . \quad (3.41)$$

With the load capacitance given by

$$C_L = \alpha^n C_1 . \quad (3.42)$$

This leads to the relationship of

$$T_d = \frac{\alpha}{\ln \alpha} t_d \ln \frac{C_L}{C_1}. \quad (3.43)$$

as

$$\alpha^n = C_L / C_1, \quad (3.44)$$

implies

$$e^{n \ln \alpha} = C_L / C_1, \quad (3.45)$$

$$n = \frac{1}{\ln \alpha} \ln\left(\frac{C_L}{C_1}\right), \quad (3.46)$$

A minimum delay time of

$$T_{d\min} = e t_d \ln \frac{C_L}{C_1}. \quad (3.47)$$

results at $dT_d / d\alpha = 0$ with $\alpha = e$. In this case the required number of inverters can be found directly from equation (3.29) by rounding up to the next larger integer.

This gives n = 9 so that, in this dissertation, a set of 9 cascaded inverters is used to create a CMOS ring oscillator. The starting point in calculating the oscillation frequency, f_{osc} involves analyzing the input capacitance of the CMOS inverter. The value of the input capacitance is

$$C_1 = \frac{3}{2}\left(C_{ox,n} + C_{ox,p}\right)\cdot WL = \frac{3}{2}C'_{ox}\left((W\cdot L)_n + (W\cdot L)_p\right). \quad (3.48)$$

The above calculations yield an oscillation frequency,

$$f_{osc} = 1\big/T_{d\min} = \frac{1}{e\cdot t_e \cdot n} \quad (3.49)$$

The output of the Spice simulation of the 9-stage ring oscillator follows in figure 3.11.

This oscillation frequency module was used in this dissertation to modify the OBIST procedure developed by Arabi and Kaminska [73]. In chapter 4, the results of applying this method of developing oscillation frequencies from the input voltage of a circuit under test are provided. The proposed oscillation frequency is generated by applying the output voltage of the biosensor circuit to the input voltage of the VCO. The frequency at the output of the VCO indicates the existence or lack of existence of a fault. Combining the VCO with the level crossing detector proposed by Arabi and Kaminska resulted in the enhanced level crossing detector built-in self-test.

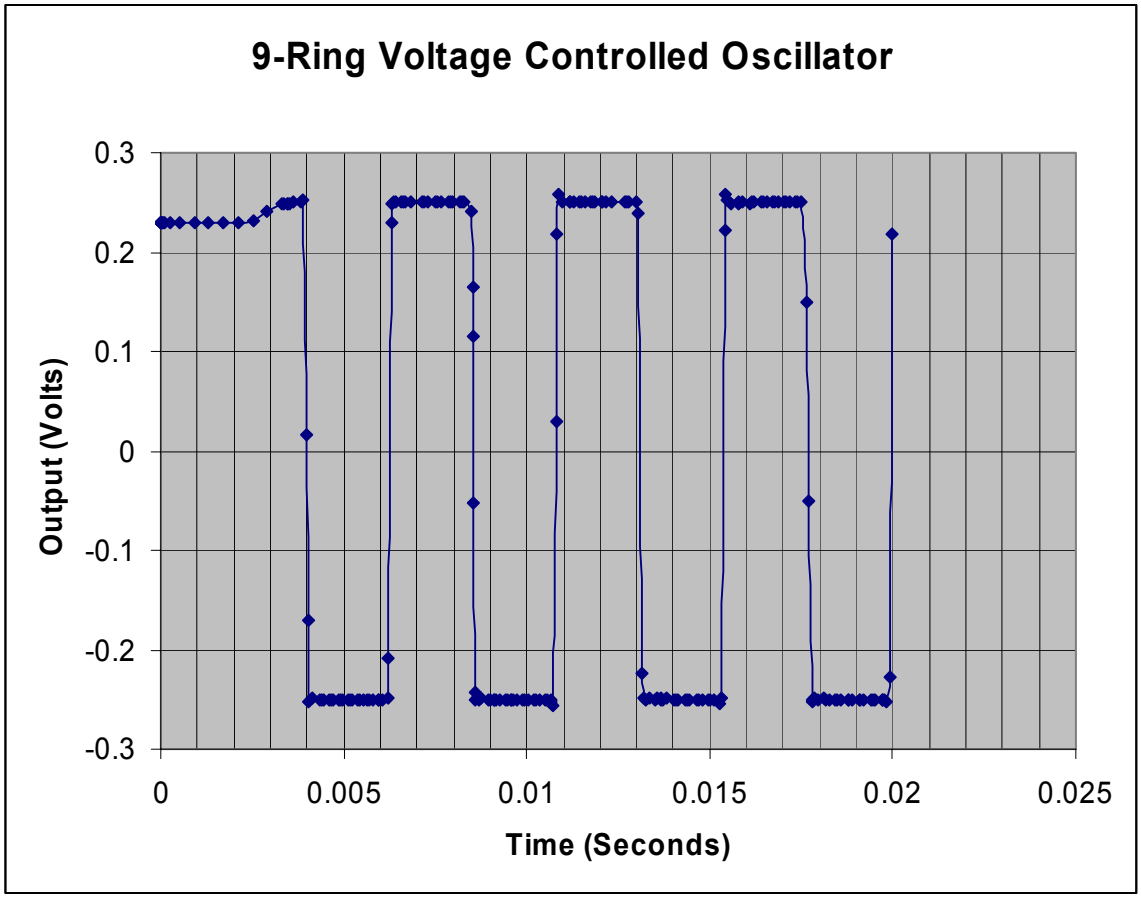


Figure 3.11 Output for 9-Stage Voltage Controlled Ring Oscillator.

Developing Models enhanced Level Crossing Detector BIST

This enhanced level crossing detector (eLCD) method of developing clock-like digital signals (as created in this dissertation) involves feeding the analog output of a circuit under test into the aforementioned VCO. The output of the VCO is then fed into the input of the Arabi-Kaminska level crossing detector (LCD). The figure below shows the output of the LCD once a VCO-altered output of the biosensor circuit has been applied to the input of the eLCD. When the output of the eLCD is

fed into the input of a SoC model of a BIST, frequency to number conversion takes place.

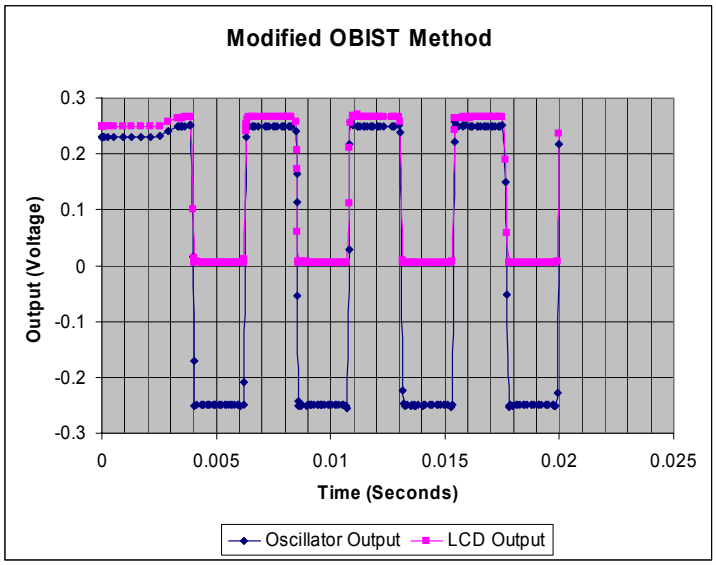


Figure 3.12. Output of Hodge Modified FNC Method

This dissertation further modifies the oscillation test strategy by developing a new LCD, the ZCD, designed to make on-chip dimensionality of all built-in self-test parameters compact. The above eLCD is flawed by its use of resistors which take up large amounts of chip area (as compared to transistors). To eliminate the use of resistors in a level crossing detector, the following zero crossing detector is proposed, developed and evaluated.

ZERO CROSSING DETECTOR (ZCD)

The zero crossing detector developed in this effort is comprised of a voltage controlled transistor and a diode connected transistor. The voltage controlled

transistor, M2, is driven by the output of the voltage controlled oscillator. The diode connected

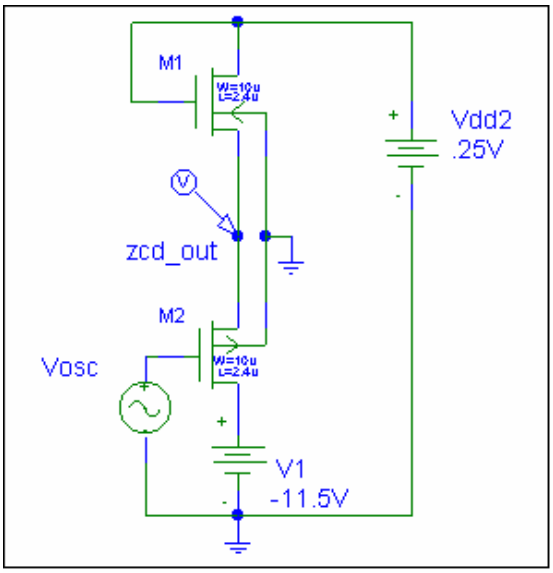


Figure 3.13. Zero Crossing Detector

transistor, M1, has an applied drain voltage of 0.25V. The width/length ratio of these transistors is 10u/2.4u. The characteristic equations for the zero-crossing detector follow.

$$v_{out} = -\left(g_{m1} \cdot v_{in}\right)\left(r_{o1} \| r_{o2}\right), \quad (3.50)$$

$$a_v = \frac{v_{out}}{v_{in}} = -g_m\left(r_{o1} \| r_{o2}\right), \quad (3.51)$$

$$\frac{v_{out}}{v_{in}} = -g_m\left(\frac{r_{o1}\cdot r_{o2}}{r_{o1}+r_{o2}}\right), \quad (3.52)$$

$$r_{o1} = \frac{1}{\lambda_1 I_{D1}}, \quad (3.53)$$

$$r_{o2} = \frac{1}{\lambda_2 |I_{D2}|}, \quad (3.54)$$

$$\frac{v_{out}}{v_{in}} = -g_{m1}\left[\frac{\left(\frac{1}{\lambda_1\lambda_2 I_D^2}\right)}{\frac{1}{I_D}\left(\frac{1}{\lambda_1}+\frac{1}{\lambda_2}\right)}\right], \quad (3.55)$$

$$\frac{v_{out}}{v_{in}} = -g_{m1}\left[\frac{1}{I_D(\lambda_1+\lambda_2)}\right], \quad (3.56)$$

$$I_D = I_{D1} = -I_{D2} = K_N(V_{GS1}-V_{TRN})^2, \quad (3.57)$$

$$\frac{v_{out}}{v_{in}} = -g_m\frac{1}{K_N(V_{GS1}-V_{TRN})^2(\lambda_1+\lambda_2)}, \quad (3.58)$$

$$\frac{v_{out1}}{v_{in}} = \frac{-2}{K_N\left(V_{GS1} - V_{TRN}\right)\left(\lambda_1 + \lambda_2\right)}, \quad (3.59)$$

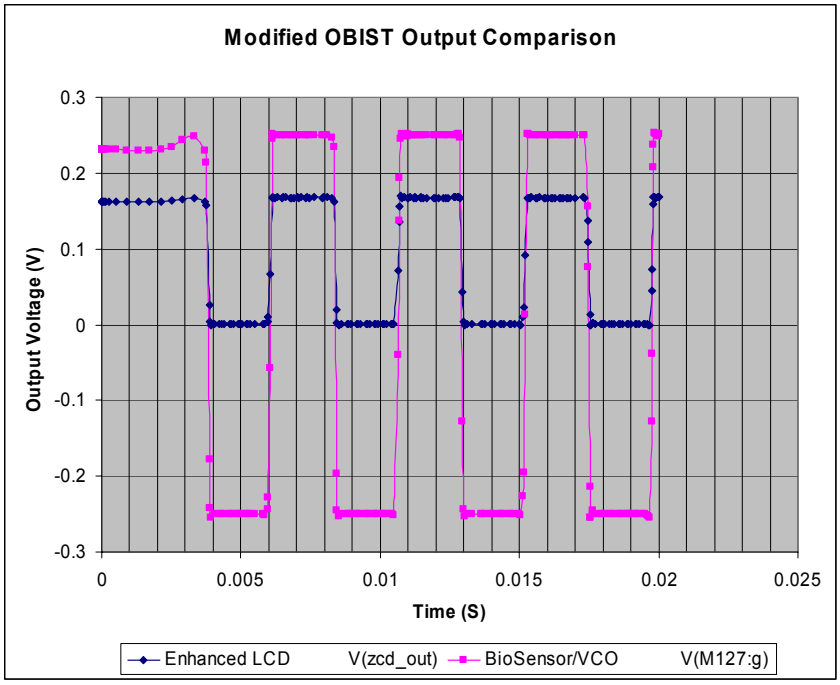


Figure 3.14. Output of modified VCO vs. ZCD.

The level crossing detector (zero-crossing detector, ZCD) developed in this dissertation is comprised of a voltage controlled NMOS transistor and a diode connected PMOS transistor. The Spice simulation of the VCO-ZCD output curves is shown in figure 3.14.

With the above characteristic equations, we can now develop system-on-a-chip models for the testbench-on-a-chip system sub-blocks. The developed models are viewed pictorially in section 3.5 as system-level designs. SystemC software implementation models are also included in the next section. The SystemC models

can be developed in SystemC, C++ or Matlab. As the Matlab implementations of the SoC models can be translated directly into C++ which is compatible with SystemC libraries and usage. The more detailed SystemC models and testbenches developed in this dissertation can be found in Appendix A.

Section 3.5 Development of SoC Models

There has been good progress in the development, design, and verification of SOC models for digital systems [74]. The current state of the art for this venue involves automatic generation of SOC models from the Very High Level Description Language (VHDL) equivalent of the Device. The models are easily created for the SoC modeling platform, SystemC, using software like VHDL2SystemC [75]. Such software is easily downloaded from various web sites that sponsor SoC related products [76]. While digital SOC modeling has shown tremendous advancement, there is a significant lag in analog SOC modeling. This is due to the complexity of most Analog designs. This concern is addressed in this work because many biosensors and BIST circuitry exist as analog circuits.

As mentioned in chapter 2, the process of developing a SoC model begins by translating a circuit design into an equivalent system-level model, generating the logic schematic of the complete digital components of the system then creating a VHDL and/or netlist equivalent of the system.

Subsection 3.5.1 Introduction to SoC Models of Biosensors and the OBIST Method

Translating VHDL system-level models into SystemC based equivalents is a relatively simple task using VHDL2SYSTEMC software. However, performing the same operation on analog circuits is not as straightforward. For analog SystemC based modeling an understanding of the characteristic equations that define the circuit is essential. These equations are essential to the development of the "process" block of SystemC based models. In the following subsection the SoC models developed and discussed in this dissertation are included. These are the VLSI adaptation of a CHEMFET, a simulated macromolecular sensor, and the oscillation-based built-in self-test. The process of transforming analytical models of analog and digital circuits into SoC models is discussed in detail.

Subsection 3.5.2 SoC Model of a Biosensor

Analog models can be developed in SystemC through the use of floating-point representations and the declaration of appropriate device behavior. The first model developed in this dissertation is for a VLSI adaptation of the CHEMFET. As discussed previously, varying the input voltage on the voltage-controlled transistor (Vin) allows for controllability in current flowing through both stages of the sensor network. This controllability allows us to determine the drain current in the second stage whose K value is the dielectric constant of the fluid under test. This information can be useful in detecting specific fluid properties for the identification of specific substances. A Spice simulation (figure 3.15) is run on the device to show the

impact of changing the KP parameter values of the fluid inside the test transistor, shown in the biosensor diagram. The KP parameter in Spice is defined as:

$$K_p = \frac{\varepsilon_{ox} \times \mu_n}{t_{ox}}, \quad (3.60)$$

The normal value for the KP parameter of a mnmosis, 1.6 micron technology device, is KP = 5.048 e-05. Increasing the "K parameter" value of the transistor, results in an increase in the input voltage necessary to balance the biosensor stages.

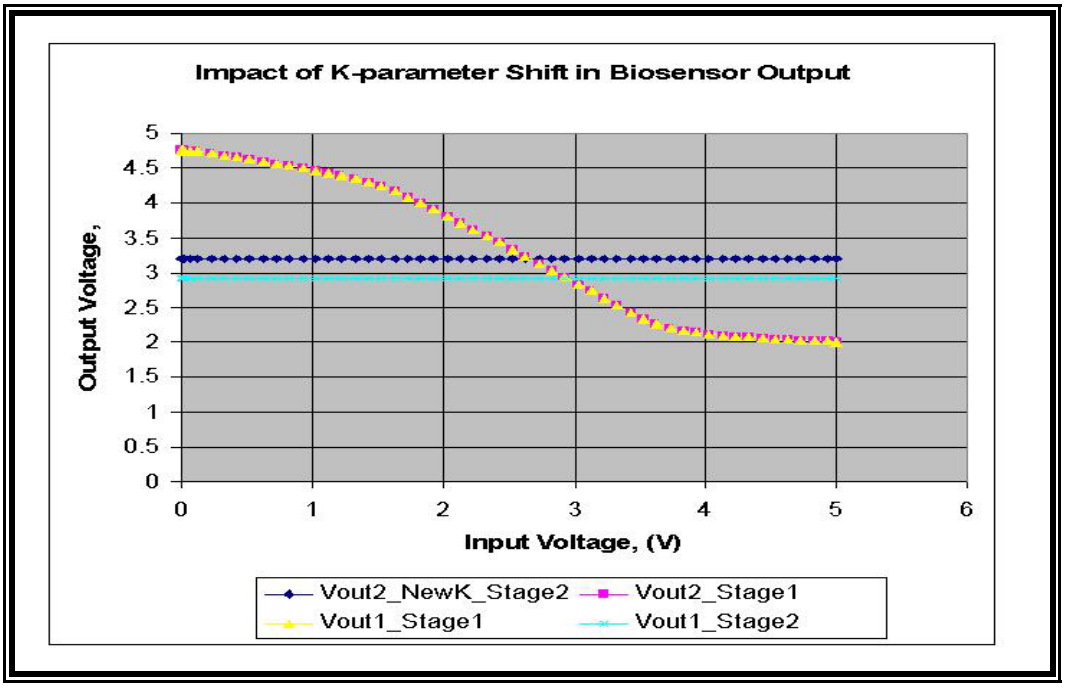


Figure 3.15 Spice Simulation Results

Decreasing the KP parameter, results in a decrease in the input voltage necessary to create a balance in the equation. The KP parameter in this experiment

was decreased to: 2.5284 e-05. As shown by the output simulation in figure 3.15, below. This figure was originally introduced in figure 3.6.

A block-based equivalent of this circuit is shown in figure 3.16. The block diagram shown is a sample system level view of the biosensor. With the relationship between

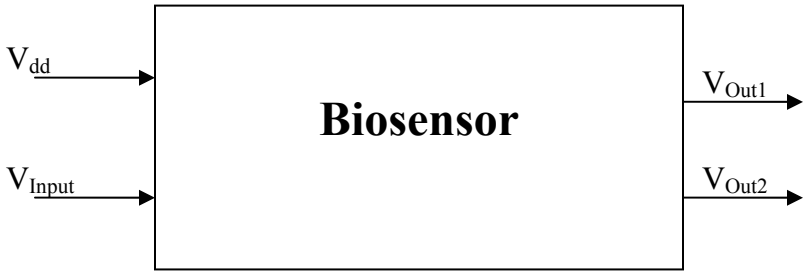


Figure 3.16 Block Based Equivalent Biosensor.

the input parameters and output parameters established, the SystemC implementation of a SoC process model for the biosensor requires the development of an equivalent SystemC based software description of the biosensor module. The software description is shown below in figure 3.17.

As with the adder example, we define the compute process in which the relationship between V_{Out} and drain current is established. Further expansion of this model requires analyzing the $V_{Out1} = V_{Out2}$ condition. This analysis would require the incorporation of an interface to the biosensor module. The interface could write the V_{Out1} and V_{Out2} values to another module capable of subtracting the values and identifying when the difference is zero. The result of the above combination of modules establishes a sub-block hierarchical relationship between two smaller

modules in the creation of an intelligent biosensor module. The block-based model of the biosensor SoC module is shown in the following figure.

Similar modules can be constructed for the gateless field effect transistor that operates as a macromolecular sensor. The SoC model implementation of this device is found in subsection 3.4.3 below.

SC_MODULE(biosensor) {
sc_in <int> V_{set4};
sc_out <int> V_{out1};
sc_out <int> V_{out2};
sc_out <int> I_{D2};
void compute() {

$$V_{OUT1} = \sqrt{\frac{K_2}{K_4}} V_{TR4}\left(V_{DD} - |V_{TR2}|\right)$$

$$V_{OUT2} = V_{DD} - |V_{TR1}| - \sqrt{\frac{K_3}{K_1}}\left(V_{IN} - V_{TR3}\right)$$

$$I_{D2} = \frac{\mu_{ox} K_{ox} \varepsilon_{ox}}{t_{ox}} \frac{W}{L}\left(V_G - V_T\right)^2$$

}
SC_CTOR(biosensor) {
SC_METHOD(compute);
sensitive << V_{set4} ;
}
};

Figure 3.17 Software Equivalent SoC Model of Biosensor

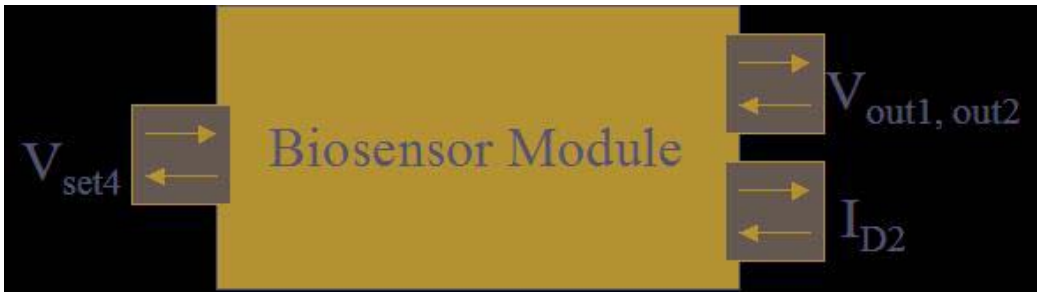


Figure 3.18 SoC Block-Based Model of Biosensor

Subsection 3.5.3 SoC Model of a Macromolecule Sensor

The depletion mode field effect transistor can be evaluated using Spice simulation to establish proof of concept for device sensitivity in the presence of unique fluids under test. One such device is shown below, in figure 3.19. This equivalent SPICE model was placed in an array of 6 devices. The drain currents for each of the transistors (M10, M11, M12, M13, M14, and M15) appear in figure 3.20. Each of the depletion mode transistors was assigned a unique KP parameter value to emulate the presence of fluids over the device.

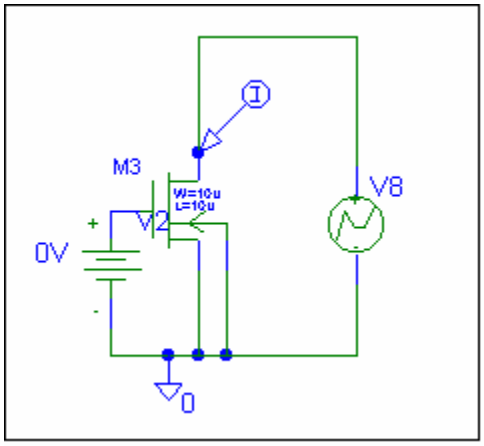


Figure 3.19 Equivalent Spice model of depletion mode FET with PWL bias voltage, V_B.

The Spice KP parameter is described by equation 3.47. The KP parameter values that were assigned to the transistors were: 4.048 e-05, 3.048 e-05, 2.048 e-05, 1.048 e-05, 0.048 e-05, and 0.024 e-05, respectively. The normal KP parameter for the device is 5.048 e-05. In figure 3.21, the drain current response for this value is compared against the other KP values as shown in figure 3.20.

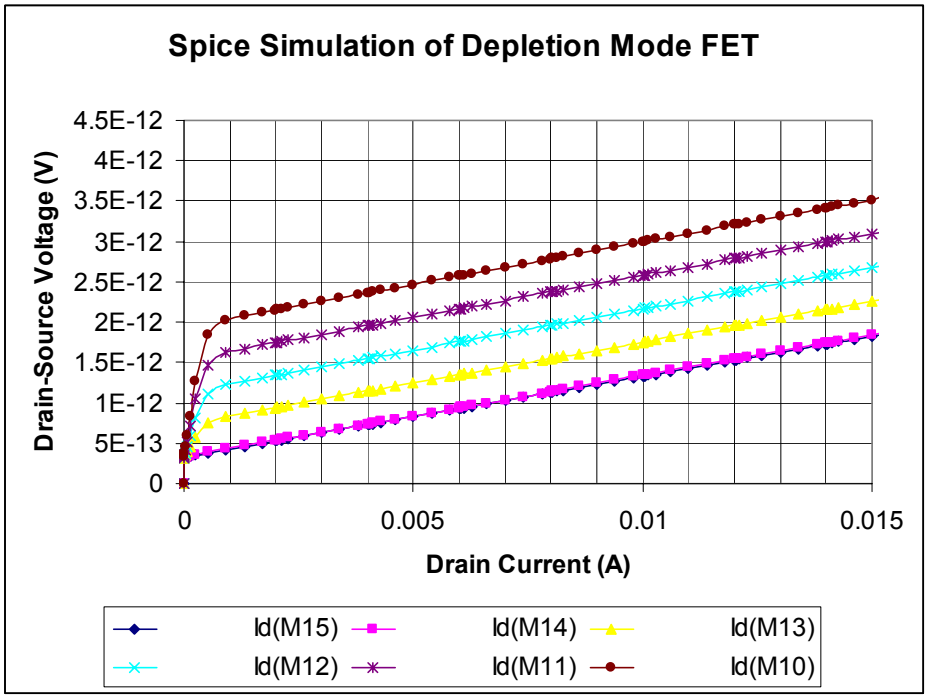


Figure 3.20 Output Spice Results comparing different K values for depletion mode FET.

In figure 3.21, we see that the drain current response to source-drain voltage, V_{DS}, is significantly greater for a KP parameter value of 5.048e-05 than for the remaining KP parameter values. The response of the depletion mode field effect transistor when KP = 5.048e-05 approaches 16 μA, while the remaining devices in the array approach 4 pA. Figure 3.20 shows the response of the sensors with KP

values less than or equal to 4.024e-05 approach zero. Upon further inspection in figure 3.20, we see these values approach ranges of 1.5 pA to 4 pA. This figure shows the sensitivity of the depletion mode field effect transistor to varying K values. For each drain current plotted from top to bottom the KP parameter value is decreased by 1.0e-05. The result is an output drain current response that decreases by 0.5 pA for drops in KP values of 10 μA.

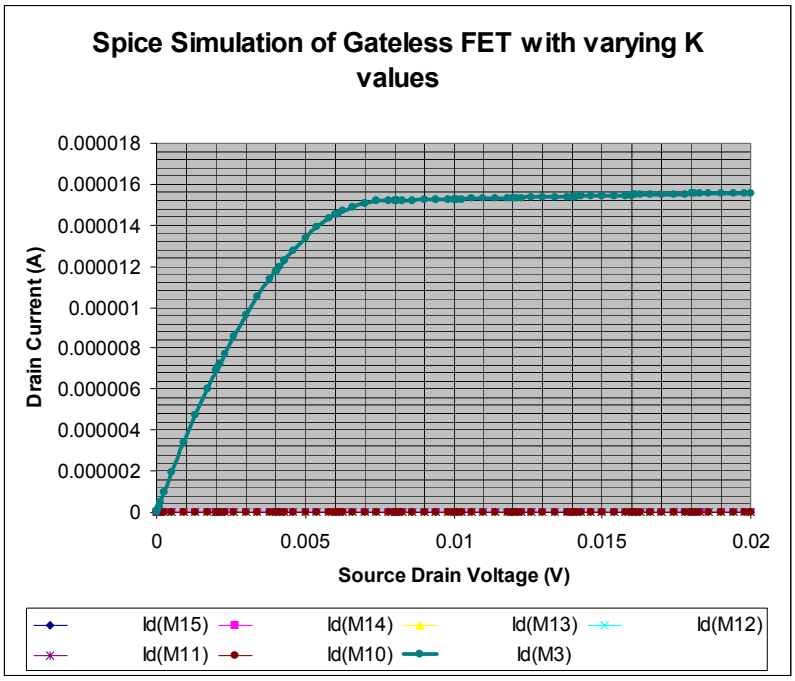


Figure 3.21 Drain current response of normal K value for depletion mode FET.

The block-based equivalent of the macromolecular sensor is shown in figure 3.22 below. This diagram is a sample system level view of the macromolecular sensor containing an interface port (for frequency mapping) to provide the module with information that relates V_{SD} input values to OBIST oscillation frequency outputs.

The SystemC implementation of this macromolecular system block is shown in figure 3.23. Included in this implementation is a module that contains information values for the parameters found in the process, "compute()", equations. An interface accesses this module and reads the data. The module is found in figure 3.24.

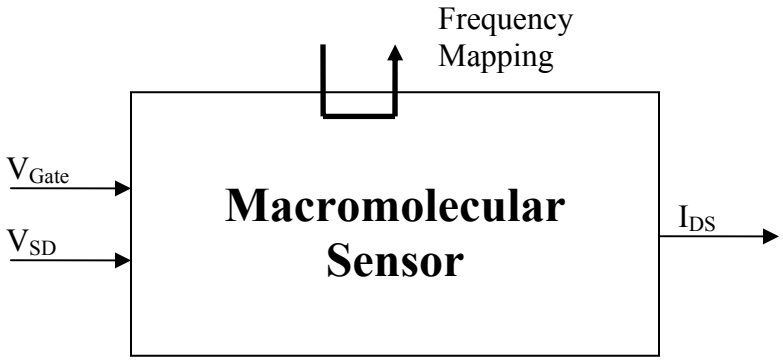


Figure 3.22 Block-based equivalent model of macromolecular sensor.

SC_MODULE(macromolecular) {

sc_in <int> V_{SD};
sc_in <int> V_{Gate};
sc_out <int> I_{DS};

void compute() {

$$I_{DS} = \frac{1}{2}\mu C_{ins}\frac{W}{L}\left(V_{th}^2 - V_{gs}^2\right);$$

}

SC_CTOR(macromolecular) {
SC_METHOD(compute);
sensitive << I_{DS} ;
}

};

Figure 3.23 Block-based equivalent model of macromolecular sensor.

```
SC_MODULE(drain_current)
{
sc_out<int> W, L;
sc_out<float> Cins, Vth, Vgs;

SC_CTOR(drain_current)
{
SC_THREAD(process);
}
void process()
{
W = 30e-6;
L = 6e-6;
Cins=0.4; // in pF/cm
Vth= -0.858V;
Vgs = -0.4V;

}

}
```

Figure 3.24 Drain Current Parameter Module for Macromolecular Sensor

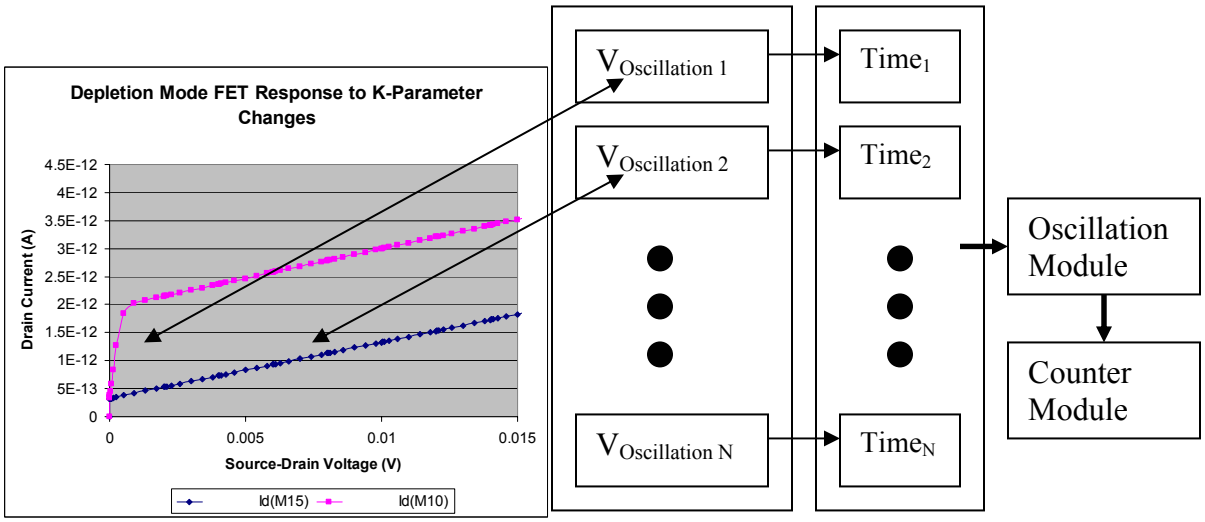


Figure 3.25 Voltage mapping from target drain current. In this sample voltage mapping, the target drain current is 1pA. This corresponds to a voltage of 64 μV for a depletion mode FET with a KP value of 4.048e-05 and 7.5 mV for a depletion mode FET with a KP value of 0.024e-05.

In terms of Spice simulation using the oscillation based BIST method which relies on the voltage controlled oscillator would prove ineffective in evaluating faults for the macromolecular sensor, however, fault evaluation of the device using the SoC model implementation of the OBIST method is plausible by mapping the expected drain current output to the input source-drain voltage, $V_{SD,}$ applied to the system. This voltage can then be fed into the OBIST module for fault evaluation and detection. An example of this mapping is provided above in figure 3.25. The information necessary to produce and SoC model implementation of this mapping, is stored in another module and accessed by read statements through the SoC interfaces described in chapter 2. The results of this method are shown in chapter 4.

For the mapping concept depicted in figure 3.25, we consider a target drain current of 0.5 pA. When the KP parameter is 0.024e-05, the target drain current corresponds to an applied source-drain voltage of 7.5 mV, shown above as the lowest curve in figure 3.20. When the KP parameter is 4.048e-05, the target drain current corresponds to an applied source-drain voltage of nearly zero, 64 μV. As these voltages are extremely small, we consider the theoretical argument for use of the OBIST method in the fault determination of macromolecular sensors. To perform the mapping, the applied source-drain voltages are directed into the voltage controlled oscillator to produce the desired oscillation output voltage. For the purpose of creating a SystemC based SoC model, a module can be created containing expected frequency and/or time response information for the VCO as it relates to specific input voltage values. Such a module would be accessible via an interface. The source-drain voltage information is read into the module with the corresponding

time/frequency relationship being extracted from the module. The output time/frequency value can then be fed into an oscillation module that creates the desired digital clock-like signal based on the timing information that corresponds to the source-drain voltage. This signal is then fed into the counter to complete fault evaluation.

Subsection 3.5.4 SoC Model of the Oscillation Built-In Self-Test

Implementation of the Oscillation Built-In Self-Test as an SoC model is similarly executed. Two sub-modules are created to produce the OBIST module. The first is a voltage controlled oscillator/ level crossing detector module. A block-based equivalent of this module is presented in figure 3.26 below.

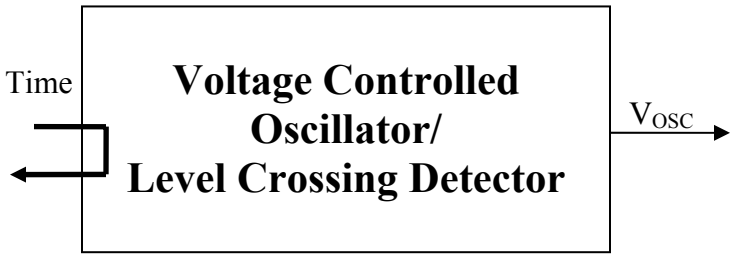


Figure 3.26 Block-Based VCO-LCD Model

The development of the VCO-LCD model is not limited to the characteristic equation method shown, as the figure 3.25 mapping method is an effective means of generating clock-like digital outputs in that it produces the required fault-sensitivity results. In figure 3.27 below, the SystemC based system-on-chip model of the VCO-LCD is presented.

```
SC_MODULE(VCOLCD) {

    sc_in<int> Time;
sc_signal>sc_unit<length>> vosc_out;

    void vosc_process()
        {
for (int j = 0; j < 20; j++)
        {
vosc_out.write(1);
 sc_cyle(TimeN);
vosc_out.write(0);
sc_cycle(TimeN);
        }

    return 0;

    }
```

Figure 3.27 SystemC based SoC Model of VCO-LCD

The second essential module for the OBIST method is a counter. The counter is used to perform on-chip fault analysis by summing up the number of zero-crossings that occur as the VCO-LCD device oscillates. A 4-bit counter is used. The block-based equivalent of the counter is shown in figure 3.28.

Figure 3.28 Block-based implementation of Counter.

The corresponding SystemC based SoC model of the VCO-LCD with counter modules is presented in figures 3.29. The SystemC implementation of the 4-bit counter appears in figure 3.30.

```
#include "systemc.h"
#include "cnt.h"
#include "cnt_display.h"

int sc_main(int ac, char *av[])
{
sc_signal<bool> reset, clock;
sc_signal<sc_uint<length> > cnt_out;

cnt cnt1("cnt1");
cnt1.reset(reset);
cnt1.clock(clock);

cnt1.cnt_out(cnt_out);
cnt_display cnt_display1("cnt_display");
cnt_display1.clock(clock);
cnt_display1.cnt_out(cnt_out);

sc_initialize();

sc_trace_file *tf = sc_create_vcd_trace_file("correct4Xfault");
sc_trace(tf, reset, "reset");
sc_trace(tf, clock, "Fault_with_4X_Error");
sc_trace(tf, cnt_out, "cnt_out");

reset.write(0);
clock.write(0);
sc_cycle(28);
reset.write(1);
sc_cycle(28);

for (int j=0; j<20; j++)
{
clock.write(1);
sc_cycle(28);
clock.write(0);
sc_cycle(28);
}

sc_close_vcd_trace_file(tf);
return 0;

}
```

Figure 3.29 SystemC-based model of VCO-LCD method.

```
struct cnt_display : sc_module

    sc_in_vosc      Vosc;
sc_in<sc_uint<length> > cnt_out;
    sc_uint<length> cnt_tmp;

    void display_process();

    SC_CTOR(cnt_display)
                {
SC_METHOD(display_process);
    Sensitive << Vosc.pos();
                }
```

Figure 3.30 SystemC-based Implementation of a 4-bit Counter

Section 3.6 Summary

In chapter 2 we observe that while much work has been conducted in the area of digital system-on-chip design, a number of open problems remain in the semiconductor industry. The open problems that existed in the SoC industry prior to this dissertation include:

1. The lag in analog intellectual property re-use as compared with digital intellectual property.
2. The large cost in chip overhead for the oscillation test strategy on-chip built-in self-test scheme.
3. The propagation of circuit under test faults in the development of oscillating outputs due to feedback networks used in the oscillation test strategy.

4. The limited development of analog system-on-chip models for pre-fabrication simulation and testing.
5. The need for inexpensive, IC based, medical devices capable of distinguishing fluid properties including but not limited to: DNA, antibody antigens, proteins and dielectric constant.

In short development of analog SoC devices has historically lagged far behind advances made to its digital counterparts. In addition, the area of development of on-chip self tests requires further study due to large chip area overhead and the propagation of oscillating faults in feedback related oscillation test strategies. Solutions to these problems are provided in this chapter using a fluid analyzer system-on-a-chip device that is developed in this dissertation.

Specific details about the components of the fluid analyzer are discussed in section 3.2. Here, the focus is on the interaction between devices contained in an array of biosensors, smart signal processing elements, built-in self-test, and parameter adjustments instituted when faults are detected.

Each of these system sub-blocks is evaluated extensively in section 3.3, "Analysis and design of biosensors for fluid testing" and section 3.4, "Oscillation based built-in self-test (OBIST)". The OBIST method developed in this work is an improvement upon the oscillation test strategy as the total area coverage of the OBIST method is significantly smaller than that of the OTS, due to the use of diode-connected transistors in lieu of resistors and the development of a zero crossing

detector whose performance mimics the performance of the level crossing detector used for the oscillation test strategy.

Continuing to aide in the resolving the lag in analog intellectual property involves development of analog SoC models for each of the devices fabricated. Included in this dissertation are models of built-in self-test components, a gateless field effect transistor, and a macromolecular sensor. A novel mapping method of performing oscillation based fault tests on the macromolecular sensor's drain-current output is discussed in section 3.5. The models developed in this dissertation are based on the SystemC design structure for systems-on-chip.

Chapter 4 Results

Section 4.1 Overview

In this chapter, an application of the proposed techniques discussed in Chapter 3 is shown in simulation and through experimental analysis. Simulation is performed on each of the key components of the proposed testbench-on-a-chip. The simulated components include: a biosensor circuit, a depletion mode MOS transistor, a voltage controlled oscillator, the developed zero crossing detector, an enhanced level crossing detector BIST system, and a zero-crossing detector BIST system. The devices that are evaluated through experimental analysis include the VLSI implementation of a chemical field effect transistor and the gateless field effect transistor macromolecular sensor.

This chapter is organized as follows. In section 4.2, a summary of the simulation and experimental results of each biosensor is presented. Section 4.3, shows the simulated results of each of the components of the built-in self test and response of the BIST methods to various parametric and catastrophic faults that exist within the circuit under test. For these simulations, the VLSI implementation of the Chemical Field Effect Transistor is evaluated as the test circuit. Section 4.4 presents the evaluations of the system-on-a-chip models developed for the key components of the testbench-on-a-chip (TBOC). The outputs of the SoC models are evaluated and compared against equivalent Spice models.

Section 4.2 Simulation and Experimental Evaluation of Biosensors

VLSI IMPLEMENTATION OF A CHEMICAL FIELD EFFECT TRANSISTOR

A multi-function smart sensor system is used to identify the properties of a fluid. The layout of the basic sensor is shown in figure ( ) below in which the fluid sensing transistor is constructed from four parallel diode connected transistors. This layout was obtained using the MAGIC layout program. As the latter can be used with different lambda values to allow for different technology sizes, this layout can be used for different technologies and thus should be suitable for fabrications presently supported by MOSIS.

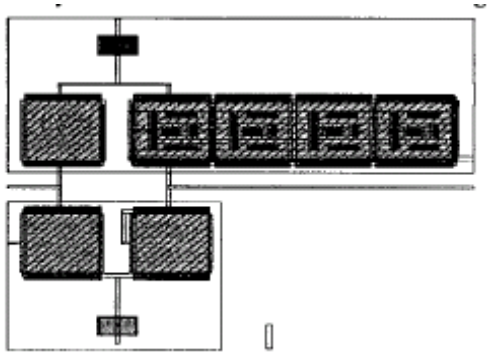


Figure 4.1 Biosensor Layout

Associated with this figure, is the figure that follows, where a cross section is shown cut through the upper two transistors in the location seen on the upper half of the figure. This cross section shows that the material over the holes in the gate is completely cut away so that an "etch" of the silicon dioxide can proceed to cut horizontally under the

remaining portions of the gate. The two layers of metal can also be seen as adding mechanical support to maintain the cantilevered portions of the gate remaining after the silicon dioxide etch.

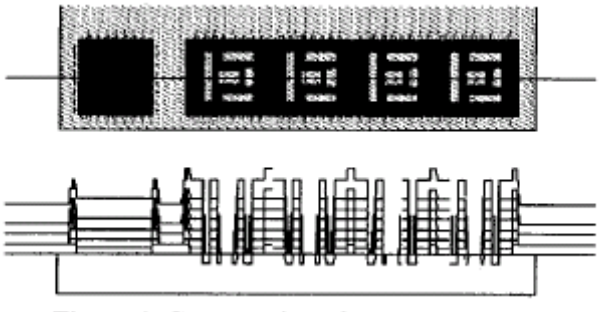


Figure 4.2 Cross-Section of upper transistors in VLSI adaptation of ChemFET.

A Spice extraction was obtained from the layout. On incorporating the BiCMOS transistor models, the extracted circuit file was run in PSpice with the result for the output difference voltage versus Vset shown in figure ( ) below. As can be seen there, adjustment can be made over a wide range. Thus it is seen that a sensor sensitive to the dielectric constant of a fluid over an 11 to 1 range of dielectric constant most likely can be incorporated into a multi-sensor chip using standard analog VLSI-MEMS processing one can use the bridge for anomalies in a fluid by obtaining Vset for the normal situation and then comparing with Vset found for the anomalous situation.

The biosensor circuitry described was fabricated on a multi-technology testbench on a chip, using the MOSIS foundation's AMI 1.6 technology. Post-processing in the form of an HF etch was performed on the biosensor. The device was evaluated after a series of

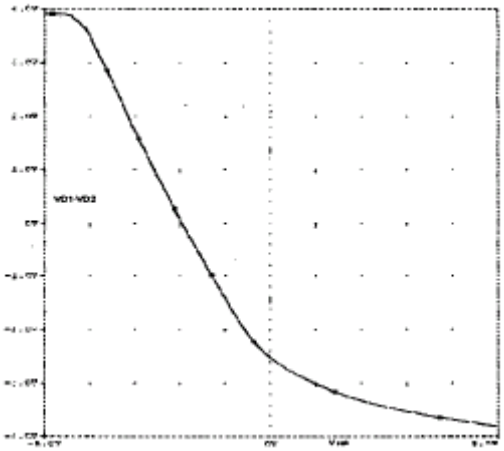


Figure 4.3 Extracted Circuit Output Voltage versus Vset.

incremental etch steps to determine the maximum amount of time necessary to fully etch out the gate dielectric. This step is important as fluids applied to the surface of the biosensor device serve as the dielectric over the gate, making the biosensor a dielectric measurement system. The second stage output voltage of the device was measured against input voltage values ranging from 0V – 6V. The analysis, shown in the following figure, provides output voltage results for the following etch times 0 seconds, 20 seconds, 80 seconds, and 200 seconds. The etchant was a 1:10 buffered HF solution in which the ratio of hydrofluoric acid (HF) to buffer was 1:10. After 18 minutes of etching and the application of the 6V in the presence of water, the biosensor collapses while the remaining circuitry on the testbench continues to perform as expected.

A 15 minute etch was performed on the circuit whose results are reflected in the following figure. This figure shows the ChemFET's response to air, Tris/EDTA buffer, and water after voltages ranging from 0V – 6V are applied in 0.5V increments. The biosensor circuit is thus shown to produce a unique output response for each of the fluids under test.

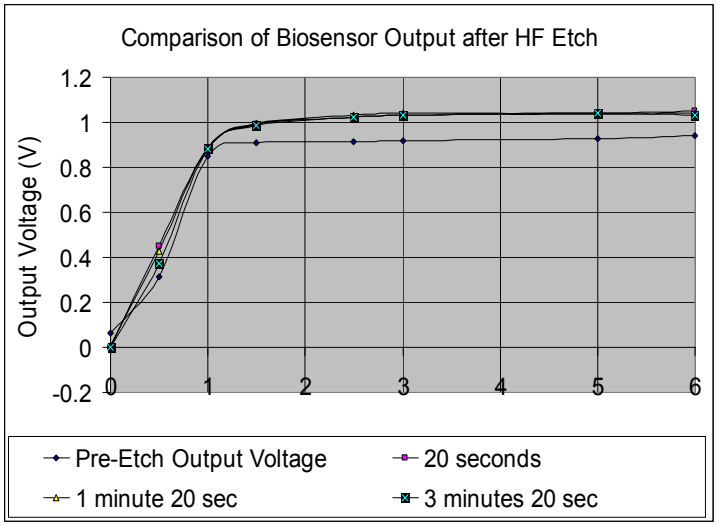


Figure 4.4 Output Voltage versus Input Voltage for Biosensor versus time in HF solution

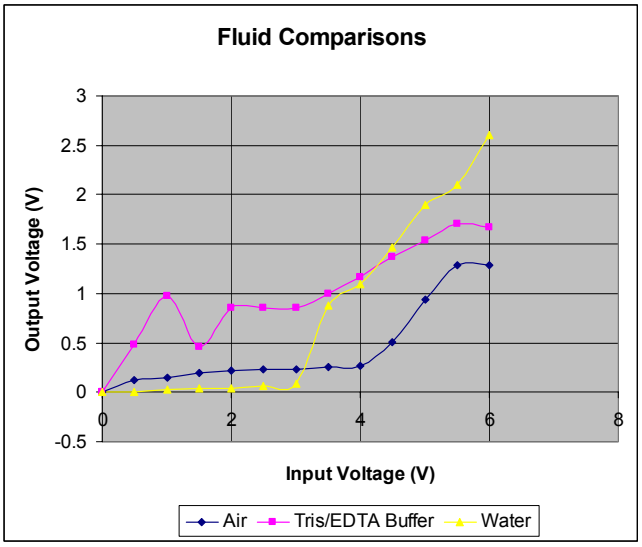


Figure 4.5 Biosensor Output Voltage versus Voltage Controlled Transistor Input Voltage for various fluids under test.

Experimental Data for Macromolecular Sensor

An array of SAM-treated gateless FETs has been implemented. The basic idea of the design is shown in figure ( ) below. These devices may be as small as microns on a side (or smaller) this allows for the ability to pack large numbers together for high-density array sensors, or for differential sampling and voting techniques. In this configuration 12 devices have been developed and packaged per chip. These chips are packaged in two ways. The majority of the packing involves the use of a standalone chip array of 12 sensors placed in a 28-pin Dual-in-Line Ceramic Package (DIP), while some chips are dual-packaged (2 chips per DIP). The purpose of the dual-packaged chips is to allow for the performance of differential sensing. Each device has a separate and independent drain contact. There is one gated test structure adjacent to every dozen

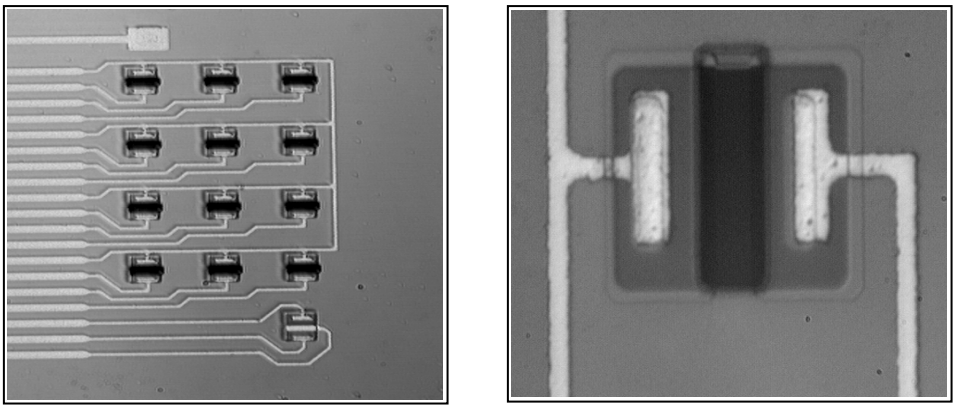


Figure 4.6 Fabricated macromolecular sensors. The figure on the left is an array of 12 fabricated macromolecule sensors with gate electrode and body contact. The figure on the right shows a single macromolecule sensor where the active area is the dark rectangle across the device middle.

sensors. Finally, we include a silver reference electrode, external to the chips. When place in a liquid solution the reference electrode acts as the gate for the depletion mode

transistors (macromolecular sensors). Once fabricated, diced, packaged, and cleaned, the devices undergo the antibody attachment chemistry discussed in chapter 3. The figure below shows the array of macromolecule sensors that were fabricated and tested in this work.

Typical current voltage (IV) traces are shown in figure ( ) below. These curves were obtained after the sensor was soaked in control solution (no DNA), a solution containing a mismatched DNA, and a solution containing target DNA. Attachment times were less than a minute (time to saturate).

The traces shown were taken over a time period of 30 seconds under computer control. These traces indicate low-frequency noise was small. Over time, the plots did exhibit some drift probably due to ionic charging of the gate insulator. For example, if the drain is set at 0.5V, the drain current will drift on the order of 20% over a period of 45 minutes. In addition, there was a similar variation of response ongoing from device to device at time zero. This is due to minimal passivation above the active channel and the lack of a gate above the active channel to prevent ion impingement. Please note that these results come from "raw data." No signal processing has been done. In spite of this, the FET traces are stable for these devices over short periods of time.

The degree of variability (sample to sample and over time) did necessitate a statistical treatment of the data [22-SST]. The sign test was used to ascertain the confidence level of detecting the targeted DNA. In the sign test, the "null hypothesis" is confidence level of detecting the targeted DNA. In the sign test, the "null hypothesis" is that a given sample lot exposed to the analyte will be randomly distributed about a mean over all samples (targets and controls). This would indicate an insensitive detector. The

statistical marker used here was the parameter-extracted insulator capacitance. The preponderance of analyte-exposed samples is above this mean, suggesting that we have achieved detection. By assuming a Poisson distribution of sampled events, we can assume a "confidence" level to the violation of the null hypothesis. For the analysis performed below, "n" is the total number of samples employed in the analysis.

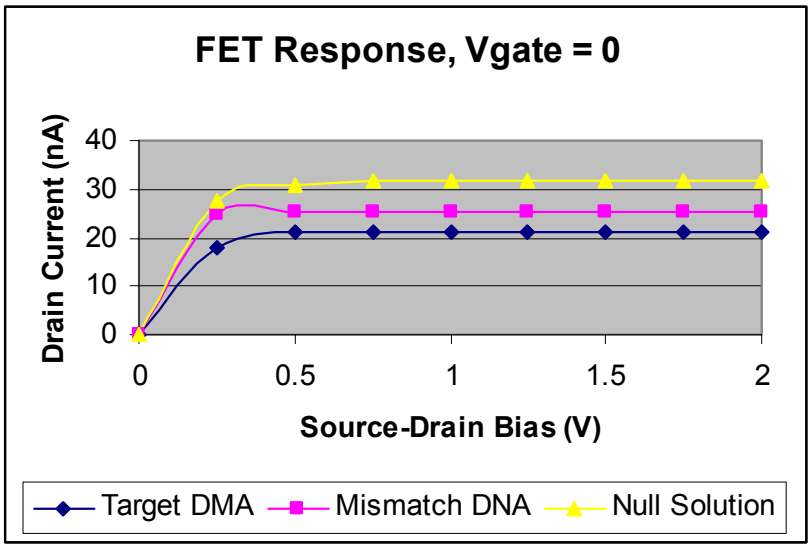


Figure 4.7 Current-voltage response curves for devices exposed to mismatched DNA, matched DNA and buffer. There was little noise in the measurement in all cases. The mismatched DNA showed slight response (which proved not to be significant). The matched DNA showed clear response. The drain-source current is on the y-axis. The source-drain bias is on the x-axis.

The overall experimental results are summarized as follows:

- We detected 1 fM 15-mer single-strand DNA with a confidence level of 92%, as ascertained by the sign test described above (n=14). Sample volume was 30 μL.
- We observed transient transistor response upon addition of single-strand DNA solution with time constant of 4 x (not device limited).

- We detected 1 mg/ml streptavidin with 95% confidence (n=17) in 30 µL sample solutions.
- The same analyses were performed using transistor threshold as the statistical parameter. Using this parameter, the null hypothesis could not be eliminated with roughly 50% confidence. Thus, the device did not respond to surface charging induced by the analyte attachment.

Typical voltage soak and current voltage (IV) traces are shown in figures 4.8 and 4.9 below. The voltage soak curves are generated by applying a steady voltage across the sensors and recording the resulting current characteristics. A fluid flows continuously over the sensors while measurements are taken. Prior to the first injection, a PBS buffer flows over the devices. The first injection is a steady flow of 1 ng/ml of Goat Antimouse IgG. The second injection is a tween rinse step whose purpose is to remove non-specific absorption of the ng/ml Goat Antimouse IgG. The last injection is of buffer. This buffer flows over the system for ten to fifteen minutes to insure removal of the tween.

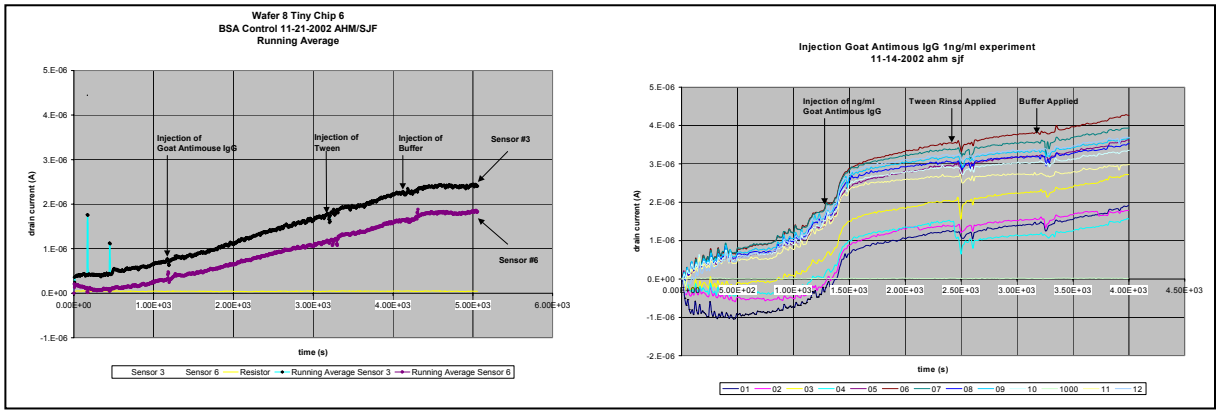


Figure 4.8 Voltage Soak Results. The graph on the left is the BSA control. The graph on the right is the antibody match.

The sensors appear to have a distinct response with the 1 ng/ml injection of IgG. The subsequent injections of tween and buffer appear to have no affect on the devices. The ng/ml injection of IgG is said to saturate the devices' ability to specifically bind the Goat Antimouse IgG. The response indicates sensitivity of the sensors to antibody antigen. Earlier experiments show device sensitivity to the presence of DNA and

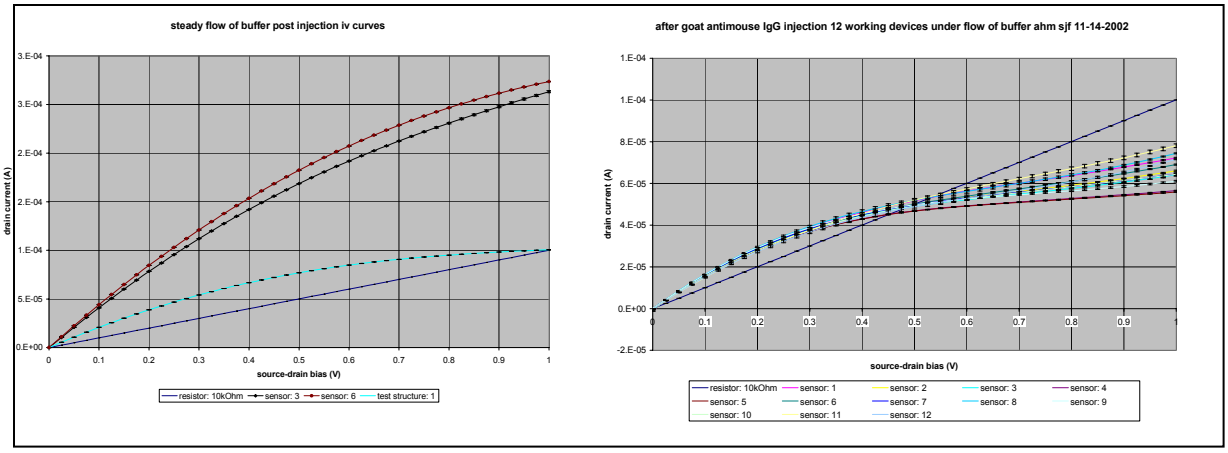


Figure 4.9 Macromolecular sensor results IV Curves. The graph on the left is the BSA control. The graph on the right is the antibody "match".

Section 4.3 Built-In Self-Test Methods

In this section the sensitivity of 3 configurations of built-in self-test is evaluated against parametric and catastrophic faults that are deliberately placed within the VLSI implementation of the ChemFET, henceforth referred to as the biosensor. The parametric fault is a 10% error in projected W/L ratio. These faults are forced to appear in the simulated circuit in the following form: (bullet). The catastrophic faults evaluated include: a 75% error in projected W/L ratio and a shorted transistor. These faults appear

within each of the "4" main transistors of the biosensor circuit. As such, the device response is evaluated for a total of 12 fault configurations.

For the purpose of comparison, a fault-free biosensor is evaluated with the Arabi-Level Crossing Detector BIST method (aLCD-BIST), the enhanced-Level Crossing Detector BIST method (eLCD-BIST) and the zero-crossing detector BIST method (ZCD-BIST). The output of the biosensor is fed into the input of each of the above BIST methods. The fault-free biosensor serves as the control for this simulation experiment. A statistical analyzer or counter can be used to evaluate the output discrepancies that exist between a fault-free biosensor and a parametric or catastrophic fault biosensor. This evaluation is effective for determining the utility of each of the three BIST procedures developed in this work. The second component of merit for such a system is that it facilitates development of a completely on-chip built-in self-test scheme. In this work, statistical analysis is used to test the effectiveness of the key BIST components developed and evaluated.

As the biosensor circuit acts as a dielectric measurement device in which a whetstone bridge-type configuration is the basis for its design, the input voltage for the BIST module is the biosensor output voltage value generated when the output stages of the device are balanced. For example, when Vout1 = Vout2, the voltage inputted into the BIST system is Vout2. For each example, the voltage that drives the input for the biosensor is chosen to be the voltage that crates a balance in the output stages.

This work compares the effectiveness of multiple BIST methods, herein developed, against distinguishing the existence of parametric or catastrophic faults from normal circuit behavior.

Subsection 4.3.1 BIST SoC Model of Counter System Sensitivity to Input Signals

The evaluation of the BIST method begins by establishing proof of concept. In chapter 3, a SoC implementation of a counter is proposed to detect on-chip fluctuations in output signals. Here two oscillating clock-like input signals are generated and inserted as input into the SoC counter model. Figure 4.10 below shows the SystemC output of the implementation. The oscillating signals differ in frequency and period. For a time of 120 nanoseconds, the counter records the first SystemC.clock V1 (with a period of 20 nanoseconds), as equaling 11. For the same time, the second SystemC.clock, V7 equals 6 (6.5).

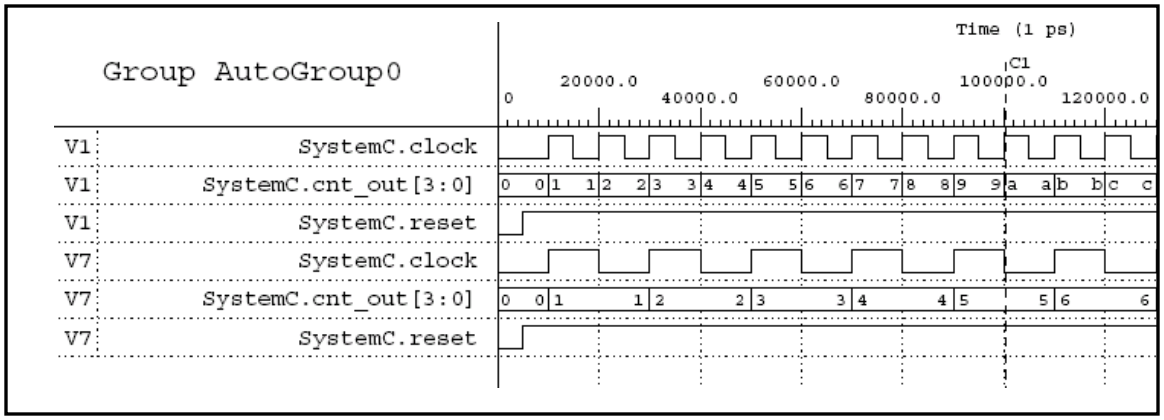


Figure 4.10 Counter Response to clock-like signals of unique periods.

In the above figure, we see that the system-on-chip implementation of a counter responds appropriately to unique clock-like inputs of different frequencies and periods. The input signal, SystemC.clock that corresponds to V1 is twice as fast as the input signal, corresponding to V7. The counter outputs for V1 and V7 are shown to be “c” and “6” respectively. For the 4-bit counter, “c” corresponds to a value of 12. As expected, the V1 signal counter output is twice that of the V7.

Subsection 4.3.2 BIST responses to simulation of the ChemFET Biosensor

In figure 4.11, we see the Spice simulation outputs of a biosensor device which acts as the sensor under test for the OBIST method developed in this dissertation. The output shown in 4.11 (a), corresponds to the biosensor output of the RHS of figure 3.4. Figure 4.11 (b) shows the output of the LHS of figure 3.4. In 4.11 (b) we see the voltage controlled oscillator output, while 4.11 (d) shows the zero crossing detector output.

Figures 4.12 through 4.26 show the individual output responses, of each of the devices in the OBIST, to faults that exist in the transistors of the biosensor circuit. For each figure, (a) corresponds to the response of the specified device to a fault in transistor M1, (b) corresponds to a fault in transistor M2, (c) corresponds to a fault in the fluid under test transistor M3, and (d) corresponds to a fault in transistor M4. Each figure shows 4 graphs. A separate figure exists for each of the device outputs in the OBIST structure. These include: biosensor stage 1 output, biosensor stage 2 output, voltage controlled oscillator output, zero crossing detector output, and level crossing detector output, respectively.

The Spice analyses correspond to applied parametric and catastrophic faults that may occur during device fabrication. The parametric fault appears as a 10% error in expected width/length ratio of the transistors in the biosensor. The first catastrophic fault shown is for width/length processing errors of 75%; while, the second catastrophic fault is for a processing error of 400%. Following the graphs is a set of tables describing each macro's sensitivity to the insertion of device faults within the biosensor. The tables show the statistical relationship between the fault-system output and the fault-free (expected) output.

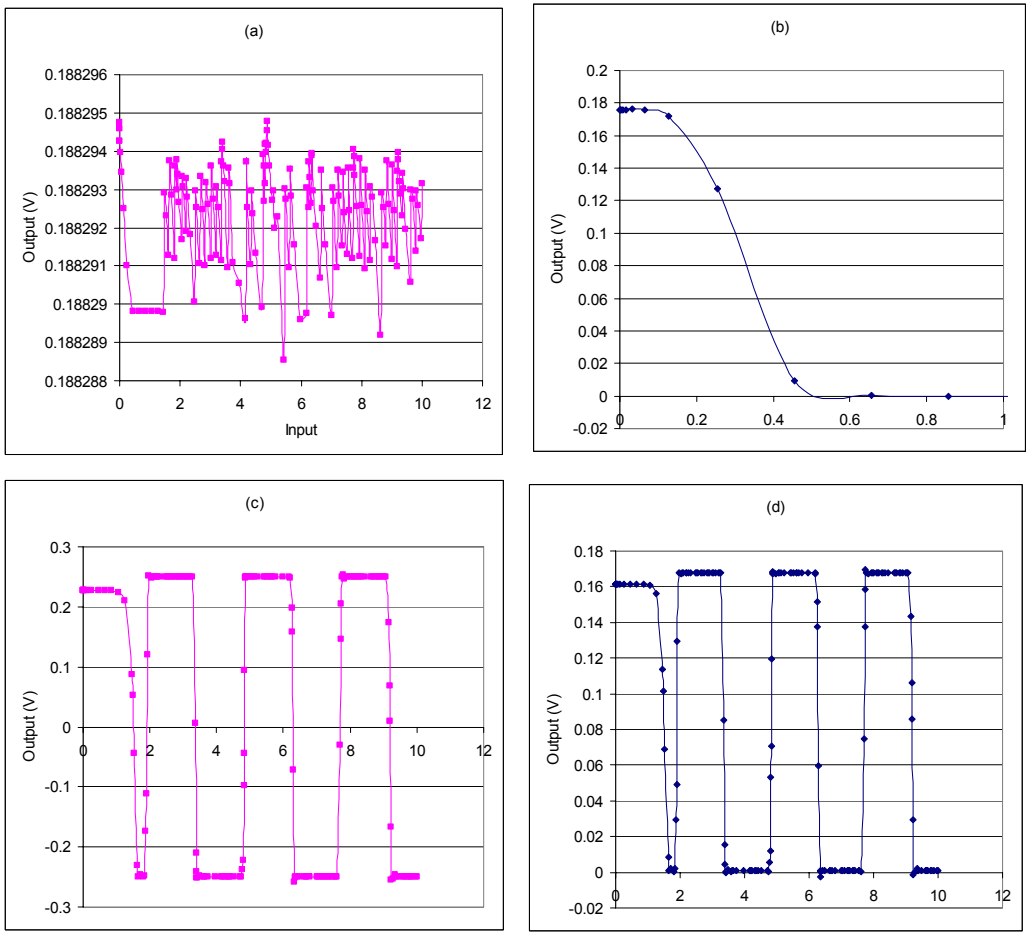


Figure 4.11 Shown are the parametric fault-free output responses of the OBIST with a normal KP parameter in use: in 4.11 (a) Biosensor Vout1, in 4.11 (b) Biosensor Bout2 in 4.11 (c) VCO, and in 4.11 (d) ZCD.

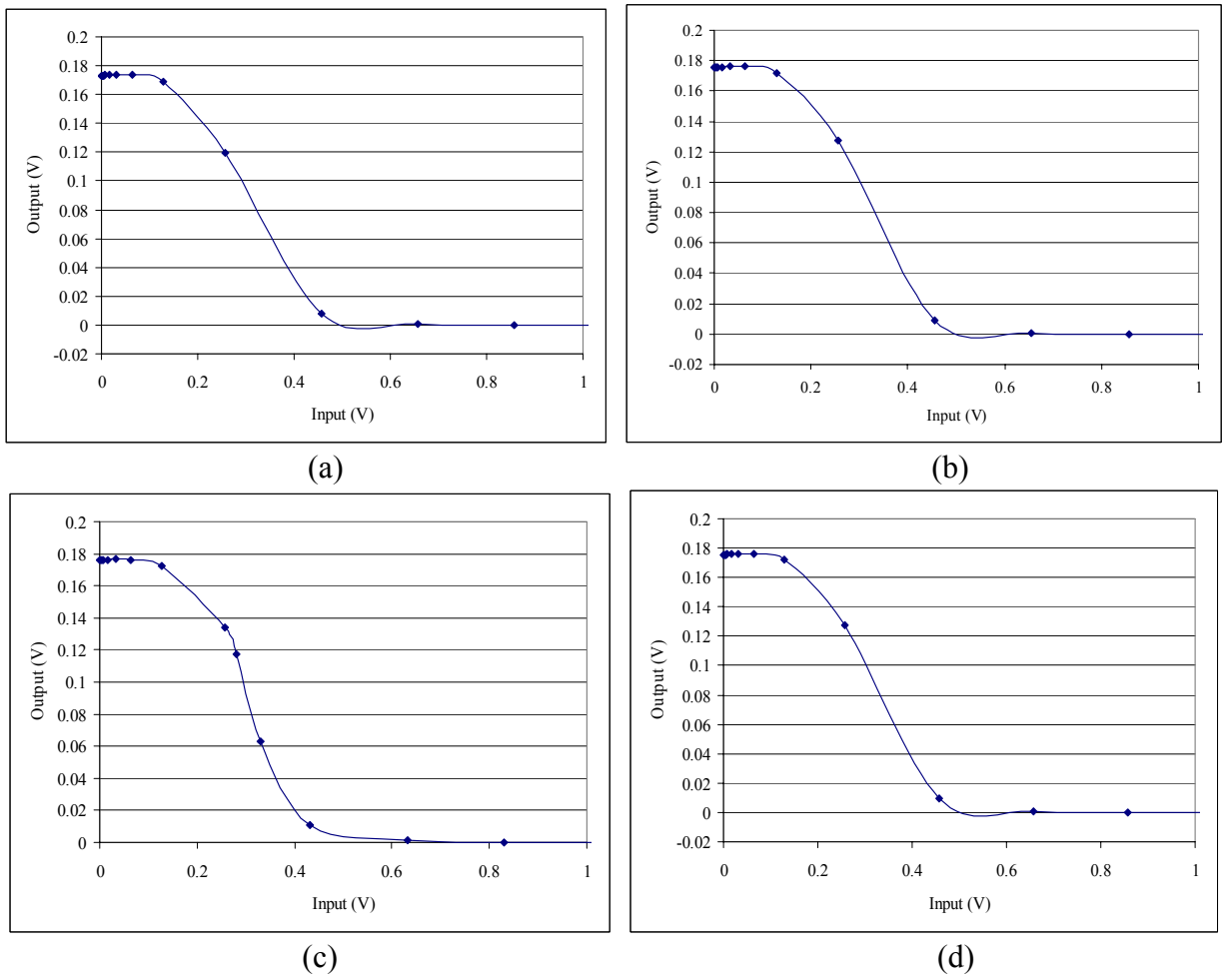


Figure 4.12 Shown are the parametric fault results on Vout2, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 10% in their respective W/L ratio. In 4.12 (a) the error is in transistor M1, in 4.12 (b), the error is in transistor M2, in 4.12 (c) the error is in transistor M3, and in 4.12 (d) the error is in transistor M4.

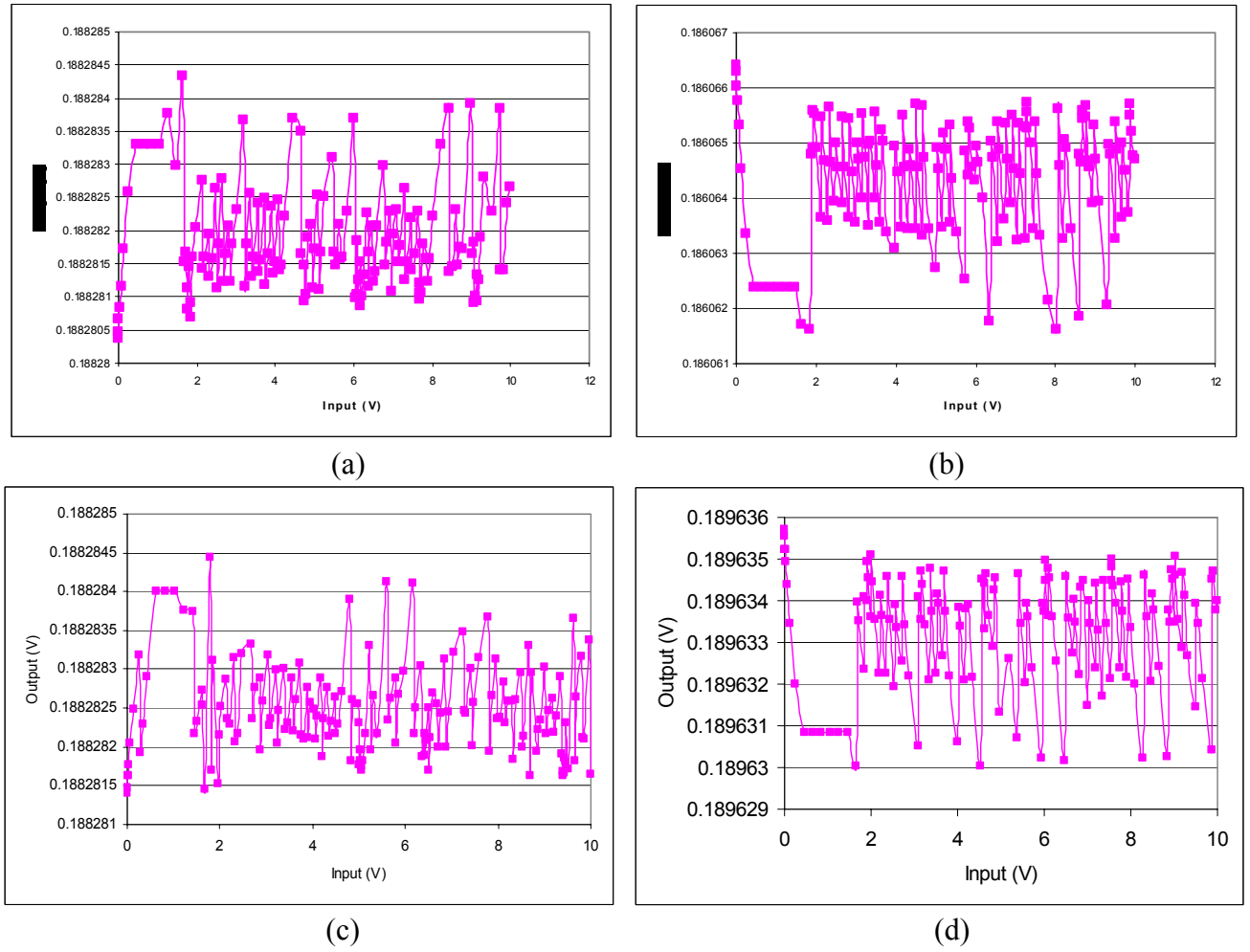


Figure 4.13 Shown are the parametric fault results on Vout1, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 10% in their respective W/L ratio. In 4.13 (a) the error is in transistor M1, in 4.13 (b), the error is in transistor M2, in 4.13 (c) the error is in transistor M3, and in 4.13 (d) the error is in transistor M4.

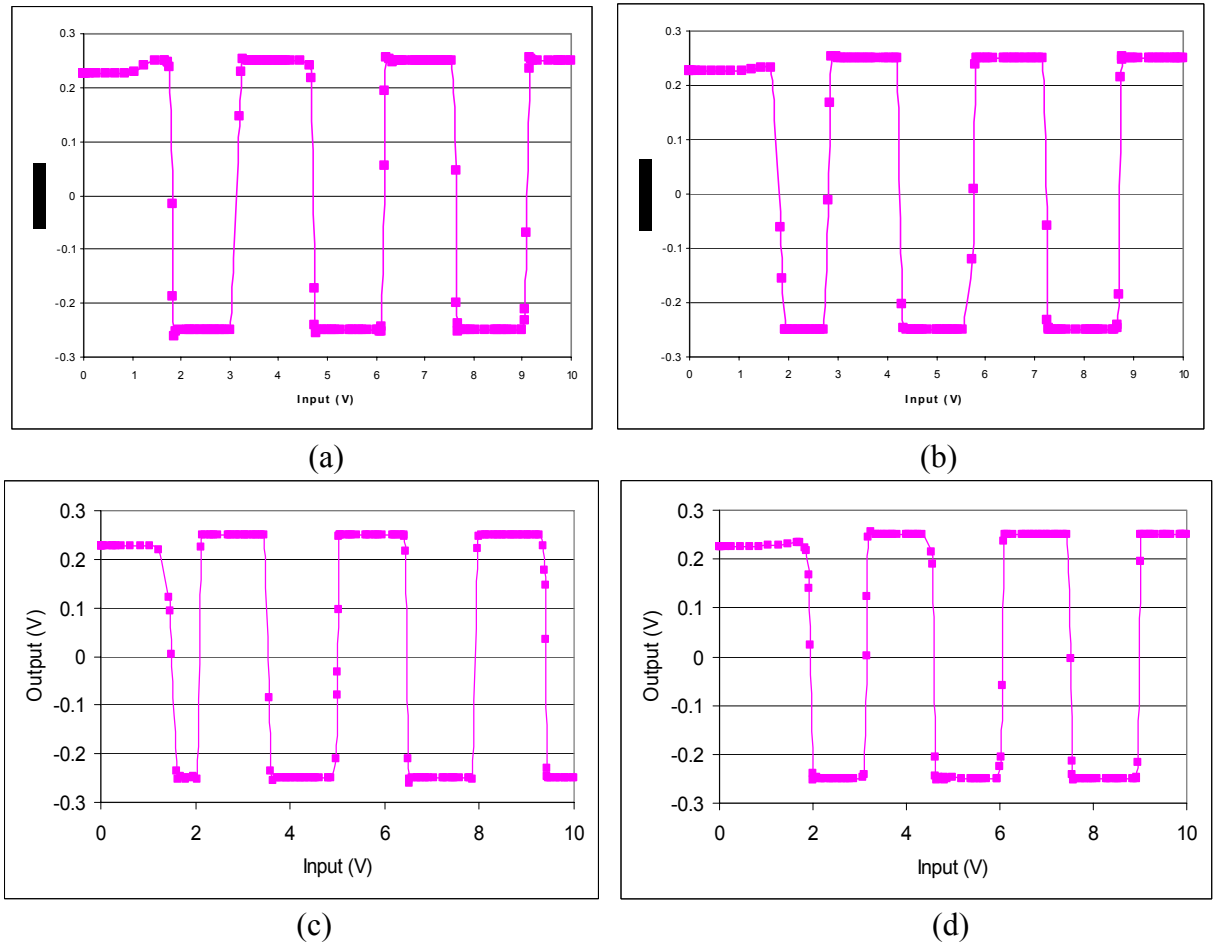


Figure 4.14 Shown are the parametric fault results on VCO, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 10% in their respective W/L ratio. In 4.14 (a) the error is in transistor M1, in 4.14 (b), the error is in transistor M2, in 4.14 (c) the error is in transistor M3, and in 4.14 (d) the error is in transistor M4.

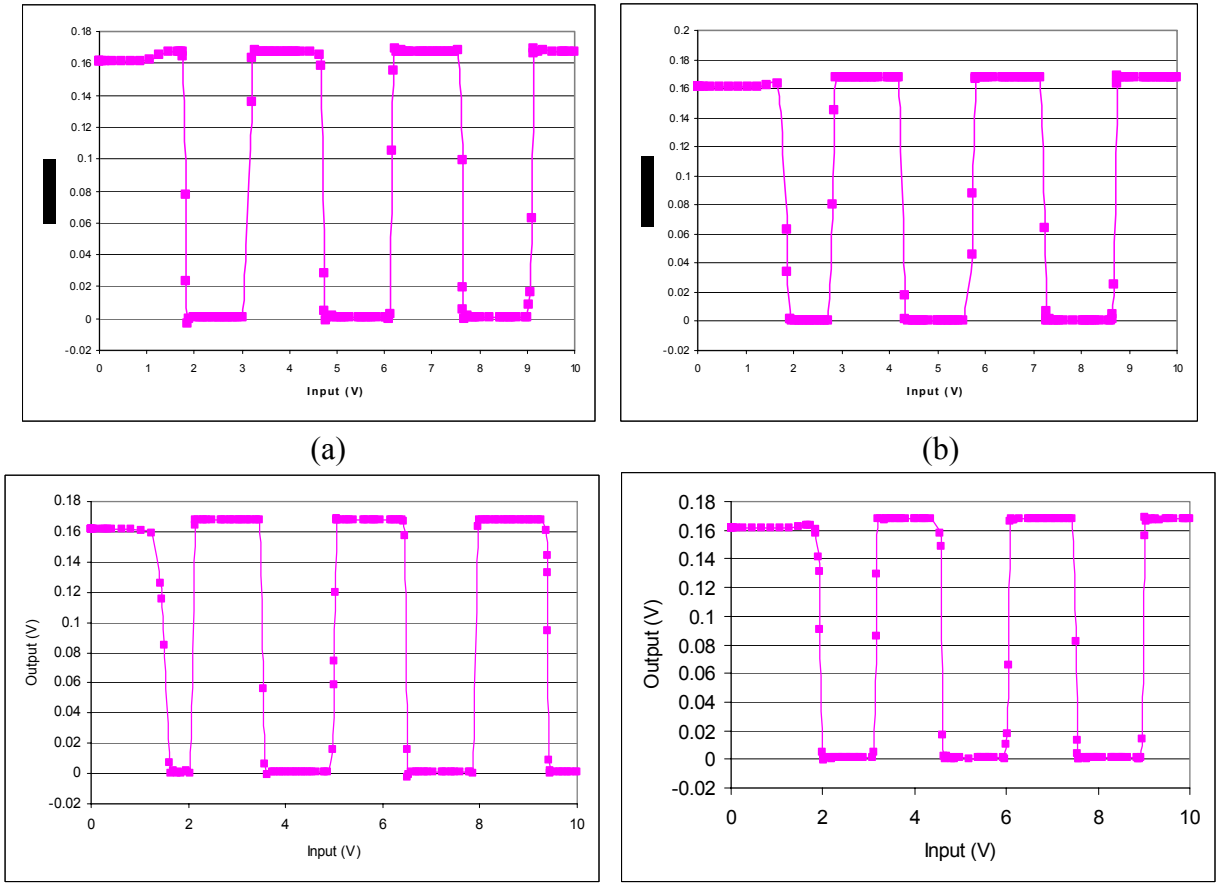


Figure 4.15 Shown are the parametric fault results on ZCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 10% in their respective W/L ratio. In 4.15 (a) the error is in transistor M1, in 4.15 (b), the error is in transistor M2, in 4.15 (c) the error is in transistor M3, and in 4.15 (d) the error is in transistor M4.

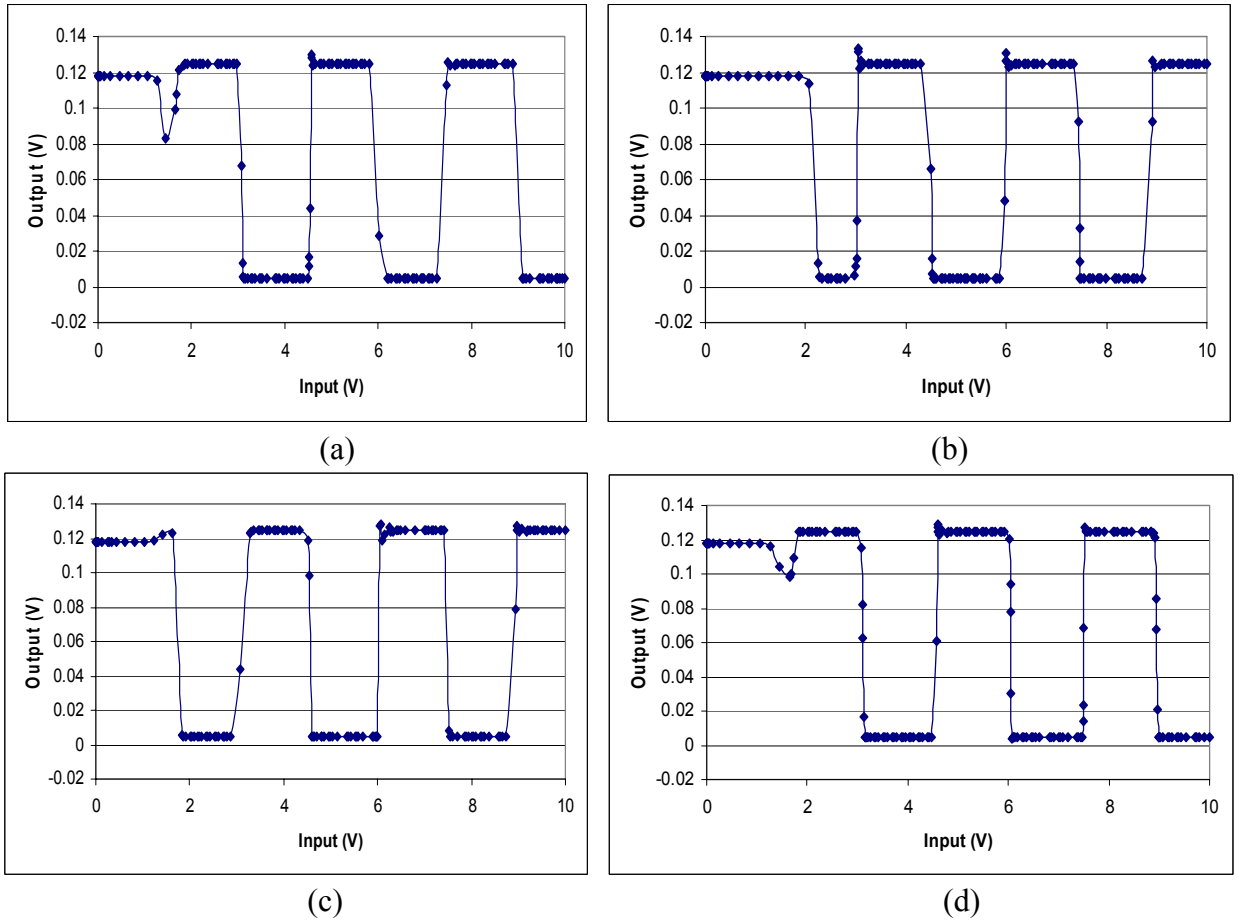


Figure 4.16 Shown are the parametric fault results on LCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 10% in their respective W/L ratio. In 4.16 (a) the error is in transistor M1, in 4.16 (b), the error is in transistor M2, in 4.16 (c) the error is in transistor M3, and in 4.16 (d) the error is in transistor M4.

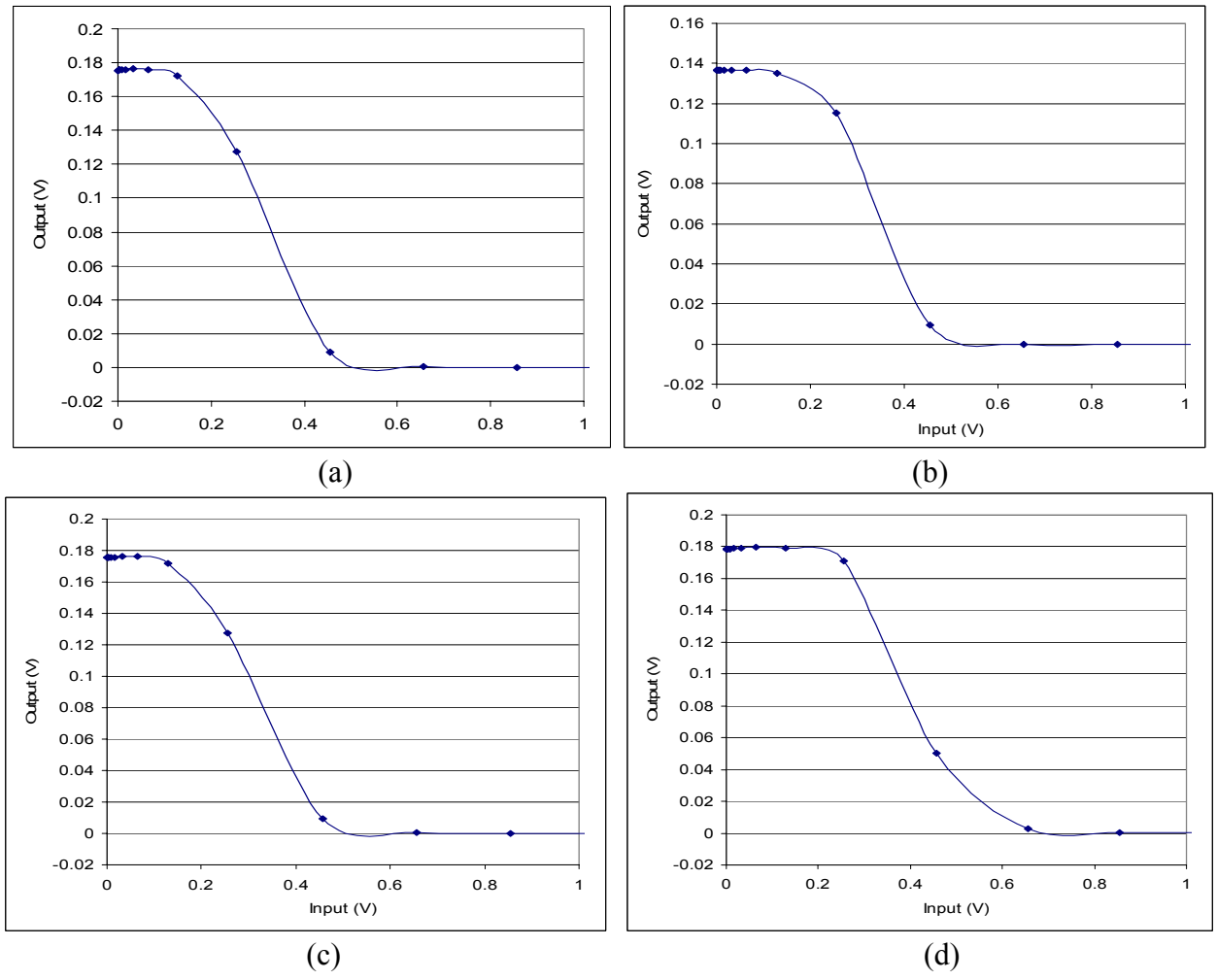


Figure 4.17 Shown are the catastrophic fault results on Vout2, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 75% in their respective W/L ratio. In 4.17 (a) the error is in transistor M1, in 4.17 (b), the error is in transistor M2, in 4.17 (c) the error is in transistor M3, and in 4.17 (d) the error is in transistor M4.

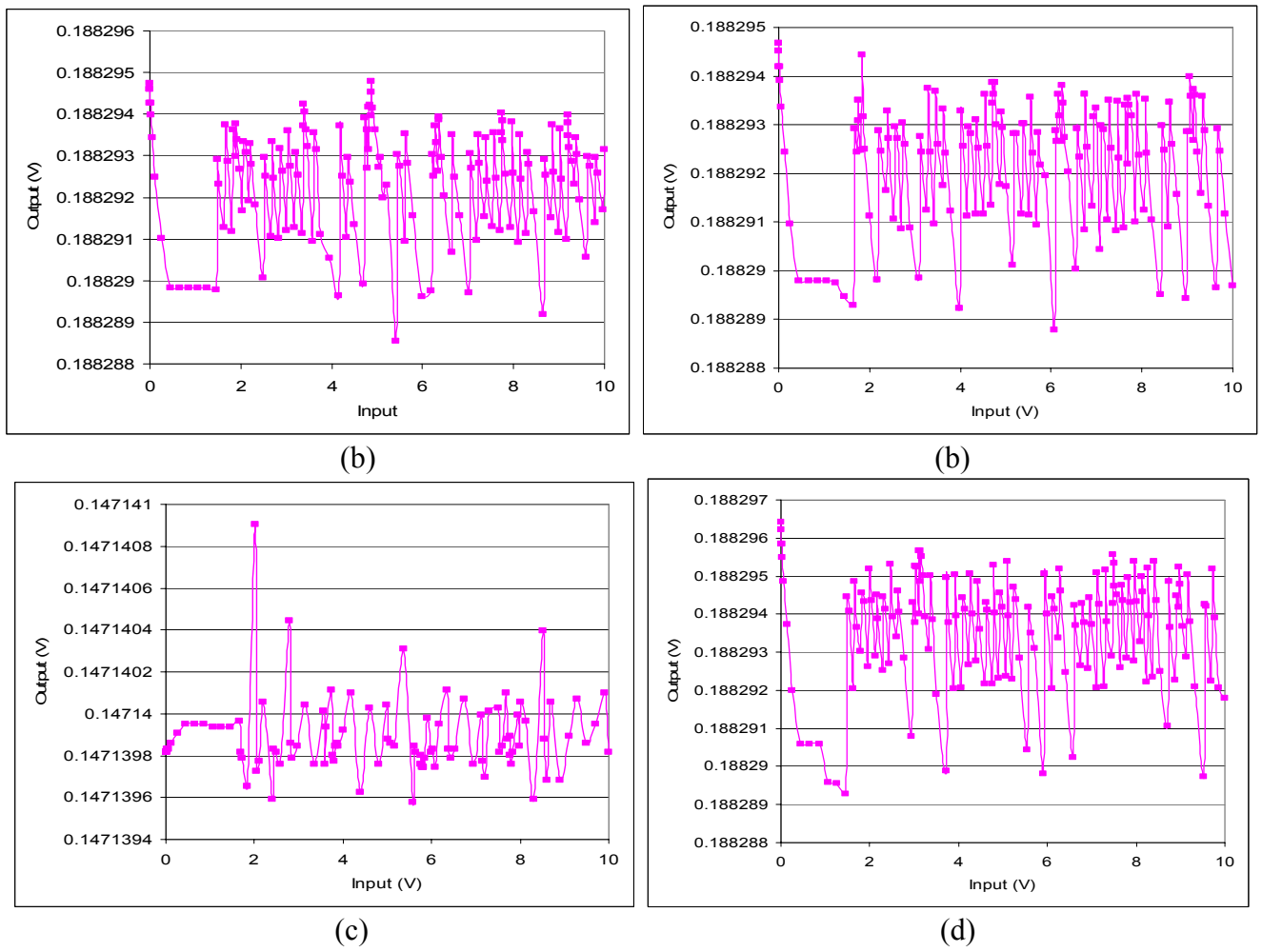


Figure 4.18 Shown are the catastrophic fault results on Vout1, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 75% in their respective W/L ratio. In 4.18 (a) the error is in transistor M1, in 4.18 (b), the error is in transistor M2, in 4.18 (c) the error is in transistor M3, and in 4.18 (d) the error is in transistor M4.

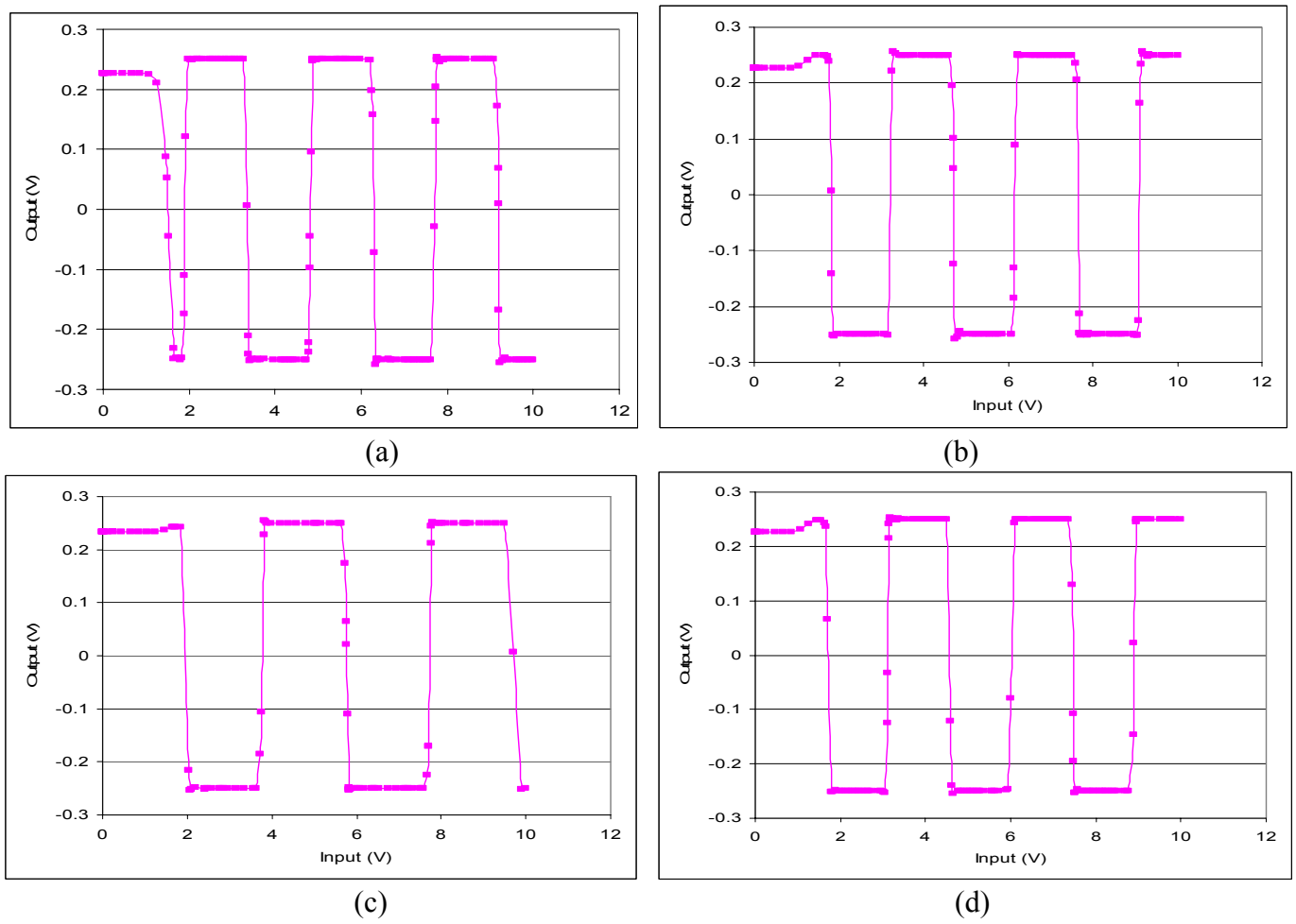


Figure 4.19 Shown are the catastrophic fault results on VCO, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 75% in their respective W/L ratio. In 4.19 (a) the error is in transistor M1, in 4.19 (b), the error is in transistor M2, in 4.19 (c) the error is in transistor M3, and in 4.19 (d) the error is in transistor M4.

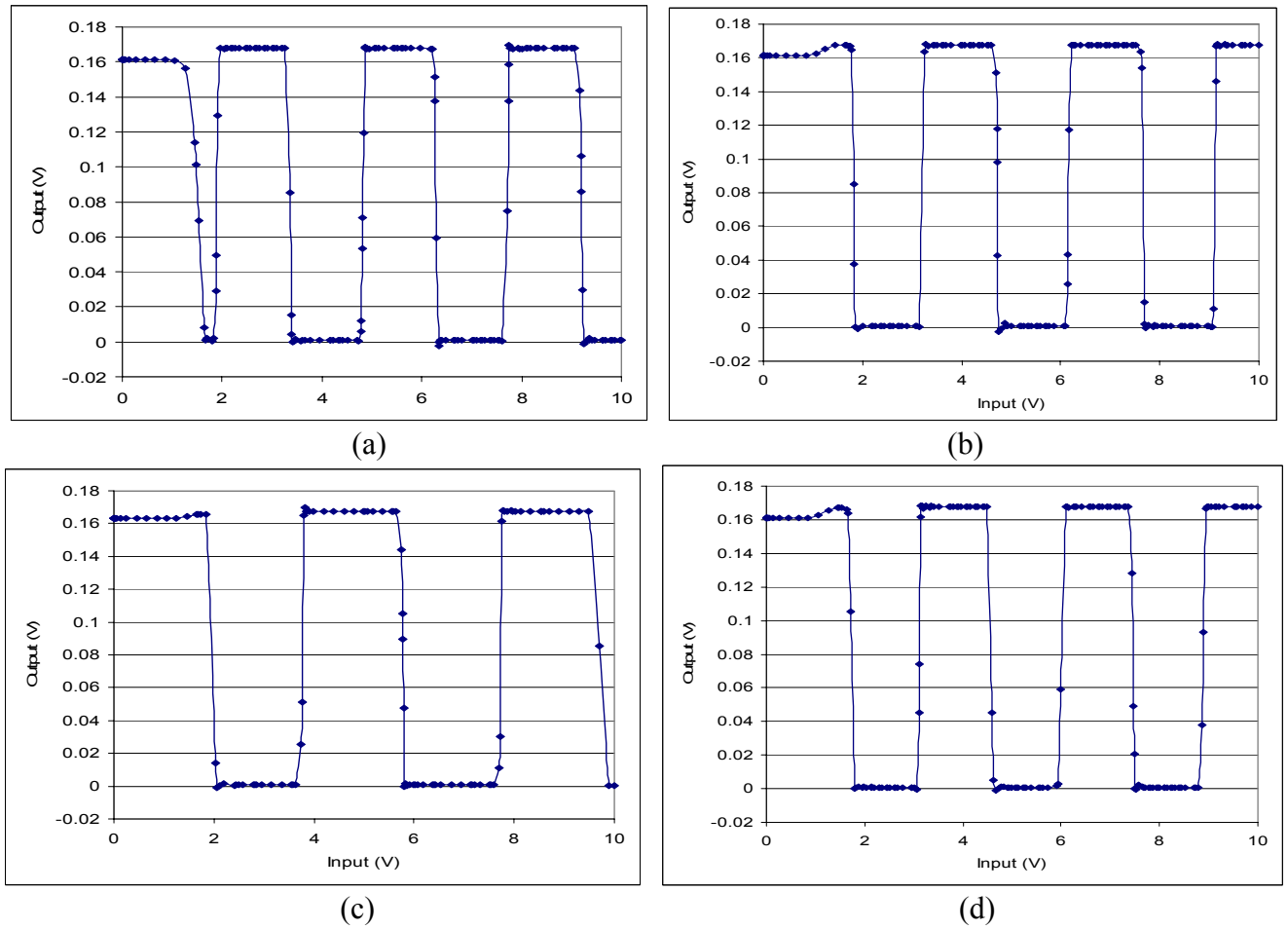


Figure 4.20 Shown are the catastrophic fault results on ZCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 75% in their respective W/L ratio. In 4.20 (a) the error is in transistor M1, in 4.20 (b), the error is in transistor M2, in 4.20 (c) the error is in transistor M3, and in 4.20 (d) the error is in transistor M4.

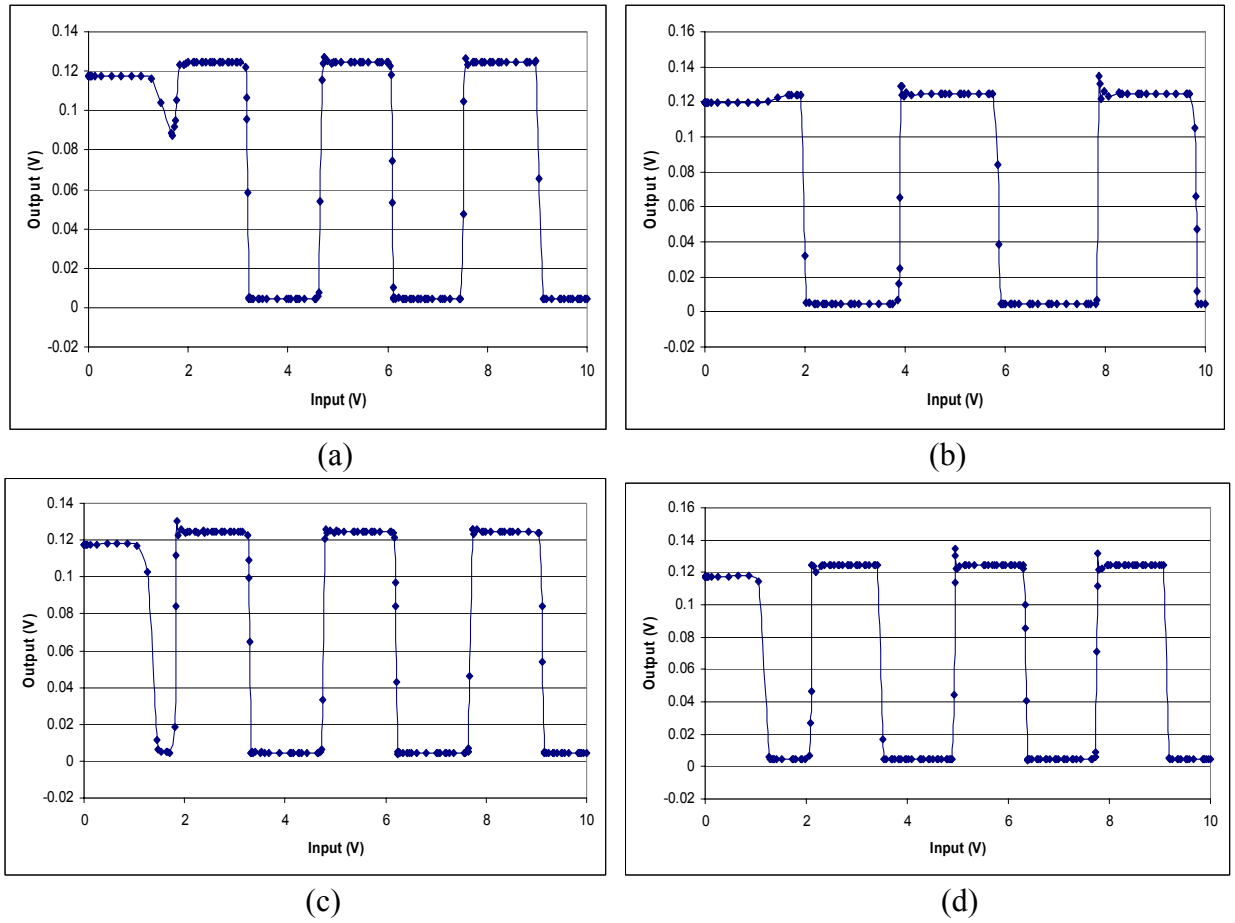
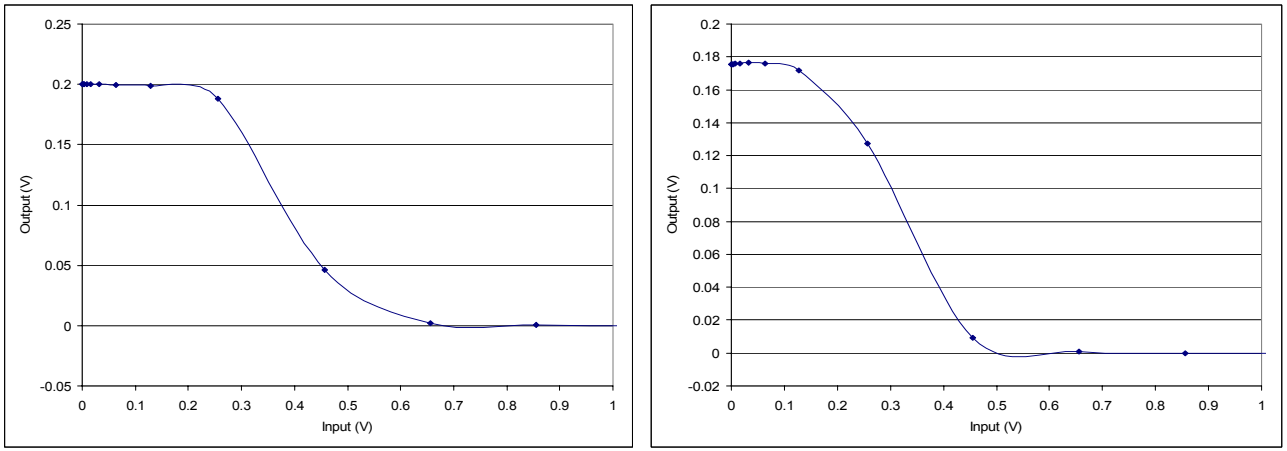
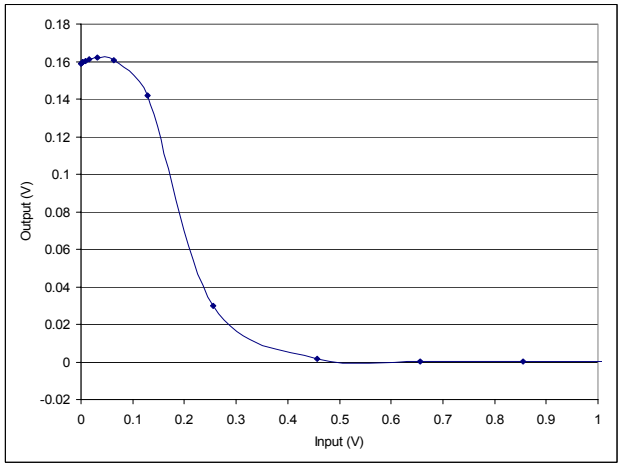


Figure 4.21 Shown are the catastrophic fault results on LCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 75% in their respective W/L ratio. In 4. 21 (a) the error is in transistor M1, in 4. 21 (b), the error is in transistor M2, in 4. 21 (c) the error is in transistor M3, and in 4. 21 (d) the error is in transistor M4.

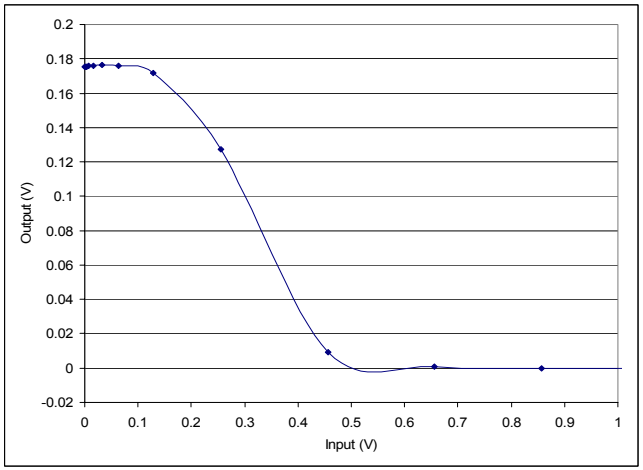


(c)

(b)



(c)



(d)

Figure 4.22 Shown are the catastrophic fault results on Vout2, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 4x in their respective W/L ratio. In 4.22 (a) the error is in transistor M1, in 4.22 (b), the error is in transistor M2, in 4.22 (c) the error is in transistor M3, and in 4.22 (d) the error is in transistor M4.

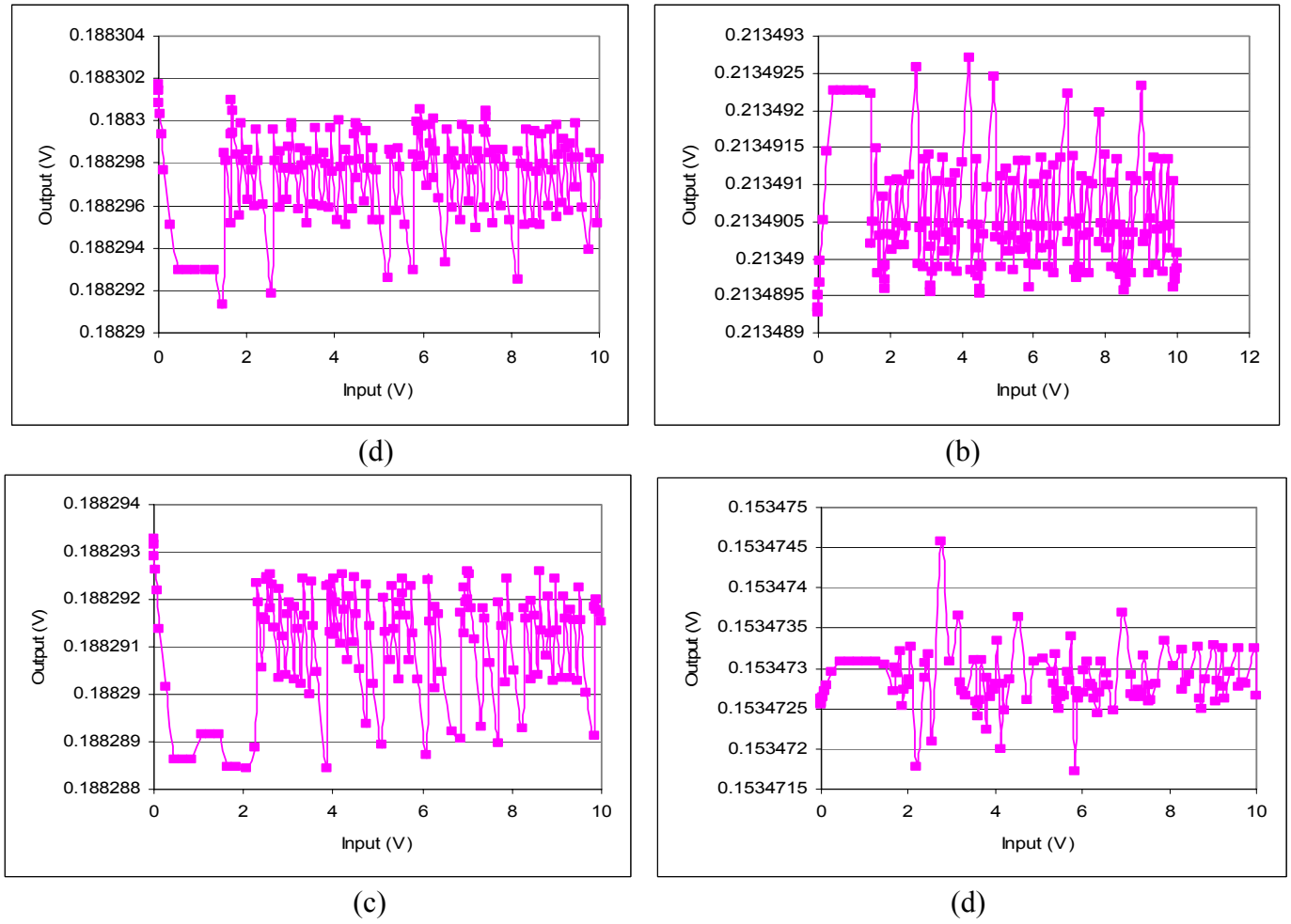


Figure 4.23 Shown are the catastrophic fault results on Vout1, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 4x in their respective W/L ratio. In 4.23 (a) the error is in transistor M1, in 4.23 (b), the error is in transistor M2, in 4.23 (c) the error is in transistor M3, and in 4.23 (d) the error is in transistor M4.

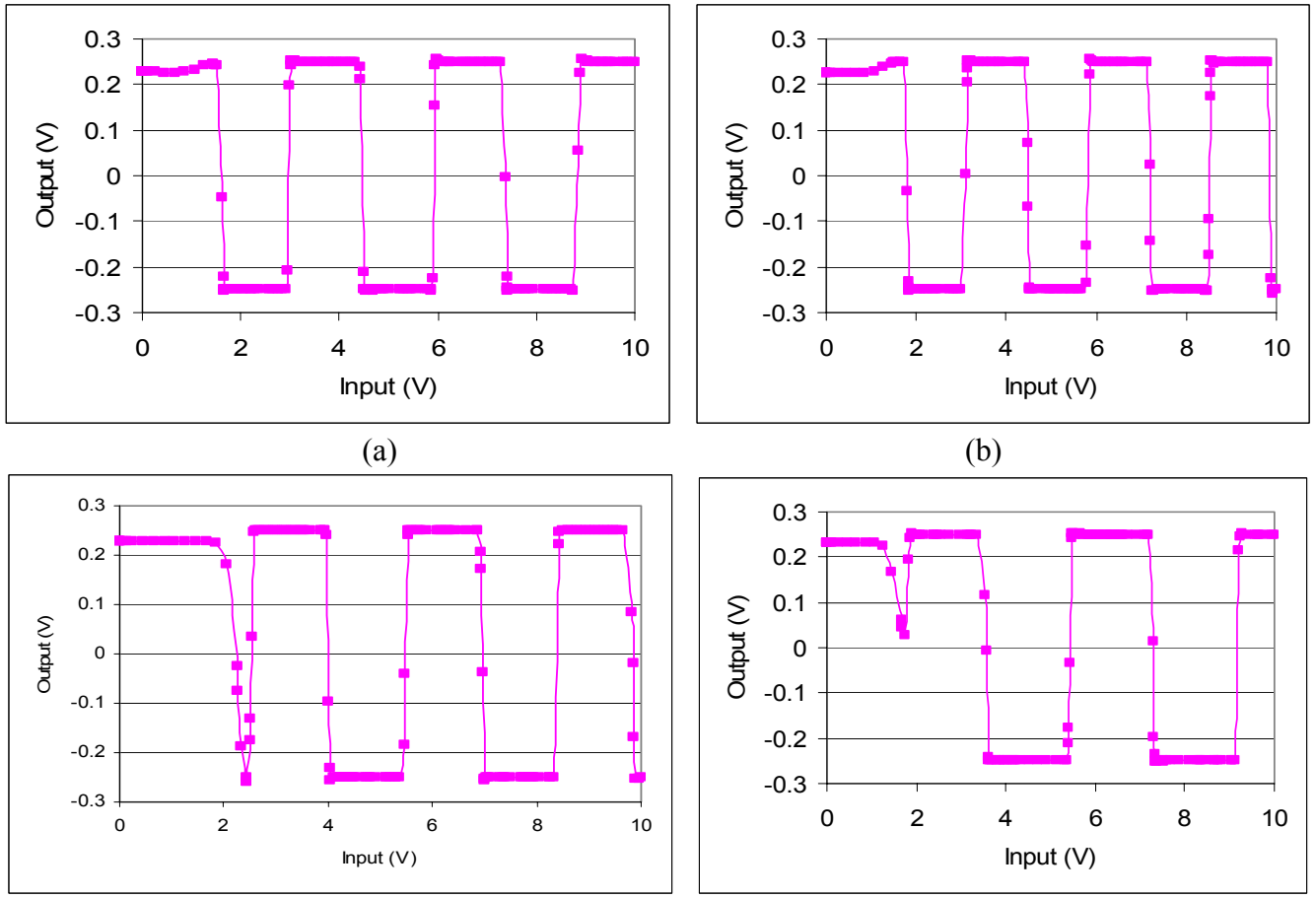


Figure 4.24 Shown are the catastrophic fault results on VCO, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 4x in their respective W/L ratio. In 4.24 (a) the error is in transistor M1, in 4.24 (b), the error is in transistor M2, in 4.24 (c) the error is in transistor M3, and in 4.24 (d) the error is in transistor M4.

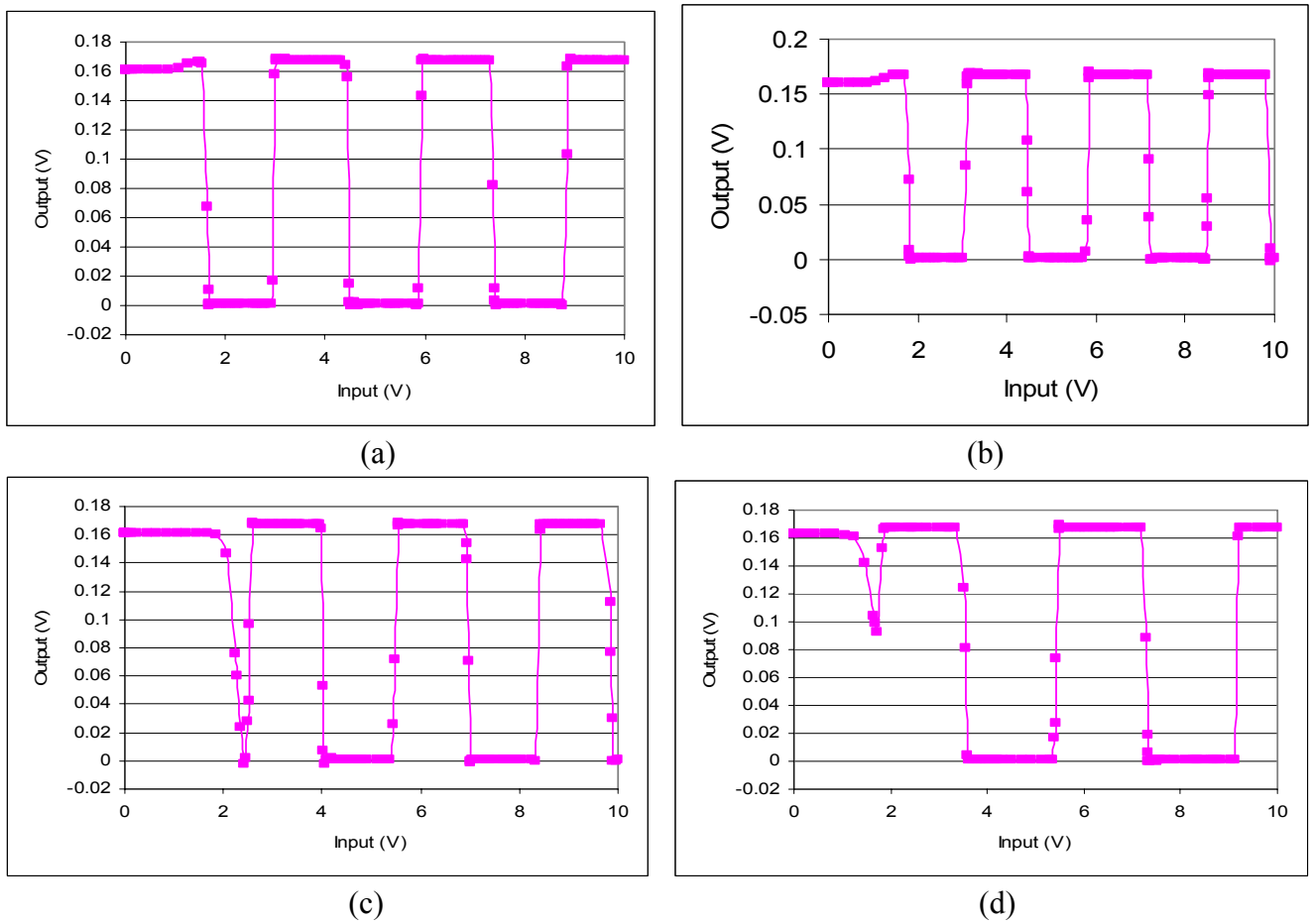
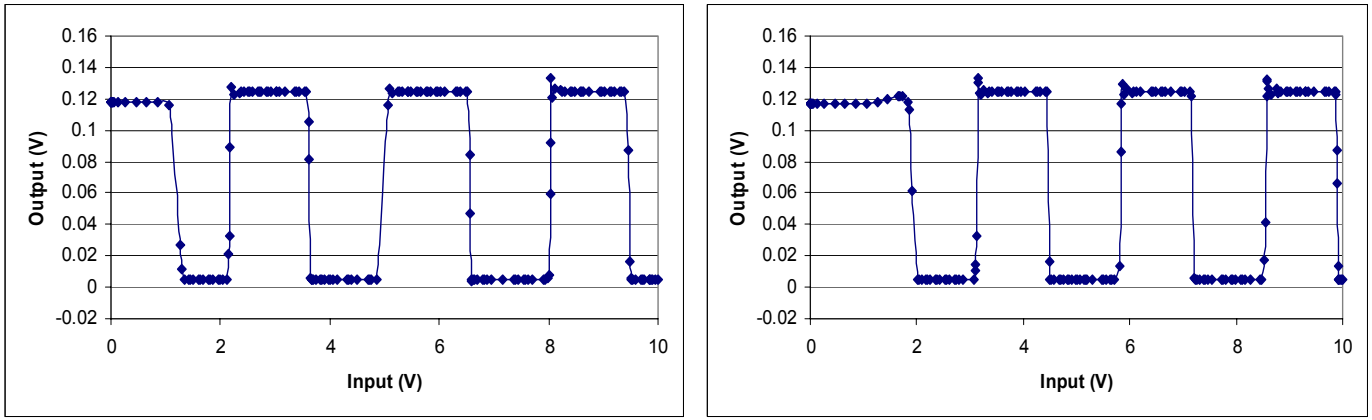
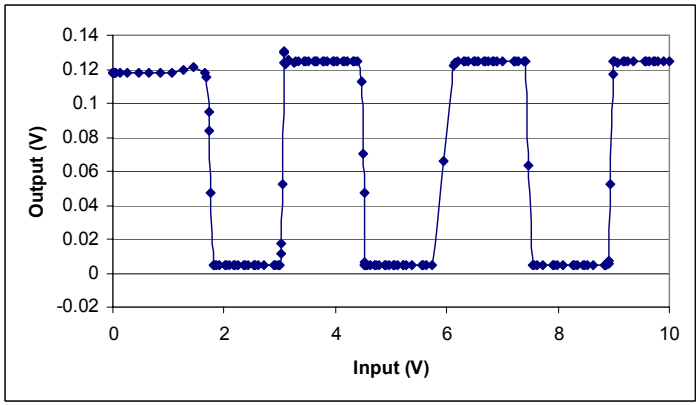


Figure 4.25 Shown are the catastrophic fault results on ZCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 4x in their respective W/L ratio. In 4.25 (a) the error is in transistor M1, in 4.25 (b), the error is in transistor M2, in 4.25 (c) the error is in transistor M3, and in 4.25 (d) the error is in transistor M4.

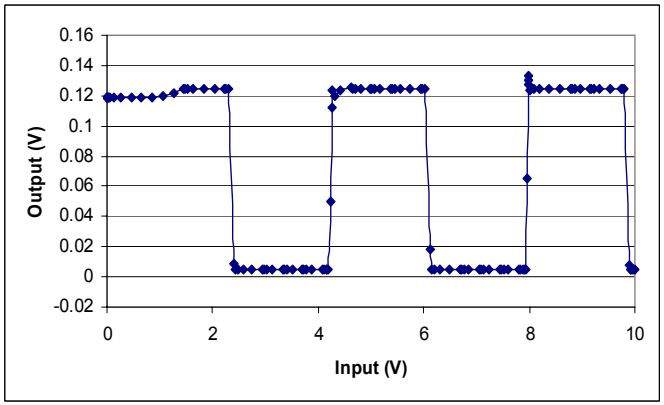


(a)

(b)



(c)



(d)

Figure 4.26 Shown are the catastrophic fault results on LCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 4x in their respective W/L ratio. In 4.26 (a) the error is in transistor M1, in 4.26 (b), the error is in transistor M2, in 4.26 (c) the error is in transistor M3, and in 4.26 (d) the error is in transistor M4.

In its raw form, the data generated by the on-chip test methods discussed, is unwieldy; therefore, very little on-chip information can be gleaned by these raw responses. As such, it is necessary to create a method (either on-chip or off-chip) to gain insight into the distinctions that exist between the faults evaluated in this work.

Biosensor (VLSI ChemFET)

Fault	90% of Expected W/L Ratio	25% of Expected W/L Ratio	400% of Expected Width Length Ratio
Mean Squared Error	8.01 e-11	0.538	8.01 e-11
FFT Matched Filter(MF)	4.17 e2	3.49 e2	4.17 e2

Table 4-1 Biosensor Response Vout1

Fault	90% of Expected W/L Ratio	25% of Expected W/L Ratio	400% of Expected Width Length Ratio
Mean Squared Error	44.44	9.19	44.14
FFT Matched Filter(MF)	1.25 e2	62.9	1.25 e2

Table 4-2 Biosensor Response Vout2

Fault	90% of Expected W/L Ratio	25% of Expected W/L Ratio	400% of Expected Width Length Ratio
Mean Squared Error	4.858 e6	1.326 e6	6.577 e6
FFT Matched Filter(MF)	33.21	13.95	38.66

Table 4-3 Voltage Controlled Oscillator (VCO) Response

Fault	90% of Expected W/L Ratio	25% of Expected W/L Ratio	400% of Expected Width Length Ratio
Mean Squared Error	272.63	563.608	272.63
FFT Matched Filter(MF)	1.85 e2	2.63 e2	1.85 e2

Table 4-4 Zero-Crossing Detector (ZCD)

The tables provide us with an understanding of the numerical sensitivity each SoC macro has when faced with the catastrophic and parametric faults studied in this work. The tables show the mean-squared error (MSE) difference in amplitude of output versus expected (no-fault) amplitude output, the MSE difference in period width from first to second period (comparing fault-devices with fault-free devices), and the MSE difference in the expected full width half maximum (FWHM) value as it relates to the fault-received value, for each oscillating signal. The information in these tables can later be used to create an on-chip means of detecting and identifying faults.

Subsection 4.3.3 Analysis with New K Values

In this sub-section we evaluate the parametric and catastrophic faults against a biosensor with a new KP parameter. The KP parameter in these evaluations is half the size of the previous KP parameter. This subsection addresses the potential impact of a fault on the biosensor's ability to detect slight changes in dielectric constant. The most telling information is provided in subsection 4.3.4, as we see contrasting graphs of the SoC OBIST model outputs. Here, we see a counter and clock-like signal output of a biosensor with normal dielectric constant compared against the biosensor with new dielectric constant. We also see a contrast between faults that occur in the normal biosensor, fluid under test transistor and the new "KP-parameter" biosensor fluid under test transistor. Figure 4.27 shows the output response of each of the OBIST macros to the new KP parameter value. Figures 4.28 through 4.42 show the influence of individual biosensor transistor faults to the OBIST macro outputs.

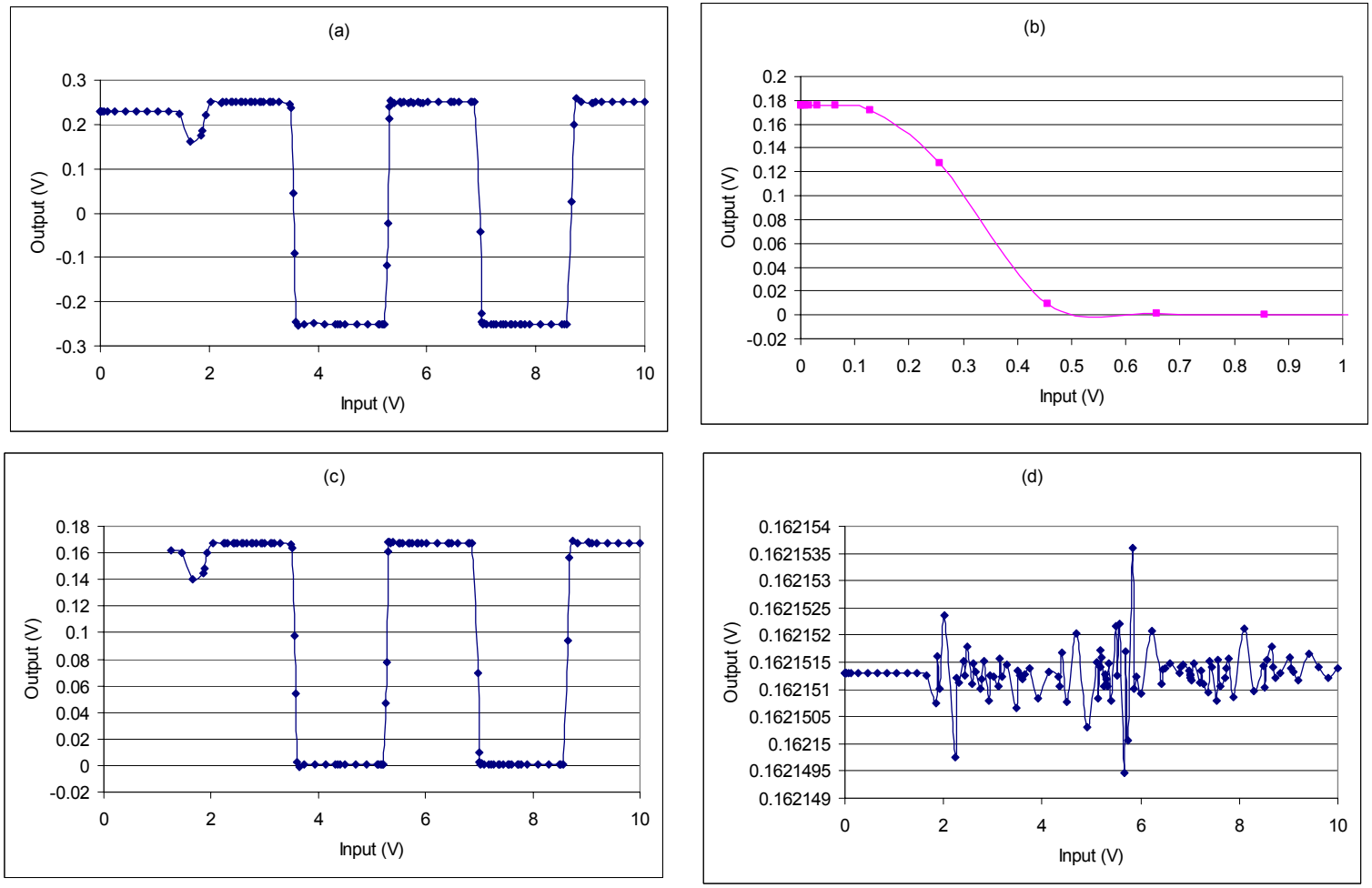
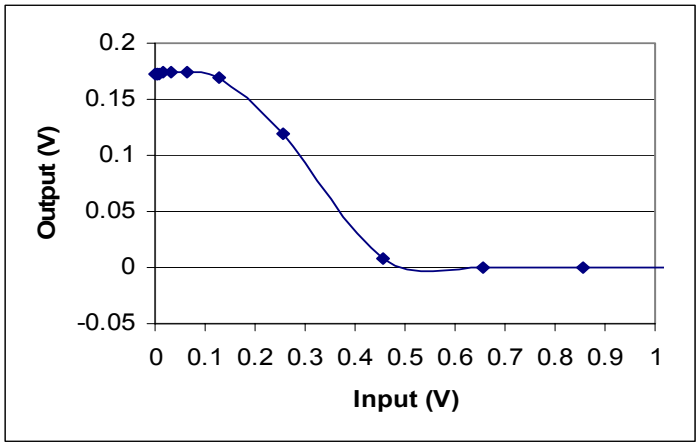
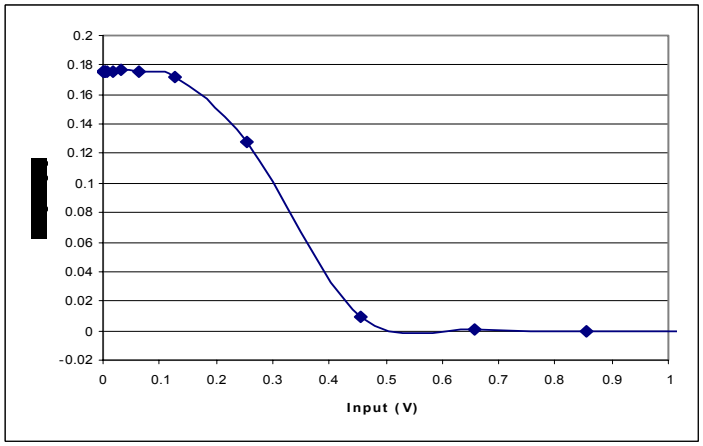


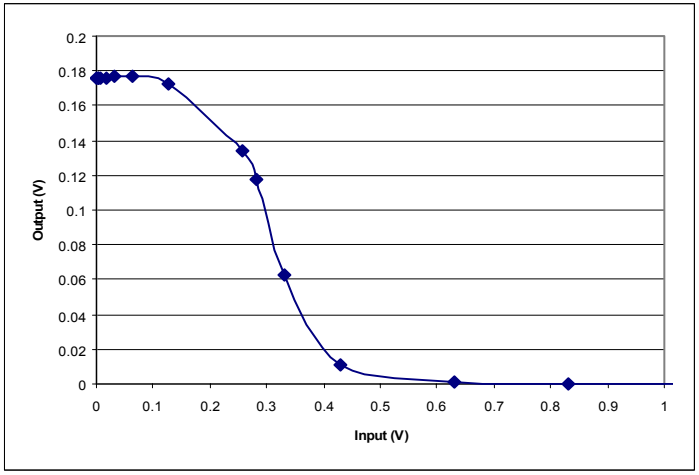
Figure 4.27 Shown are the parametric fault-free output responses of the OBIST with a new KP parameter in use. In 4.27 (a) Biosensor Vout1, in 4.27 (b) Biosensor Bout2 in 4.27 (c) VCO, and in 4.27 (d) ZCD.



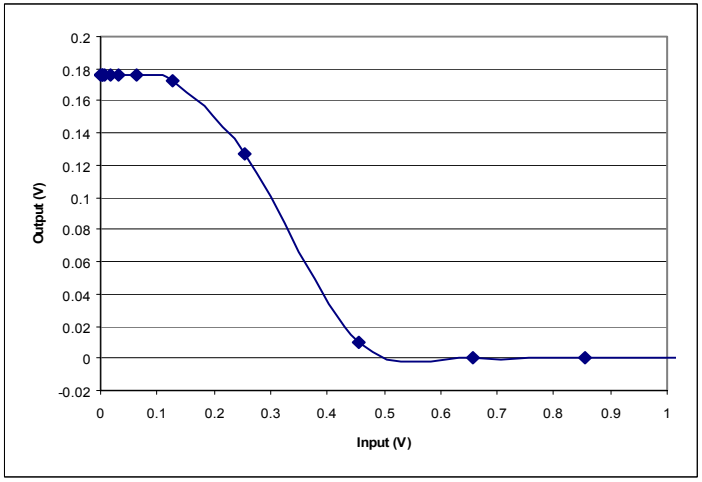
(e)



(b)



(c)



(d)

Figure 4.28 Shown are the parametric fault results on Vout2, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 10% in their respective W/L ratio. In 4.28 (a) the error is in transistor M1, in 4.28 (b), the error is in transistor M2, in 4.28 (c) the error is in transistor M3, and in 4.28 (d) the error is in transistor M4.

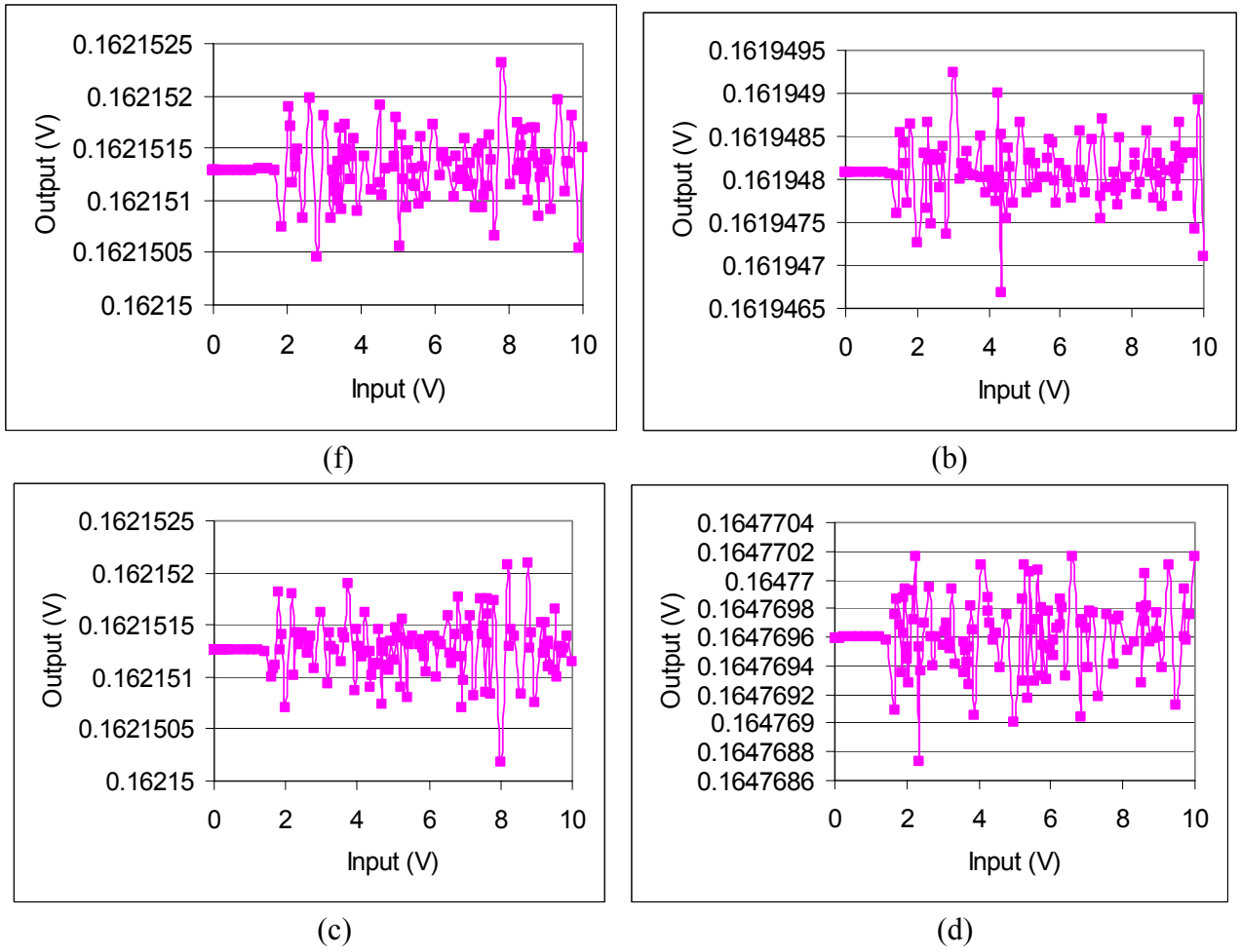
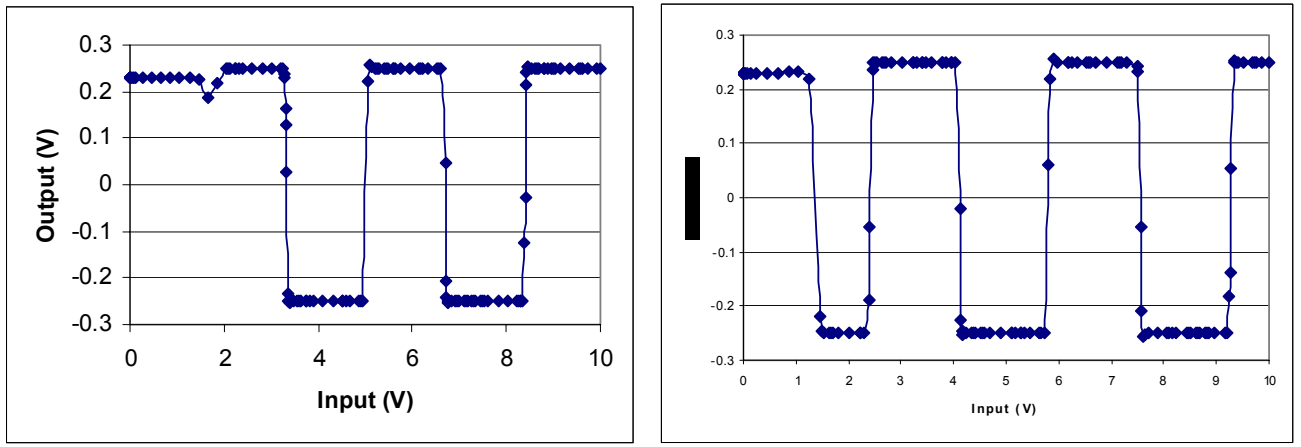
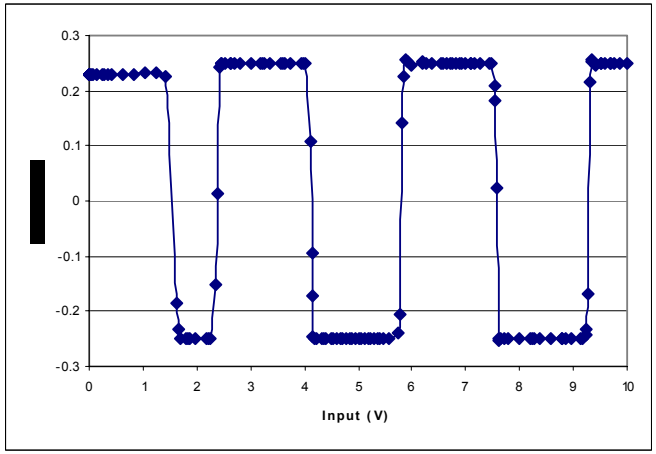


Figure 4.29 Shown are the parametric fault results on Vout1, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 10% in their respective W/L ratio. In 4.29 (a) the error is in transistor M1, in 4.29 (b), the error is in transistor M2, in 4.29 (c) the error is in transistor M3, and in 4.29 (d) the error is in transistor M4.

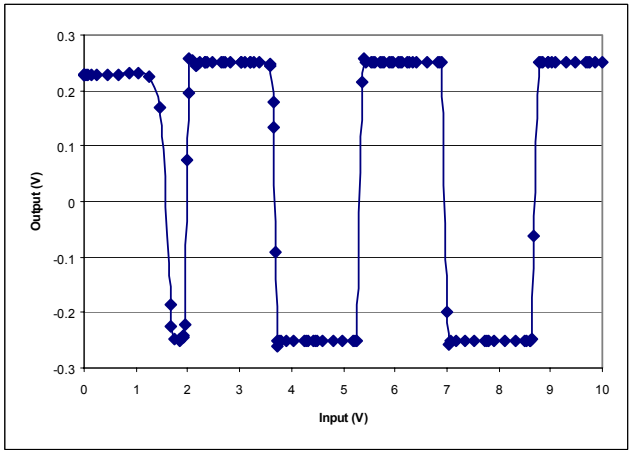


(a)

(b)



(c)



(d)

Figure 4.30 Shown are the parametric fault results on VCO, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 10% in their respective W/L ratio. In 4.30 (a) the error is in transistor M1, in 4.30 (b), the error is in transistor M2, in 4.30 (c) the error is in transistor M3, and in 4.30 (d) the error is in transistor M4.

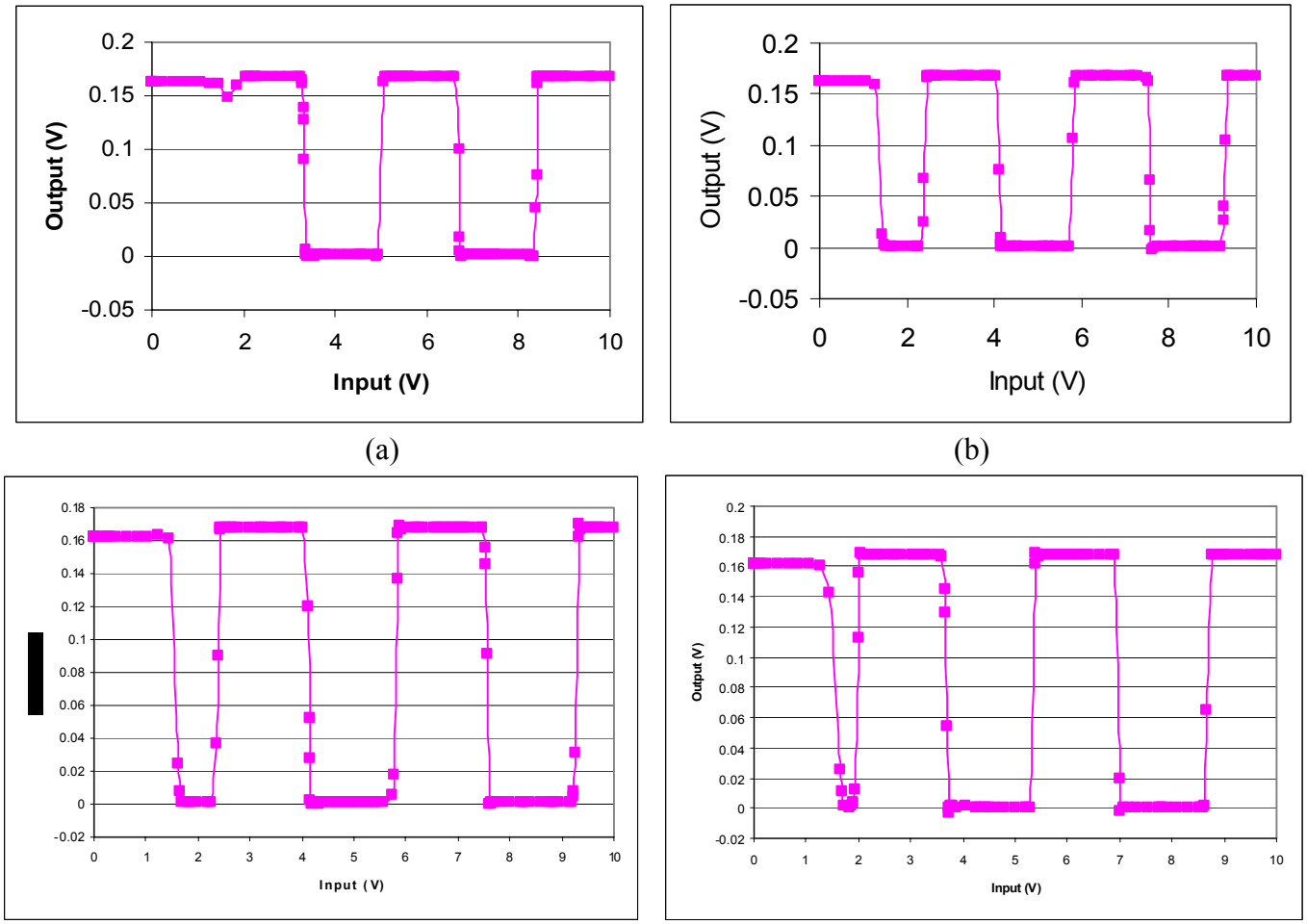
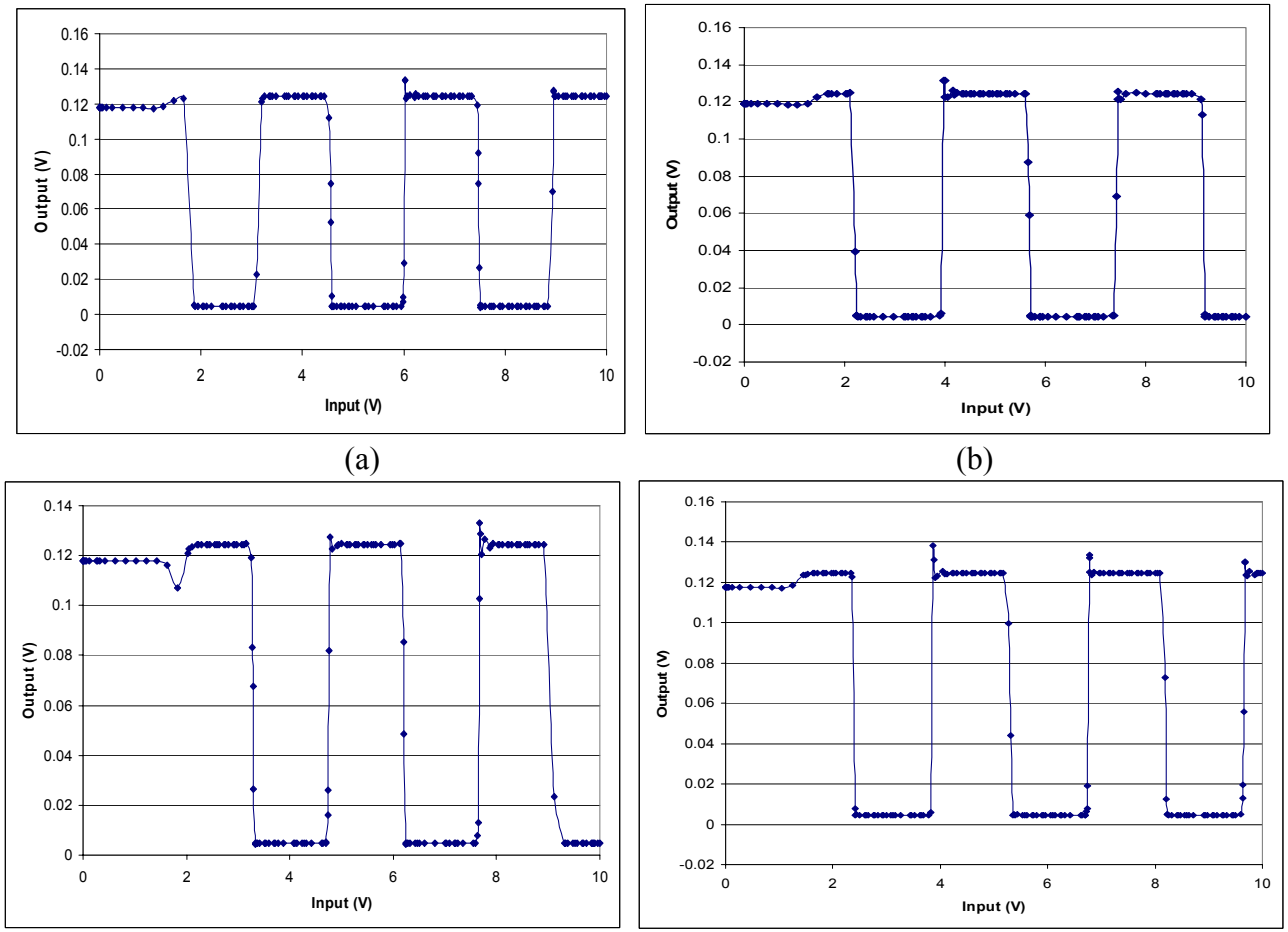


Figure 4.31 Shown are the parametric fault results on ZCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 10% in their respective W/L ratio. In 4.31 (a) the error is in transistor M1, in 4.31 (b), the error is in transistor M2, in 4.31 (c) the error is in transistor M3, and in 4.31 (d) the error is in transistor M4.



(a) (b)

(c) (d)

Figure 4.32 Shown are the parametric fault results on LCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 10% in their respective W/L ratio. In 4.32 (a) the error is in transistor M1, in 4.32 (b), the error is in transistor M2, in 4.32 (c) the error is in transistor M3, and in 4.32 (d) the error is in transistor M4.

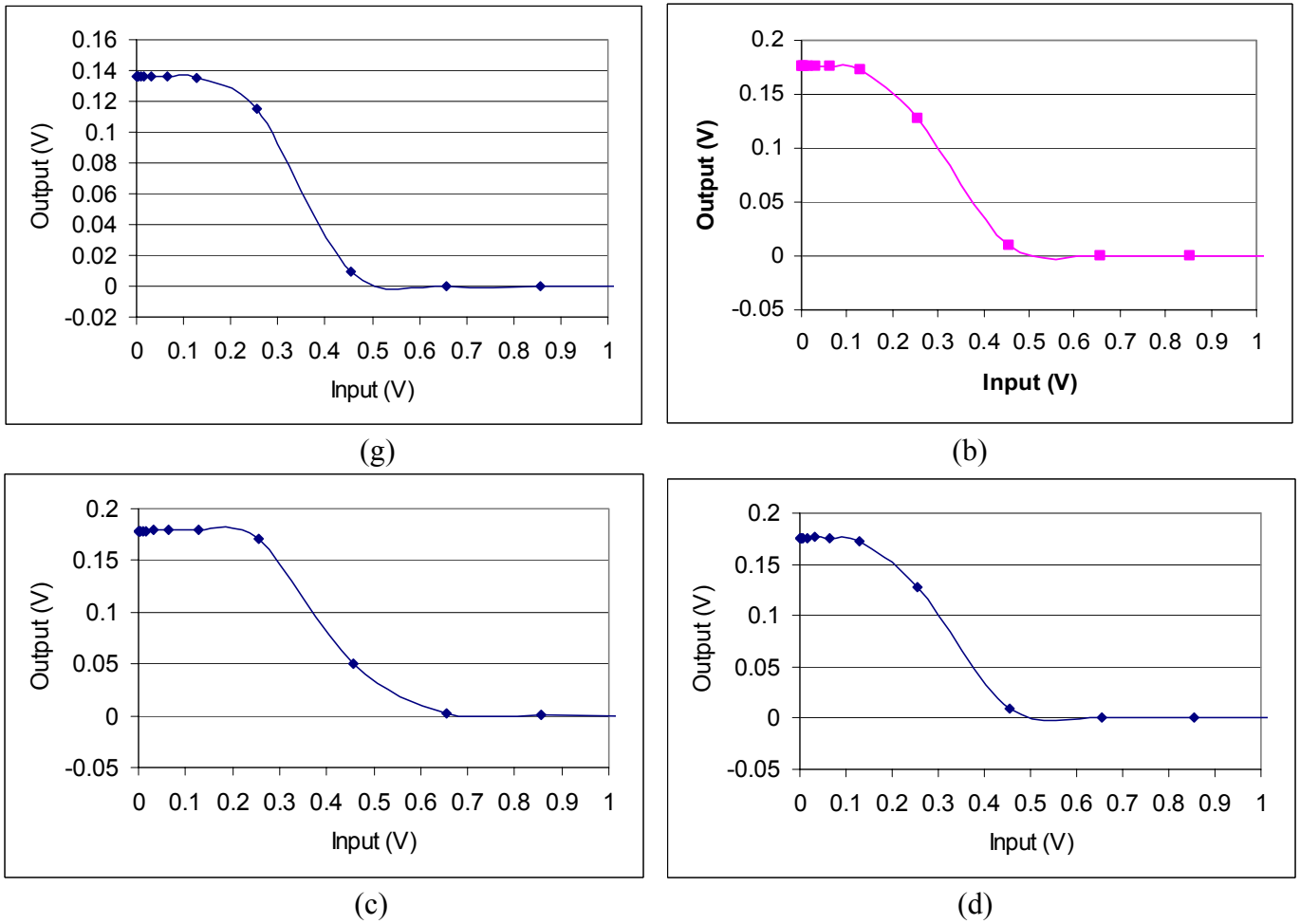


Figure 4.33 Shown are the catastrophic fault results on Vout2, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 75% in their respective W/L ratio. In 4.33 (a) the error is in transistor M1, in 4.33 (b), the error is in transistor M2, in 4.33 (c) the error is in transistor M3, and in 4.33 (d) the error is in transistor M4.

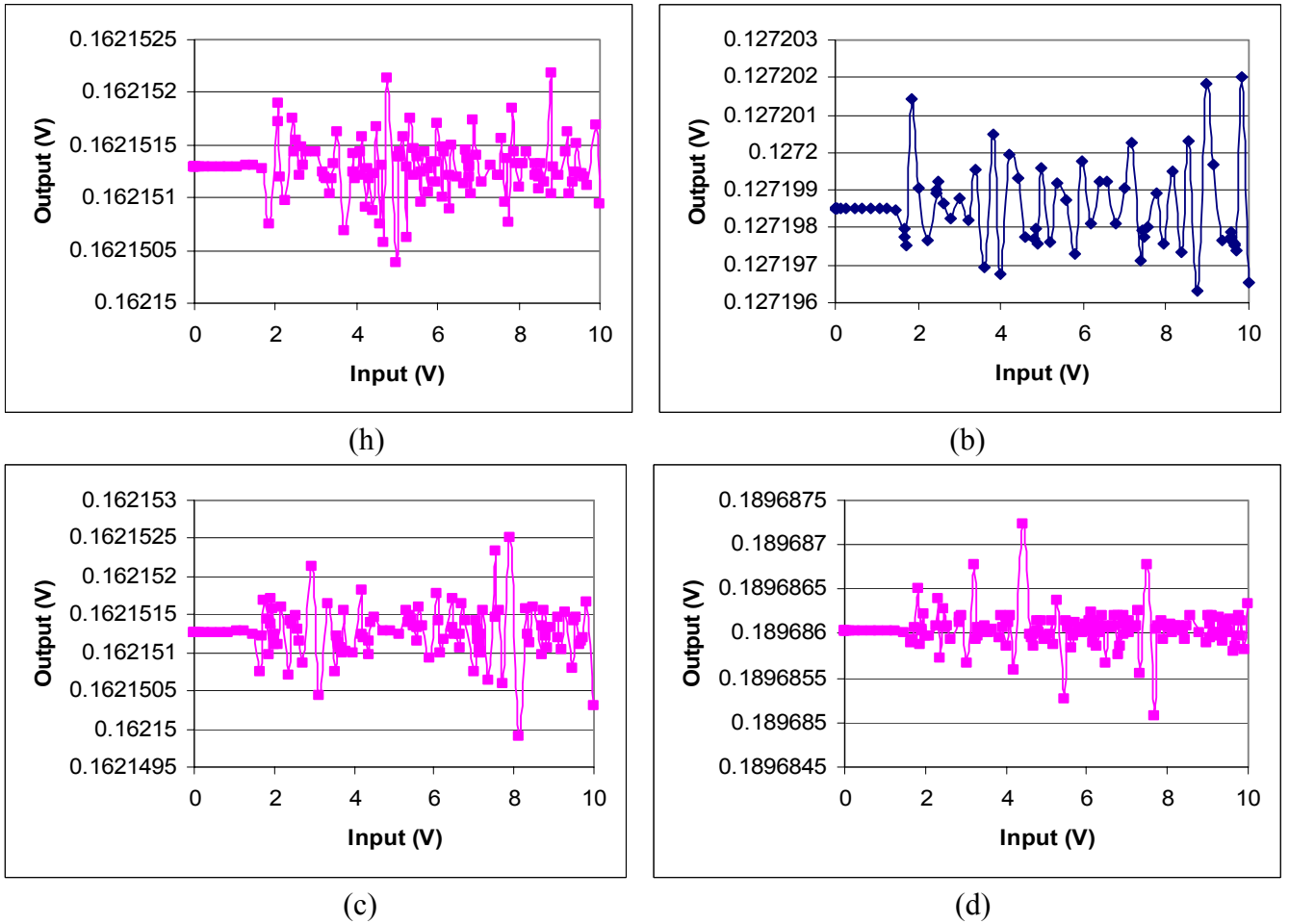


Figure 4.34 Shown are the catastrophic fault results on Vout1, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 75% in their respective W/L ratio. In 4.34 (a) the error is in transistor M1, in 4.34 (b), the error is in transistor M2, in 4.34 (c) the error is in transistor M3, and in 4.34 (d) the error is in transistor M4.

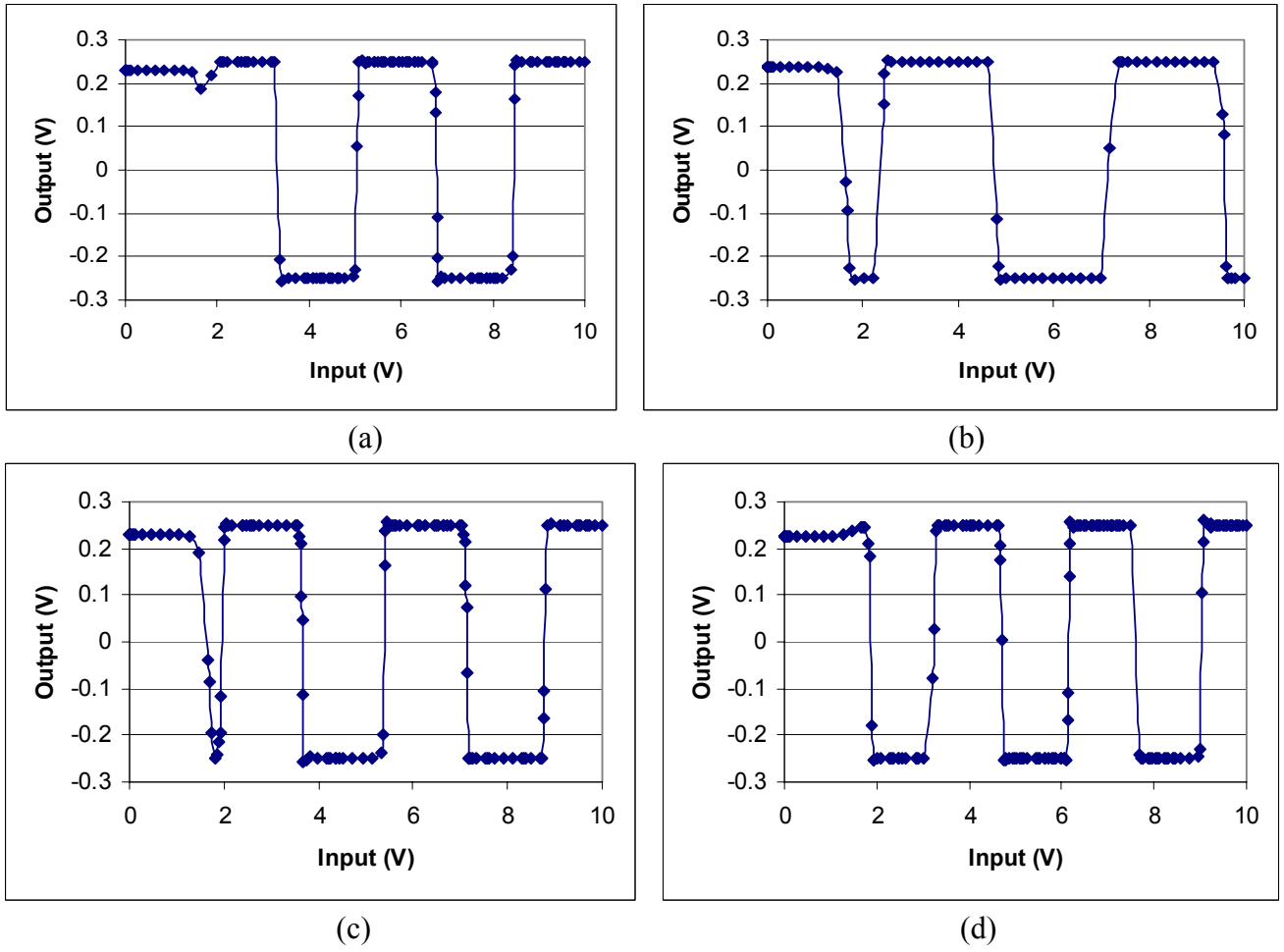


Figure 4.35 Shown are the catastrophic fault results on VCO, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 75% in their respective W/L ratio. In 4.35 (a) the error is in transistor M1, in 4.35 (b), the error is in transistor M2, in 4.35 (c) the error is in transistor M3, and in 4.35 (d) the error is in transistor M4.

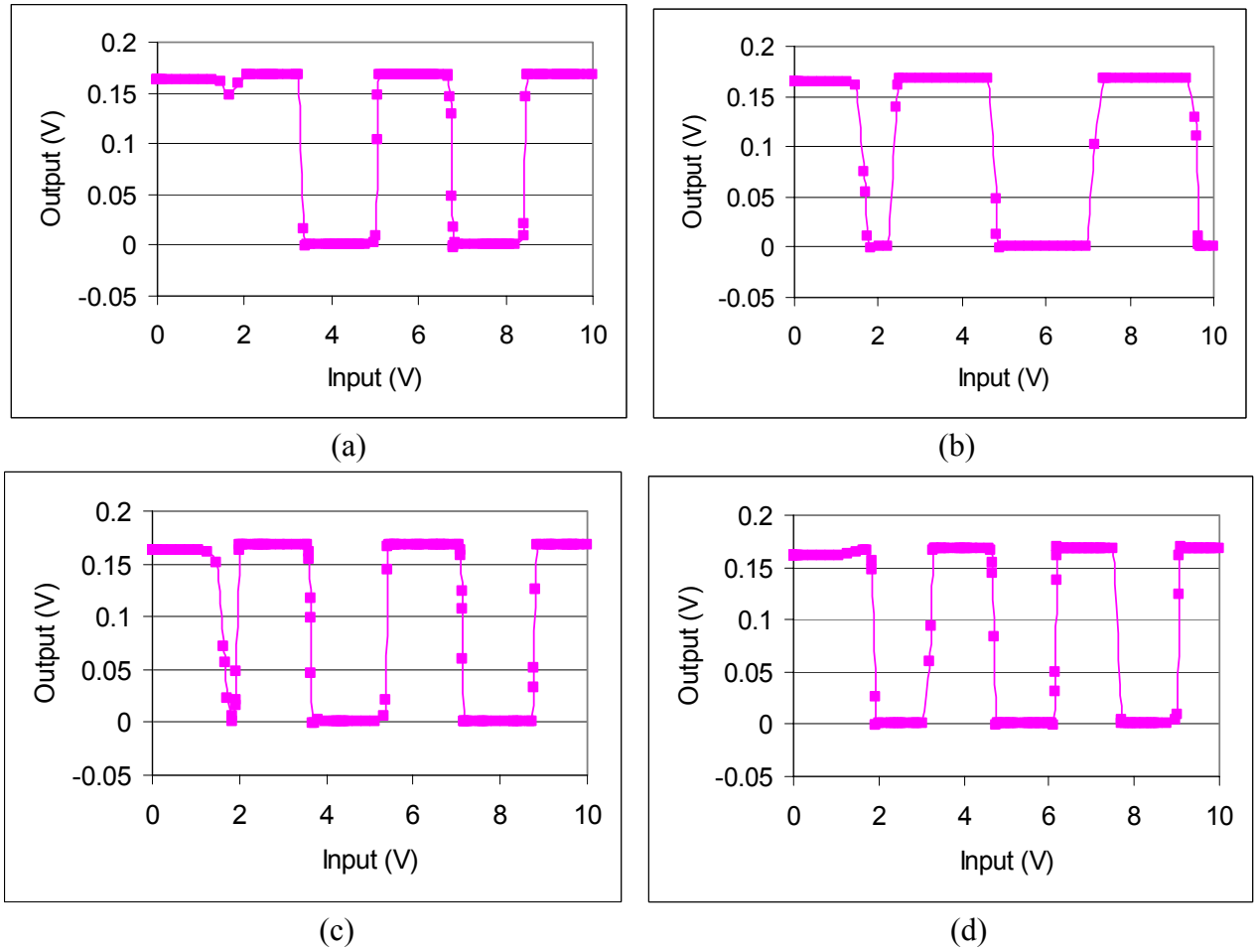


Figure 4.36 Shown are the catastrophic fault results on ZCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 75% in their respective W/L ratio. In 4.36 (a) the error is in transistor M1, in 4.36 (b), the error is in transistor M2, in 4.36 (c) the error is in transistor M3, and in 4.36 (d) the error is in transistor M4.

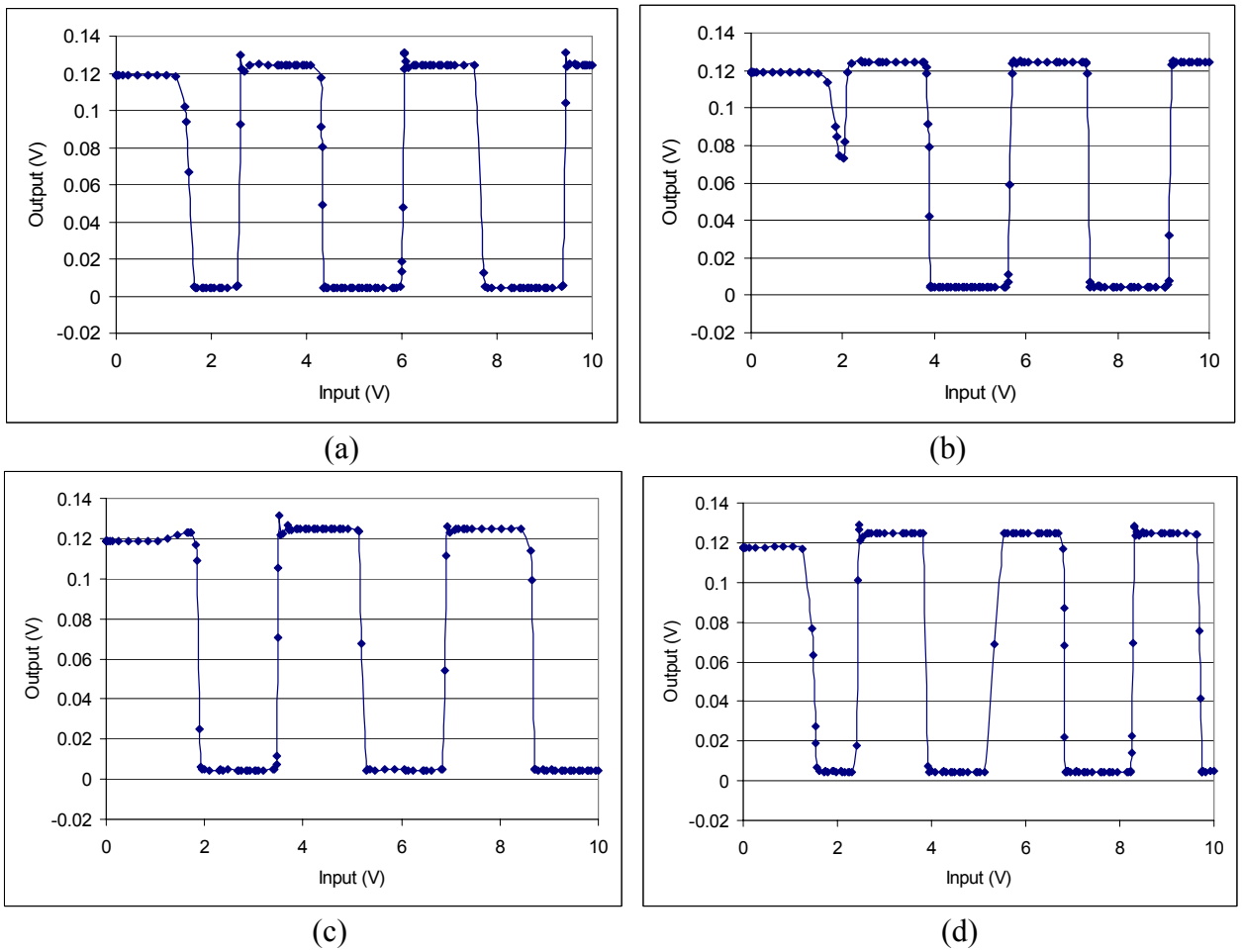
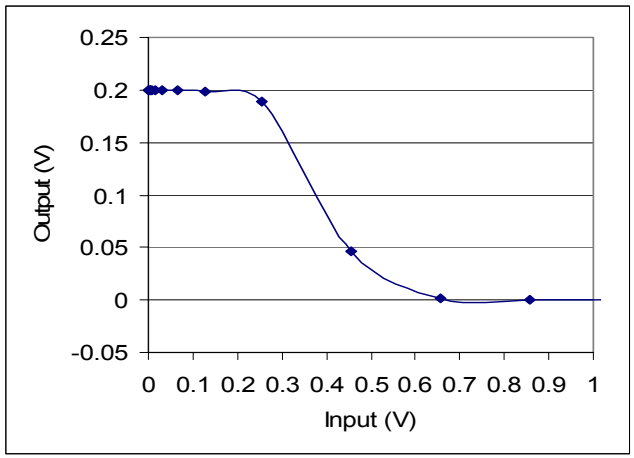
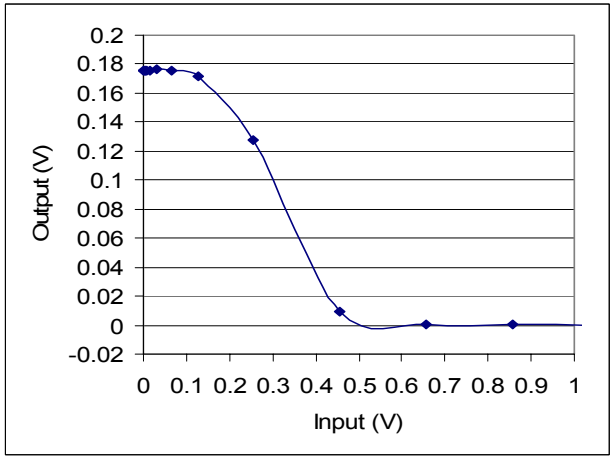


Figure 4.37 Shown are the catastrophic fault results on LCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 75% in their respective W/L ratio. In 4.47 (a) the error is in transistor M1, in 4.37 (b), the error is in transistor M2, in 4.37 (c) the error is in transistor M3, and in 4.37 (d) the error is in transistor M4.



(i)



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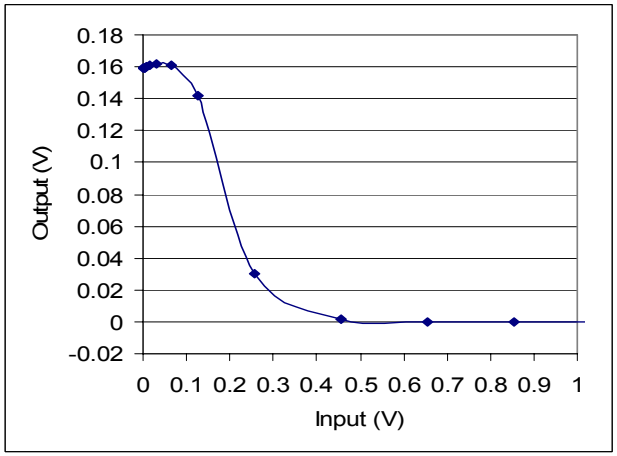

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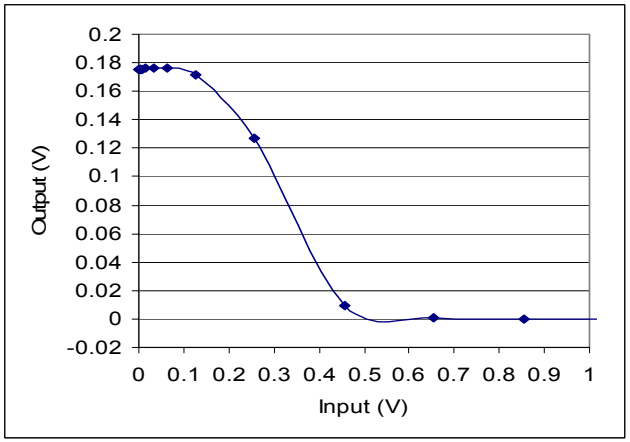

(d)

Figure 4.38 Shown are the catastrophic fault results on Vout2, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 4x in their respective W/L ratio. In 4.38 (a) the error is in transistor M1, in 4.38 (b), the error is in transistor M2, in 4.38 (c) the error is in transistor M3, and in 4.38 (d) the error is in transistor M4.

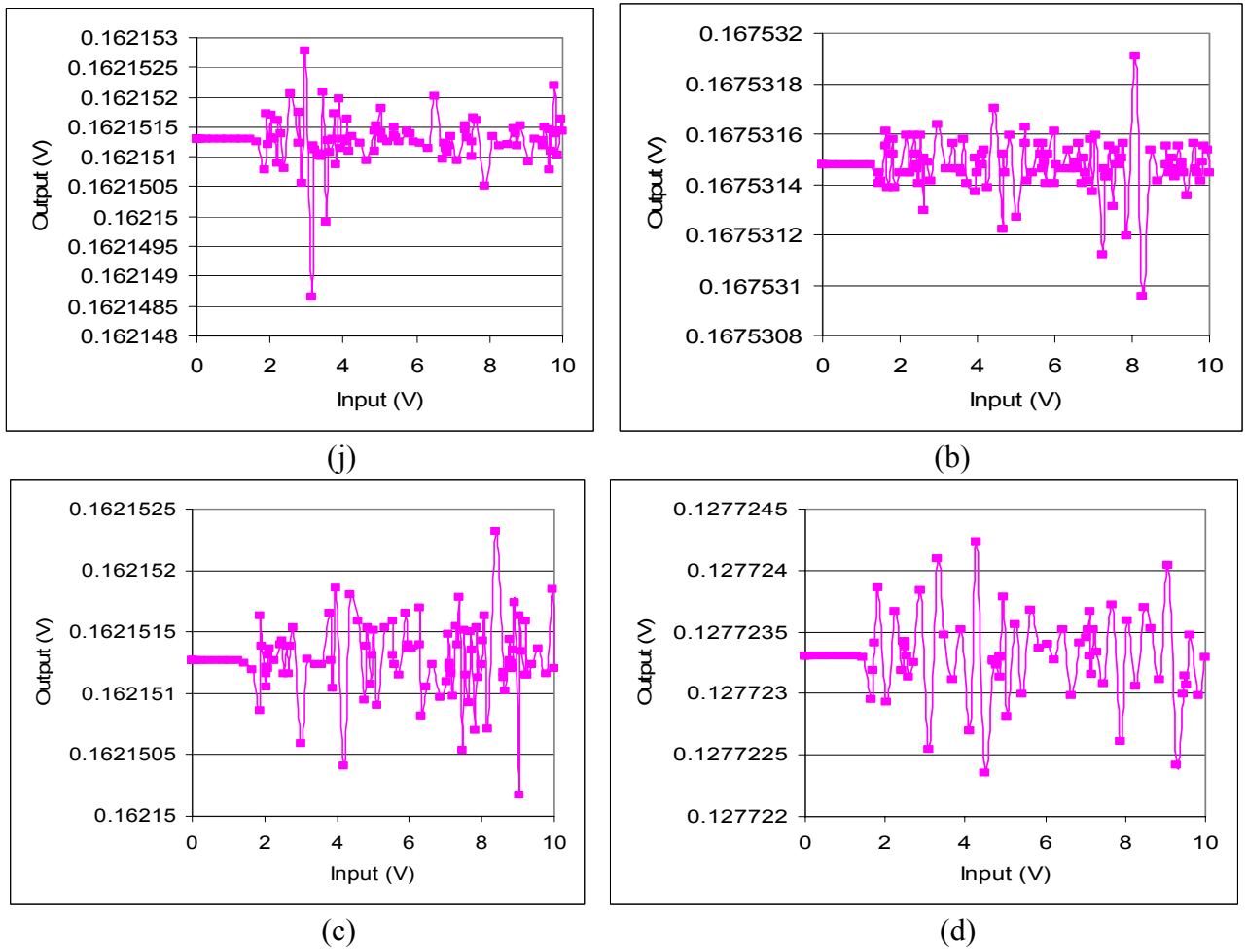

Figure 4.39 Shown are the catastrophic fault results on Vout1, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 4x in their respective W/L ratio. In 4.39 (a) the error is in transistor M1, in 4.39 (b), the error is in transistor M2, in 4.39 (c) the error is in transistor M3, and in 4.39 (d) the error is in transistor M4.

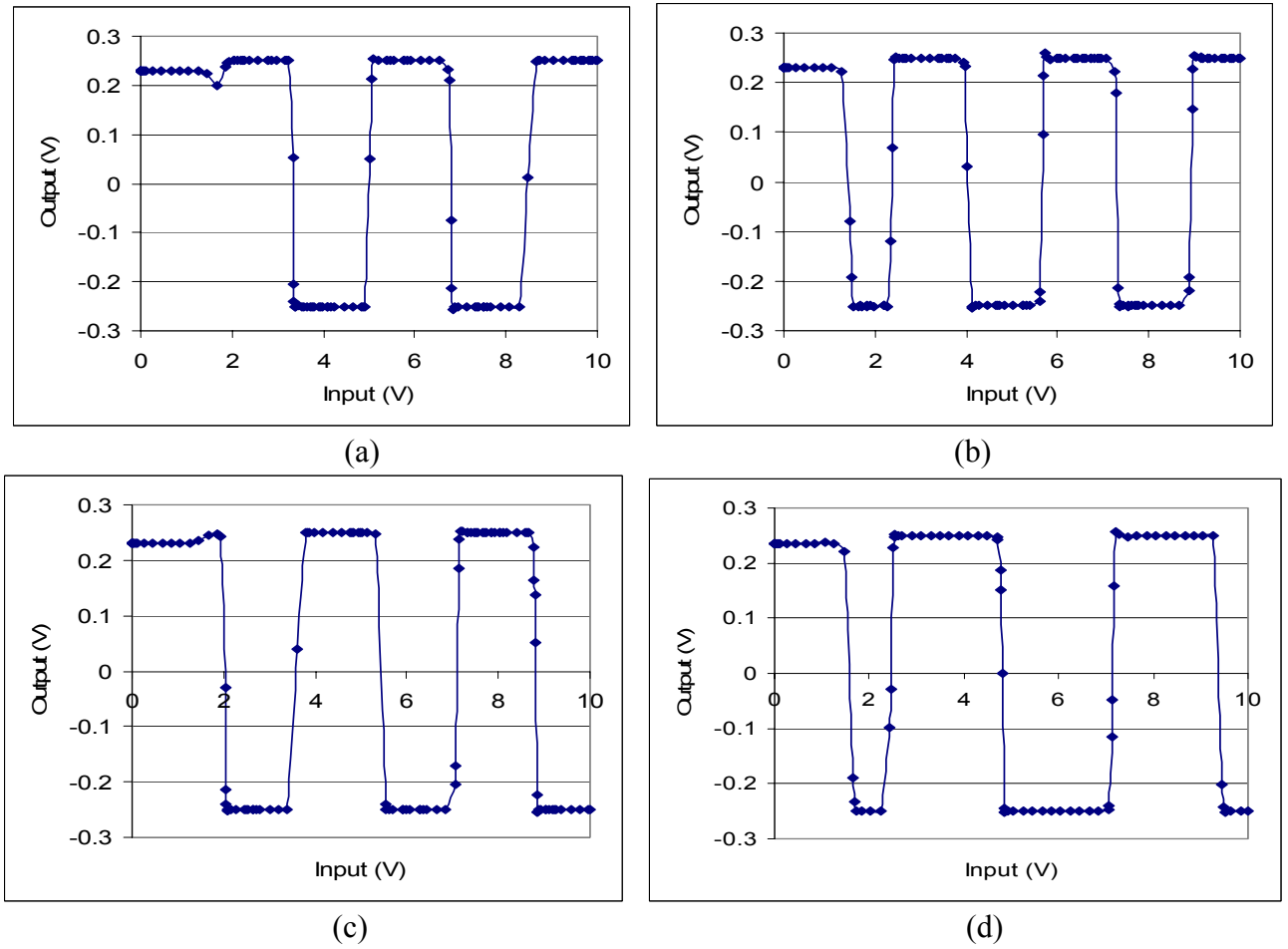

Figure 4.40 Shown are the catastrophic fault results on VCO, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 4x in their respective W/L ratio. In 4.40 (a) the error is in transistor M1, in 4.40 (b), the error is in transistor M2, in 4.40 (c) the error is in transistor M3, and in 4.40 (d) the error is in transistor M4.

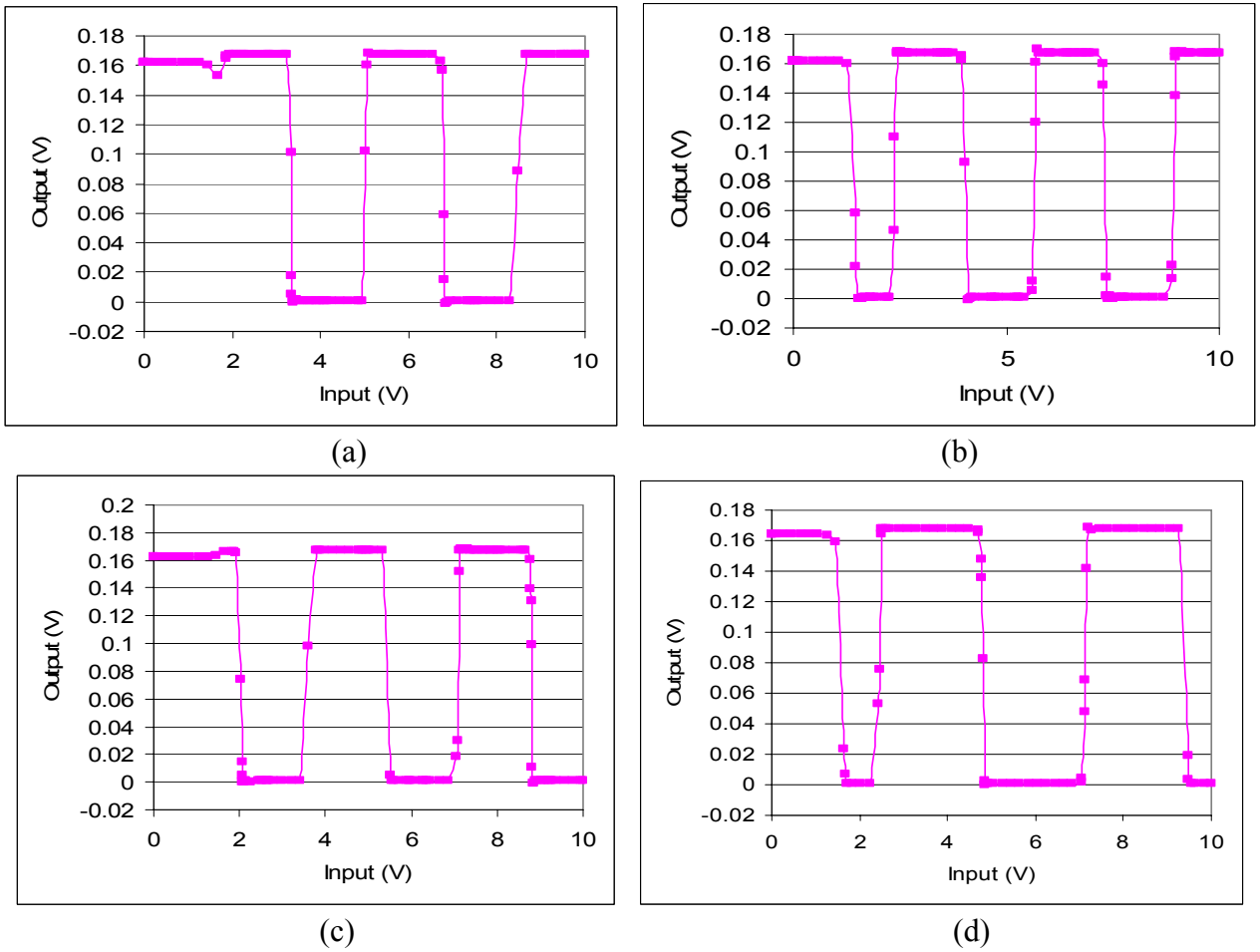

Figure 4.41 Shown are the catastrophic fault results on ZCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 4x in their respective W/L ratio. In 4.41 (a) the error is in transistor M1, in 4.41 (b), the error is in transistor M2, in 4.41 (c) the error is in transistor M3, and in 4.41 (d) the error is in transistor M4.

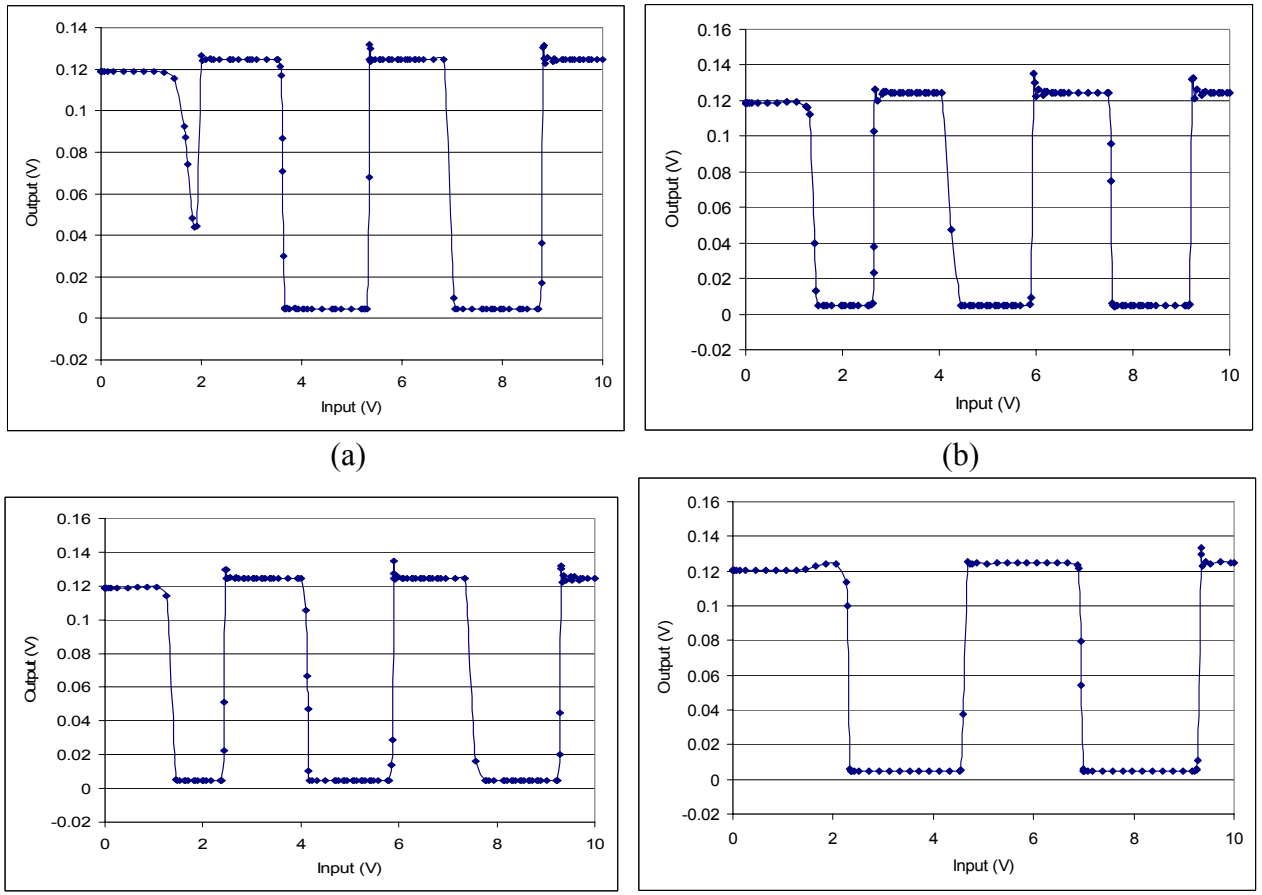

Figure 4.42 Shown are the catastrophic fault results on LCD, in which the four transistors for the VLSI adaptation of the Chemical Field Effect Transistors have an error of 4x in their respective W/L ratio. In 4.42 (a) the error is in transistor M1, in 4.42 (b), the error is in transistor M2, in 4.42 (c) the error is in transistor M3, and in 4.42 (d) the error is in transistor M4.

With New K Values (VLSI ChemFET)

Fault	90% of Expected W/L Ratio	25% of Expected W/L Ratio	400% of Expected Width Length Ratio
Mean Squared Error	1.86 e-10	18.02	1.945
FFT Matched Filter(MF)	3.78 e2	23.64	3.40 e2

Table 4-5 Biosensor Response Vout1

Fault	90% of Expected W/L Ratio	25% of Expected W/L Ratio	400% of Expected Width Length Ratio
Mean Squared Error	4.953	402.19	7.896
FFT Matched Filter(MF)	1.536 e2	4.757 e3	1.32 e2

Table 4-6 Biosensor Response Vout2

Fault	90% of Expected W/L Ratio	25% of Expected W/L Ratio	400% of Expected Width Length Ratio
Mean Squared Error	8.78 e-4	7.3 e9	2.07 e-1
FFT Matched Filter(MF)	2.328	8.98 e2	2.825

Table 4-7 Voltage Controlled Oscillator (VCO) Response

Fault	90% of Expected W/L Ratio	25% of Expected W/L Ratio	400% of Expected Width Length Ratio
Mean Squared Error	349.04	2.355e3	435.80
FFT Matched Filter(MF)	1.73 e2	1.67 e2	1.59 e2

Table 4-8 Zero-Crossing Detector (ZCD)

Section 4.4 System-on-Chip Model Outputs

In this subsection we compare the SoC model outputs for a biosensor circuit under test containing an normal KP-parameter value and one containing an adjusted KP-parameter value. The normal value is 5.048 e-5, while the adjusted KP-parameter value is 2.024 e-5. Table 4-9 below shows the period of oscillation for the normal KP-parameter biosensor. The conditions evaluated include the case in which no faults are found in the transistor, no faults are found in the new KP parameter transistor, a 10% parametric fault exists in the fluid under test transistor (M3), a 75% catastrophic fault exists in the fluid under test transistor, and a 400% catastrophic fault exists in transistor M3. In figure 4.43, we see the SystemC-based output of the OBIST model's response to each of these faults.

Biosensor Condition	Period of Oscillation (ms)	Equivalent SoC Cycle Time
No Faults, Normal K	3.0	30
10% Parametric Fault	3.0	30
75% Catastrophic Fault	4.2	42
4X Catastrophic Fault	2.8	28
New K Parameter, No Transistor Faults	3.35	34

Table 4-9 Parameters for the SoC Built-In Self-Test model. The period of oscillation and equivalent SoC cycle time was derived from the data in figures 4.11, 4.14, 4.18, 4.24, and 4.27. For the faults indicated, in all instances, the faults shown here existed in transistor M3, the fluid under test transistor.

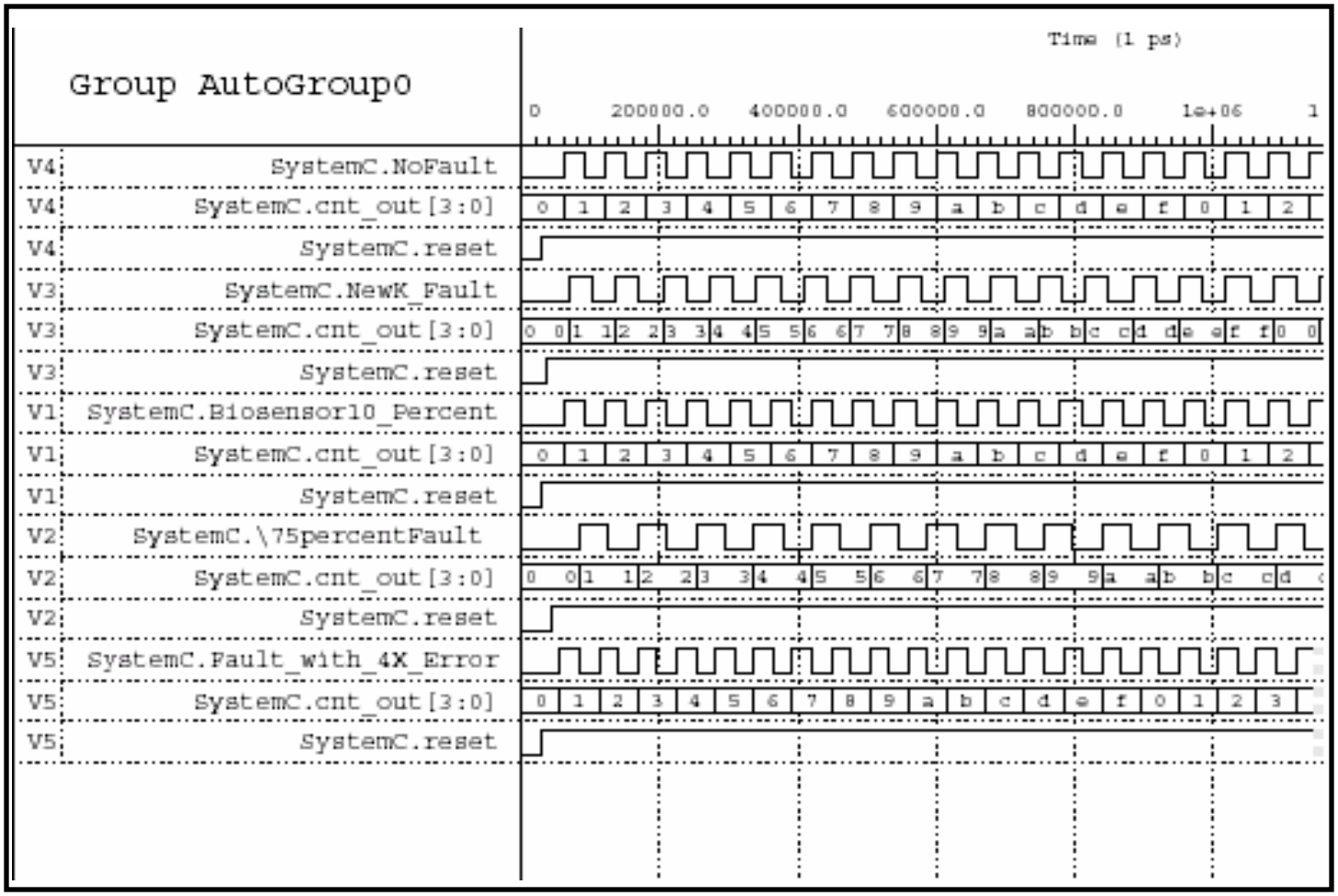

Figure 4.43 Output of SystemC based BIST Model. Here we see the results of a comparison of the faults indicated in the table above. Shown are clock-like signal outputs and counter results.

Table 4-10 shows the period of oscillation and equivalent SoC cycle time for the 10%, 75%, and 400% faults in a fluid under test transistor operating with a dielectric constant value that is 50% of the original dielectric constant value. We note the subtle differences in SoC Cycle Time for each of the faults in this table. The differences are more pronounced in table 4-9, in which the KP-parameter is twice that of the one shown in the analysis below.

Biosensor Condition	Period of Oscillation (ms)	Equivalent SoC Cycle Time
New KP Parameter, No Transistor Faults	3.35	34
10% Parametric Fault	3.5	35
75% Catastrophic Fault	3.25	33
4X Catastrophic Fault	3.65	37

Table 4-10 Parameters for the SoC Built-In Self-Test model with new KP parameter in biosensor circuit.

The period of oscillation and equivalent SoC cycle time for the above table, were derived from the data in figures 4.27, 4.30, 4.35, and 4.40. For the faults indicated, in all instances, the faults shown here existed in transistor M3, the fluid under test transistor.

In figure 4.43, we see the SystemC-based output of the OBIST model's response to each of these faults. It is interesting to note that the subtle differences in equivalent SoC Cycle time are easily detected by the OBIST method. For example, the counter assigns an output value of 17.5 (a mid-cycle 17) to the fault-free, new KP

parameter biosensor, a value of 17 to the 10% width/length ratio fault, a value of 18 to the 75% width/length parameter fault, and a value of 15 to the 4X width/length ratio fault.

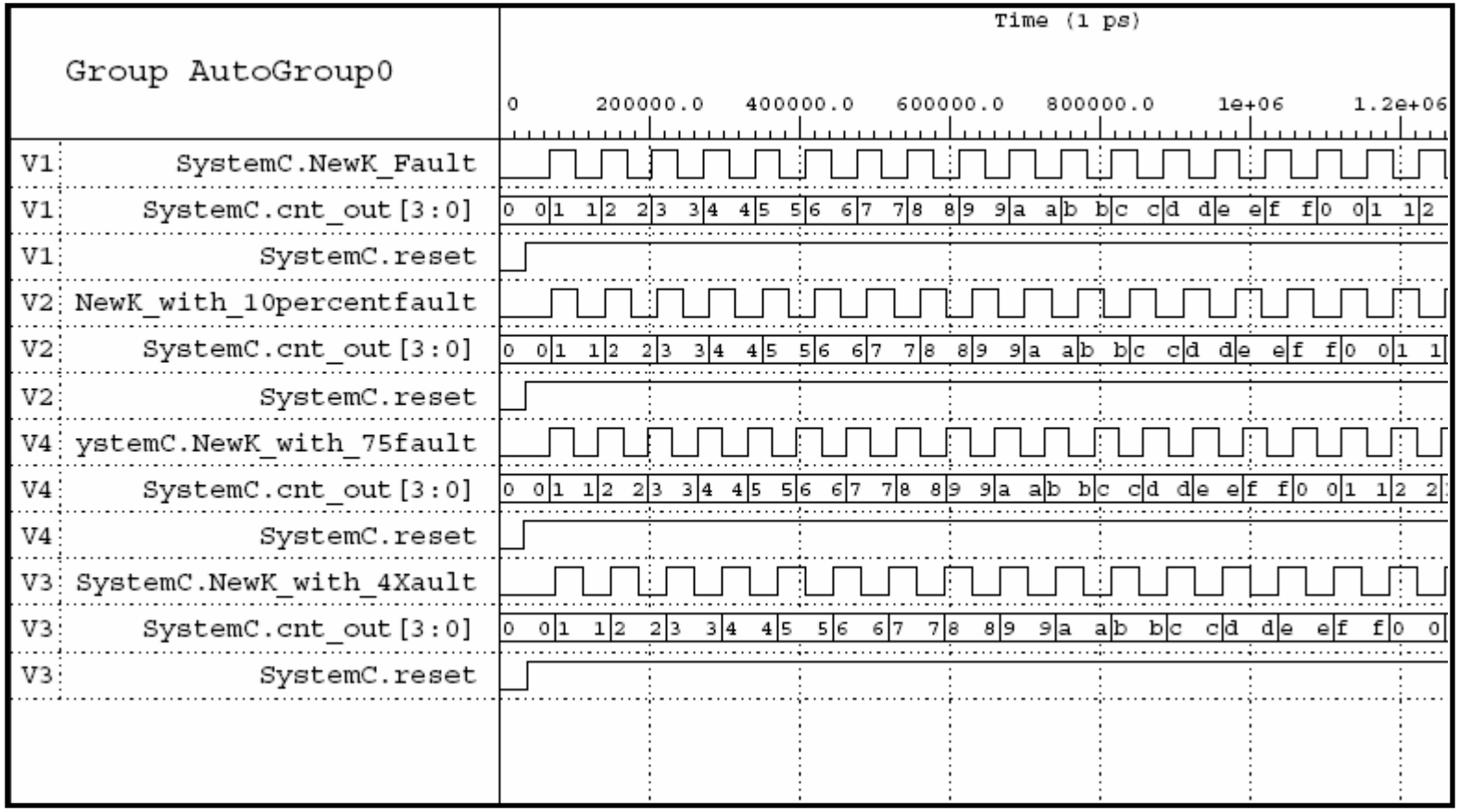

Figure 4.44 Output of SystemC based BIST Model with new K parameter for biosensor fluid under test transistor. Here we see the results of a comparison of the faults indicated in the table above. Shown are clock-like signal outputs and counter results.

Section 4.5 Summary

In this Chapter the results of biosensor analyses are presented. In section 4.2 we observe the unique response of the VLSI chemical field effect transistor to buffer, water, and air. We also see the sensitivity of the macromolecular sensor to the presence of nominal concentrations of DNA. In section 4.3 the results of the analog SoC oscillation-based built-in self-test are provided. Here the VLSI adaptation of the chemical field effect transistor is altered to contain several faults including a parametric fault and two catastrophic faults. Each of these is applied to individual transistors in the device. The output of the biosensor is fed into the input of the oscillation-based built-in self-test method to evaluate the impact of each of these faults against the OBIST. The OBIST is found through Spice simulation and SoC model simulation to be sensitive to the majority of the faults. In section 4.4, we see the outputs of the SoC models of the OBIST method's response to faults in the ChemFET.

Chapter 5 Conclusions and Open Problems

Section 5.1 Overview

This dissertation provides solutions to some of the roadblocks to development of systems-on-chip (SoCs) using analog mixed-signal (AMS) intellectual property (IP). One of the objectives of this dissertation is to bridge the gap between the development of analog IP cores and digital IP cores for the SoC domain. To this end, SystemC based SoC models of various analog sub-blocks are developed and tested. Another objective is to improve upon traditional methods of performing on-chip testing of analog and digital cores, while decreasing the amount of area overhead covered by the test structures. This is achieved through the development of an oscillation based built-in self-test (OBIST) method. The third objective is to investigate the aforementioned principles by creating an analog SoC. As such, a fluid analyzer system-on-chip is designed, fabricated, and tested. This dissertation's final objective involves investigations of novel biosensors for their ability to distinguish fluid properties such as antibody antigens, concentrations of DNA, and dielectric constant.

Subsection 5.1.1 Background in Analog System-on-Chip Devices

System-on-chip devices are single-chip entities comprised of multiple technologies. A typical system-on-a-chip can contain: analog-to-digital converters, amplifiers, smart signal processing elements, on-chip testing devices, and

microprocessors, to name a few. Each of these IP elements is referred to as a system sub-block, core, or macro.

Among the key components that should be included in all SoC designs is a method of performing on-chip test and evaluation of each system sub-block. On-chip tests should be comprehensive enough to cover a wide range of different types of macros, while limiting the amount of area overhead associated with the built-in self-test (BIST) method. Among the most common on-chip test procedures is the oscillation test strategy (OTS) described in chapter 2 of this dissertation.

SoC design also requires the development of models to simulate and test the effectiveness of cores prior to fabrication. SystemC is useful for creating SoC models and is a class library implemented in standard C++. It provides a modeling platform which enables the development and exchange of system-level C++ models. SystemC was developed by the Open SystemC Initiative (OSCI) and is available for free download through www.systemc.org. SystemC based models are created in chapter 3 section 3.5. They are evaluated in chapter 4 sections 4.2 and 4.3.

Subsection 5.1.2 Roadblocks Addressed in This Dissertation

The 2003 Technology Roadmap for Semiconductors indicates that the semiconductor industry focus has seen a significant shift. The introduction of application-driven technologies is the focus of today's new technology solutions. For example, digital microprocessors for personal computers have been joined by mixed-signal systems for wireless communications and embedded applications. Moreover,

the ubiquitous use for cell phones and wireless devices has made battery-powered mobile devices as strong a driver as wall-plugged servers. SoC designs that incorporate the use of intellectual property from multiple sources are supplanting single-source, in-house chip designs. The problem, however, is with the development of analog mixed signal intellectual property cores as analog IP core development lags far behind that of digital IP. This is largely due to the inherent complexity of analog circuitry. As such, little work has been done to develop analog IP for the SoC domain. To bring analog IP development in line with its digital IP counterpart requires the development of SoC models of the analog circuits as well as methods of performing on-chip self-tests for each IP core used.

While the OTS method has been effective in distinguishing the existence faults in CMOS amplifiers and related circuitry, flaws in the design exist, that make OTS ill suited for use in other devices. The first is that the method is based on the development of oscillations induced by feedback networks around the circuit under test (CUT). This is problematic as by the nature of the design, part of the output of a system is returned to its input in order to regulate oscillating outputs. This means, the error that exists in the circuit under test continues to be propagated throughout the system, making the oscillating output of no consequence should the error that is propagated nullify the existence of internal faults. The oscillation test strategy is further flawed as it consumes a large amount of chip area due to its use of multiple external resistors and a capacitor.

Section 5.2 Dissertation Results for fluid analyzer Analog System-on-Chip

Subsection 5.2.1 Oscillation Based Built-In Self-Test (OBIST)

An oscillation-based built-in self-test (BIST) method is presented for functional testing of mixed signal devices in chapter 3, section 3.4 and evaluated in chapter 4, section 4.3. One of the integral contributions of this method is that a voltage controlled oscillator is used to produce an oscillating signal from the analog output of a circuit under test. This signal varies with faults that exist in the CUT. The OBIST method was simulated in SPICE with components (including the voltage controlled oscillator and level crossing detector) fabricated in the fluid analyzer SoC. A second contribution of this method is the use of a zero-crossing detector, developed in chapter 3, section 3.4, to transform the oscillating VCO output into a digital clock like signal. The OBIST method is an improvement upon the oscillation test strategy in that less chip area overhead is covered by the OBIST due to the elimination of external resistors and capacitors. The other improvement involves the fact that faults recursively propagated through the OTS feedback network, are no longer a concern, due to the use of the VCO to produce oscillating outputs as shown in section 3.4. This prevents possible cancellation of fault detections in the CUT.

The OBIST contribution to analog intellectual property appear in the following: [66]

Subsection 5.2.2 Biosensors for Fluid Analysis

There are currently a number of off the shelf biosensors in industry today. The majority of these have application to the medical and food industries. There are

biosensors for monitoring: glucose levels [77], recombinant proteins in process media [78], and cell concentration and activity [79]. The majority of these sensors perform off-chip test tube chemical reactions whose fluorescence responses are measured with on chip LEDs. The glucose reader that has been manufactured since the late1960s detects blood sugar levels by measuring color changes on a chemical test strip. This method of monitoring glucose levels is commonly referred to as the "finger-stick" method. Many finger-stick glucose readers provide a digital display output of blood-sugar levels. In each of these examples, only one type of biological fluid can be evaluated.

The biosensors studied in this dissertation are more beneficial to the medical and food industries because they allow for the determination of multiple types of biological fluid characteristics on a single chip. This is because an array of biosensing field effect transistors can be fabricated on a single chip. In fact, each biosensor can be designed to be sensitive to a specific protein, strand of DNA, or other antibody antigen. Specific biological fluid sensitivity is created in some of the devices studied in this dissertation with the use of a self-assembled monolayer (SAM) treatment, applied to the gate of the transistors as shown in chapter 3, section 3.3 and chapter 4, section 4.2. The application of unique SAM treatments for specific strands of DNA or protein sensitivities is plausible for each sensing transistor in the array. This is unlike traditional off-the shelf biosensors, which target one biological property. The advantage of the second style of biosensor studied in this work, see chapter 4, section 4.2, is that without the use of additional surface chemistries, it too is capable of determining fluid properties of multiple types of fluids. This occurs

because of the device's ability to extract dielectric constants from fluids based on the input voltage applied to the sensor system. The novel devices mentioned here will be discussed in great detail in the next two subsections: VLSI Adaptation of CHEMFET (latter) and Evaluation of Gateless Field Effect Transistor (former).

Subsection 5.2.2.1 VLSI Adaptation of CHEMFET

A VLSI adaptation of a chemical field effect transistor is developed in chapter 3, section 3.3, from a set of transistors that operate in a whetstone bridge configuration. The novel aspect of this biosensor is that it acts a dielectric constant measurement device. It is a two stage device that is controlled by a voltage input. The voltage input that is applied to the CHEMFET to balance the output of the stages of the device (such that Vout1 = Vout2) is a function of the dielectric constant of the fluid under test (FUT) in stage 2. As such, the dielectric constant of the FUT can be extracted from the Vinput value. Specific details about the device operation and results are found in chapter 3, section 3.3, and chapter 4, section 4.2, of this dissertation. The VLSI adaptation of the CHEMFET used (for the first time) in this dissertation as a biosensor, was simulated, fabricated and tested for its response to buffer, water, and air, after the gate dielectric was etched out of the device. The analysis of this device appears in [67, 80].

Subsection 5.2.2.2 Evaluation of Gateless Field Effect Transistor

The macromolecular sensor described in section 3.3 was developed at the Naval Research Laboratory through research sponsored by the National Institute of Health. The device was designed, fabricated, and patented by [81]. Ten wafers containing 288 biosensing transistors each were fabricated. Prior to wafer dicing, each transistor was tested with a microprobe. Three wafers were tested in this dissertation. As such, several hundred transistors were tested prior to attachment chemistry processing. Of these fewer than 5% generated the appropriate drain current response. The remaining devices were treated as open circuits by the test system, developed at the Naval Research Laboratory [82]. The working devices were packaged, wirebonded, SAM-treated, and evaluated as part of the research of this dissertation. The results of the devices that survived the linker attachment chemistry appear in chapter 4. In addition, this dissertation contributed to the evaluation and simulation of threshold voltage response to charge trapping.

The gateless field effect transistor (macromolecular sensor) was evaluated for its effectiveness in detecting matches and mismatches in DNA strands of goat/antimouse IgG. Several concentrations of the IgG were tested, with the smallest concentration being dissolved in buffer at a ratio of 1 ng/ml. Several gateless field effect transistors responded favorably to the IgG DNA match solution. Two gateless field effect transistors showed a lack of sensitivity to the injection of the IgG DNA mismatch solution. These results were as expected. In addition to this, chapter 4, shows favorable drain current versus source-drain voltage response for a single

gateless FET to match and mismatch concentrations of strains of DNA. These results appear in the following proceedings [83].

These results were not repeatable from one packaged chip to the next and leads to an open problem discussed in section 5.4. This is due to inherent instability of the macromolecular sensor and to the harshness of the surface chemistry applied to the device. The macromolecular sensors instability was reflected in its failure to work consistently from one moment to the next. After 5-10 minutes of testing, sensors that were originally recorded as functioning properly would shift to open circuits. In fact, some sensors that were originally recorded (by the NRL test system) as open circuits, would be labeled functioning devices in later runs. Over the course of several days of testing, these circuits would eventually remain open circuits.

An explanation (developed in this dissertation) for the devices instability and overall lack of repeatability is that the devices are open circuits by design. The gateless depletion mode field effect transistor developed by the Naval Research Laboratory is fabricated with a source and drain only. For the majority of the sensors, the externally attached (platinum/gold electrode) did not register with the device. The presumption made by the inventors is that the fluid under test would reach the macromolecular sensor gate oxide area and through the use of an electrode form the appropriate metal gate contact. In this dissertation a test was performed to evaluate the fluorescents of the linker chemistry after application and to the macromolecular sensor. The evaluation, under microscope, showed that the chemical treatment was accurate (as the packaged chip area fluoresced) however, no fluorescence was seen over the gate-oxide areas suggesting that the open glass cut for these devices was too

small to allow fluid to penetrate. In the absence of the required gate oxide (fluid) contact, the devices must operate as open circuits. This argument could explain the 95% device failure rate.

Subsection 5.2.3 System-on-Chip Modeling

Analog SoC models for the VLSI adaptation of the CHEMFET, the depletion mode transistor, and the OBIST are developed in chapter 3, section 3.5, of this dissertation. These models are simulated as well. The simulation results appear in chapter 4, section 4.2. SoC model simulations for the oscillation-based built-in self-test, show favorable responses to the sensitivity of this on-chip test to parametric and catastrophic faults. The fault responses appear in the digital clock-like output of the system as changes in oscillation frequency. An SoC counter is used to generate an on-chip sum of zero crossings which assigns a numerical value to the clock-like signal. This number can be used to aide in the interpretation of a fault from a non-fault situation as it can easily be compared against the expected counter response number.

Section 5.3 Open Problems and Future Work

Subsection 5.3.1 Built-In Self-Test

The response of the built-in self-test simulations are favorable both at the SPICE and SystemC modeling levels, however, proof of concept through device

fabrication has yet to be determined. While the device was successfully fabricated using the MOSIS foundry processing, a catastrophic fault was found in one of the BIST test circuits, causing it to fail to produce any output response, oscillations or otherwise.

The current process of on-chip fault declaration involves outputting a fault-free CUT clock-like signal response (via a SystemC or SPICE model) and the fault CUT signal response to a computer monitor. An additional modification to the device, therefore, would involve the use of a simple output indicating whether or not the circuit under test operates within desired specifications. This could be achieved with an array of three LEDs which when lit (individually) could indicate that the device is: working, operating at 80% of the expected norm, or contains a catastrophic fault. When a catastrophic fault is detected, an automated method of performing parameter adjustment through the selection of on-chip device redundancies (extra biosensor circuitry, for example in the fabricated fluid analyzer SoC) should be developed.

A third improvement in the OBIST method would be to generate on-chip circuit under test oscillations using MOS oscillator circuits. These devices would further reduce the size of the system as the MOS oscillator circuits are produced with nano-technologies [84].

Subsection 5.3.2 System-on-Chip Modeling and Analog Intellectual Property

While this dissertation provides insight into the development of SystemC based analog models for various components of the fluid analyzer circuit, more work

needs to be done in the area of analog development. The analog devices developed herein are software implementations which can be downloaded from any web-site. One of the goals of the SoC industry is to provide analog intellectual property models for both hardware and software aspects of a design, both of which are downloadable from the web. As such, hardware equivalents of each of the SoC models must also be developed. The SystemC architecture does not currently support hardware analog SoC models, however work is being performed by members of the OSCI to make this possible [85]. The required architecture standards are discussed and applied to various analog circuits in [86], [87]. In [Subproject], a vibration sensor array is described with SystemC-AMS 0.12. In [Analog and Mixed-Signal], a signal processing dominated application is modeled. For each of these examples, the software aspects of the design dominate. Future work, therefore, requires the implementation of hardware models that possess the same level of robustness of the software counterparts.

Subsection 5.3.3 Biosensor Stability and Longevity

The biosensors evaluated in this work show good potential for consumer manufacturing, however, more work needs to be done to resolve stability issues and to make the device responses to specific fluids under test more consistent. To resolve stability issues, it is suggested that the open glass cut area over the gate oxide be made larger in order to ensure contact between the fluid under test and the gate oxide. This dissertation hypothesizes that contact was not made for the gateless depletion mode field effect transistor as the area over the gate failed to fluoresce under the

microscope. Designing larger devices overall would be best, with experiments showing the sensitivity effect of incrementally decreasing device size.

Once stability is reached, further testing and evaluation of the biosensors would involve the use of on-chip signal generators capable of applying the necessary system inputs. Ideally the outputs of the biosensors would include an IED response indicator light or digital screen output stating the positive or negative identification of materials in a fluid.

In addition, more work needs to be done to improve the sensor's shelf life. Typically off the shelf biosensors have, as a minimum, three-weeks of on-going reliable testability with minimal degradation in performance. The shelf-life of the macromolecular sensors ranged from minutes to several days. Increasing this shelf life to 3-weeks is necessary to ensure marketability of the devices.

Section 5.4 Summary

The solutions developed in this dissertation address many of the problems listed in chapter 1. This was accomplished through the development of an analog fluid analyzer system-on-chip. This device contains an array of biosensors, smart signal processing elements, and a built-in self-test core that includes parameter adjustment components. In this dissertation, an oscillation based built in self test (OBIST) on-chip test method is developed to determine faults that exist within each of the SoC macros. In this, particular attention is given to faults existing in a VLSI adaptation of the CHEMFET. This dissertation shows the development of SystemC

based analog SoC models for the OBIST, VLSI CHEMFET, and a simulated gateless field effect transistor. The dissertation shows the design, fabrication, and evaluation of biosensors capable of distinguishing fluids containing: antibody antigens (DNA), buffer, or variations in dielectric constant.

Publications based on these contributions appear in the curriculum vitae.

Appendix A: Trapped Charge

The degradation due to trapped charge Q_{ox}, results in localized build up of interface states (N_{it}) and oxide charges (N_{ot}) near the drain junction during hot-carrier stressing [88, 89, 90]. Several techniques are routinely used to electrically characterize defects at or near the interface in MOS transistors. The most practical methods are the charge-pumping, midgap, and dual-transistor-mobility techniques. There are potential advantages and disadvantages of using each of the above techniques. For example, the dual transistor-mobility and midgap techniques have the advantage of being simple to implement and generally provide accurate estimates of threshold-voltage shifts due to oxide traps and interface traps [91, 92, 93]. These estimates, however, become ineffective in the presence of significant charge lateral non-uniformities in the oxide [94] or at short times after irradiation [93, 95]. Charge lateral non-uniformities, have been found to have little effect on charge-pumping measurements [94]. Moreover, charge pumping is relatively easy to use, has high sensitivity to small interface-trap densities and can be applied to short-time measurements [94].

In analysis of the charge pumping (CP) the gate of the MOSFET is pulsed from accumulation to inversion using either a triangular, trapezoidal, or rectangular waveform. The substrate, source, and drain are shorted to ground. The dc current that develops in response to the electron-hole recombination at the interface states is measured at the source and drain. The charge pumping current that arises from an unstressed symmetric transistor is given by equation A.1 below [96]:

$$I_{CP}(V_{top}) = qfW\left[\int_{-y_m}^{-y_1} N_{it}(y)dy + \int_{y_1}^{y_m} N_{it}(y)dy\right], \text{ (A.1)}$$

Here the edges of the charge pumping zone are defined by $V_T(y_1) = V_{top}$ and $V_{FB}(y_m) = V_{base,min}$. For stressed transistors, the drain junction is the location in which interface changes and trapped charges occur. As such, local threshold and flat band voltage distributions are changed near the drain junction due to the presence of charges in the interface states and oxide traps. Therefore, the post stress charge pumping currents given by varying V_{base} and V_{top} are as shown in equation A.2 (a) and A.2 (b).

$$I_{cp,s}(V_{base}) = qfW\left[\int_{-y_1}^{0} N_{it}(y)dy + \int_{0}^{y_{1,s}} N_{it,s}(y)dy\right], \text{ (A.2 a)}$$

$$I_{cp,s}(V_{top,s}) = qfW\left[\int_{-y_m}^{-y_2} N_{it}(y)dy + \int_{y_{1,s}}^{y_m} N_{it,s}(y)dy\right], \text{ (A.2 b)}$$

In the above $N_{it,s}(y)$ is the post-stress interface-state density along the channel and the new (stressed) charge pumping edge $y_{1,s}$ is given by $V_{FB,s}(y1,s) = V_{base}$, where $V_{FB}(y)$ is the post-stress local flatband voltage distribution in the drain half of the channel. Similarly, the post-stress local threshold voltage distribution is $V_{T,s}$ and the edge $y_{1,s}$ will correspond to a new pulse top level defined by $V_{T,s}(y1,s) = V_{top,s}$. "$y_2$" is the unstressed charge pumping edge that corresponds to $V_{top,s}$ and is defined by

$V_T(y_2) = V_{top,s}$. $V_{FB,s}(y_m) = V_{FB}(y_m) = V_{base,min}$ because for y_m deep inside the junction, the N_{it} and N_{ot} generated at y_m are not significant to make any appreciable change in the V_{FB} distribution. At any point y along the channel, the post-stress local V_T and V_{FB} values are related to the pre-stress ones by equations A.3 and A.4 below:

$$V_{T,s}(y) = V_T(y) - \frac{q\Delta N_{ot}(y)}{C_{ox}} + \frac{q\Delta N_{it}(y)}{2C_{ox}}, \text{ (A.3)}$$

$$V_{VFB,s}(y) = V_{FB}(y) - \frac{q\Delta N_{ot}(y)}{C_{ox}} - \frac{q\Delta N_{it}(y)}{2C_{ox}}. \text{ (A.4)}$$

As such, the threshold voltage shift associated with trapped charge changes equation results in equation A.5.

$$V_{T,s}(y) = \frac{1}{C_{ins}}\left(qN_d x_d + Q_{ins}\right) - \frac{q\Delta N_{ot}(y)}{C_{ox}} + \frac{q\Delta N_{it}(y)}{2C_{ox}}, \text{ (A.5)}$$

Appendix B: List of References for Self-Assembled Monolayer Applications

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Appendix C: SystemC-based SoC Models of Sample Counter and OBIST

System-on-Chip (SoC) Model of Counter

The 4-bit counter example is made up of 5 pieces of code including cnt.h and cnt.cpp, the counter header file and c++ source file. "cnt_display.h" and cnt_display.cpp" are the display module header file and c++ source file. The counter testbench appears in "cnt_tb.cpp". The standard output for the counter was originally displayed in chapter 3 and repeated here for simplicity.

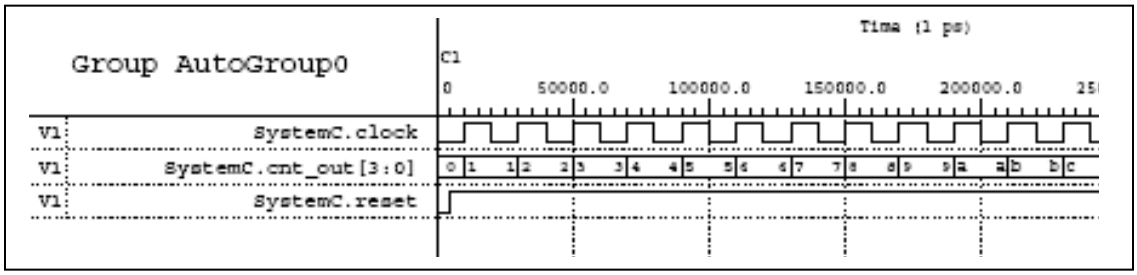

Figure A.1 System Response for SoC Counter

```
// main.cpp


#include "systemc.h"
#include "cnt.h"
#include "cnt_display.h"

int sc_main(int ac, char *av[])
{
      // signals //////////////////////
    sc_signal<bool> reset, clock;
      sc_signal<sc_uint<length> >   cnt_out;
      ////////////////////////////////

      cnt cnt1("cnt1");
      cnt1.reset(reset);
      cnt1.clock(clock);
      cnt1.cnt_out(cnt_out);

      cnt_display cnt_display1("cnt_display");
      cnt_display1.clock(clock);
      cnt_display1.cnt_out(cnt_out);


      sc_initialize();        //Initialize simulation


      // generate WIF file
//    sc_trace_file *tf = sc_create_wif_trace_file("cnt");
//    sc_trace(tf, reset, "reset");
//    sc_trace(tf, clock, "clock");
//    sc_trace(tf, cnt_out, "cnt_out");

      // generate VCD file
      //sc_trace_file *tf = sc_create_vcd_trace_file("cnt");
      //sc_trace(tf, reset, "reset");
      //sc_trace(tf, clock, "clock");
      //sc_trace(tf, cnt_out, "cnt_out");

//    reset.write(0);
//    clock.write(0);
//    sc_cycle(5);
//    reset.write(1);
//    sc_cycle(5);            // 1 clock cycle
//
//    for (int j=0; j<20; j++)
//    {
//          clock.write(1);
//          sc_cycle(10);
//          clock.write(0);
//          sc_cycle(10);
//    }

//    sc_close_wif_trace_file(tf);
//
      return 0;
}
```

```
// cnt.cpp

#include "cnt.h"

void cnt::cnt_process()
{
	if(reset.read()==0)
	{
		cnt_tmp = 0;
		cnt_out.write(0);
	}
	else if (clock.read()==1)
	{
		cnt_tmp = cnt_tmp + 3;
		cnt_out.write(cnt_tmp);
	}
}
```

```
// display.cpp

#include <systemc.h>
#include "cnt_display.h"

void cnt_display::display_process()
{
      cnt_tmp = cnt_out.read();
      cout << "counter value: " << cnt_tmp << endl;
}
```

```
// cnt_display.h

#include "systemc.h"

#define length    4

struct cnt_display : sc_module
{
      // port ///////////////////////
      sc_in_clk                     clock;
      sc_in<sc_uint<length> > cnt_out;
      ////////////////////////////////

      // internal signals
      sc_uint<length>   cnt_tmp;


      void display_process();

      SC_CTOR(cnt_display)
    {
            SC_METHOD(display_process);
            sensitive << clock.pos();
    };
};
```

Biosensor to OBIST Testbench

These are the main programs for chances in oscillation frequency of OBIST clock-like signal.

The following model encompasses the impact of the equivalent SoC cycle time for a biosensor with normal K and no fault and the biosensor whose fluid under test transistor. These devices have equivalent SoC cycle times of 30.

```
// main.cpp

#include "systemc.h"
#include "cnt.h"
#include "cnt_display.h"

int sc_main(int ac, char *av[])
{
        // signals ////////////////////
   sc_signal<bool> reset, clock;
        sc_signal<sc_uint<length> > cnt_out;
        ////////////////////////////////

        cnt cnt1("cnt1");
        cnt1.reset(reset);
        cnt1.clock(clock);
        cnt1.cnt_out(cnt_out);

        cnt_display cnt_display1("cnt_display");
        cnt_display1.clock(clock);
        cnt_display1.cnt_out(cnt_out);


        sc_initialize();          //Initialize simulation

        // generate VCD file
        sc_trace_file *tf = sc_create_vcd_trace_file("nofault");
        sc_trace(tf, reset, "reset");
        sc_trace(tf, clock, "nofault");
        sc_trace(tf, cnt_out, "cnt_out");

        reset.write(0);
        clock.write(0);
        sc_cycle(30);
```

```
        reset.write(1);
        sc_cycle(30);           // 1 clock cycle

        for (int j=0; j<20; j++)
        {
                clock.write(1);
                sc_cycle(30);
                clock.write(0);
                sc_cycle(30);
        }

        sc_close_vcd_trace_file(tf);

        return 0;
}
```

Testbench program for SoC model of 75% Catastrophic Fault

```
// main.cpp

#include "systemc.h"
#include "cnt.h"
#include "cnt_display.h"

int sc_main(int ac, char *av[])
{
        // signals ////////////////////
    sc_signal<bool> reset, clock;
        sc_signal<sc_uint<length> > cnt_out;
        ////////////////////////////////

        cnt cnt1("cnt1");
        cnt1.reset(reset);
        cnt1.clock(clock);
        cnt1.cnt_out(cnt_out);

        cnt_display cnt_display1("cnt_display");
        cnt_display1.clock(clock);
        cnt_display1.cnt_out(cnt_out);


        sc_initialize();          //Initialize simulation

        // generate VCD file
        sc_trace_file *tf = sc_create_vcd_trace_file("75Percent Catastrophic
fault");
        sc_trace(tf, reset, "reset");
        sc_trace(tf, clock, "75Percent ");
        sc_trace(tf, cnt_out, "cnt_out");

        reset.write(0);
        clock.write(0);
        sc_cycle(42);
        reset.write(1);
        sc_cycle(42);          // 1 clock cycle

        for (int j=0; j<20; j++)
        {
                clock.write(1);
                sc_cycle(42);
                clock.write(0);
                sc_cycle(42);
```

```
        }

        sc_close_vcd_trace_file(tf);

        return 0;
}
```

SoC OBIST model of 400% catastrophic fault in biosensor.

```
// main.cpp

#include "systemc.h"
#include "cnt.h"
#include "cnt_display.h"

int sc_main(int ac, char *av[])
{
        // signals //////////////////////
   sc_signal<bool> reset, clock;
        sc_signal<sc_uint<length> > cnt_out;
        ////////////////////////////////

        cnt cnt1("cnt1");
        cnt1.reset(reset);
        cnt1.clock(clock);
        cnt1.cnt_out(cnt_out);

        cnt_display cnt_display1("cnt_display");
        cnt_display1.clock(clock);
        cnt_display1.cnt_out(cnt_out);


        sc_initialize();          //Initialize simulation

        // generate VCD file
        sc_trace_file *tf = sc_create_vcd_trace_file("400Percent Catastrophic
fault");
        sc_trace(tf, reset, "reset");
        sc_trace(tf, clock, "400Percent ");
        sc_trace(tf, cnt_out, "cnt_out");

        reset.write(0);
        clock.write(0);
        sc_cycle(28);
        reset.write(1);
        sc_cycle(28);          // 1 clock cycle

        for (int j=0; j<20; j++)
        {
                clock.write(1);
                sc_cycle(28);
                clock.write(0);
```

```
            sc_cycle(28);
        }

        sc_close_vcd_trace_file(tf);

        return 0;
}
```

SoC OBIST model of new K parameter

```
// main.cpp

#include "systemc.h"
#include "cnt.h"
#include "cnt_display.h"

int sc_main(int ac, char *av[])
{
        // signals //////////////////////
   sc_signal<bool> reset, clock;
        sc_signal<sc_uint<length> > cnt_out;
        ////////////////////////////////

        cnt cnt1("cnt1");
        cnt1.reset(reset);
        cnt1.clock(clock);
        cnt1.cnt_out(cnt_out);

        cnt_display cnt_display1("cnt_display");
        cnt_display1.clock(clock);
        cnt_display1.cnt_out(cnt_out);


        sc_initialize();            //Initialize simulation

        // generate VCD file
        sc_trace_file *tf = sc_create_vcd_trace_file("newK_parameter");
        sc_trace(tf, reset, "reset");
        sc_trace(tf, clock, " newK_parameter ");
        sc_trace(tf, cnt_out, "cnt_out");

        reset.write(0);
        clock.write(0);
        sc_cycle(34);
        reset.write(1);
        sc_cycle(34);             // 1 clock cycle

        for (int j=0; j<20; j++)
        {
                clock.write(1);
                sc_cycle(34);
                clock.write(0);
                sc_cycle(34);
```

```
        }
        sc_close_vcd_trace_file(tf);
        return 0;
}
```

SoC models of the 10% parametric, 75% catastrophic, and 400% catastrophic faults are similar with changes in SoC cycle times of 35, 33, and 37, respectively.

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EDUCATION **2000- 2005 University of Maryland College Park, MD**
Doctor of Philosophy of Electrical Engineering, May 2005.

1996-1998 Stanford University Palo Alto, CA
Master of Science of Electrical Engineering, June 1998.

1991-1996 University of Maryland College Park, MD
Bachelor of Science of Electrical Engineering, 1996.

DISSERTATION PUBLICATIONS

1. Hodge, A.; Newcomb, R.; Hefner, A.; "Use of the oscillation based built-in self-test method for smart sensor devices", The 2001 IEEE International Symposium on Circuits and Systems, Volume 2, 6-9 May 2001, pp. 281 – 284 volume 2.
2. Hodge, A.M.; Newcomb, R.W.; "Evaluation of the VLSI adaptation of the CHEMFET, a biosensor for fluid analysis", IEEE International Symposium on Circuits and Systems, Volume 2, 26-29 May 2002, pp. II-580 – II-583.
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7. Hodge-Miller, A.M.; Newcomb, R.W.; “System-on-a-chip (SoC) Modeling of a Bio-MEMS Sensor”, IEEE International Workshop on Biomedical Circuits & Systems, 1-3 December 2004, Singapore.

ADDITIONAL PUBLICATIONS

1. R. W. Newcomb, C.-H. Yang, and A.M. Hodge, “Quantum Dot Neural Network Neurons”, ICARV 2002, Singapore.
2. C.A. Richter, E.M. Vogel, A.M. Hodge, and A.R. Hefner, “Differences Between Quantum-Mechanical Capacitance-Voltage Simulators”, Simulation of Semiconductor Processes and Devices 2001 (SISPAD-01) conference.
3. A.M. Hodge, R.W. Newcomb, M. Zaghloul, “Synchronizing the Oscillation in two coupled pairs of NTCs”, Proceedings ISCAS-1996.
4. A.M. Hodge, W. Zhen, R.W. Newcomb, “On the Inverse Hopfield Design of Neural Networks”, Proceedings: Conference on Signals and Systems (CASS-1996)
5. A.M. Hodge, R.W. Newcomb, “VLSI Chaos Generation, Hysteresis, and the Neural Type Cell”, Proceedings, World Congress on Neural Networks (WCNN), July 1995

WORK EXPERIENCE

DEPARTMENT OF DEFENSE (12/2001 – PRESENT)
ELECTRICAL ENGINEER/ RESEARCH SCIENTIST, NP-III

US ARMY: NIGHT VISION AND ELECTRONIC SENSORS DIRECTORATE
8-2003 to Present; 40 hours per week

- Analysis and Development of Algorithms for performing target detection and classification in long-wave, broadband mid-wave, hyperspectral, and shortwave infrared imagery.
- Principle Investigator for automated target detection and recognition of human intention for real-time thermal surveillance in urban warfare environments. Algorithm development, image analysis, data collection and assessment, project planning, resource solicitation, report writing, and program management.
- Survey Team Leader: Managed a team to conduct ground positioning systems (GPS) site surveys.
- Test director for infrared imagery data collections that targeted the development of problem sets.
- Acting Branch Chief

US NAVY: NAVAL RESEARCH LABORATORY
12-2001 to 8-2003; 40 hours per week

- Developed methodology for detecting fluidic flow using gateless field effect transistor.
- Worked on a team to develop CMOS sub-micron analog-to-digital converter.
- Performed functional testing for fabricated biosensors.
- Performed multivariate statistical analysis on biosensor device data.
- Performed post-processing of multi-technology biosensor device.
- Developed and analyzed architecture for multi-technology bio-compatible System-on-a-Chip.
- Published results of work can be found in the IEEE: International Symposium on Circuits and Systems-2002 and 2003 (ISCAS-2002, ISCAS-2003) conference proceedings and GOMAC-2003.
- Reviewed and prepared patents for biomedical/biotechnology devices and electrical circuitry.

DEPARTMENT OF COMMERCE
ELECTRICAL ENGINEER/RESEARCH SCIENTIST, ZP-III

NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
05-2000 to 12-2001; 40 hours per week

- Worked in Power Devices Group of Semiconductor Electronics Division. Main project goals revolved around development of metrology issues and

procedures to integrate multiple device technologies onto a single silicon substrate.
- Established Built-In Self-Test (BIST) method for multi-technology biosensor system.
- Completed research proposals for investigation of built-in self test (BIST) of biosensor devices and System-on-a-Chip (SoC) devices
- Investigated using a VLSI adaptation of the Chemical Field Effect Transistor (CHEMFET)as a biosensor device
- Fabricated biosensor circuit with aide of L-Edit and Mosis Design services
- Received training in processing of semiconductor devices including performing dry/wet etches, RCA clean processes, photolithography, and resist spinning
- Used Medici to uncover metrology issues associated with CAD device simulators
- Researched metrology and standardization issues associated with System-on-a-Chip devices. Researched standardization issues related to block-based design processes
- Published results of work can be found in the IEEE: International Symposium on Circuits and Systems-2001 (ISCAS-2001) conference proceedings

ALLIED SIGNAL AEROSPACE
ELECTRICAL ENGINEER – SUMMER CO-OP

05-1996 to 09-1999; 40 hours per week; (12 Months Total)
- Researched redundancies in commercial aircraft systems
- Designed program for the Enhanced Ground Proximity Warning System, EGPWS
- Worked with contractors in area of Imaging Systems
- Used Matlab to assist in development of a computer simulation of meteorological radar systems.
- Debriefed team managers, monthly, on status of simulator
- Worked with AlliedSignal employees in the area of VLSI
- Created library for 1.2 micron bulk process
- Investigated Synopsys Synthesis Tool, a computer package used to evaluate VLSI designs.
- Presented findings of research to AlliedSignal Managers
- Provided weekly updates at staff meetings
- Evaluated Mentor Graphics FlexTest tool, a computer program used to test VLSI designs for accuracy. Evaluated Electrical Rules Checker
- Regression tested a CMOS .8 micron library using Mentor Graphics tools;

UNIVERSITY OF MARYLAND AT COLLEGE PARK
RESEARCH ASSISTANT

09-1994 to 08-1996; 20 hours per week;
- Analyzed coupled CMOS Neural Type Cells (NTCs) that operate with the aid of an NTC synchronizer
- Created chaos in all MOS Neural Type Cell
- Published results of work can be found in ISCAS-96 conference proceedings and proceedings of the World Congress on Neural Networks, July 1995

SILICON GRAPHICS INTERNATIONAL, SGI
COMPUTER PROGRAMMER/INFORMATION TECHNOLOGY – SUMMER CO-OP

05-1995 to 09-1995; 40 hours per week; (3 months total);

- Computer Programmer: Perl, HTML, CGI-BIN Scripts
- Created web-based market driven quality surveys
- Updated department members weekly on the status and findings of the surveys

INTERNATIONAL BUSINESS MACHINES, IBM
INFORMATION TECHNOLOGY SPECIALIST – SUMMER CO-OP

06-1992 to 09-1993; 40 hours per week; (7 months total);

- Reviewed Knowledge-Base (Artificial Intelligence Systems) programming paradigms
- Conducted Market Driven Quality (MDQ) surveys
- Reported on results of MDQ surveys
- Trained department members to run, update, and utilize, The Integrated Reasoning Shell (TIRS) knowledge base system.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
ENGINEERING RESEARCHER - SUMMER CO-OP

NASA/GODDARD SPACE FLIGHT CENTER
06-1990 to 09-1991; 40 hours per week; (4 months total);

- Researched quality assurance issues associated with the procurement of flight safety systems
- Researched affects of phosphorus deficiency in soybeans
- Published results of research can be found in 1990/1991 GSFC SHARP research book.

INVENTION DISCLOSURES
PATENT APPLICATIONS

"ANALOG-TO-DIGITAL CONVERTER APPARATUSES AND METHODS", filed in the United States on January 31, 2005, and assigned serial no. 11/053,756.

End Notes

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