ABSTRACT

Title of Dissertation: EFFECT OF SURFACE FINISHES AND INTERMETALLICS ON THE RELIABILITY OF SnAgCu INTERCONNECTS

Yunqi Zheng, Doctor of Philosophy, 2005

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Power semiconductor devices are used in a wide range of applications, including power supplies and motor control. In these applications, power semiconductor devices are required to handle large currents and as a result they tend to dissipate large amounts of heat. In addition, the device and their attendant packages must be capable of withstanding power cycling for many years. Traditionally, devices have used high lead die attaches for high electrical and thermal conductivity. Now, with the drive in industry to replace lead-contained solder with lead-free solder alternatives, there is a drive to assess lead-free solder to use as the die attach in power device packages. This dissertation assesses the reliability of Sn3.5Ag0.8Cu lead-free die attach under accelerated power cycling conditions, especially the effect of surface finishes from the die and the substrate on die attach reliability because of the thin die attach thickness (<100μm), which is expected to increase the influence of intermetallics formed at the interfaces on the joint reliability.

The main part of the thesis is to evaluate the power-cycle reliability of Sn3.5Ag0.8Cu die attach in power MOSFET modules subjected to power cycling. Accelerated power cycling tests, failure analysis, thermal transient analysis and thermo-mechanical modeling were conducted. 3D thermal analysis correlated an increase in the package thermal impedance to the amount of crack propagation and determined that crack initiation is the limiting process under power cycling. In the experiments, die tilt was observed and die attach cracks always occurred near the middle of the bond line on the side with thicker die attach. This is not addressed in typical thermo-mechanical simulations on solder joint reliability. Such simulations predicted that the thinner side exhibits higher stress than the thicker side and were expected to be easier to fail. Microstructural characterization provided evidences that microstructure of die attach changes with thickness. First, a higher Ag_3Sn concentration was observed in the thinner die attach due to dissolution of Ag from backside die. Second, a more uniform distribution of Ag_3Sn precipitates exists in the thinner die attach due to faster cooling. So a thinner Sn3.5Ag0.8Cu die attach is more resistant to fatigue failure even under higher stresses.

EFFECT OF SURFACE FINISHES AND INTERMETALLICS ON THE RELIABILITY OF SnAgCu INTERCONNECTS

by

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Dissertation submitted to the faculty of the Graduate School of the
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DEDICATION

To my parents, husband, and advisor

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Chapter 1 Introduction

1.1 Power semiconductor package

Power semiconductors are used in a wide-range of commercial and industrial applications, which require switching of high current or voltage, such as the following[1]:

1. Power supplies
2. Electrical machine control
3. Heating and lighting
4. Automotive electronics
5. Electrochemical processing

The typical life cycle requirements for power devices range from 10 years (pumps) to more than 30 years (locomotive traction) [3]. IGBTs (Insulated Gate Bipolar Transistors) and MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) are the most common power semiconductor switching devices for high power and high frequency respectively. These power semiconductor devices are often packaged in multi-chip packaging systems. (See Figure 1. 1) The large amount of power dissipated by the devices (as high as megawatts for IGBTs and kilowatts for power MOSFETs) creates a large amount of heat, even if the device has a high level of device efficiency. This power dissipation results in a temperature increase when the devices are on and a decrease when the devices are off. Such power cycling is one of the main causes of failure in the packaging system.

The reliability of a power module depends largely on its package structure.[2] The package (Figure 1. 1 & Figure 1. 2) has to provide a convenient method for electrical current to flow to and from the device, and give mechanical support to the device, while enabling heat generated by the devices to be conducted away to the ambient. Typically, power modules consist of several layers including the die, die attach, Direct Bond Copper (DBC) substrate, substrate attach and a copper base plate (or heat spreader). The layers are designed to be thin and large in area in order to dissipate heat efficiently. DBC substrates, for example, consist of a thermally conductive ceramic (usually Al_2O_3 or AlN) layer with the thickness of around 0.635mm sandwiched between two copper layers with the thickness around 0.3mm. To complete the packages, large diameter (125~375μm)

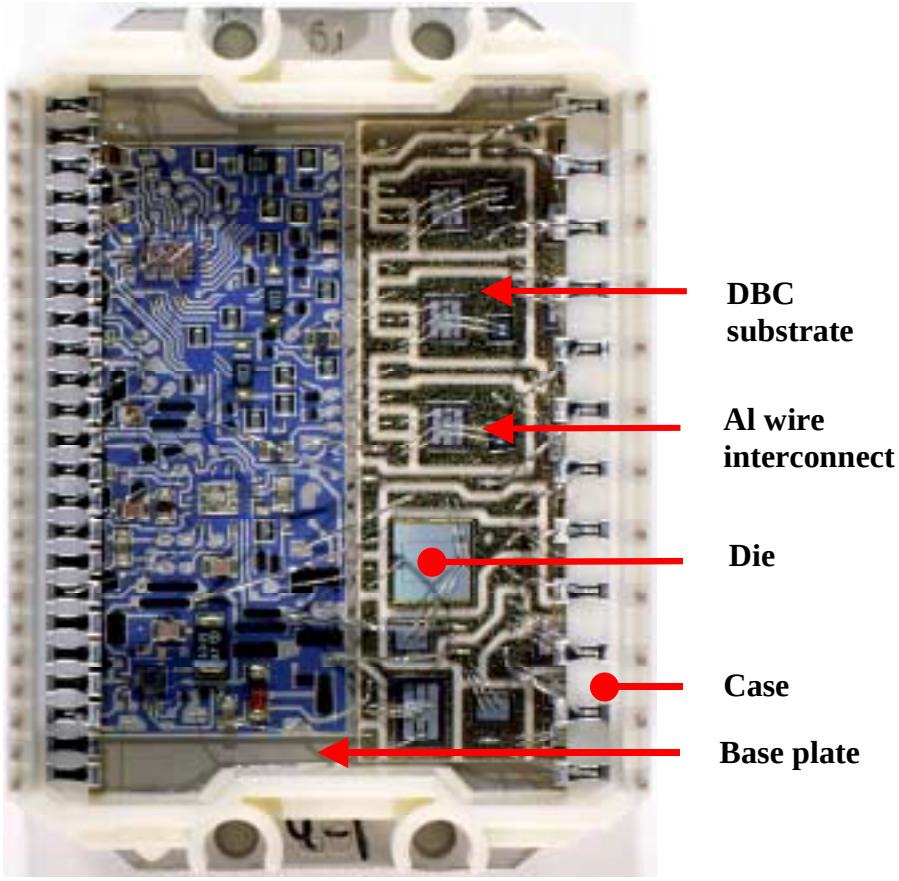


Figure 1. 1 Actual power module used in pumps (Courtesy of Grundfos A/S)

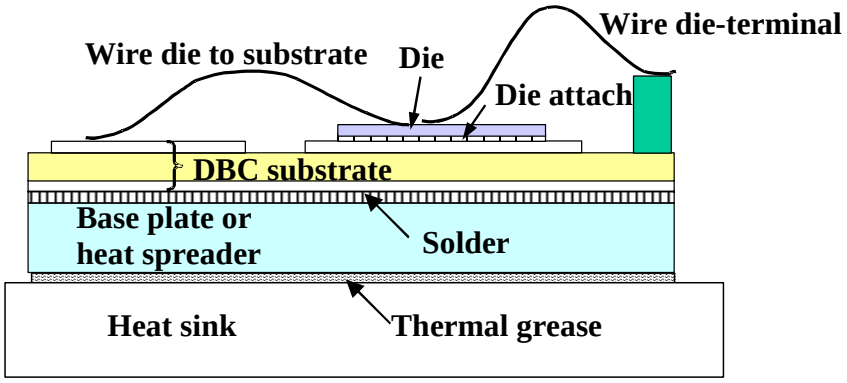


Figure 1. 2 Cross-section of a typical structure of a power module

aluminum wires are used to interconnect the die, substrate, and terminals. The heat spreader (or base plate) is often attached to a heat sink through thermal grease to dissipate the heat.

During application, packages experience temperature fluctuations introduced by the switching operation. Different layers in the package have different coefficients of thermal expansion (C.T.E), so they will expand/contract at different rates in response to this fluctuation. The different expansions generate thermal stress in the modules, especially in the solder attach and wire bonds. In fact, thermal stress induced die attach fatigue cracking has been reported as a major failure mechanism for power MOSFETs. It is critical that the die attach is able to sustain the thermo-mechanical stress generated by power on/off operation over intended life span of the module.

1.2 Why SnAgCu die attach

In power modules, metallic solders are used for die attach because of their thermal and electrical conductivity. The solder material used to attach the die to the substrate can be categorized into two groups: hard solders and soft solders.[5] Hard solders are usually gold-based eutectics such as Au-3%Si, Au-12%Ge and Au-20%Sn. Those solders have high strength and do not quickly degrade from fatigue damage during power cycling. However, they are expensive and will transfer high stresses to the die, which may cause die fracture for any but the smallest die (<5mmx5mm). On the other hand, soft solders, including virtually all low-melting lead-, tin- and indium- based solders, have low strength and high ductility. During temperature or power cycling, these solders transmit very little stress to the die. Therefore those solders can be used to join much larger die and are also relatively inexpensive. Of these solders, the ones with the highest melting points are high lead-solders (T_{melt}>290°C). As a result, high lead solders such as Pb5Sn, Pb10Sn are extensively used in the power semiconductor packages, despite the fact that they often experience extensive fatigue cracking.

The toxic effects of Pb, however, have brought about the reduction or elimination of Pb in many applications. For example, in the Europe Union, there is a lead-free directive, the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS), banning several materials including lead (Pb). Today passenger vehicles in the United States operate on lead-free fuel. The use of Pb has been banned in the manufacture of paint due to the health hazard posed to children. [8] Although the use of Pb in the electronics industry accounts for less than 7% of the total Pb consumption in

the U.S., pressure is mounting to remove Pb from electronic manufacturing processes. At the moment, high lead solder die attach that used in power semiconductors packages are not subjected to ban, since the related applications are usually involves long life cycles and good candidates to replace high lead solder in those applications is yet to be determined. In response to the concern over Pb used in electronic products and manufacturing applications, efforts have been ongoing to find acceptable Pb-free solders. The U.S. National Electronics Manufacturing Initiative (NEMI) in USA recommends SnAg3.9Cu0.6 for surface mount reflow soldering and SnCu0.7 for wave soldering, and the Japan Electronic Industry Development Association (JEIDA) selected Sn3.5Ag0.75Cu, Sn(2~5)Ag(>5)Bi(0.5~4)Cu, Sn0.7Cu0.3Ag and Sn57Bi1Ag.[9] The IDEALS consortium in Europe preferred SnAg3.8Cu0.7 for reflow soldering and SnAg3.8Cu0.7Sb0.25 for wave soldering. The SOLDERTEC lead-free roadmap in Europe recommends alloys in the range SnAg(3.4-4.1)Cu(0.45-0.9) for reflow and wave soldering.

These lead-free solders are usually tin-based (>90%wt) with a small percentage of other elements such as Cu, Ag, Bi or Sb. Some of them, such as Cu and Ag, easily form intermetallics with Sn. Another common characteristic of these lead-free solders is that their melting point (around 220°C) is much higher than Sn37Pb solders (183°C). Presently, The SnAgCu family is undergoing a great deal of study for use as a component attach.[10] The study of SnAgCu used as die attach in power semiconductor packages is rather limited compared to its application in other packaging systems.

1.3 Die attach fatigue

In order to replace lead-tin solder with SnAgCu as the die attach material of choice in power semiconductor packages, it is necessary to develop a guideline to evaluate the thermo-mechanical fatigue life of the SnAgCu die attach.

The ability of die attach used in the power module to withstand power cycling with failure is a function of many parameters such as device design (size of the die, solder composition and mechanical properties, thickness of solder, etc.), fabrication process (method of soldering, soldering temperature, soldering atmosphere, package ambient, etc.) and cycling conditions (power input, junction temperature, cycling time, cooling methods, etc.). It is necessary to consider the critical parameters that most influence die attach fatigue.

1.3.1 Critical factors influencing die attach fatigue

There have been many studies of the reliability of solder die attach used in power modules under accelerated temperature/power cycling test conditions. Those studies are helpful in understanding the failure mechanisms and the critical factors that influence die attach fatigue life.

Several experiments[4][14][15][16] have been conducted to evaluate lead-tin solder fatigue in power modules under temperature/power cycling. In the module, solder tested is located either between die and substrate or between substrate and base plate. The results show that cycles to failure are correlated to either the temperature change (ΔT)

during temperature cycling or junction temperature change (ΔT_j) during power cycling. Based on experiments, Ciappa[21] and Naderman[15] have proposed a fatigue model, which correlates N_f to ΔT under temperature cycling through a power law relationship.

ΔT is not the only critical factor. One study[103] has experimentally determined that the thickness of die attach is another critical parameter in determining the fatigue life of die attach and thicker die attach leads to longer fatigue life.

The critical effects of both ΔT and the thickness of die attach is logical since they are both related to level of cyclic stress/strain due to a C.T.E. mismatch between different layers, the direct cause for die attach fatigue failure. Cracks in die attach usually initiate from the edges and propagate toward the center since cyclic stress/strain usually reaches maximum on the edges, although cracking at one side is also observed under die tilt. [103] Consequently, researchers have focused on determining the cyclic stress/strain and correlating them to the fatigue life of the die attach.

In addition to the cyclic loading conditions and the geometry of the packages, the mechanical properties of the solder die attach are also important, as will be discussed in detail later.

1.3.2 Thermo-mechanical analysis on die attach fatigue

In order to evaluate the stress and strain, especially the maximum stress/strain in the ends during cyclic loading, either a simplified analytical model or FEM analysis can be used.

Then an empirical fatigue model is developed to correlate the cyclic strain/stress to the cycles to failure based on experiments.

There have been several studies to develop an analytical die attach fatigue model based on cyclic shear strain (γ) for lead-tin solder[5][22] under power cycling. Typically there are two challenges: First, how to incorporate the elastic, time-independent plasticity, and time-dependent visco-plasticity (creep) properties of the solder. Dennis et al[5] assumed that all the shear strain due to C.T.E. mismatch between die and substrate ($\Delta\alpha\Delta T_j L/thickness$) is completely converted to plastic strain. However, this assumption overestimates the plastic strain. R. Sundarajan et al [22] has also proposed a model to incorporate the elastic, plastic and creep properties of the die attach into the stress model, but it involves a very complex partial differential equation and is difficult to solve numerically.

Secondly, how to capture the temperature changes in the module. R. Sundarajan et al [22] simplified this by using average junction temperature change (ΔT_{jm}) and substrate temperature change (ΔT_{sm}). ($(\alpha_j \Delta T_{jm} - \alpha_s \Delta T_{sm})L/thickness$). This assumption certainly decreases the accuracy of the model since not only the junction temperature change (ΔT_j), but also transient temperature change and the temperature gradient across the module are important to die attach fatigue. This is because the ramp rate under power cycling is usually faster than temperature cycling, making the transient temperature effects more pronounced and limiting the creep deformation per cycle. Ramp up/down state plays a larger part of the cycle. Engelmaier[6][7] suggested that the thermal stress under power

cycling is different from temperature cycling. Herr et al[16] compared the crack distribution between the power modules under power cycling and those under temperature cycling. They found the crack under temperature cycling grows uniformly from corners; but under power cycling, the crack are distributed more irregularly throughout the area and are more affected by voids. Conclusively, it is necessary to accurately capture the temperature profile of the power modules under power cycling conditions and apply it to the stress analysis,

Finally, other stress/strain components than shear strain could be important to the die attach fatigue and should not be neglected. For example, under power cycling, the temperature gradient across the power module will cause normal stress. This certainly changes the stress distribution and could induce other stress critical components such as hydrostatic stress, since a compressive hydrostatic stress can suppress crack formation. [118]

These challenges make analytical models less applicable than FEM based model, which can overcome these challenges. First, in FEM modeling, the nonlinear properties for the solder are easily incorporated to capture die attach deformation. FEM based modeling on the solder joints are extensively used in other types of packages, such as Ball Grid Array (BGA) packages, has been extensively used. [23][24][25]

Secondly, through transient thermal FEM analysis, the temperature profile for the power model is easy to be captured. J. Wilde et al[26] has proposed a method to evaluate the

thermal mechanical stress in the Pb5Sn2.5Ag substrate attach under power cycling. First, a 3D thermal analysis is conducted to obtain the temperature profile under power cycling. Then the temperature profile is transferred to the 2D diagonal stress analysis. This is a good approach that successfully takes power cycling into account.

Finally, it is easy to estimate normal stress as well as hydrostatic stress in FEM. FEM simulation can also estimate the effect of constraint posed by both the die and the DBC substrate. It has been reported that for thin adhesives used to bond non-deforming metals, constraint provided by the base metals can restricts the transverse contraction of the soft adhesive under tensile loading could make thinner adhesive stronger. [119][120]

In addition, during power cycling tests, die attach cracking will increase thermal impedance from the junction to the base plate. As a result, the increase in thermal impedance can be monitored during power cycling and used as an indication of crack propagation. It has been reported that once thermal impedance starts to increase, it increases dramatically[103][18]. However, the relationship between increase in the thermal impedance and crack propagation has yet to be established quantitatively, which can also be evaluated through thermal transient analysis.

1.3.3 Constitutive properties of SnAgCu solder

The constitutive model of the solder alloy is needed to evaluate the deformation occurring in the die attach and usually includes elasticity, rate-independent plasticity and rate-dependent creep.[39]

Elastic deformation is usually described, where Young's modulus, E, is used to represent the linear relationship between stress and strain. E is a temperature-dependent material constant. Elastic deformation is recoverable; where as inelastic deformation is permanent deformation. For a solder alloy, a large amount of inelastic deformation usually occurs during temperature cycling or power cycling, and it is the ultimate cause of fatigue failure.

Some studies separate inelastic deformation into rate-independent plasticity and rate-dependent creep.[39] A power law is used to represent the plastic flow.

$$\gamma_{pl} = C_{pl}\tau^{n}$$

Under a constant load or stress, solder also undergoes progressive inelastic strain over a period of time, called creep.

When the test specimen is subjected to a constant load, the initial, instantaneous response includes elastic and time-independent plastic flow. After the initial response, the effects of creep then occur in three stages: primary, secondary and tertiary creep (see Figure 1.5). During primary creep, metals strain-harden. The creep strain rate decreases over time, as hardening of the metal makes creep increasingly difficult, leading to a region of steady rate called the secondary creep. For most metals, secondary creep is the dominant deformation mode at temperatures above half the melting point(T_m) in degrees Kelvin. The melting point for eutectic SnAgCu is 217°C = 490°K and 1/2 T_m = 245°K = - 28°C. This shows that SnAgCu solder readily creeps at temperature well below room temperature.

The relationship used to represent the steady state creep of solder in shear is:

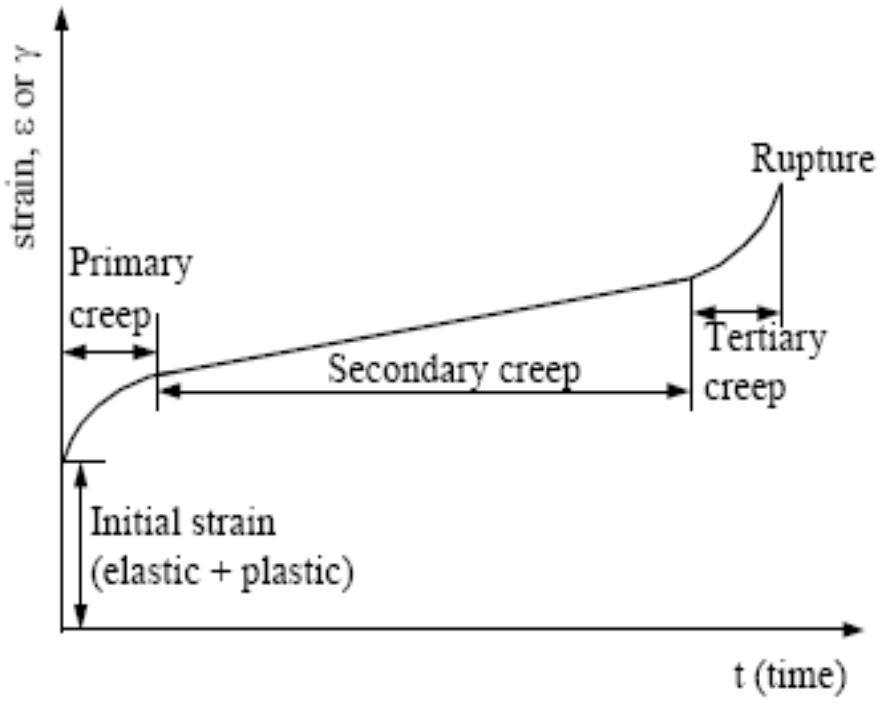


Figure 1. 3 Three stages of creep

$$\dot{\gamma}_{creep} = \frac{d\gamma_{creep}}{dt} = C[\sinh(\alpha\tau)]^n \exp\left(-\frac{Q}{kT}\right)$$

Where

$\dot{\gamma}_{creep}$ Steady state creep strain rate

τ applied stress

Q Activation energy

T absolute temperature (in degree Kelvin)

C, α, n constant

k Boltzmann constant

There have been many experiments conducted to test the constitutive properties for SnAgCu solder. [43][35]

Time-independent plasticity is also important and expected to play a larger role when the loading rate is higher. Zhang[39] have tested the both creep and plasticity at various temperatures and loading frequencies. Power cycling usually involves a fast temperature-loading rate (in seconds) and plasticity should be considered. The constitutive properties from their study are implemented in this study.

Some researchers have also used Anand's model to describe the constitutive behavior for lead-free solders. In Anand's model, both rate-independent plastic and rate-dependent creep deformations can be combined as rate-dependent inelastic deformation in unified constitutive models. Amagai[34] et al have obtained the constants for Sn3.5Ag0.75Cu and Sn1.0Ag3.5Cu bulk solder specimens. Y. Lee[33] found the constants for Sn3.5Ag.

1.3.3 Differences in constitutive properties between bulk solder versus joint

Studies have also determined that the mechanical properties of the solder joint are different from the bulk solder material. NIST[43] compared isothermal creep data from three independent studies on bulk solder material and the results are plotted as tensile strain rate (per second) versus tensile stress (MPa) as in Figure 1. 4.The data covers two orders of magnitude on the stress axis and eight orders of magnitude on the strain rate axis.

Although there appear to be a few outliers, and the SnAgCu alloys have slightly different Ag and Cu weight percentages (including the Sn-2.5Ag-0.8Cu-0.5Sb Castin^{TM} alloy), the creep data sets from three independent sources show consistency in the creep rate. (See Figure 1. 4) Slight variation in the composition does not seem to alter the creep properties of the bulk samples much. However, mechanical test data from bulk solder samples is significantly different from solder joints used in the packages probably due to the differences in the microstructure and mechanical constraints.[32]

Table 1. 1 Specimens used in the studies[43]

Publication	Alloys	Specimen		
		Shape	Length (gauge length	Cross-section
Schubert &Wiese	Sn3.8Ag0.7Cu	Dog-bone	60mm(30mm)	3mmx3mm
Neu	Sn2.5Ag0.8Cu0.5Sb	Cylinder	127mm(12.7mm)	13mm^2
Kariya	Sn3.8Ag0.7Cu Sn3.0Ag0.5Cu	Dog-bone	(60mm)	11.28mm^2

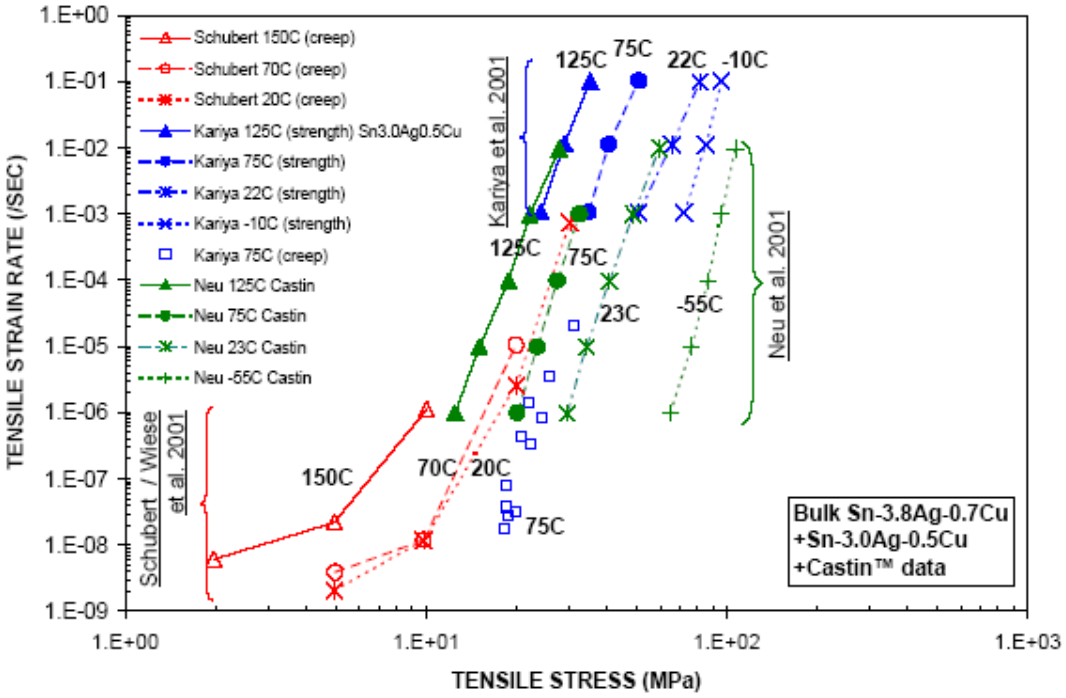


Figure 1. 4 Creep rate comparison[43]

Wiese et al[35] found that there is an obvious discrepancy existed when solder joints instead of large bulk solder material is tested. They have tested the creep behavior of Sn3.8Ag0.7Cu bulk solder and Sn4.0Ag0.5Cu flip chip solder joints. The results show that SnAgCu flip chip solder joints have much lower absolute creep rates than the bulk solder. (Figure 1. 5) They have not pinpointed the cause and speculate that the tiny (5nm and 50nm) Cu_6Sn_5 precipitates in the Sn matrix serve as potential obstacles for dislocation movements and increase the creep resistance.

The differences in mechanical properties between bulk solder and solder joint very likely link to different microstructures, which can be affected by many parameters such as intermetallics, joint or specimen size, cooling rate of the assembly after soldering, aging in service, etc. The leads to the necessity to characterize the microstructure of solder joint

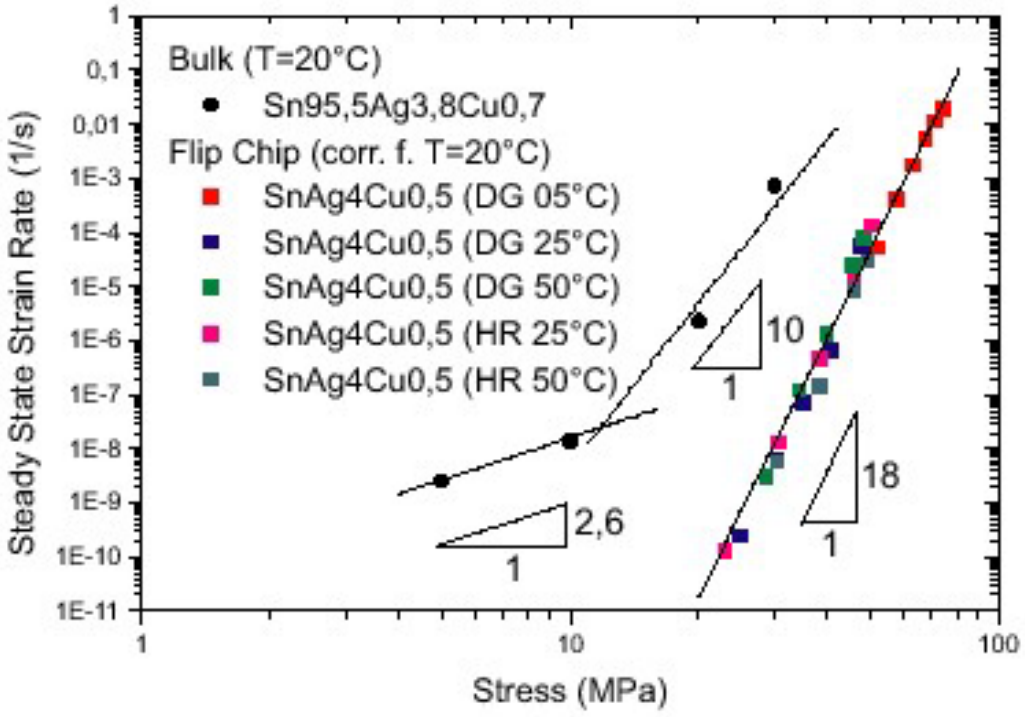


Figure 1. 5 Comparison of creep data from bulk Sn3.8Ag0.7Cu solder and Sn4.0Ag0.5Cu flip chip solder joints at 20°C [35]

when modeling solder joint or die attach reliability, especially for die attach application where the thickness is usually less than 100μm.

1.3.4 Microstructure of SnAgCu solder

A homogenous eutectic structure is desired for SnAgCu solder joints due to its low melting point and good mechanical properties. The eutectic composition is composed of a dominant percentage of Sn and a small portions Ag and Cu(shown in Figure 1. 7) and falls in the range of Sn+[3.2-4.1]%Ag+[0.45-1.1]%Cu[9] [11][12].

Ideally, SnAgCu eutectic solder would consist of a lamellar eutectic mixture of the Ag_3Sn intermetallic and Sn, with small precipitates of Cu_6Sn_5 dispersed throughout (see Figure 1. 6).[13]

However, The exact composition, soldering process, and geometry of the joint can cause the microstructure of the solder alloy to vary even within the same joint.[12] This is one of the major causes for variations of solder properties from one study to another. (See

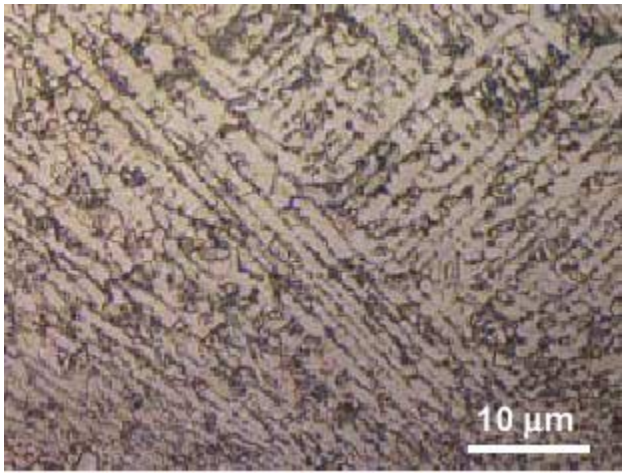


Figure 1. 6 Lamellar eutectic structure of SnAgCu solder [13]

Figure 1. 8) Normally the intermetallic particles are small (less than 100 nm), but occasionally, large Ag_3Sn and Cu_6Sn_5 precipitates have also been detected.[11]

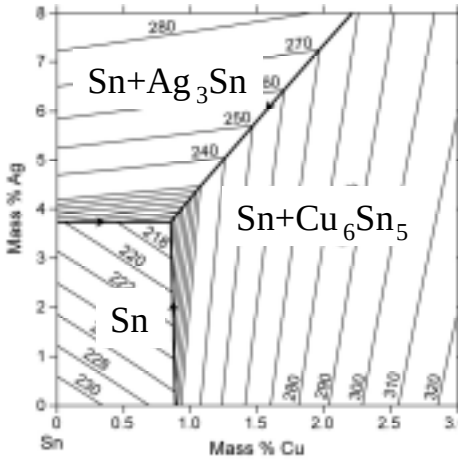


Figure 1. 7 Sn-Ag-Cu phase diagram at Sn side[12]

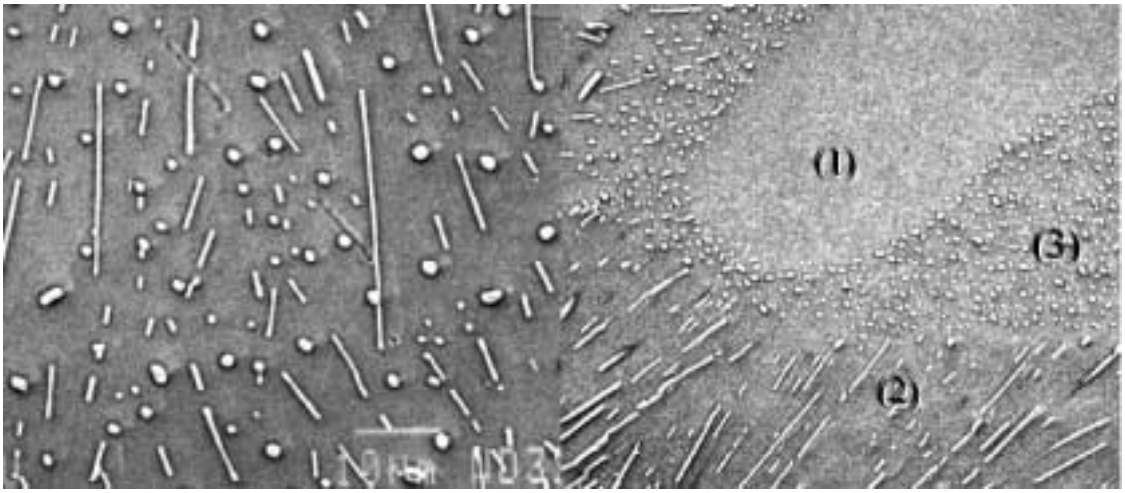


Figure 1. 8 SEM micrographs of eutectic SnAgCu structures A. ternary eutectic structure(matrix: (Sn), needle shape: Ag_3Sn, and disk shape Cu_6Sn_5). B. region with co-existing (Sn)+ Cu_6Sn_5 (region (3)) and (Sn)+Ag_3Sn(region (2)) fine two phase[12]

Those studies have revealed the critical role of intermetallics in determining the microstructure. Studies[121][122][123] have further confirmed that very few grains can be expected within a typical SnAgCu solder ball under normal soldering conditions due to extremely rapid growth of the Sn phase (>20 cm/s). (Shown in Figure 1. 9) As a result, few grains are expected to appear in SnAgCu die attach in the thickness direction and grains are not expected to play a critical role in determining thermo-mechanical properties of SnAgCu die attach.

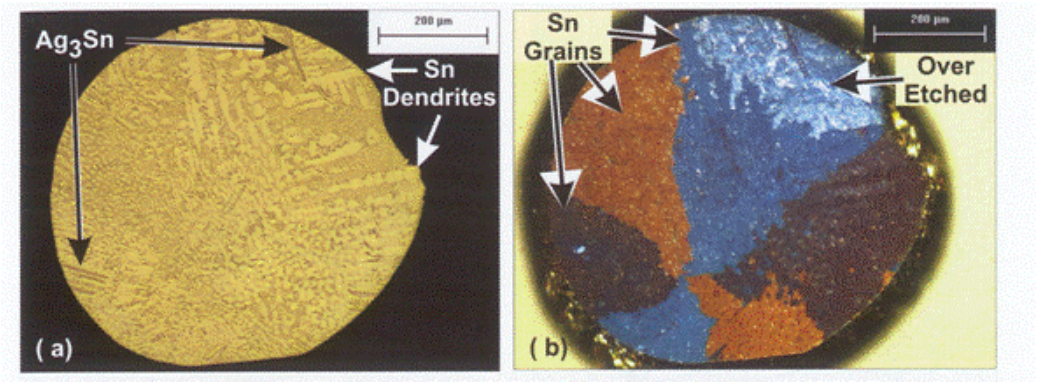


Figure 1. 9 Sn3.9Ag0.6Cu cooled at a rate of 1°C/sec from a temperature of 250°C. (a) bright field image and (b) cross-polarized light image which revealed two twined grains existed in the solder ball. [121]

Due to limited solubility of Ag and Cu in the SnAgCu solder, most Ag and Cu forms Ag_3Sn and Cu_6Sn_5 precipitates with Sn in the solder. Those precipitates, although occupying only a small portion (<5wt%), have an obvious influence on the mechanical properties, known as precipitation hardening (or strengthening), leading to an obvious increase in the hardness and other mechanical properties (such as yield strength) [127].

There are various possible mechanisms responsible for this strengthening effect.[127][128] It is related to the fact that the strength of the ductile solder is governed by dislocation flow past obstacles. The precipitate particles with different elastic constants, density, or coefficient of thermal expansions from the matrix, can cause a stress field to be set up when a dislocation approaches it and make the dislocation flow more difficult and resulted in a higher strength. Those mechanisms are listed as:

1. Coherency hardening due to difference in density between precipitates and matrix give rise to elastic stresses in the vicinity of the precipitates. This won't occur in SnAgCu solder because Ag_3Sn particles are not coherent with Sn matrix.
2. Modulus hardening due to difference in the elastic modulus between precipitates and matrix resulting in image forces when a dislocation in the matrix approaches a precipitate.
3. Dislocation hardening due to thermal residual stress. The difference in coefficient of thermal expansion will cause residual plastic strains around precipitates as the solder is cooled down, increasing the dislocation density.
4. Orowan hardening. If the precipitates offer sufficient resistance to the passage of dislocations, the dislocations will not pass through them, instead, they will pass

between the precipitates and leave closed loops around the particles. Additional loops are formed around each precipitate obstacle as more dislocations proceed. This will decrease the effective spacing between the obstacles, making it more difficult for more dislocations to pass through.

5. Order hardening, which occurs due to passage of a dislocation through an ordered precipitate, e.g. Ni_3Al in superalloys, resulting a disordered lattice and the creation of antiphase boundaries. This is not expected to happen in the SnAgCu solder.
6. Chemical hardening. When a precipitate is sheared, it creates new surface, increasing the area of the interphase boundary. Therefore the energy associated with the interface is increased and an additional force must be exerted on the dislocation to force it through the particle. This is not expected to occur to the SnAgCu solder since a much higher stress is needed to shear the intermetallics than the stress needed to induce Orowan loops and Orowan hardening.

The effect of the hardening depends on parameters such as precipitate size, spacing, and volume fraction. Large precipitates are stronger to impede the dislocation flow. However, under the same volume fraction, larger precipitates lead to much fewer precipitates dispersed in the matrix and thus decrease the extent of strengthening.

In the SnAgCu solder, Ag_3Sn and Cu_6Sn_5 intermetallic precipitates formed first during solidification with minimal undercooling, while Sn solidifies later with a much higher undercooling (15~30 °C) [122][129]. Therefore, Ag_3Sn and Cu_6Sn_5 can aggregate and

grow into large precipitates before the solidification of Sn arrests the process. So large Ag_3Sn precipitates, in the shape of needles or plates, have been detected in SnAgCu solder joints. Those large precipitates certainly decrease the presence of small precipitates that serve to strengthen the solder. They may also provide a preferred crack propagation path [125] [129]. Therefore, those large precipitates are likely to decrease the reliability of the solder joint and should be avoided. Henderson et al[129] have further found that the large Ag_3Sn plates may be effectively minimized by utilizing higher cooling rates and/or using SnAgCu alloys with less Ag (<2.7 wt%) for BGA applications.

For thin die attach (thickness <100 μm), differences in the microstructure are likely to change its mechanical properties. There are two possible causes: 1) the difference in soldering process, especially the cooling rate; 2) the variation in the intermetallic formation related to surface finishes and interfaces. The difference in the intermetallic precipitate distribution should also be considered.

1.3.5 Effect of soldering process

The soldering process plays a very critical role in determining the microstructure of the bulk solder especially the extent and type of intermetallic formation. For SnAgCu solder, the effect of soldering process is much greater than the effect of any subsequent temperature aging. Intermetallic pinning ensures that only slight grain growth occurs during subsequent aging.[123] There are several important parameters involved in the soldering profile: heating rate, peak temperature, time above the liquidus point, and

cooling rate. Cooling rate is critical in determining the microstructure of the soldering joint.

Differences in the soldering process produce differences in the structure and size of Sn dendrites as well as the distribution and size of intermetallics. This will induce a different mechanical behavior between bulk material and the actual solder joints. [32] Kim et al[37] have found a slower cooling rate will result in the formation of large Ag_3Sn platelets and degradation in the tensile strength. Joo et al[36] have compare creep properties of as-cast Sn3.5Ag0.7Cu bulk specimen (TS) and as-soldered thin specimen (FC). For FC the cooling rates is between 140K/sec and 150K/sec. It is extremely fast compared to cooling rate under reflow soldering (<4K/sec). In FC specimen, the size of the β-Sn dendrites (prior to testing) was 5-10 μm. In TS specimen, the size of the β-Sn dendrites (prior to testing) was 50-100 μm. The creep test showed FC (Fast cooled) specimen had much lower minimum creep rates (10^2 times lower) and higher rupture time (10^2 times) than the TS specimen. Here, we have to be careful to state that the microstructures and properties of FC specimen don't represent those of typical solder joints that were cooled at a much lower rate.

The microstructure itself, for example intermetallic formation, as well as the size of the β-Sn globules in SnAg and SnAgCu alloys, depends very much on the specimen-cooling rate and geometry. It is important to put the both mechanical properties and fatigue data in perspective with deliberate characterization of the microstructure.

1.3.6 Effect of surface finishes

The effect of interfaces, such as surface finishes, is another important factor that cause the differences in the microstructure and mechanical properties between solder joints. It is anticipated that the effect of the solder/substrate interfaces on the behavior of the solder attach will be very important especially as the size of the attach is less than 100μm. It has long been suspected that for the thin die attach, surface finishes from die and substrate side, especially intermetallic formation, will pose a high influence on the reliability of die attach. This suspicion is yet to be confirmed.

There is two related effects that can influence die attach fatigue: First is the effect of interfacial intermetallics formed between surface finishes and die attach at both the die and substrate side. Kang et al [20] has suspected that Ni-Sn formed at interface may greatly alter the mechanical properties of the die attach. Thebaud et al[4] have compared the crack propagation of several types of Ni plating and didn't find any significant difference. Huff et al[17] have reported that for the Sn4.0Ag0.5Cu and Sn3.5Ag die attach, cracks under power cycling start from the edges at solder-DBC substrates interface. Morozumi et al [18][19] studied a different type of SnAg based die attach and found cracks to appear in the center between the solder/die interfaces. Those two studies on SnAg based lead-free die attach have shown the possibility of interface related failure that may be related to interfacial intermetallics.

Second is the effect of dissolution of surface finishes or base material from the die or substrate. The effect is expected to be more obvious for die attach than for other types of

solder joints since the thickness of the die attach is less than 100μm. Thebaud[4] observed the presence of Cu-based intermetallic due to copper dissolution in the die attach. Although those intermetallics are not directly responsible for die attach crack propagation, they seem to alter the thermo-mechanical properties of the joint. Those issues are yet to be investigated.

1.4 Effect of PCB surface finishes on SnAgCu solder joint reliability

Studies on the effect of surface finishes on die attach reliability is rather limited and most of the studies on surface finishes have been focused on the effect of printed circuit board (PCB) surface finishes on other types of solder joints used in Ball Grid Array packages. A literature review about the effects of PCB surface finishes on SnAgCu solder joint reliability could help us in understanding the interaction between surface finish material and SnAgCu solder joints and possible related effects that could also be important to SnAgCu die attach.

The PCB finishes are critical for achieving good solder joints as they facilitate the soldering process during printed circuit board (PCB) assembly. The Hot Air Soldering Level (HASL) process for creating Sn37Pb solder board finishes, has been extensively adopted in PCB manufacturing for many years. With the movement to lead-free electronics, the electronics industry has been exploring a number of new options to eliminate Pb in these processes. Some possible options include organic solderability preservative (OSP), Ni/Au (ENIG), pure Ag, pure Sn for board finishes and Ni/Pd/Au, Sn/Bi, and Sn/Cu for component finishes. The assessment of these finishes has been

under way by some industry consortia including NEMI, ITRI, and the Printed Wiring Board Manufacturing Technology Center (PMTEC). There is no superior finish to be identified among them. Each option has its own disadvantages: Ni/Au and Ni/Pd/Au are expensive; pure Sn has the possibility to grow tin whiskers; there are manufacturing difficulties for Sn/Bi and Sn/Cu.

There have been extensive studies characterizing the intermetallic growth at the interface between the solder and surface finishes. During assembly, tin from the solder will react with the material from the pad and/or component finishes and form intermetallics. Intermetallic growth is a diffusion-controlled process necessary initially to form a high strength bond, but it can continue during temperature cycling/aging to form a thick, brittle interface.

Intermetallic growth depends not only on the solder material, but also on the finish type from components or PCBs. A number of studies have examined intermetallic growth when solders, including Sn37Pb and Sn3.5Ag, are reflowed on bare copper or gold over electroless nickel (NiAu). It is commonly accepted that for bare copper, copper from the pad will interact with tin from the solder and form Cu_6Sn_5 at the interface. If the joint is aged for a long period of time at a high enough temperature, a Cu_3Sn layer will form between Cu_6Sn_5 and the bare copper pad. For NiAu plating, gold will dissolve into the bulk solder during the soldering process, possibly forming $AuSn_4$ in the bulk, and permitting a layer of Ni_3Sn_4 to form at the interface. Some $AuSn_4$ has been observed to form at the interface after high temperature aging, which might cause a brittle interface

fracture.[55] Cu_6Sn_5 has also been observed to be the dominant intermetallic at the interface of SnAgCu solder on bare Cu. For Ni/Au plating, a ternary intermetallic, Cu-Ni-Sn or quaternary intermetallic, Cu-Sn-Ni-Au was detected at the interface with SnAgCu solder. Zribi[59] and Zeng[58] found the intermetallic to be $(CuNi)_6Sn_5$, which can grow significantly faster than Ni_3Sn_4.

Amagai et al [34] have observed that under tensile testing, failure locations of SnAgCu solder joints shift towards the interface if Au/Ni finishes is used, while the fracture happened in the solder when copper pad finishes are used. They attribute it to the increase in the strength of bulk solder due to the gold dissolution from the pad finishes. Seelig[88] has also reported interfacial weakness when SnAgCu is soldered on Hot Air Solder Leveling (HASL) PbSn finishes. Those studies indicated that mechanical behavior of solder joints could be greatly influenced by surface finishes and the influence is surface finish dependent.

However, the microstructural characteristic of SnAgCu on other potential lead-free finishes such as immersion silver and immersion tin have not been fully studied. Comparison studies of SnAgCu solder on those typical finishes help us better understand the effect of surface finishes on the microstructures as well as mechanical behavior and will be covered in this study.

1.5 Problem statement

SnAgCu solder is emerging as the lead-free candidate to replace high lead solder in power semiconductor devices, a design guideline is needed to estimate thermo-mechanical fatigue life of SnAgCu die attach under power cycling conditions. Former experiments on high lead die attach [103] have found the thickness of the die attach is one critical factor in determining the fatigue life and that thinner die attach could lead to shorter fatigue life.

For die attach used in power semiconductor packages, the thickness is usually less than 100 μm for better heat dissipation capability. Researchers have long suspected for such a thin die attach, there will be a high influence from interfaces. As we have discussed, there are several possible factors that could pose important influences on the thermo-mechanical behavior of die attach:

1. It has been widely accepted that either cyclic Von-Mises or shear stress/strain is the direct cause for die attach fatigue, but will there be a high compressive hydrostatic stress present in the die attach that can suppress the crack formation?
2. It has been widely reported[119][120] that under tensile loading, thinner adhesives can be stronger, because the constraint provided by the non-deforming metals restricts the transverse contraction of the soft adhesive. Here, the stress in the die attach is expected to have both shear and tensile components, so it is necessary to investigate all stress component in the die attach to determine if a similar effect exists.

At the same time, the effect of thickness on the microstructure, especially intermetallic formation, of SnAgCu die attach needs to be studied since microstructure is related to the mechanical properties. Intermetallic formation could change with thickness and result in different thermal-mechanical properties of SnAgCu die attach due to the following reasons:

1. Studies[17][18][19] have observed the interfacial failure for SnAg based die attach, which could be related to the interfacial intermetallics, formed between surface finishes and SnAgCu die attach. Will it happen to Sn3.5Ag0.8Cu die attach? If so, what's the mechanism? Is it related to the type of surface finishes being used? Is it thickness-dependent?
2. Intermetallic formation in the die attach is enhanced if surface finishes, such as Ag, Cu and Au dissolve into die attach and contributed to the intermetallic formation. It could change the microstructure as well as mechanical properties of the die attach especially for such a thin die attach. The influence is expected to increase with decreasing thickness. When will this influence become important and should be considered?

It has been widely reported that solder joint will behave differently from bulk solder, especially as joint sizes keeps decreasing. This research is of practical importance to understand:

1. How the microstructure as well as thermo-mechanical properties of the Sn3.5Ag0.8Cu die attach change as thickness decreases? What are the causes?

2. When will these thickness effects become critical and should them be considered in the thermo-mechanical analysis?

1.6 Scope of the study

Chapter 2 will discuss the evolution of the microstructure on various PCB surface finishes and its influence on the shear strength of the Sn3.8Ag0.7Cu solder under high temperature aging. Chapter 3 will report on the accelerated power cycling experiments on power MOSFET modules using Sn3.5Ag0.8Cu die attach. Failure mechanisms will be determined. In Chapter 4, thermo-mechanical simulation will be conducted to obtain the temperature profile of the power module under power cycling conditions and determine the stress/strain distribution of the module. Chapter 5 will characterize the microstructure of Sn3.5Ag0.8Cu dies attach and discuss the effects of thickness on the microstructure of the die attach especially the distribution of intermetallics.

Chapter 2 Effect of PCB finishes on reliability of Sn3.8Ag0.7Cu solder

The objective of this study is to investigate the effect of five different types of Printed Wiring Board (PWBs) finishes on the microstructural characteristics at the interfaces, as well as in the bulk of Sn3.8Ag0.7Cu solder joints after high temperature aging. The influence of the finishes on the microstructures both immediately after soldering and after subsequent aging at high temperatures is studied. Shear testing is conducted to determine the effect of surface finishes and related intermetallic formation on the shear strength of the joints.

2.1 Experiment procedure

Sn3.8Ag0.7Cu solder balls with a diameter of 635μm were reflowed onto pads on boards coated with the following five commercial surface finishes: organic solderability preservative (OSP) over bare copper, immersion tin (ImSn), immersion silver (ImAg) , and immersion gold over electroless nickel (ENIG) from two different manufacturers(T and M). Manufacturer T also supplied Hot Air Solder Level (HASL) PbSn.

First, Sn3.8Ag0.7Cu solder paste (thickness:0.006”) was stencil printed over the pads. Then the Sn3.8Ag0.7Cu solder balls were manually placed and reflowed to prepare samples for aging and shear testing. The reflow profile (shown in Figure 2. 1) is a typical profile for SnAgCu solders recommended by solder suppliers. After reflow, one board from a group of three for each finish was aged at 0.8Tm(=119 °C), $0.85T_m$(=143.5 °C) or $0.9T_m$(=168 °C) in order to accelerate the effects of long-term exposure to steady state

temperature. One board from each group was exposed for 10 hours, one for 100 hours, and one for 1000 hours. Therefore, each board represented a specific condition of specific surface finishes, aging temperature and aging time. Each board contained over 30 sample solder joints for analysis.

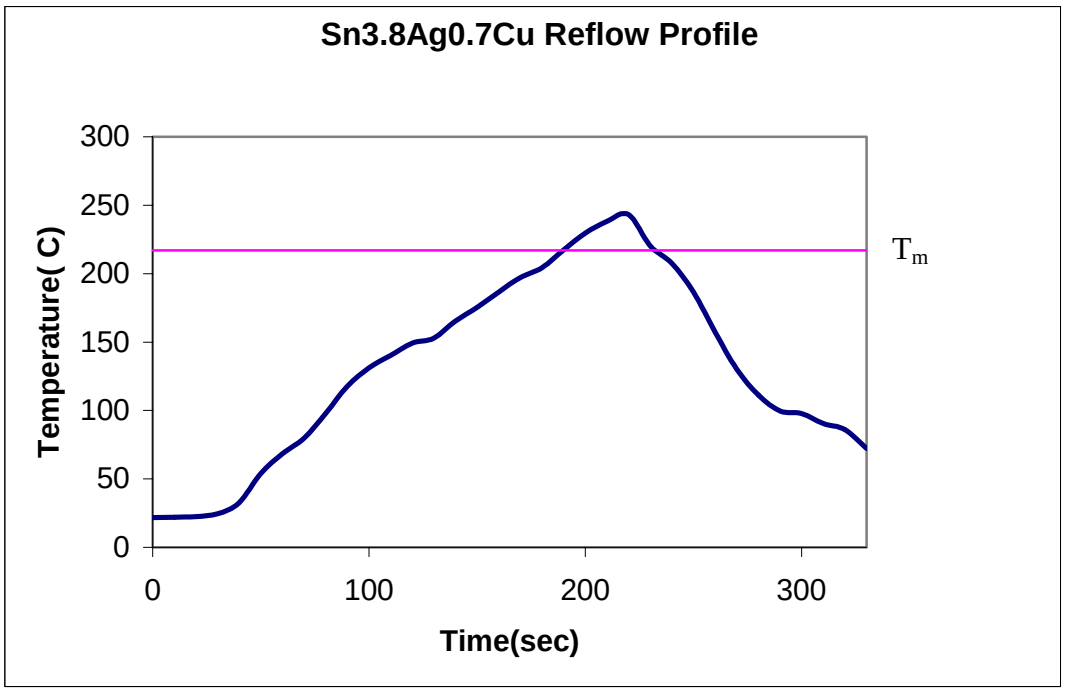


Figure 2. 1 Reflow profile used in the experiment (T_m is the melting temperature)

2.1.1 Material characterization

Two solder joints from each board were cross-sectioned, polished and etched with 5% HCL; 2% HNO_3; 93% methanol to reveal the thickness and uniformity of the intermetallic layers at the interface, and the morphology of the intermetallics in the bulk. Average intermetallic thickness at the interface was measured using image analysis software on optical photomicrographs. Both optical microscopy and Scanning Electron Microscopy/Energy Dispersive X-Ray Analysis (SEM/EDX) were used to characterize microstructures and compositions.

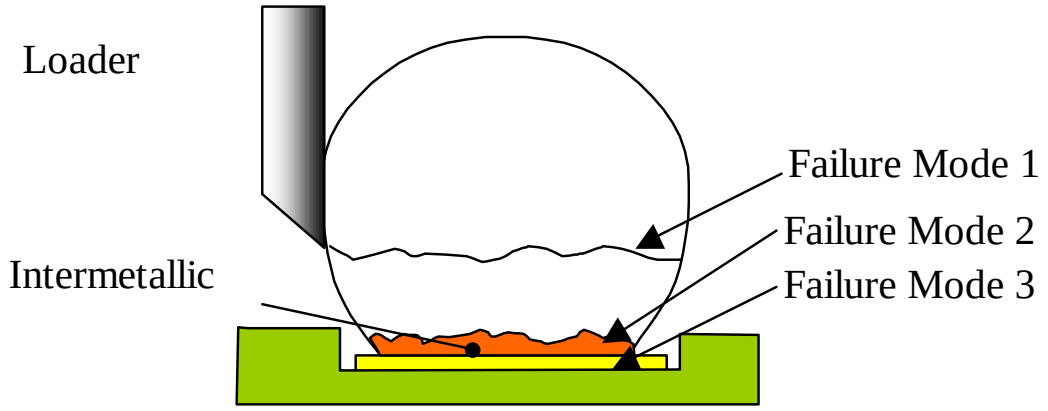


Figure 2. 2 Schematic diagram of the failure modes experienced during shear test

2.1.2 Shear test

A minimum of 25 solder joints from each board were shear tested using a Dage 2400 bond shear testing system at a shear speed of 100μm/s. The shear force was designated to be the maximum force applied during the test. The following three failure modes are expected (see Figure 2. 2):

Mode 1: Cohesive failure through the bulk solder, this signifies ductile failure of a good solder joint.

Mode 2: Adhesive failure at the solder/pad interface. This could be due to poor wetting or to weakness at the interface, it may be caused by brittle intermetallics.

Mode 3: Adhesive failure at the pad/board interface. This is related to poor adhesion between the pad and the board and is seen when the board is poorly manufactured or damaged in reflow or aging.

Shear strength was calculated as shear force divided by average shear area. It is difficult to measure the exact shear surface area corresponding to each solder ball, so shear area was obtained by randomly choosing ten solder joints and measuring the maximum diameter of each solder joint on the optical images based on the assumption that the joint is a sphere. The mean shear strength is calculated based on the maximum shear force of

25 solder joints. Any shear strength values corresponding to failure mode 3 were not considered here. A 3-parameter Weibull distribution is used to calculate the mean shear strength of the solder joint.

2.2 Results

2.2.1 Shear test

The dominant failure mode is mode 1(through bulk solder) for all the samples. However, failures by mode 2 are also detected on several joints on the HASL finishes after 100 hours aging at $0.9T_m$ or 1000 hours aging at $0.85T_m$. Some PCBs aged for 1000 hours at $0.8\ T_m$ and $0.85\ T_m$ exhibited failure mode 3 (pad lift) due to poor adhesion at the copper pad-laminate interface probably caused during manufacturing. All printed wiring boards (PCBs) aged for 1000 hours at 0.9Tm charred to such an extent that further cross-sectioning and shear testing could not be performed.

The average shear strength was steady for all surface finishes systems for all the aging conditions that produce no mode 3 failure. The shear test data are shown in Appendix A. This implies that the bulk microstructure does not deteriorate in strength after long-term high temperature aging.

Shear force to fail solder joints on boards from manufacturer T was smaller than that for manufacturer M because the stencil opening was smaller, which resulted in less solder deposition and a smaller shear area of the solder joints under shear testing. But the same nominal shear area was used to calculate the shear strength for both of them. As a result, a lower effective shear strength was reported on T boards.

2.2.2 Bulk microstructure

Immediately after reflow, the bulk Sn3.8Ag0.7Cu solder microstructure consists of tin dendrites and a dispersed phase (dark area), which in turn consists of small Ag_3Sn and Cu_6Sn_5 particles in a tin matrix (light area) as shown in Figure 2. 3 and Figure 2. 4. Under all aging conditions, large Cu_6Sn_5 intermetallic particles also appear in all types of surface finishes boards except ENIG as shown in Figure 2. 5. This is due to the dissolution of copper from the pads. Large Ag_3Sn needles only appear for ImAg finishes where they extend from the interface as shown in Figure 2. 6).

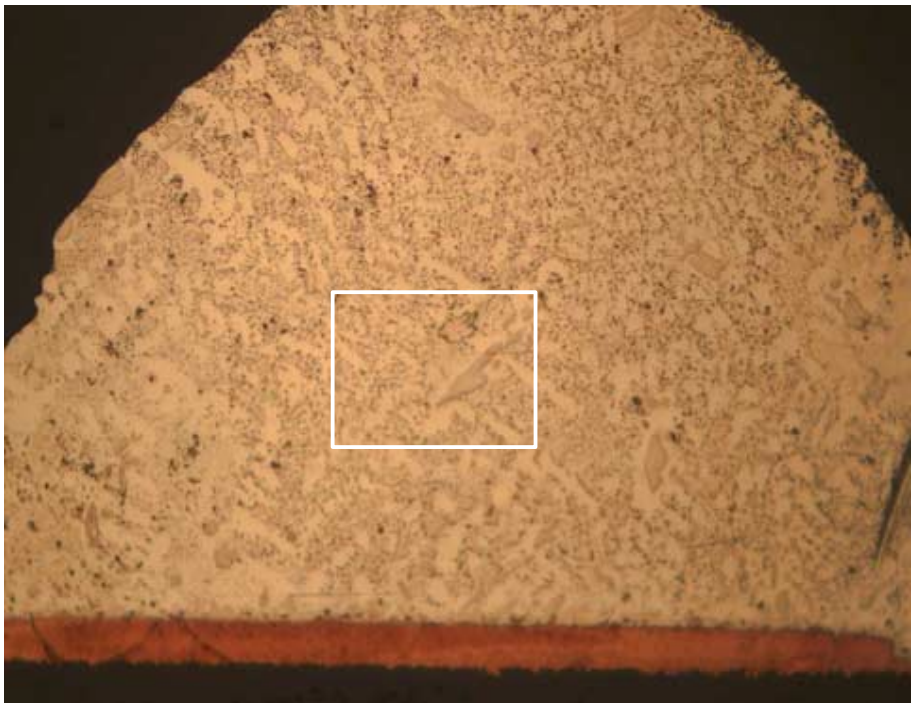


Figure 2. 3 Optical image of Sn3.8Ag0.7Cu solder on OSP with large Cu_6Sn_5 precipitate appearing in the bulk

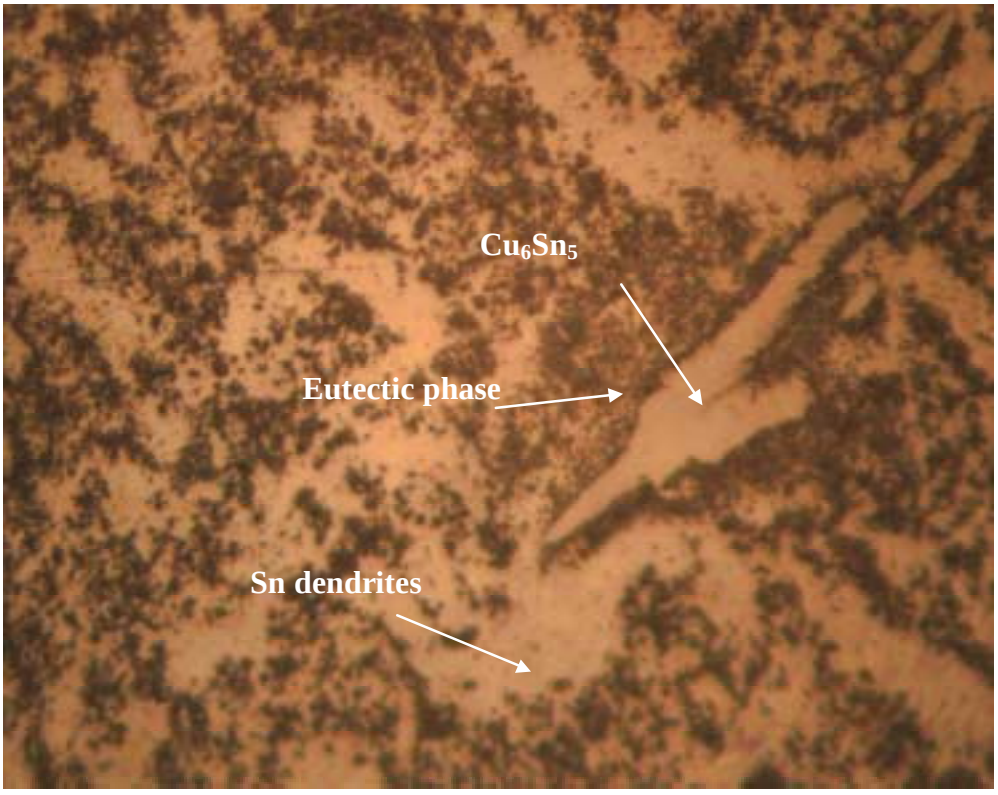


Figure 2. 4 Optical image of Sn3.8Ag0.7Cu after light etching, the area corresponds to the white circle in Figure 2.3

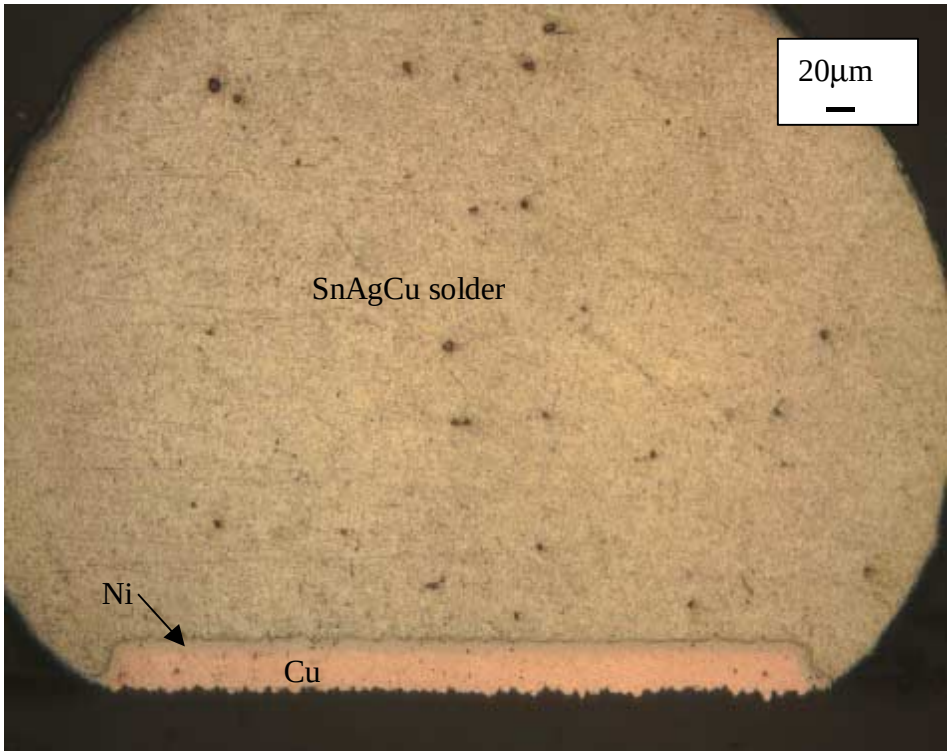


Figure 2. 5 Optical image of Sn3.8Ag0.7Cu solder on ENIG without any large intermetallics precipitate in the bulk

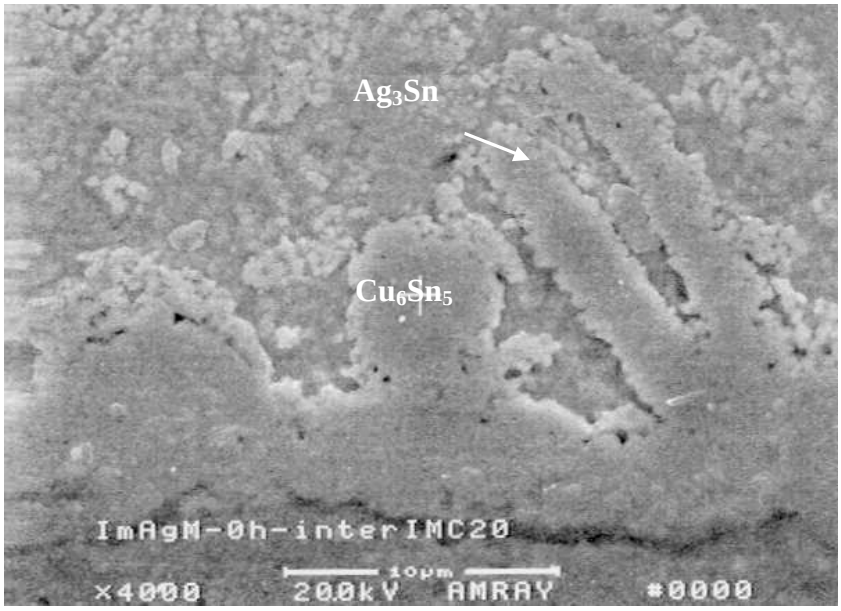


Figure 2. 6 SEM image of Sn3.8Ag0.7Cu solder joint on ImAg boards just after reflow

2.2.3 Interfacial intermetallic growth

The extent of the intermetallic growth at the interface was determined. The growth is diffusion controlled and self-limiting. The intermetallic growth rate and composition depended on the type of surface finish as well as the manufacturer. After aging for 1000 hours at $0.9T_m$, the difference in the thickness of Cu-Sn intermetallics between various surface finishes is small for both manufacturers, except ENIG, where the thickness is much smaller due to the limited supply of Cu from the solder (Figure 2. 7).

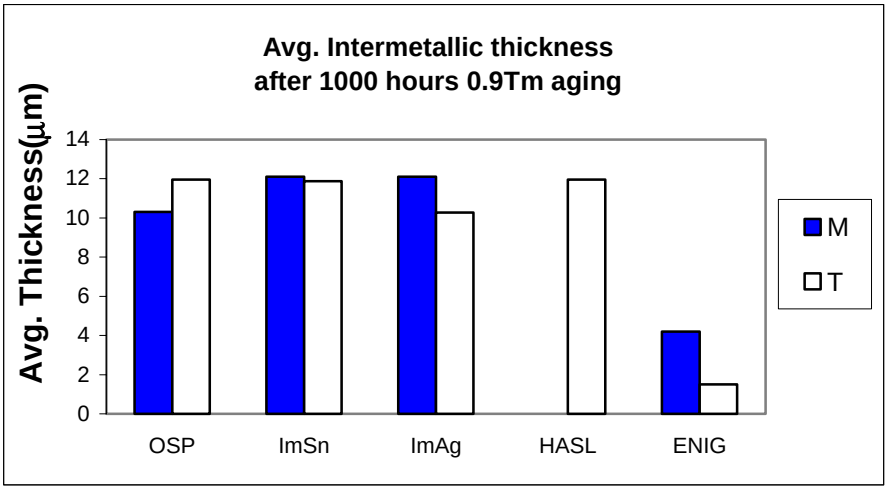


Figure 2. 7 Average thickness of intermetallic on different finishes after 1000 hours aging at $0.9T_m$

2.2.3.1 OSP

The initial morphology of the interfacial intermetallic for PWBs with both OSP^T and OSP^M finishes is scallop-like (see Figure 2. 8), but it becomes thicker and more uniform after aging (see Figure 2. 9). A Cu_6Sn_5 layer will form first after reflow. Next, a Cu_3Sn intermetallic layer will appear between the Cu_6Sn_5 layer and the copper pad after higher and longer temperature aging. This is similar to the intermetallic growth previously observed on bare copper as would be expected, given a negligible effect of the protective coating[47]. Large Cu_6Sn_5 intermetallics are detected under all aging conditions because of the dissolution of copper from underlying copper pad, participating in the reaction to form the Cu_6Sn_5 intermetallics.

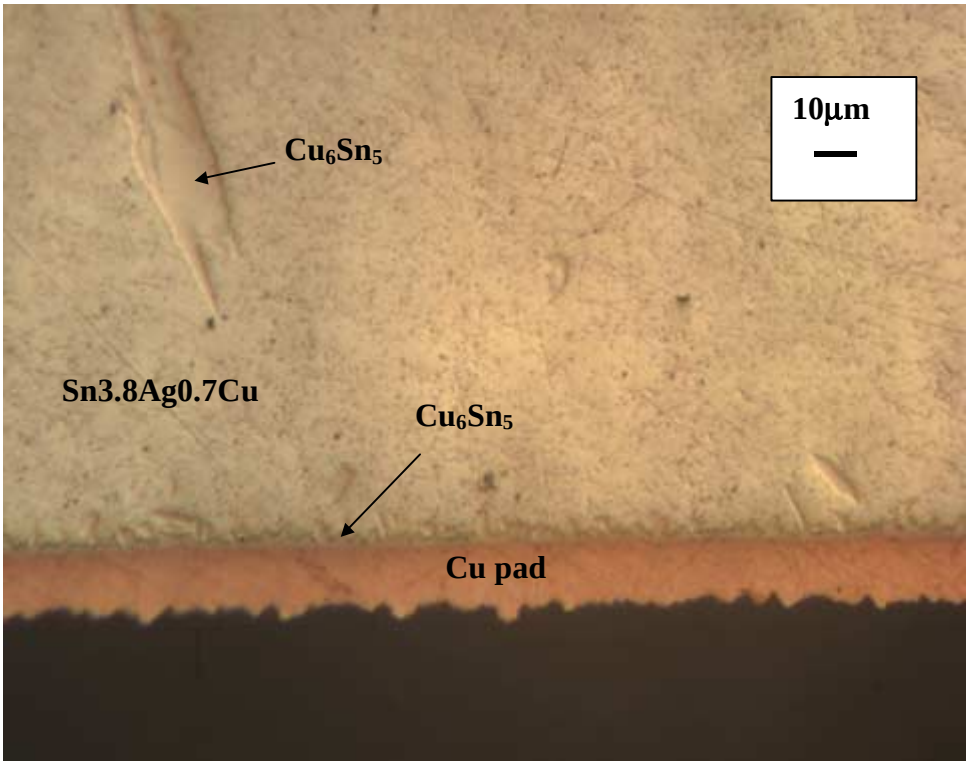


Figure 2. 8 Optical microscopy image of Sn3.8Ag0.7Cu solder joint (without etching) on OSP surface finishes boards. just after reflow;

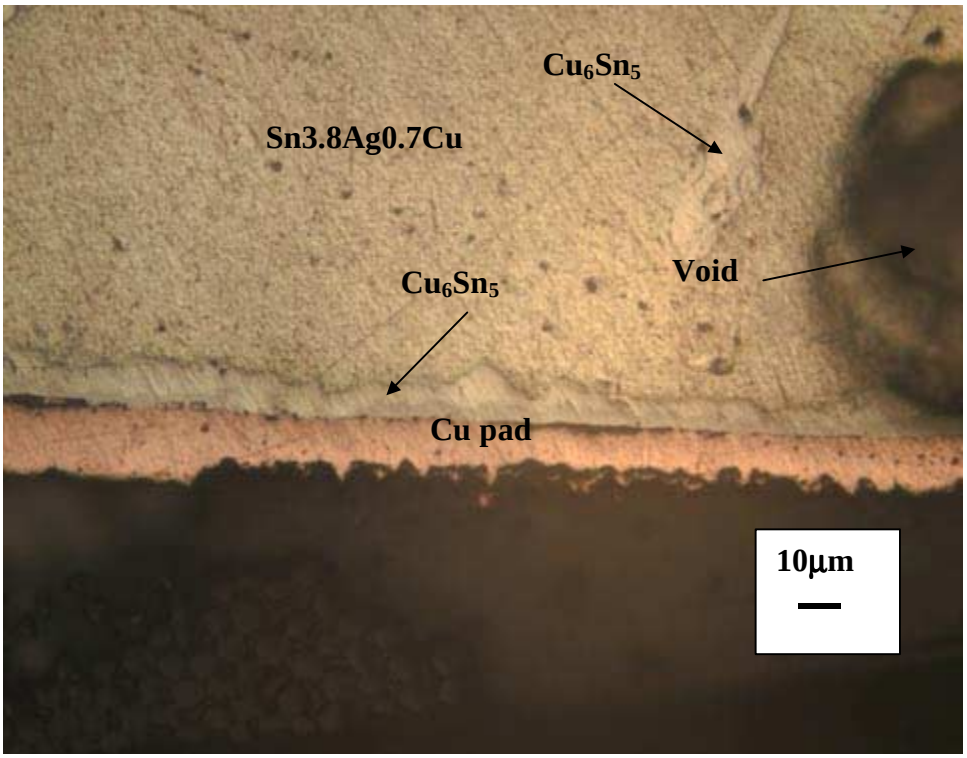


Figure 2. 9 Optical microscopy image of Sn3.8Ag0.7Cu solder joint (without etching) on OSP surface finishesboards. after 1000hours aging at 0.9Tm(168°C)

2.2.3.2 ImSn

The intermetallic growth on PCBs with ImSn finishes is quite different between manufacturers. The intermetallic on $ImSn^T$ is scallop-like after soldering and becomes thicker and more uniform after aging. The growth is very similar to OSP^T. But the interfacial intermetallic layer on $ImSn^M$ was smooth and uniform in thickness after reflow.(See Figure 2. 10) This layered structure remained after 1000 hours aging at $0.85T_m$ with a relatively constant average intermetallic thickness of around 4~5μm. The different growth for $ImSn^T$ and $ImSn^M$ may have been due to the different plating processes of the different manufacturers. But it is more likely that in the case of uniform $ImSn^M$ some of the intermetallic was formed by reaction between the Sn finishes and the underlying copper pad before the initial reflow, thereby assuming a more uniform layered

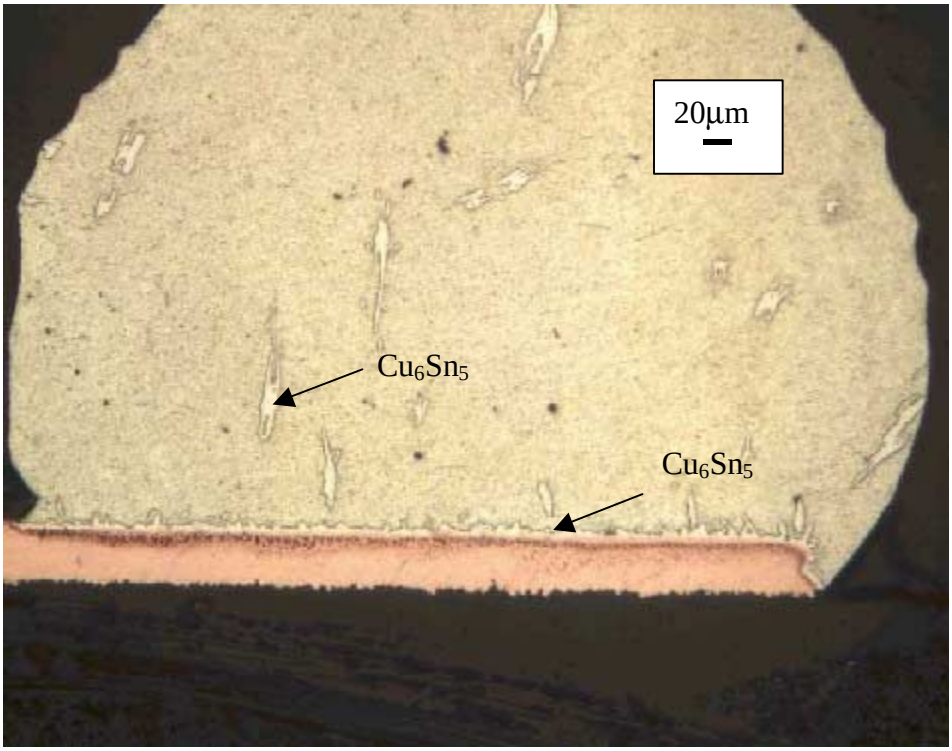


Figure 2. 10 Optical image of Sn3.8Ag0.7Cu soldered on $ImSn^T$ after reflow with a uniform Cu_6Sn_5 intermetallic formed at the interface

shape that was maintained throughout the reflow and subsequent aging.

2.2.3.3 ImAg

The dominant composition of the interfacial intermetallics on ImAg is the same as those on OSP and ImSn. (Figure 2. 11) Most of the Ag from the finish diffuses into the bulk solder during reflow, but some remains at the interface (see Figure 2. 6) and forms needle shaped Ag_3Sn. Intermetallic growth on both $ImAg^T$ and $ImAg^M$ is irregular. Cu from the pad and Sn from the solder form the dominant Cu-Sn intermetallic at the interface. The

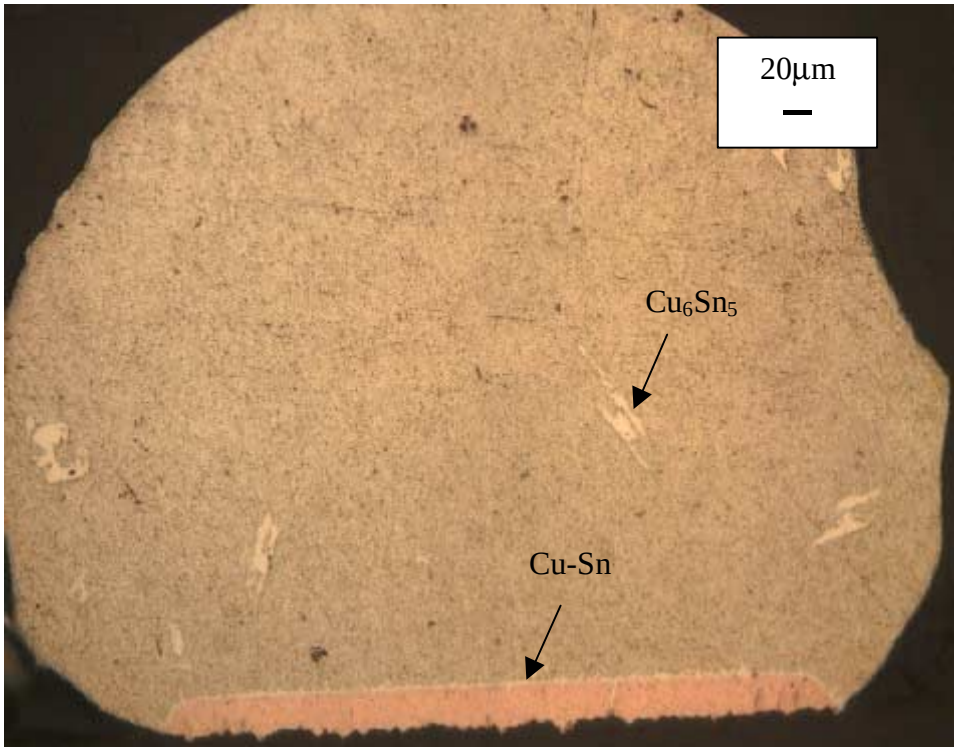


Figure 2. 11 Optical image of Sn3.8Ag0.7Cu soldered on $ImAg^T$ after reflow, Cu-Sn was the dominant intermetallic formed at the interface

average thickness is normally between 3μm and 8μm. The percentage increase of Ag due to dissolution is small since Ag finishes is usually less than 0.25μm.

2.2.3.4 HASL

Cu_6Sn_5 is the main intermetallic formed at the interface and a Cu_3Sn layer appears after longer aging times, as with other surface finishes. The intermetallic thickness on $HASL^T$ generally increases with longer aging time and/or higher temperature. The thickness after reflow is around 3~5μm and it increases to reach as high as 12μm after 1000 hours aging at $0.9T_m$.

Shear testing indicates that a weakened interface forms above the intermetallic. For solder joints which have experienced 100 hours aging $0.9T_m$, 44% of the failures happen at the interface (see Figure 2. 12) instead of through bulk solder, which is the common failure mode during shear test for other board finishes during shear testing. Samples with interfacial failure is due to tin from the surface finishes migrating toward the pad and forming intermetallic with copper, which leaves the lead and voids behind. A relatively Pb-rich region will thus form above the intermetallic, which coarsens and becomes weaker after high temperature aging. Similar failures have been investigated by Seelig [88] when a product is assembled with Sn/Ag/Cu solder alloy and a Sn/Pb coated leaded component. Sn/Pb coating will cause lead contamination and result in an intergranular separation of the lead-free alloy grains by Pb.

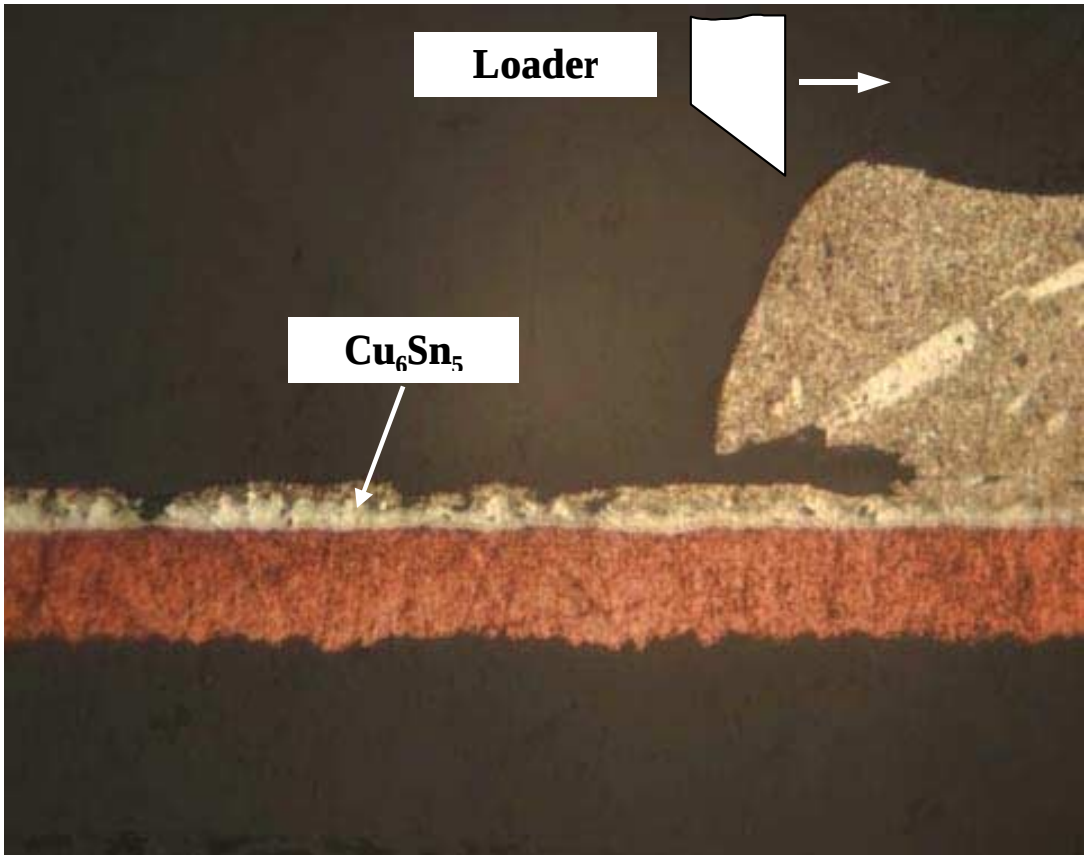


Figure 2. 12 Cross-section of interfacial failure for SnAgCu on HASL^{T}

2.2.3.5 ENIG

For ENIG^{M}, nickel from the pad, together with tin and copper from the solder participate in the reaction to form a ternary intermetallic $(Cu,Ni)_6Sn_5$ at the interface.(See Figure 2. 13) Generally, as aging continues, the intermetallic will grow to a maximum thickness of about 5~6μm, less than that of the other finishes, due to the limited amount of copper available from the solder to form intermetallic at the interface and in the bulk. Diffusivity of copper from the pad is neglected because the nickel layer is a diffusion barrier to copper. However, the intermetallic growth on ENIG^{T} is different from ENIG^{M}. For ENIG^{T}, $(Cu,Ni)_6Sn_5$ reaches maximum thickness (5~6μm) after 100 hours of aging at 0.85 T_m. Instead of remaining constant, the thickness then decreases so much by 1000

hours of aging at 0.85 T_m that the intermetallic is difficult to differentiate from the nickel layer. On the other hand large intermetallics are detected in the bulk and are characterized as $(Cu,Ni)_6Sn_5$. It implies that $(Cu,Ni)_6Sn_5$ at the interface might be unstable and will dissolve into the solder after extended high temperature temperature aging and thus the thickness of interfacial $(Cu,Ni)_6Sn_5$ will decrease. The concentration of gold coming from the pad here is very small and could not be detected.

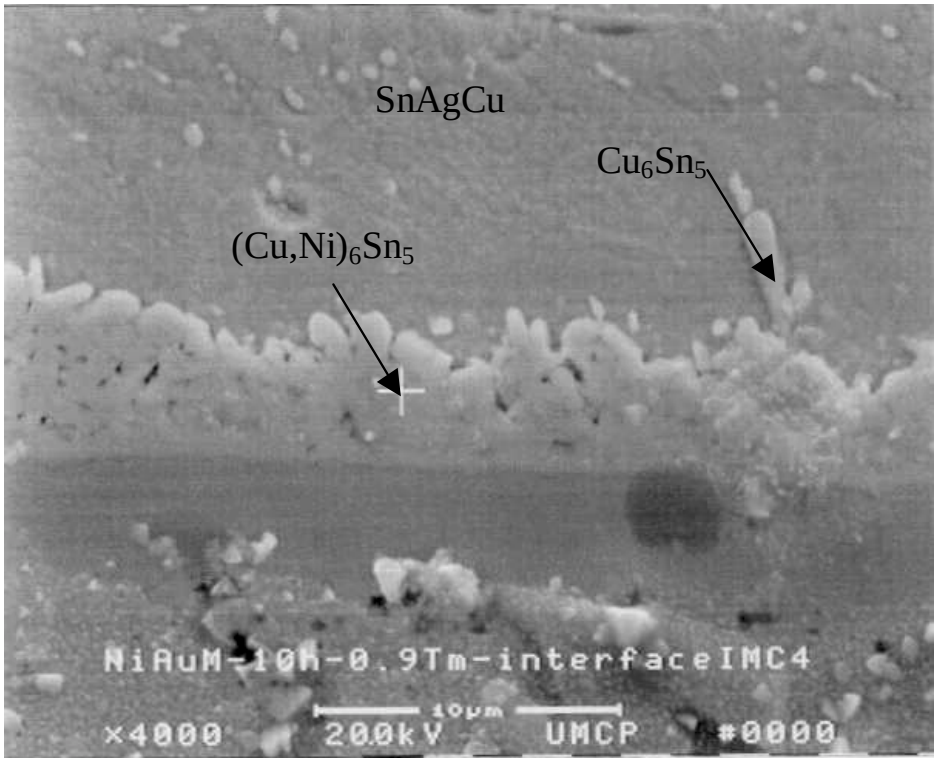


Figure 2. 13 SEM image of Sn3.8Ag0.7Cu soldered on $NiAu^M$ after aging at 0.9Tm for 10 hours, $(Cu,Ni)_6Sn_5$ was the dominant intermetallic formed at the interface,

2.3 Summary

Intermetallic growth in Sn3.8Ag0.7Cu varies with surface finishes and manufacturers. The most significant variation is that the intermetallic is much thinner on ENIG surface finishes (see Figure 2. 7). However, the average intermetallic thickness is less than 12 μm

even after 1000 hours aging at $0.85T_m$ for all the surface finishes. Instead, higher reflow temperature and high tin content in the solder cause copper from the finish to dissolve into the solder and change the microstructure of the bulk solder.

Dissolution of copper or silver from the surface finishes and substrate pads will contribute to the formation of large intermetallics in the bulk solders. In ENIG surface finishes, copper from the substrate doesn't dissolve into the bulk solder and no large Cu_6Sn_5 is formed in the bulk. Instead, copper from the solder migrates toward the interface to help form Cu-Ni-Sn intermetallic.

Large Cu_6Sn_5 intermetallic precipitates have a negligible effect on the shear strength of the solder joints. It is because intermetallics formed in the solders due to dissolution is very limited and care hardly reflected during overstress shear testing. However, as the size of the solder joints decrease, the effect of the intermetallic related surface finishes is expected to increase and could influence thermo-mechanical fatigue properties of the joint.

Another critical finding of the research is that no weak interface exists on lead-free finishes. A weak interface does appear in the joints on HASL(PbSn) surface finishes after high temperature aging, causing interfacial failure during shear test.

Finally, in appendix G, we have studied the solder joint failure under different strain rate and drop testing. It is concluded that intermetallic brittle failure only occurred to the SnAgCu solder joint under high strain rate and drop testing. Under the low strain rate, usually experienced under temperature/power cycling loading conditions, solder fatigue is the dominant failure mechanism.

Chapter 3 Power cycling experiments

3.1 Introduction

Power cycling causes temperature fluctuations that in turn generate thermo-mechanical stresses in electronic modules (Figure 3. 1) due to mismatch in the coefficients of thermal expansion for different materials. Cyclic thermo-mechanical stress leads to die attach fatigue. As a result, die attach cracks have been reported as a major failure mode for power modules. In the experiments, thermal grease is used to attach the power module to the heat sink. It is also possible that thermal grease will wear out during power cycling. Wire-bond lift-off may also occur.

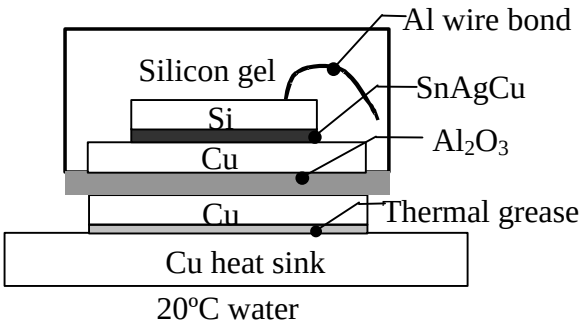


Figure 3. 1 Schematic drawing of the power MOSFET under power cycling

Power cycling experiments were performed at four power levels and three different die attach thicknesses. Samples with thermal grease degradation are excluded and samples with die attach cracking are the focus of the study. A thorough failure analysis was conducted to characterize the critical features such as tilt and wetting. Finally, power cycling results are used to perform thermo-mechanical analysis.

3.2 Experimental setup

Accelerated power cycling experiments were conducted to investigate the effect of power level, and die attach thickness on the durability of power MOSFET modules.

3.2.1 Test specimen

The test specimen (see Figure 3. 2) consists of a single chip package of a 7.70mm(l) x 6.55mm(w) x 0.375mm(th) silicon power MOSFET, the backside of which was coated with a triple finish layer of Cr-NiV-Ag (thickness: 0.1μm-0.2μm-0.25μm). The finish layer enabled the drain connection to be made to a DBC substrate: Cu (13mm x 13mm x 0.3mm) /Al_2O_3 (14mm x 16mm x 0.635mm)/Cu (17mm x 19mm x 0.3mm), using a standard alloy bond process with Sn3.5Ag0.8Cu solder. The die was then wire bonded to the lead frame in a plastic case, which was then filled with silicone gel. Then the single chip package was mounted on a Cu heat sink with thermal grease. The heat sink was

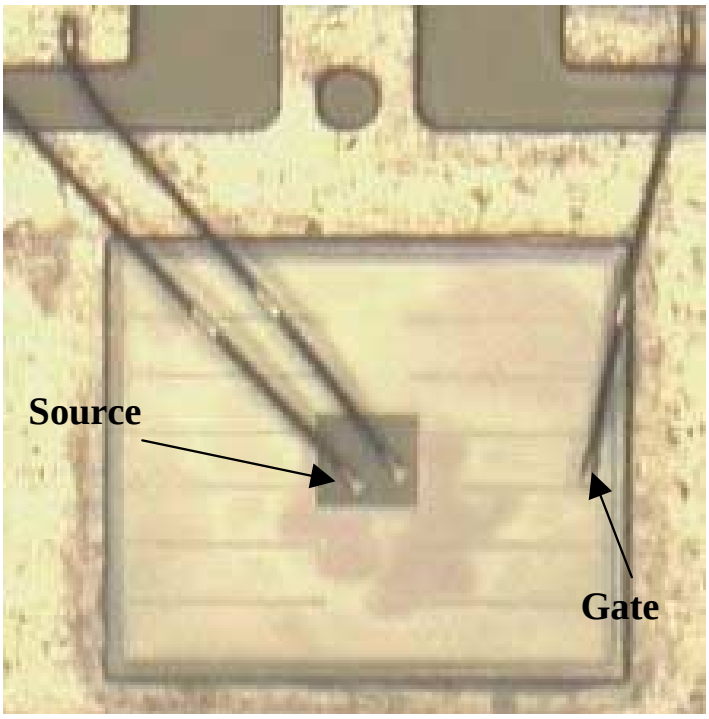


Figure 3. 2 Top view of the power MOSFET mounted on (Drain is located on the backside)

cooled by 20°C flowing water. Spring clips were also used to secure package, ensuring good thermal contact to the heat sink. (See Figure 3. 3)

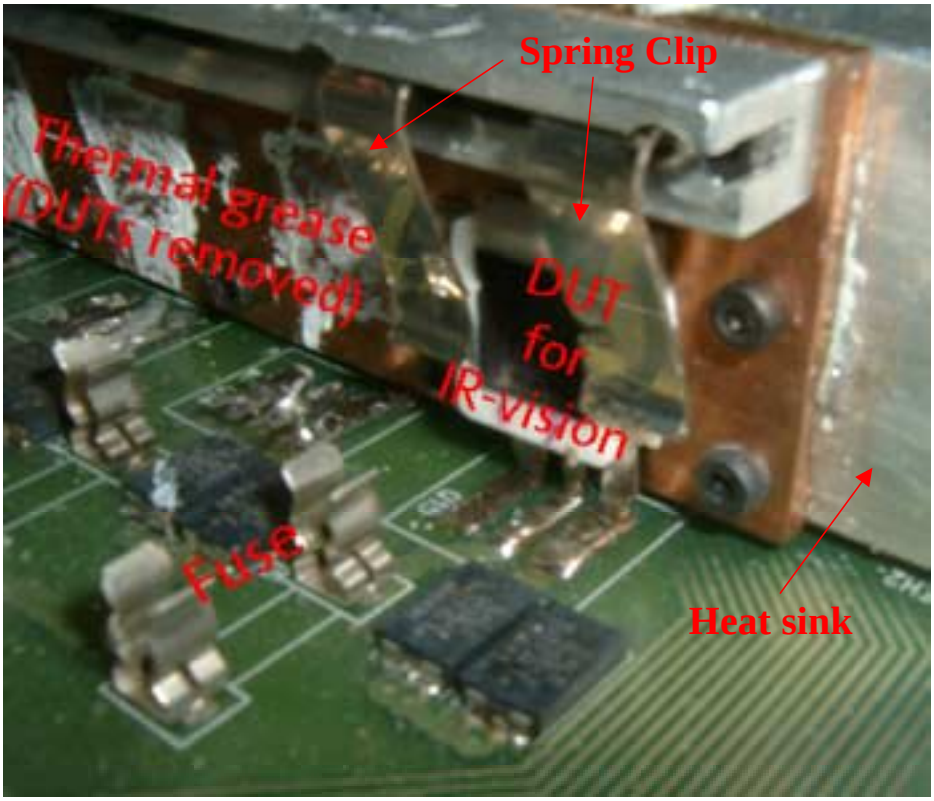


Figure 3. 3. One corner of the test board, DUTs(Device under test) on the left have been removed. On the right, one DUT was still attached to the heat sink. Here, spring chips were used.

3.2.2 Soldering process

Vapor phase soldering was used to attach the die to the DBC substrate with a solder perform of a size about 75% of the die. The soldering was performed in a vacuum environment to minimize the occurrence of voids in the die attach. Large voids are to be avoided since they will introduce temperature variation in the die that deteriorate device performance[96]. The calibrated soldering profile is shown in Figure 3. 4.

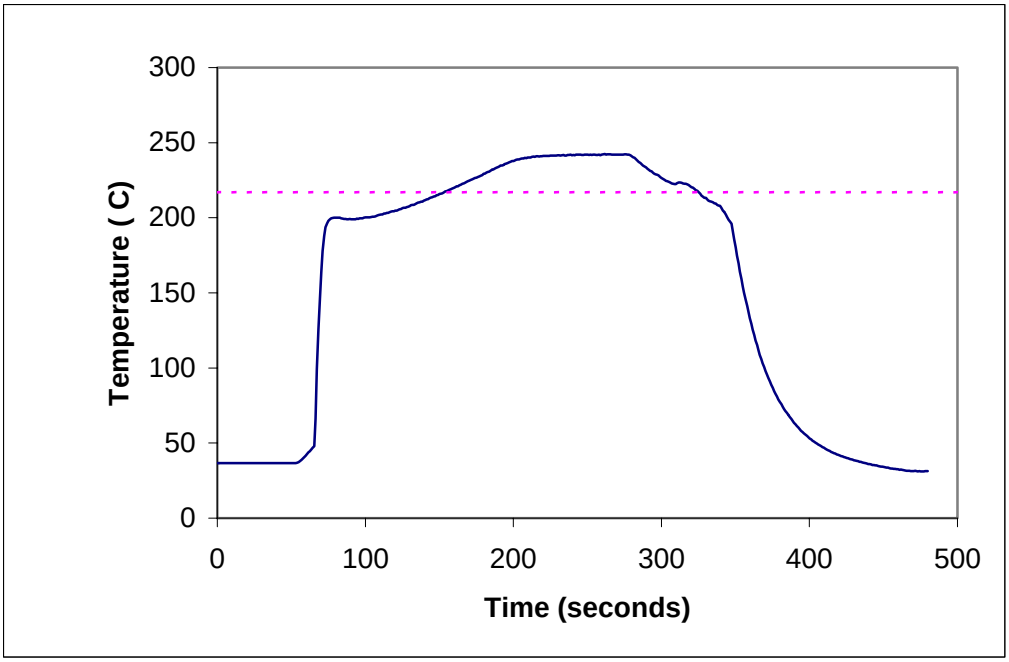


Figure 3. 4 SnAgCu die attach soldering profile (dot line is the melting temperature)

3.2.3 Power cycling

Power MOSFETs can be operated at a wide range of frequencies. Fast start/stop operation is regarded to be the worst-case loading conditions for the power module in pump application. In order to reflect the worst-case field condition, the frequency was set at 2 seconds on and 2 seconds off. (See Figure 3. 5)

As power was applied, the temperature of the module gradually increased with the junction temperature (T_j) of the die being the highest temperature in the module.

3.2.4 Test setup

The power cycling test system used in the experiments (See Figure 3. 6) includes a PLC controller, power supply, and a power cycling test board (see Figure 3. 8). The PLC controller controls the power level and power cycling frequency. It also monitors and records the number of cycles that have been applied.

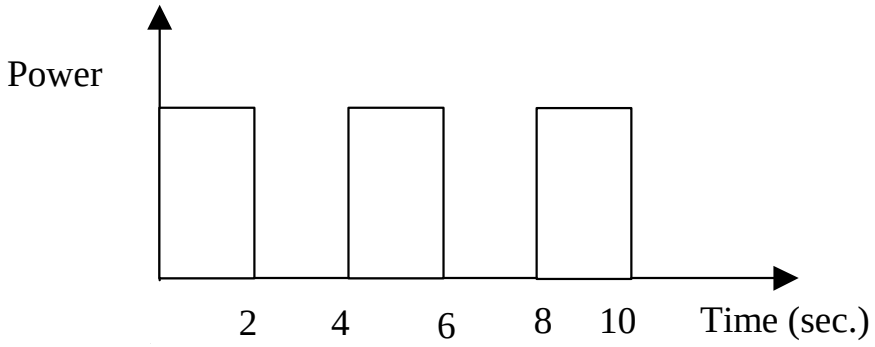


Figure 3. 5 Power cycling used in the experiment

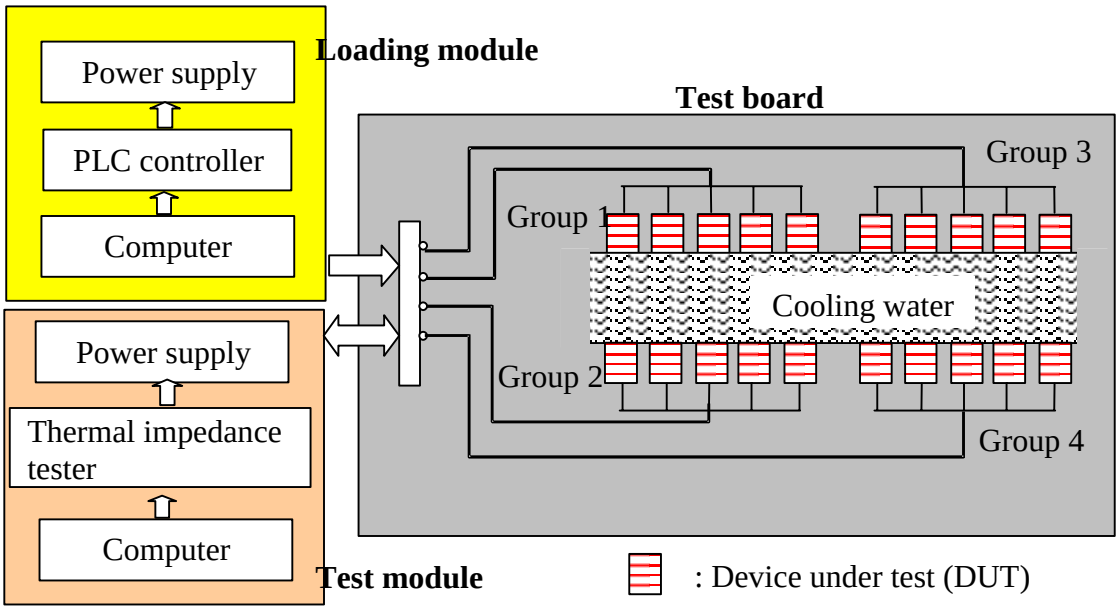


Figure 3. 6 Schematic drawing of the power cycling system

The test board (Figure 3. 7) can be used to test 4 groups of modules at the same time. The power cycling is applied by the loading module. Each group contains 5 devices, which are all tested at the same power levels. All the devices were covered with silicon gel except the die of one device ("black MOSFET") from each group, which was exposed and painted with ink. Later, an IR camera was used to calibrate the temperature for the thermal impedance tester. The test board also is alternately connected to the test module to measure the thermal impedance.

Die attach fatigue cracking impedes heat dissipation, increasing the thermal impedance of the structure and the junction temperature (T_j) of the devices. In the power cycling experiment, the failure due to die attach fatigue is monitored by the increase in the thermal impedance from the junction to the base of the heat sink. [2][4]

Thermal impedance can be calculated by the temperature difference between the chip and

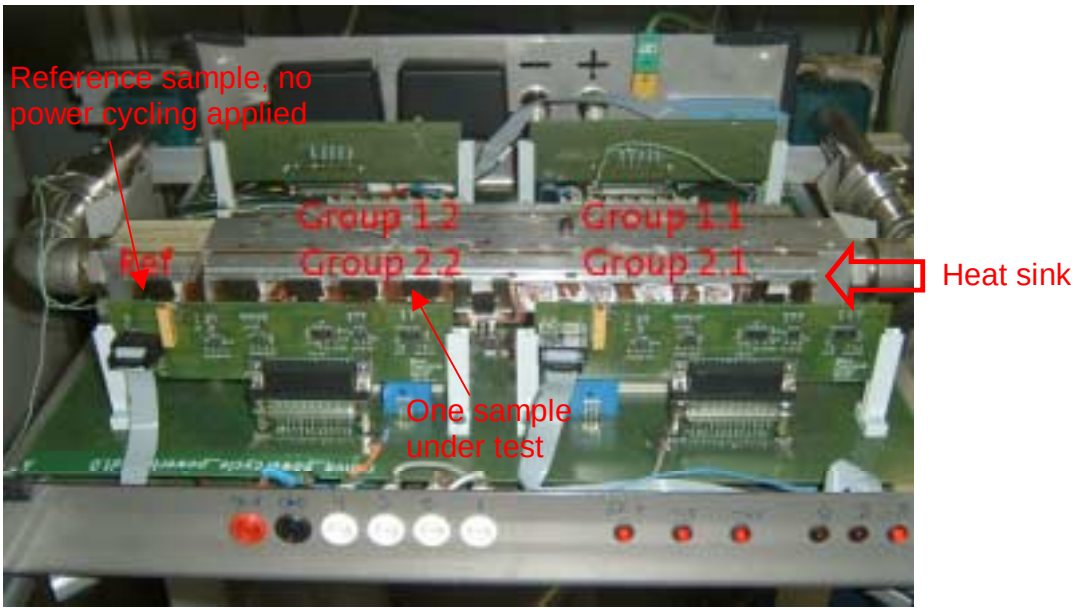


Figure 3. 7 Power cycling test board. Here, four groups(5 samples for each group) could be tested at the same time. One reference sample was also used

the bottom of the heat sink divided by the power dissipation during power cycling

$$Z_{jc}(t) = \frac{\left(T_j(t) - T_{base}\right)}{P}$$

Here, $T_j(t)$ is the transient junction temperature and T_{base} is the bottom temperature of the heat sink and it is fixed at 20°C here due to water-cooling, which was also confirmed by thermocouple measurment. The junction temperature is determined indirectly. For power MOSFETs, the junction temperature has a linear relationship with forward voltage drop (ΔV) of the devices and can be determined indirectly by measuring the forward voltage drop and calibrated with IR camera on the "black MOSFETs". After every 10,000 cycles, the power cycling was suspended and a small amount of current was applied to determine the thermal impedance from the junction to the heat sink by measuring the resulting forward voltage drop across the junction. (See details in Appendix B)

The thermal impedance tester measures the thermal impedance at 80ms, 300ms and 2s for each group. Failure criterion was set as a 10% increase in thermal resistance at 2s. The cycling will be stopped once this criterion is reached.

Although die attach fatigue cracking causes an increase in the thermal impedance, an increase in the thermal impedance is not always due to die attach cracking only. Thermal grease degradation is another potential cause. Viswamath et al [126] have proposed two failure mechanisms for thermal grease degradation: First, under the high temperature aging experienced during power cycling, the formulation chemistries utilized in the grease could result in separation of the polymer and filler matrix due to the migration of the polymer component. The separation and loss of polymeric material could result in poor wettability at the interfaces, resulting in an increase in the thermal impedance.

Second, under cyclic loading, thermo-mechanical stress exerted because of the flexure between the die and the base of the heat sink can lead to loss of grease material. The effect of second failure mechanism is expected to be limited in this study because the high stiffness of the DBC substrate makes the flexure difficult.

It is necessary to differentiate thermal grease failures from die attach failures. This is realized by measuring thermal impedance at different times as power is turned on. As soon as power is applied, heat is generated in the active device. Then the heat flux flows down toward the heat sink. Due to the small heat capacitance of the die and die attach, it takes a very short time (t_1) for heat to pass through those two layers and reach the DBC substrate, from there the heat will spread across toward the thermal grease interface. At time t_2, heat flux reaches the thermal grease interface. Finally, the heat flux flows through to the heat sink and the thermal profile reaches steady state. [98][99][100][101]If thermal impedance is measured between t_1 and t_2, it won't have any influence from thermal grease. t_1 and t_2 can be determined from thermal transient analysis. Simulation results have shown that t_2 is around 100 ms. Based on transient thermal simulation (see Appendix E) thermal impedance measurement at 80ms therefore will see only the effect of die attach while measurements at 300ms and 2s will be affected by both the die attach and the thermal grease.

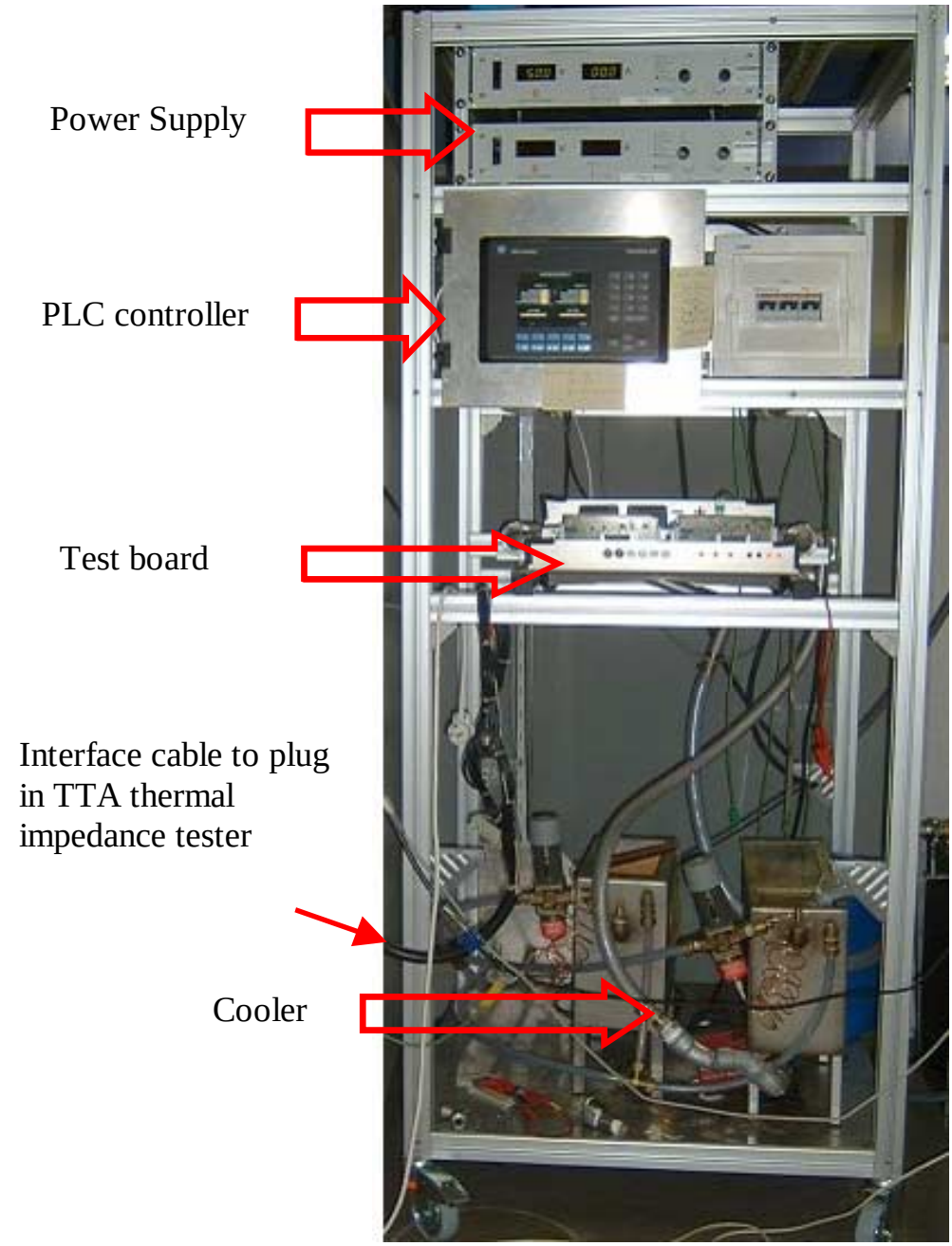


Figure 3. 8 Power cycling test equipment

3.2.5 Design of experiment matrix

Six groups of five samples each were tested. Four groups were tested at the same nominal die attach thickness and different power levels. Three groups were tested at different nominal thickness. (See Table 3. 1) Later failure analysis has found a variance in the die attach thickness fore those devices in the same nominal thickness. This variantion was introduced during the soldering process. They will be explained in further detail in section 1.4.2.

Table 3. 1 Power cycling experiment test matrix

Group#	Power (w)	Nominal die attach thickness*	Sample #
(30w, 40μm)	30w	~40μm	21,22,41,42,66
(50w, 40μm)	50w	~40μm	23,24,43,44,67
(70w, 40μm)	70w	~40μm	25,26,45,46,69
(90w, 40μm)	90w	~40μm	27,28,47,48,70
(70w, 20μm)	30w	~20μm	12,13,14,15,17
(70w, 80μm)	30w	~80μm	71,73,75,76,77

*Exact thickness varies

3.3 Power cycling results

After the thermal impedance of a sample increased 10% at 2s, the experiment was stopped. Then the sample was demounted from the heat sink. The test was also terminated for some samples without reaching a 10% increase because of time constraints. Thermal impedances at 80ms and 300ms were also measured. The following plots showed the relative thermal impedance at 80ms, 300ms and 2s at the end of the cycling for each sample. Corresponding cycles to failure are also shown.

The samples with nominal thickness of 40μm are discussed first. For group (30w, 40μm) (see Figure 3. 12) and group (50w, 40μm)(see Figure 3. 11), thermal impedance at 80ms

had a negligible increase at the end of the power cycling, indicating those samples failed at the thermal grease instead of die attach; For Group (70w, 40μm) (see Figure 3. 10) and (90w, 40μm)(see Figure 3. 9), all the thermal impedances for 4 out of 5 samples has increased, indicating die attach cracking. For those two groups, thermal impedance at 80ms, 300ms and 2s increase at the same time, excluding the possibility of thermal grease failure happening first and accelerating die attach fatigue. Therefore die attach cracking is the cause for increase in the thermal impedance (See Appendix C Thermal impedance results) . Later failure analysis has also confirmed the presence of die attach cracking.

For samples with nominal die attach thickness either higher (Group (70w, 80μm)) (see Figure 3. 14) or lower (Group (70w, 20μm)) (see Figure 3. 13), thermal grease failure was observed before any die attach cracking was observed.

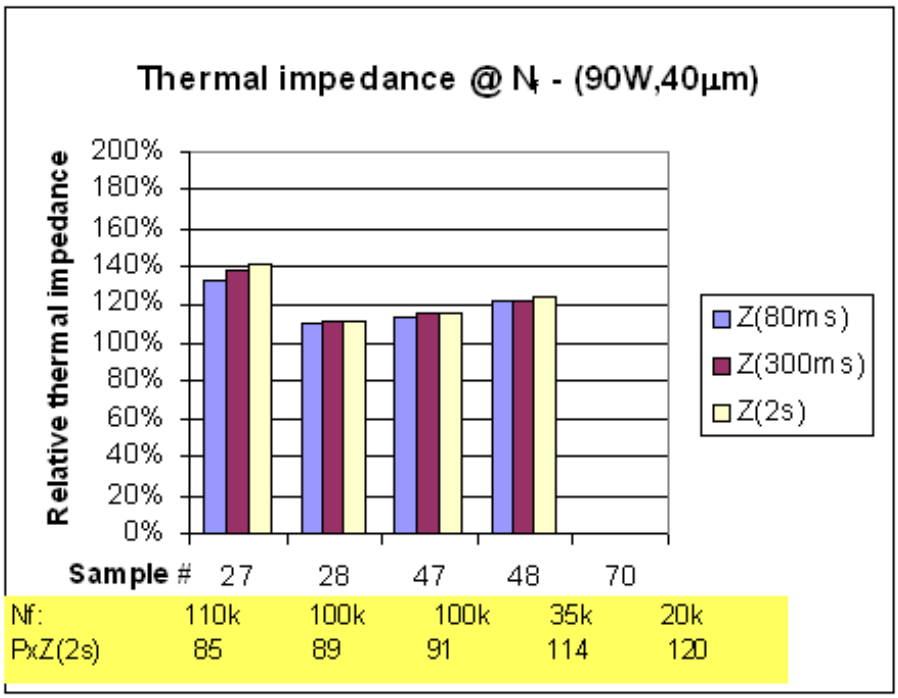


Figure 3. 9 Thermal impedance increase correspoding to N_f for group(90w,40µm) (PxZ(2s) is ΔT_j at 2s) sample 70 failed prematurely due to assembly

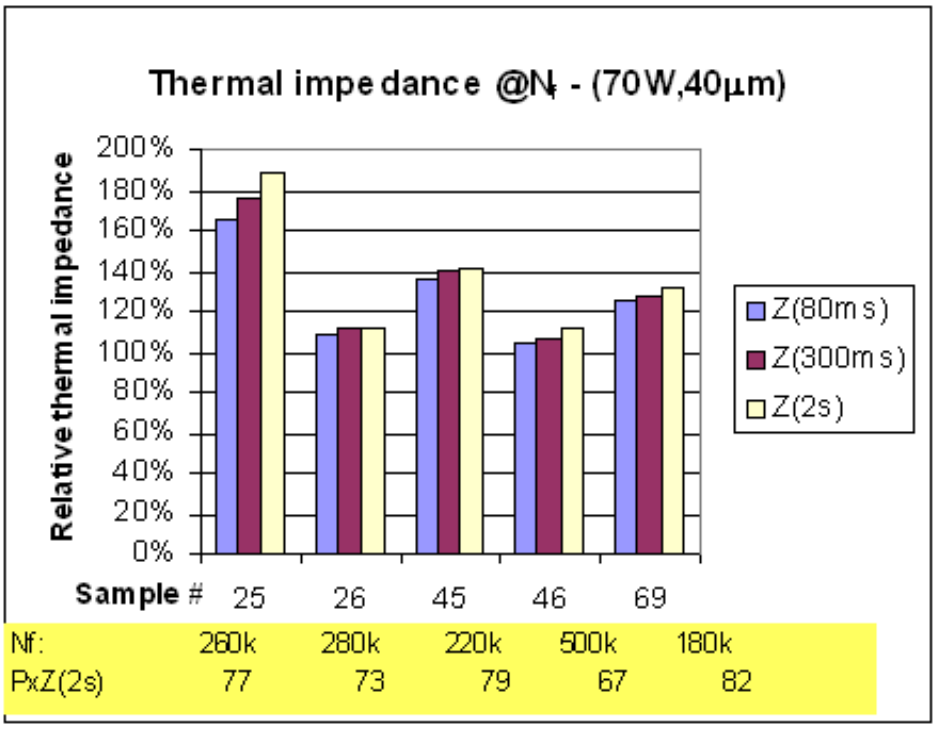


Figure 3. 10 Thermal impedance increase correspoding to N_f for group(70w,40µm) (PxZ(2s) is ΔT_j at 2s) not die attach cracking in sample 46

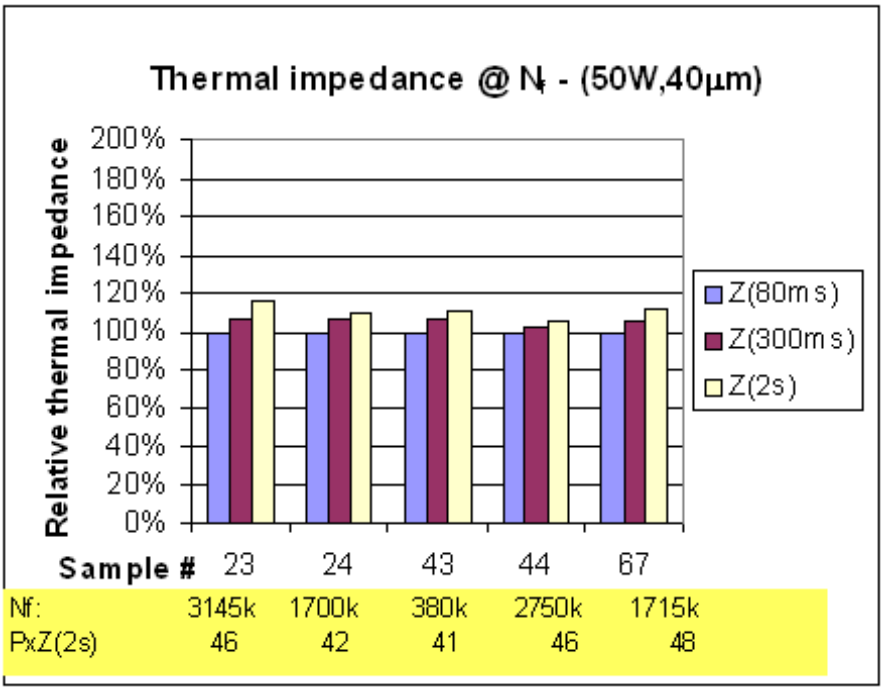


Figure 3. 11 Thermal impedance increase correspoding to N_f for group(70w,40µm) (PxZ(2s) is ΔT_j at 2s)

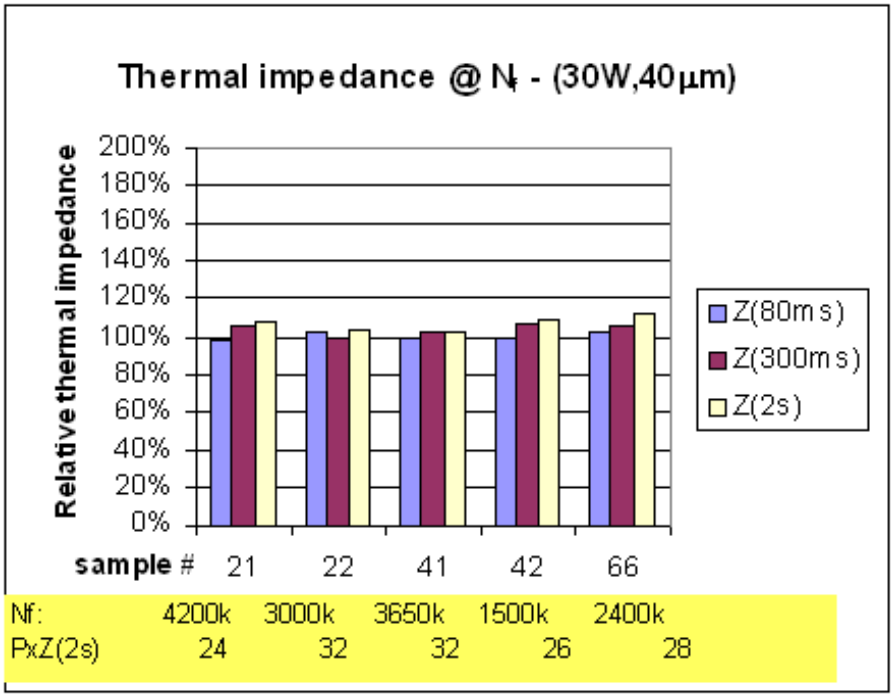


Figure 3. 12 Thermal impedance increase correspoding to N_f for group(70w,40µm) (PxZ(2s) is ΔT_j at 2s)

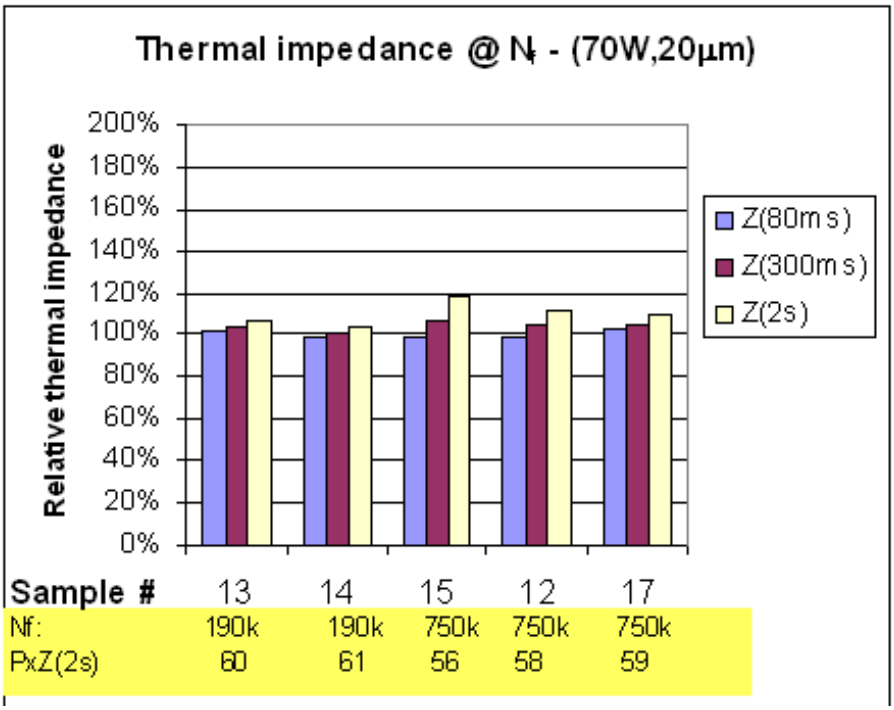


Figure 3. 13 Thermal impedance increase correspoding to N_f for group(70w,40µm) (PxZ(2s) is ΔT_j at 2s)

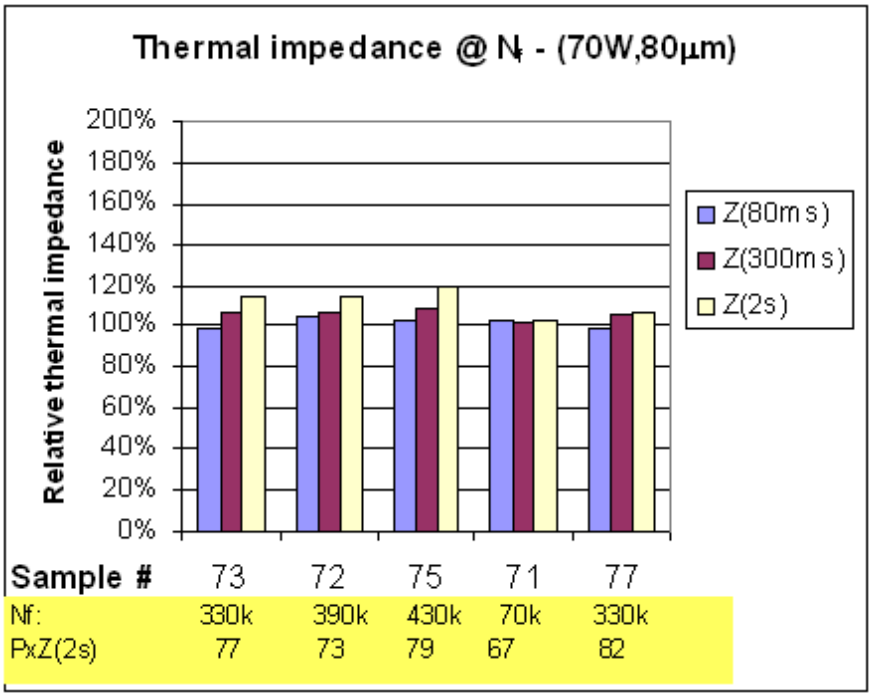


Figure 3. 14 Thermal impedance increase correspoding to N_f for group(70w,80µm) (PxZ(2s) is ΔT_j at 2s)

For the group (70w, 40μm) and (90w, 40μm) that due to die attach cracking, the cycles to failure are related to ΔT_j. (See Figure 3. 15) Although five samples were tested under the same power level (either 70w or 90w), the junction temperature for those five samples varied due to the difference in the thermal impedance as a result of the different thickness of thermal grease.

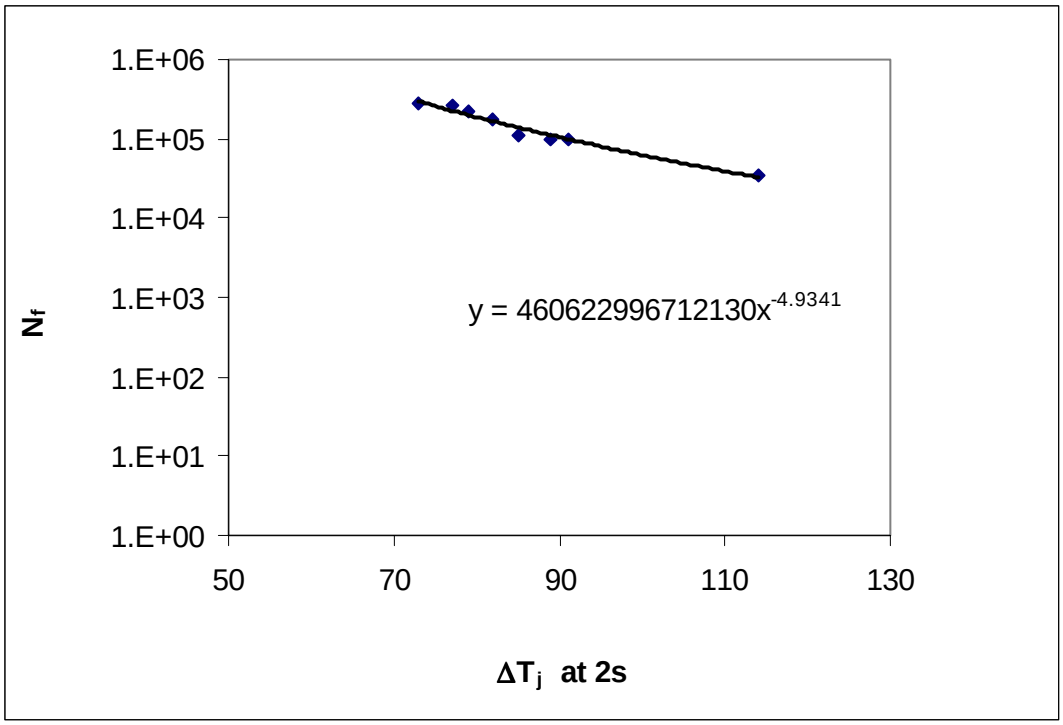


Figure 3. 15 Power cycles to failure versus (junction temperature change (T_j) at 2s for group (70w, 40μm) and (90w, 40μm)

A large spike characterizes the increase in the thermal impedance for the two groups of samples with die attach cracking (see Figure 3. 16& Figure 3. 17). It is possible that fast crack propagation leads to rapid increase in the thermal impedance. In the next chapter, thermal impedance increase and crack propagation will be correlated through simulation. Then the rate of crack propagation will be determined.

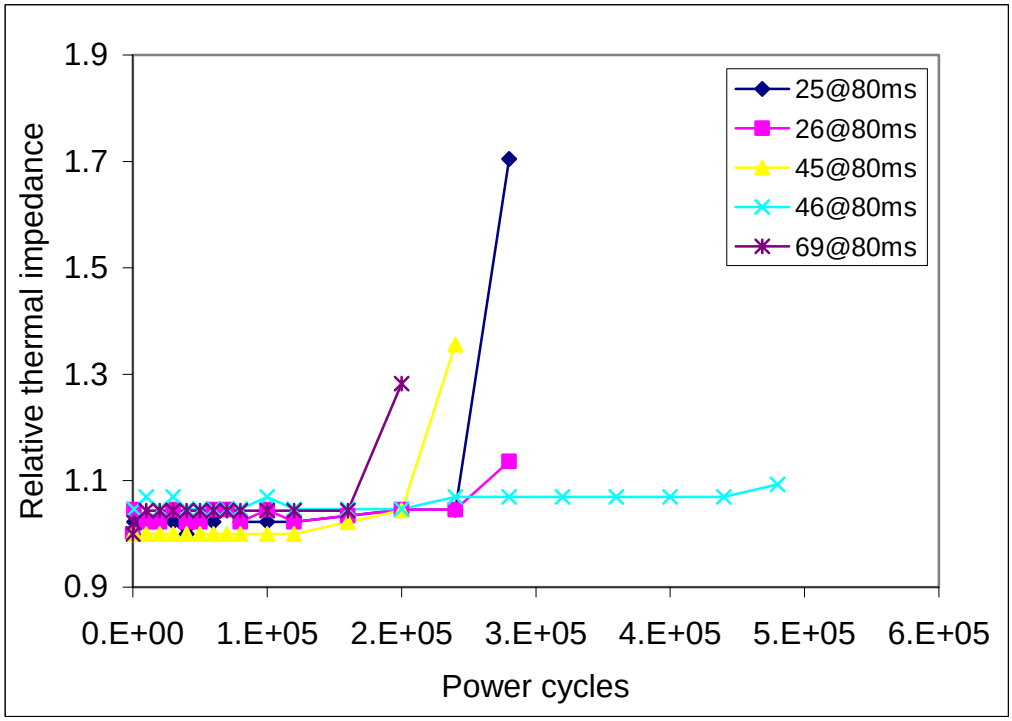


Figure 3. 16 Relative thermal impedance at 80ms change with power cycles for group (70w, 40μm) (No die attach cracking for sample 46)

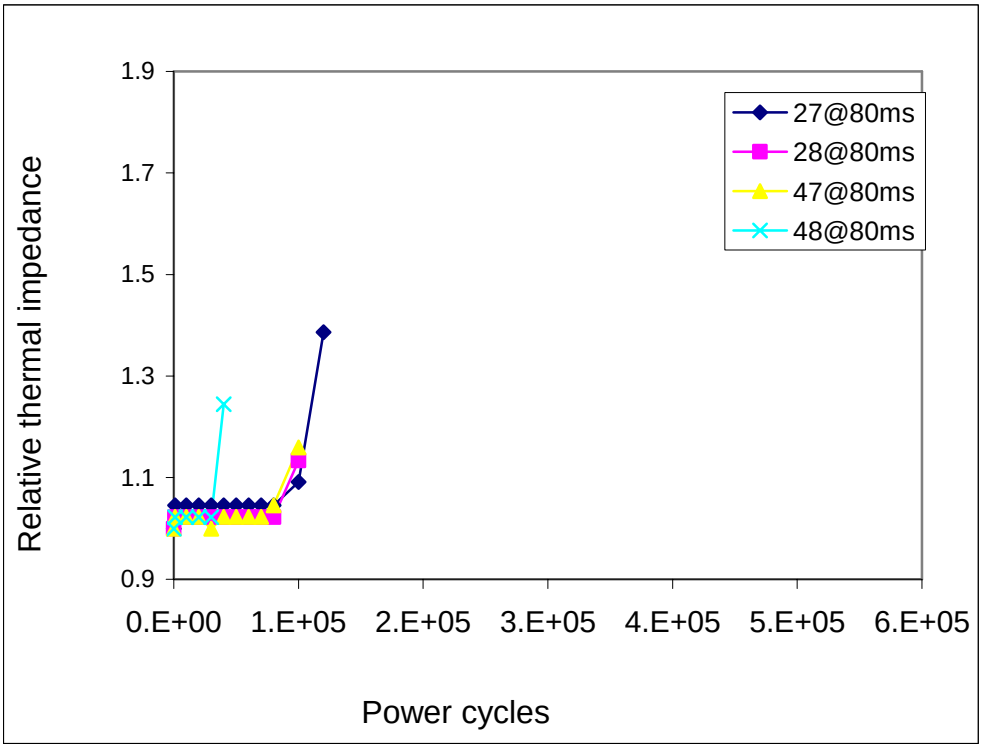


Figure 3. 17 Relative thermal impedance at 80ms change with power cycles for group (90w, 40µm)

3.4 Failure analysis

3.4.1 Procedure

The failure analysis procedure are performed in the following sequences:

1. Demount samples from the heat sink
2. Electrical testing
3. Remove silicon gel
4. Visual inspection of wire bond
5. C-SAM inspection
6. Stepped cross-section
7. Microstructure characterization

When the increase in thermal impedance exceeded 10%, samples were detached from the copper heat sink and analyzed. First, electrical testing was performed to check if the device was still connected. Then, the silicon gel and plastic case were removed. Second, visual inspection using optical microscopy and tweezers was conducted to see if failure had occurred at the wire bonds. Scanning acoustic microscopy (SAM) was used to check the presence of voids and/or cracks before and after power cycling. Next, in order to get information about the 3D distribution of the crack, a stepped cross-section was used. (See Figure 3. 18) For each section, microscopy was used to check the microstructure and locate the crack. As a result, the crack distribution and microstructure throughout the whole die attach region were determined. Both optical microscopy and scanning electron microscopy (SEM) /EDX or SEM/WDX were used to characterize the microstructure.

3.4.2 Failure analysis results

Electrical testing has found that all devices are still electrically connected. Then silicon gel is removed; wire and wire bonds are checked to see if they are still attached. If the samples do not show obvious wire detachment from the die, a small force was applied to the wires. The wires that have already lost most of their bonding strength will be detached. Wire bond lift-off occurred on some samples, but experiments have determined that the wire bond lift-off failure mechanism has an negligible effect on the increase in the thermal impedance and it is either die attach cracking or thermal grease degradation that caused the observed increase.

Scanning acoustic microscopy (SAM) is an imaging technique for non-destructive internal sample inspection allowing the detection of voids and cracks in the package.

Before power cycling, pulse-echo C-SAM using a 75MHz transducer was used to check for large voids or cracks in the die attach from the DBC substrate side. The results show only a few small voids in the sample.

In order to obtain a more complete picture of crack distribution, Samples 27,28,47,48,69 and 70 have been chosen and cross-section was performed at several depths (stepped cross-section) gradually from one side from section I to section IV and then section V from the opposite side. (See Figure 3. 18)

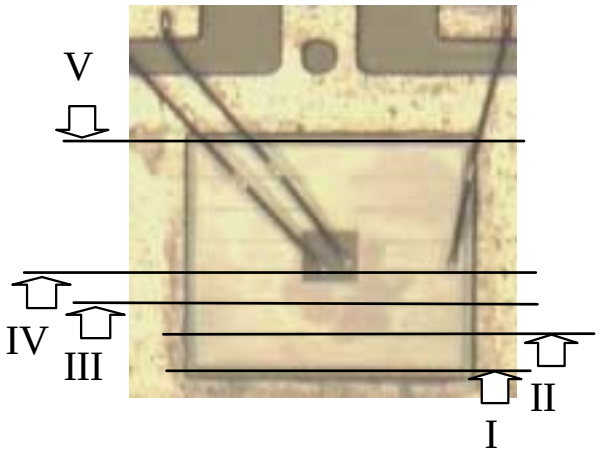


Figure 3. 18 Description of stepped cross-section plan

With optical microscopy, thicknesses of die attach and the locations of the crack were able to be determined. The result shows that thicknesses of the die attach are not uniform from one side to another. For the samples with die attach cracking, nominal die attach thicknesses are 40μm, the actual average thickness for those samples varies from 49μm to 53.5μm. The actual values throughout the whole region are listed in Figure 3. 20. Tilt was also detected for the samples without die attach cracking.

Cross-section also confirmed thermal impedance results that die attach cracking has only occurred to group (70w, 40μm) and group (90w, 40μm). For those samples, die attach cracking always occurred on one side, where the die attach is thicker. (See Figure 3. 20.

&Figure 3. 21) The thicker side could be on the gate side or the opposite side, indicating cracking is not related to the input source. Cracks are estimated to occupy 15~20% of the total area. (Complete results in Appendix D)

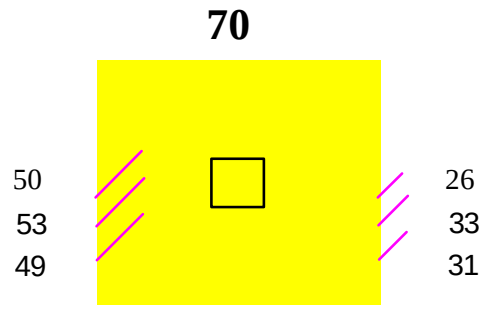


Figure 3. 19 Tilt exists in sample 70 without the presence of crack

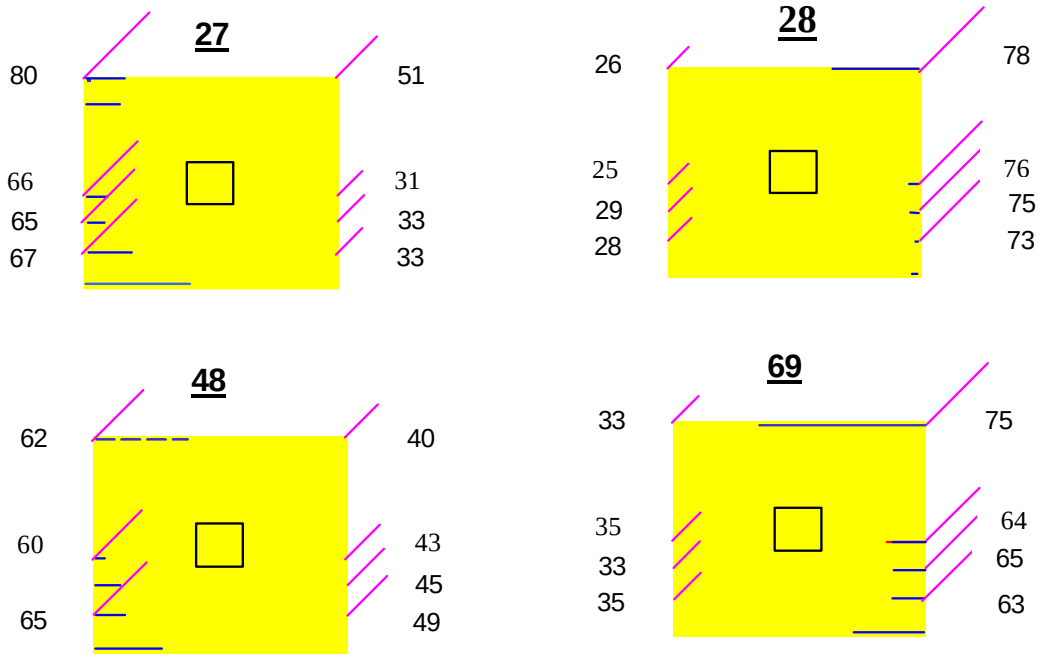


Figure 3. 20 Cracks occur at the thicker side, thickness at the ends is shown at both sides (unit: μm) Right is the gate side

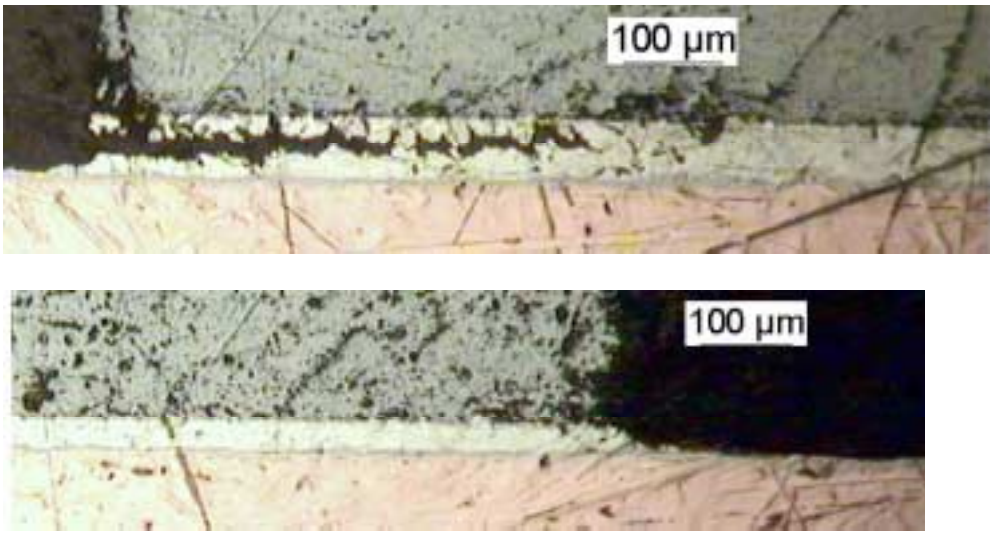


Figure 3. 21 Optical image of die attach at thick side (top) with crack across the middle of the die attach and thin side (bottom)

This difference in the die attach thickness is related to die tilt in power modules.[103][105][106] Here, the tilt angles here are less than 0.4°. The guidance provided by the manufacturer have recommended that up to 3° of tilt can be tolerated across the device and tilt should not be easily detectable in other axis <1°[105]. The extent of the tilt here is within the tolerance.

The tilt of the die does have an important effect on the die attach fatigue failure. Evans et al[103] have also reported uneven die attach thickness will result in crack at one side. However, Evans et al have attributed this to the wetting difference. From stepped cross-section (see Appendix D), we have found that the fillet shape at the edges does not have a correlation with the thickness and thus excluded wetting as the root cause for side cracking. Cracks usually occur across the bulk die attach and not at the interfaces.

In the following chapters, thermo-mechanical modeling as well as further microstructural characterization will be conducted to check the difference between the thin sides and thick sides.

Die attach thicknesses of three samples from group (70w, 80μm) and (70w, 20μm) have been measured. Die tilt has also been detected in those samples. The average thickness from group (70w, 80μm) changes from 60μm to 63μm and for group (70w, 20μm) from 20μm to 24μm. So the actual average die attach thickness is about 60μm for group (70w, 80μm), 50μm for group (70w, 40μm) and (90w, 40μm), and 20μm for group (70w, 20μm).

Cycles to failure (N_f) for those four groups are also compared to examine its relationship with average die attach thickness. N_f for group (70w, 80μm) and (70w, 20μm) is recorded when thermal grease failed, while die attach cracking has not started. Therefore N_f due to die attach cracking is expected to be longer for those two groups. The power cycling results have indicated that under the sample power level of 70w, die attaches of group (20μm, 70w) (average thickness: 20μm) and (80μm, 70w) (average thickness: 60μm) have a longer fatigue life than the ones of group (20μm, 70w) (average thickness of 50μm).

3.5 Conclusions and discussions

Power cycling continues in the experiments until either die attach fatigue cracking or thermal grease degradation causes at least 10% increase in the thermal impedance.

Through thermal impedance measurement and failure analysis, we were able to differentiate thermal grease degradation from die attach fatigue and determined that die attach fatigue is independent of thermal grease degradation. Die attach fatigue cracking has only occurred in the samples of group (70w, 40μm) and group (90w, 40μm). For those samples, thermal impedance at 80ms and 2s increase at the same time. It is shown that there was no thermal grease failure before die attach fatigue occurred, excluding the possibility that die attach failure is caused by thermal grease degradation. So die attach cracking is the cause for increase in the thermal impedance.

For three groups tested under 70w and one group under 90w with various average thickness, the results indicate that die attach with both thinner (20μm) and thicker (60μm) average thickness have a longer die attach fatigue life than the ones with 50μm average thickness under the same power cycling loading conditions. Typically, under the same loading conditions, thinner die attach leads to higher thermo-mechanical stress and results in a shorter fatigue life. However, the results indicate that samples of group (70w, 20μm) (average thickness: ~20μm) have a longer fatigue life than samples with thicker die attach, even when the smaller ΔT_j to group (20μm, 70w) is taken into account.

Experimental data has shown that once thermal impedance begins to increase, it increases at a high rate and quickly exceeds 10%. It is very likely that die attach crack initiation, under high frequency power cycling, is the dominant process and crack propagation will be very fast. Thermal modeling is needed to determine the relationship between crack area and thermal impedance increase.

In the study, die attach cracking has been observed to start from the edges, which is expected due to higher stress and strain on the edges. Instead of happening at all the

edges, however, the crack is always located on one side. Cross-section has revealed that die attach is always thicker on one side and thinner on the other side and crack always happens at the thicker side, indicating that tilt of the die has an important effect on the die attach fatigue. It is the direct cause of side crack and should be considered in the modeling. Further structural analysis will be conducted to determine the stress and strain difference between thick and thin side. Through cross-section, it is concluded that it is neither distribution of defects nor change of wetting behavior with thickness that cause the side crack. Wetting behaviors at the die attach edges changes from one sample to another, from one side to another randomly and could not be correlated with thickness. Cross-section has also confirmed that die attach cracking did not happen at the interfaces; instead, it is through the bulk solder. Interface failure is not an issue here.

Chapter 4 Thermo-mechanical modeling

4.1 Introduction

Modeling of the temperature and stress on the power modules during power cycling was conducted. Thermal transient analysis was applied to determine the temperature profile through the whole module during power cycling. At the same time, correlations between crack propagation in the die attach and the thermal impedance was also determined through thermal analysis. Next, the temperature profile was transferred to a 2D diagonal structural model to determine the stress and strain in the die attach.

4.2 Thermal transient analysis

Thermal transient analysis is used to determine the temperature distribution in the power module under power cycling. The temperature can then be used in later structural analysis. Thermal analysis can also establish the relationship between the extent of die attach cracking and the thermal impedance. Combining the simulation of crack size vs. thermal impedance increase with power cycling data on thermal impedance increase with cycling, the crack propagation rate can be estimated. Thermal transient analysis can also be used to determine the time required to differentiate failures at different layers in the module that contribute to thermal impedance increase, thus permitting differentiation of the increase of thermal impedance due to thermal grease degradation from that due to die attach cracking.

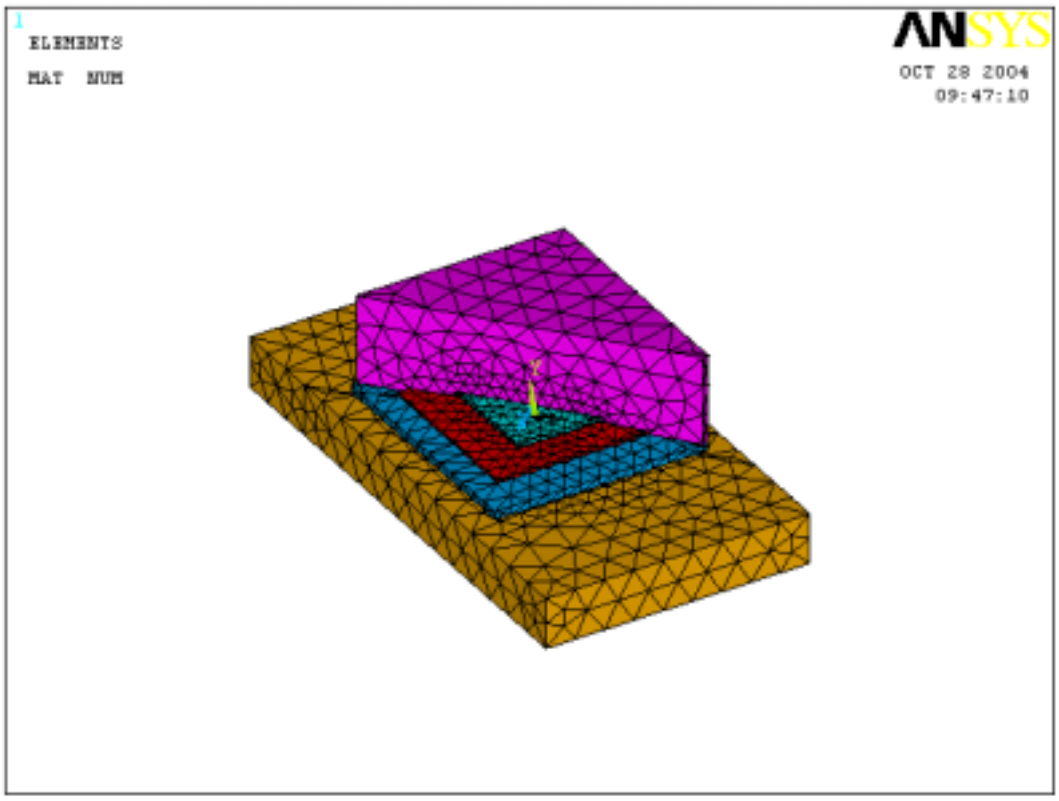


Figure 4. 1 ANSYS mesh of the power module used in thermal transient analysis (half silicone gel has been removed temporally to better reveal the inside structure

4.2.1 ANSYS Model

A power module including die, die attach, DBC substrate, thermal grease, heat sink and silicone gel was modeled here. (See Figure 4. 1) The effect of wire bonds was neglected. Silicone gel was assumed to fully cover the die and exposed top copper layer surfaces. The dimensions of the die and DBC substrate are modeled to be the same as described in the power cycling experiments. The heat sink is modeled to be 4mm-thick. Unless specified, the thickness of the die attach is defined to be 40 μm. The thickness of thermal grease is defined to be 51 μm.

Power is applied uniformly across the heat-generating region of the die as heat flux, which is located at 15 μm below the die surface. The bottom of the heat sink is fixed at

20°C as verified by thermocouple measurement. The power cycling frequency is 2 seconds on and 2 seconds off. In the model, Solid 70 was adopted as the thermal analysis element..

The thermal properties of the material are listed in Table 4. 1. Thermal conductivities for

Table 4. 1 Material thermal properties used in the simulation (Supplied by Grundos)

	κ w/mK	Density kg/m3	Cp J/KgK
Si	*	2.33e3	700
SnAgCu	75	7.40e3	213
Cu	385	8.93e3	385
Al_2O_3	**	3.97e3	765
Grease	0.3	1.00	1
gel	0.19	0.96e3	1400

both silicon die and Al_2O_3 in the DBC substrate are temperature dependent.

For die: κ= -0.42*T+274.16

For Al_2O_3, κ = -0.0703*T+46.019 (T: temperature in Kelvin)

4.2.2 Transient analysis results

Table 4. 2 Geometry parameters used in the simulation (Supplied by Grundfos)

	Length x width x thickness (mm^3)
Heat generated region	6.94x5.79x0.005*
Die	7.70x6.55x0.375
Die attach	7.70x6.55x(0.03~0.08)
Cu up layer	13x13x0.3
Al_2O_3	14x16x0.635
Cu bottom layer	17x19x0.3
Grease	17x19x0.045
Heat sink	21x39x4
Gel	14x16x(0.02~0.08)

This section presents the results of the thermal transient modeling. Figure 4. 2 shows a cross-section view of the temperature distribution of the power module at the end of the "on" portion of the power cycling for a power of 70w. Figure 4. 3 shows the peak temperature distribution on the die during the 3rd cycle when temperature is stabilized.

The simulation was compared to results measured by IR camera where silicone gel is excluded. In the simulation, the junction temperature reaches maximum in the center. A

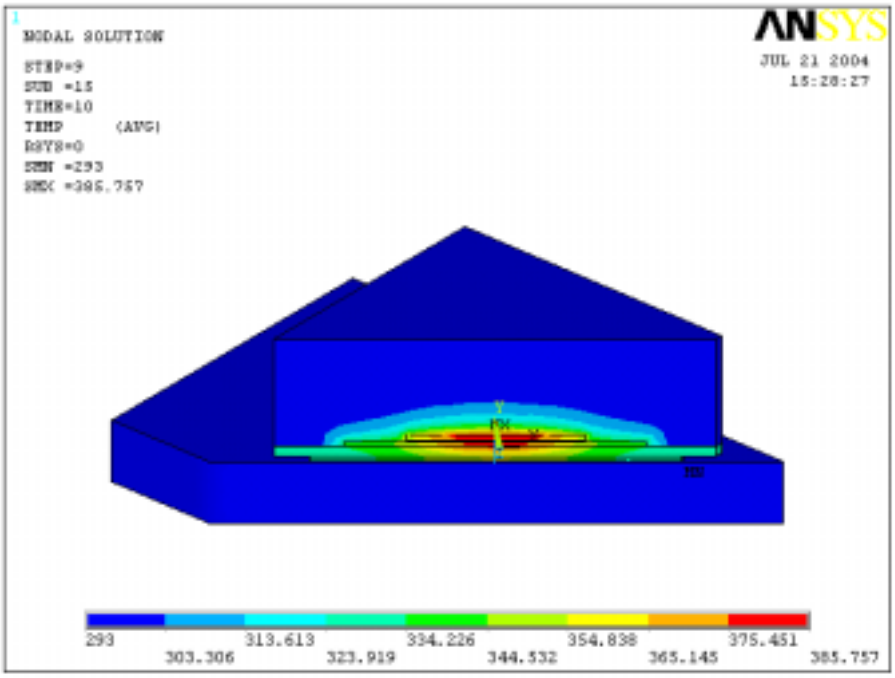


Figure 4. 2 Temperature distribution of the power module with 40 µm thick die attach and 51µm thick thermal grease

similar distribution is also detected with IR camera. The IR camera was also used to measure the maximum junction temperature (T_{jmax}) that appears on the die surface, which was compared to the T_{jmax} from the simulation. (Figure 4. 4)

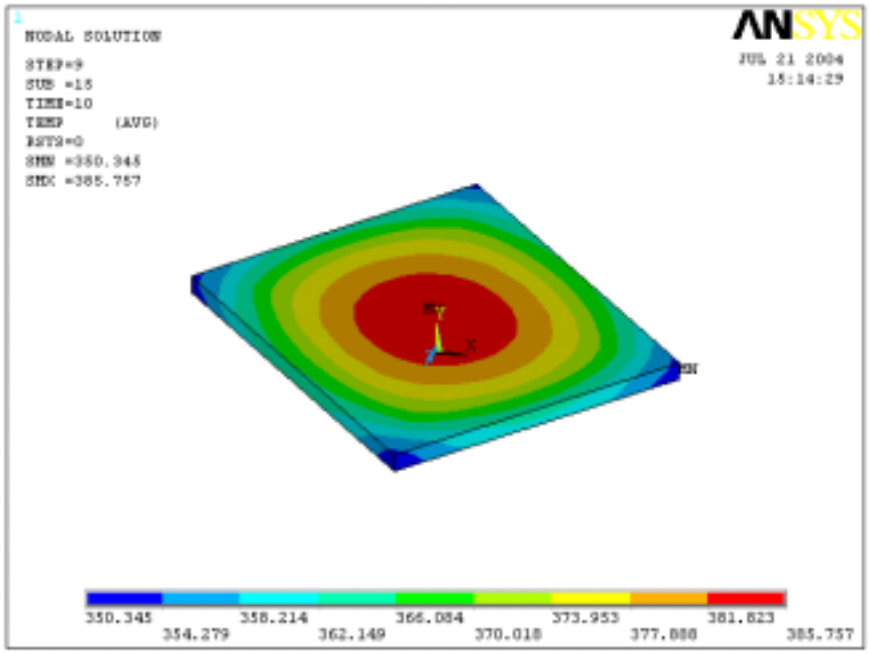


Figure 4. 3 Temperature distribution on the die with 40 µm thick die attach and 51µm

In the power cycling experiments, the initial thermal impedance varied from one DUT sample to another. (See Appendix C) There are two possible causes for the variation:

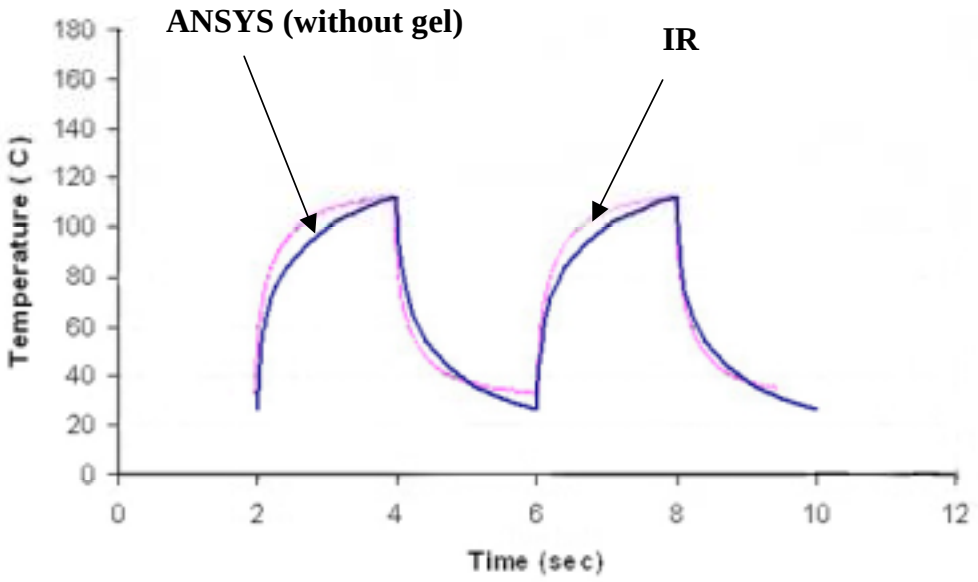


Figure 4. 4 Comparison of maximum junction temperature between simulation and measurements from IR camera

first, a variation in the thickness at the die attach that has been confirmed by cross-section; second, a variation in the thickness of the thermal grease. It is very difficult to determine the thickness of the grease directly. Instead, grease thickness is obtained indirectly by adjusting the thickness value in the simulation until the calculated thermal impedance matched the value measured by thermal impedance tester.

The junction temperature (T_j) used to calculate thermal impedance should be the average temperature over the heat-generating region. In the simulation, it is calculated by averaging the temperature of all the nodes that belong to the heat-generating region. Since most of the elements in the region are almost equal in the size, this method is accurate enough to estimate the average junction temperature (T_{javg}).

4.2.2.1 Effect of die attach thickness on thermal impedance

Cross sectioning has revealed that the die attach thicknesses ranges from 20 to 80µm between samples and to a less extent across the width of a sample. Figure 4. 5 shows the corresponding thermal impedance for a fixed thermal grease of 51µm. T_j (average temperature over heat-generated region) is used to calculate thermal impedance by the following equation:

$$Z_{jc}(t) = \frac{(T_j(t) - 293)}{Power}$$

The results revealed that variation in the die attach thickness in the actual samples has a negligible effect on both the junction temperature and overall thermal impedance. This is

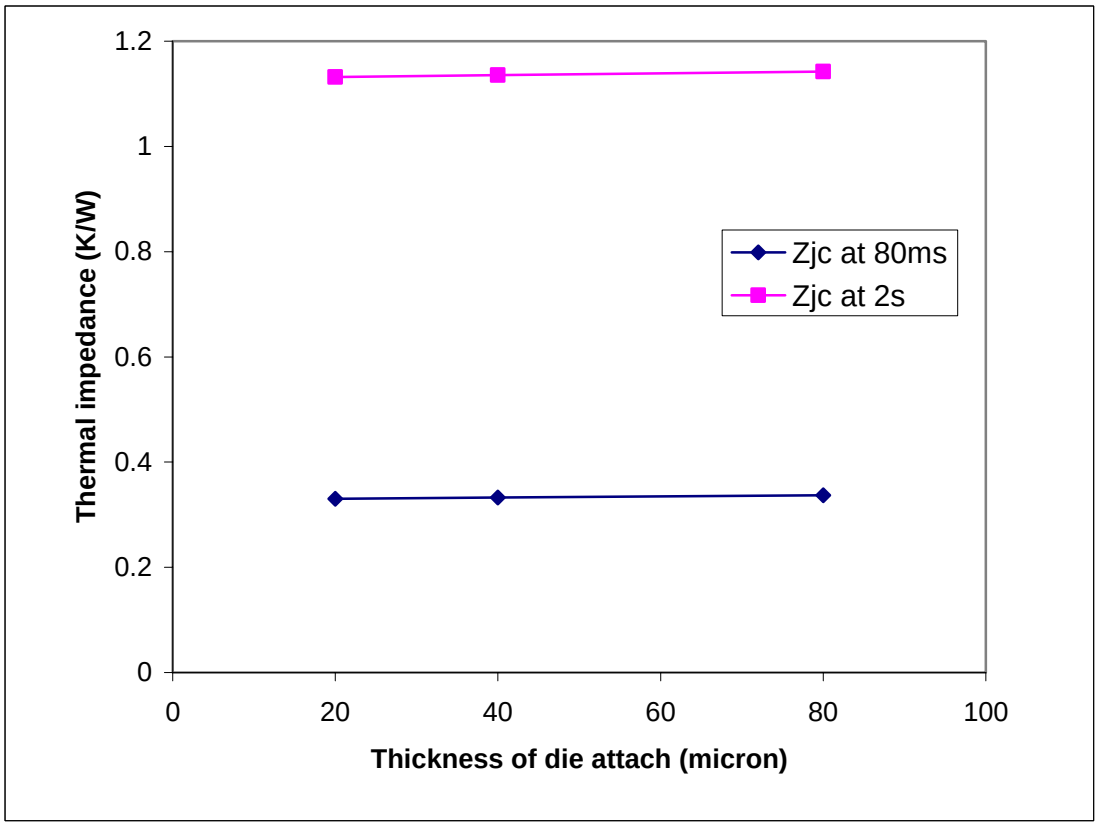


Figure 4. 5 Effect of die attach thickness on the increase of thermal impedance

expected due to its small thickness and high conductivity. Its effect on the thermal impedance can be ignored and it is not the cause for any observed variations.

4.2.2.2 Effect of thermal grease thickness on thermal impedance

Thermal grease usually comprises a large part of the thermal impedance of the multilayer module due to its very low thermal conductivity (0.3 w/mK). Simulation confirmed that as thermal grease changes from 20μm to 80μm, thermal impedance at 2s increases from 0.799 to 1.392. (Figure 4. 6) The results have also confirmed the variation in the thermal grease thickness has a negligible effect on the thermal impedance measured at 80ms. The actual thermal impedances for the samples measured by the thermal impedance tester vary from 0.74 to 1.41 at 2s (see Appendix C). So the variation in the grease thickness is the dominant cause to the difference in the initial thermal impedance in the samples.

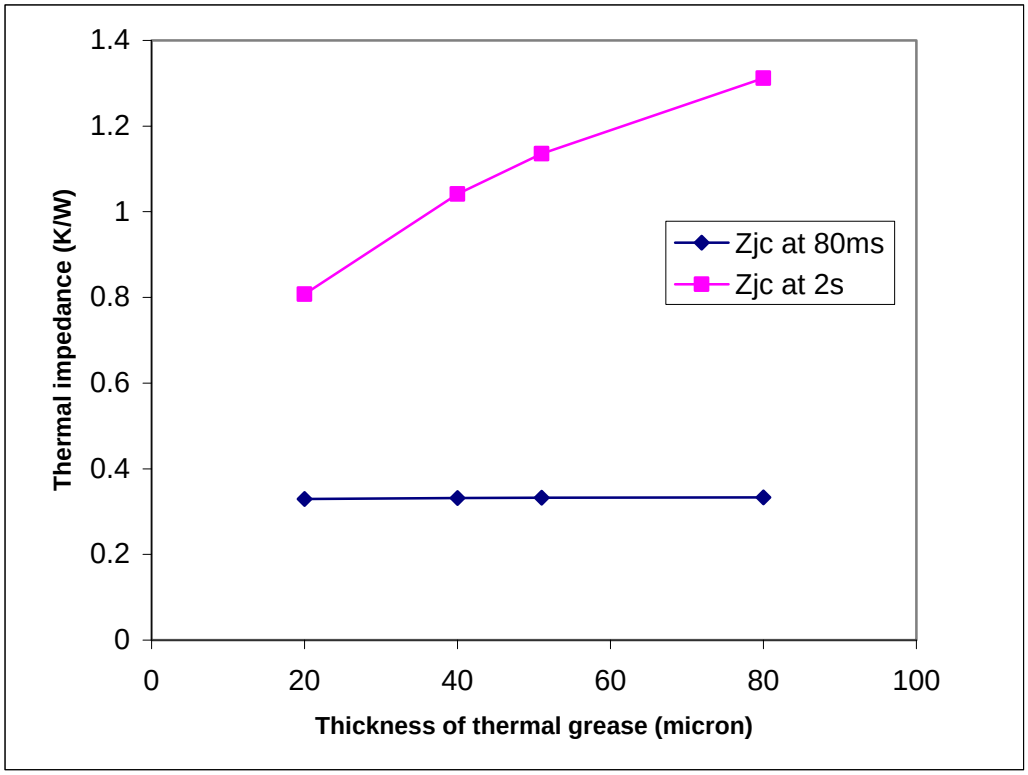


Figure 4. 6 Effect of thermal grease thickness on the thermal impedance

Since the thickness of thermal grease could not be determined directly, thermal transient analysis is used to estimate the thickness of the thermal grease for each sample. First, correlation between the thickness of the thermal grease and thermal impedance is established through thermal transient analysis shown in Figure 4. 6. Next, based on the relationship, the thickness of the grease is estimated since the thermal impedance is already available through power cycling experiments.

4.2.3 Effect of crack propagation on thermal impedance increase

In order to model die attach fatigue, it is important to understand the crack propagation behavior during power cycling. Crack propagation could not be directly monitored during power cycling. Instead, thermal impedance increase is used as an indication of the die attach fatigue cracking. Thermal impedance is monitored at both 80ms and 2s every 10,000 cycles until the increase exceeds 10% at 2s. Based on the cross-section results, the crack area is very irregular and always located at one side. Through thermal transient analysis, the relationship between thermal impedance increase and crack area is determined. In the thermal analysis, cracks are modeled by specifying the properties of the elements in the die attach crack region as air. Once the relationship is established, we can estimate crack propagation based on the experimental data of thermal impedance increase monitored during power cycling.

In the first case, thermal grease is 51μm thick and the die attach is 40μm thick. The crack area is simulated at 0%, 5%, 10%, 15% and 20% of the die attach region. For simplification, only rectangular side cracks are considered. Figure 4. 9~Figure 4. 13 show

the corresponding temperature distribution of the die surface at 2 seconds. The results (from Figure 4. 8 to Figure 4. 13) show that as crack initiates from the edge, the temperature of the die located above the crack starts to increase. In the beginning, the influence of the crack on the temperature of the junction where heat flux is applied is minimal (shown in Figure 4. 8). After the crack reaches 10%, the temperature above the crack continue to increase and the influence on the temperature in the heat-generating region starts to increase. (See Figure 4. 11& Figure 4. 13) This can be attributed to the fact that after the crack reaches 10%, it begins to block the dominant downwards heat dissipation path, which is just below the active region. This has an obvious effect on the junction temperature and induces an obvious “hot spot” just above the crack. Figure 4. 8 shows the temperature distribution in the middle across the length of the top die surface at 2 seconds as side cracking propagates from 0% to 20%. It is clear that the peak temperature is located in the center before the cracking reaches 10%. It will finally shift toward the crack as crack proceeds to 15% and 20%.

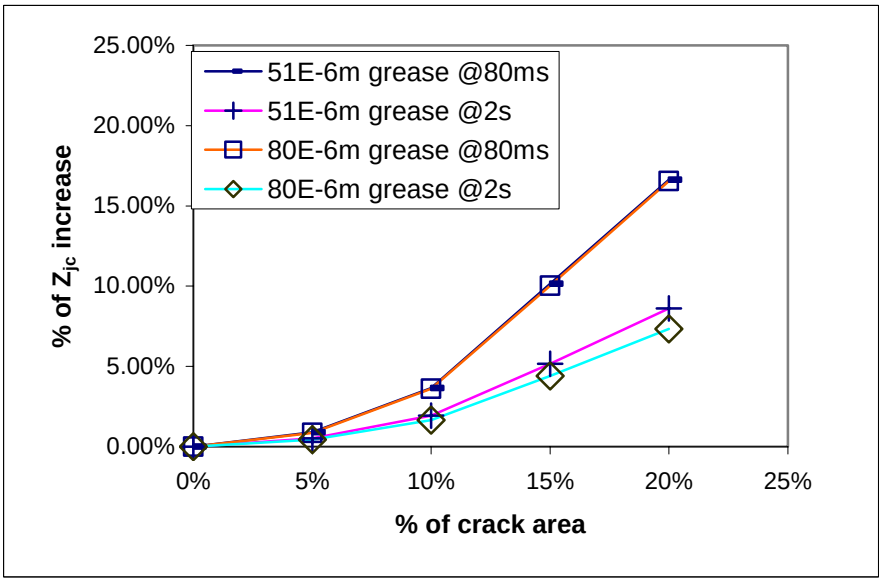


Figure 4. 7 Correlation between thermal impedance increase and die attach side crack

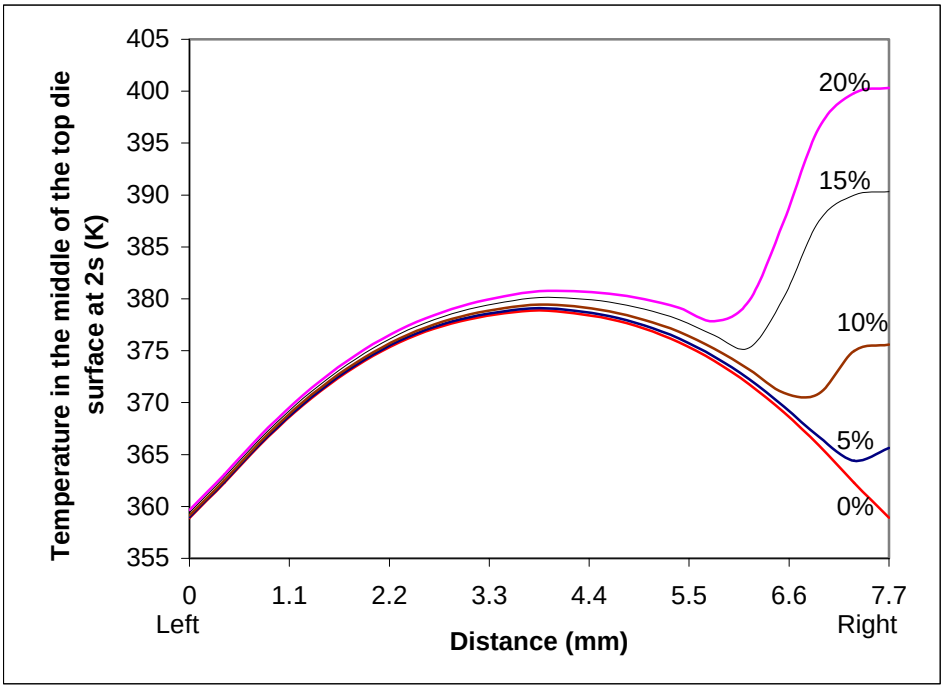


Figure 4. 8 Temperature distribution in the middle line of the top die surface at 2 seconds at different extent of side crack (located at right side)

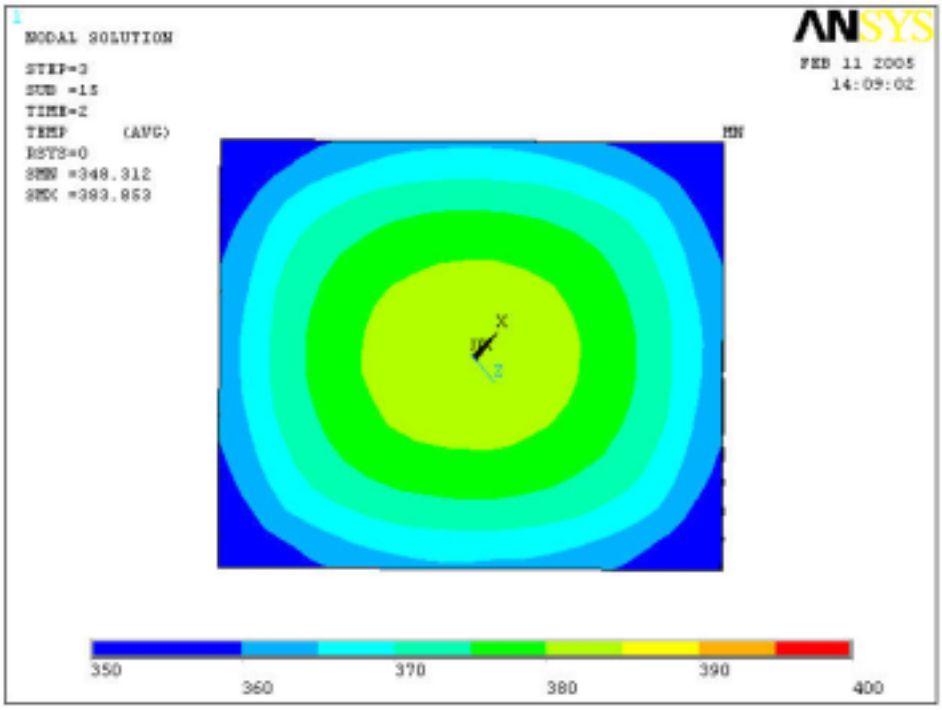


Figure 4. 9 Temperature distribution on top die surface without crack

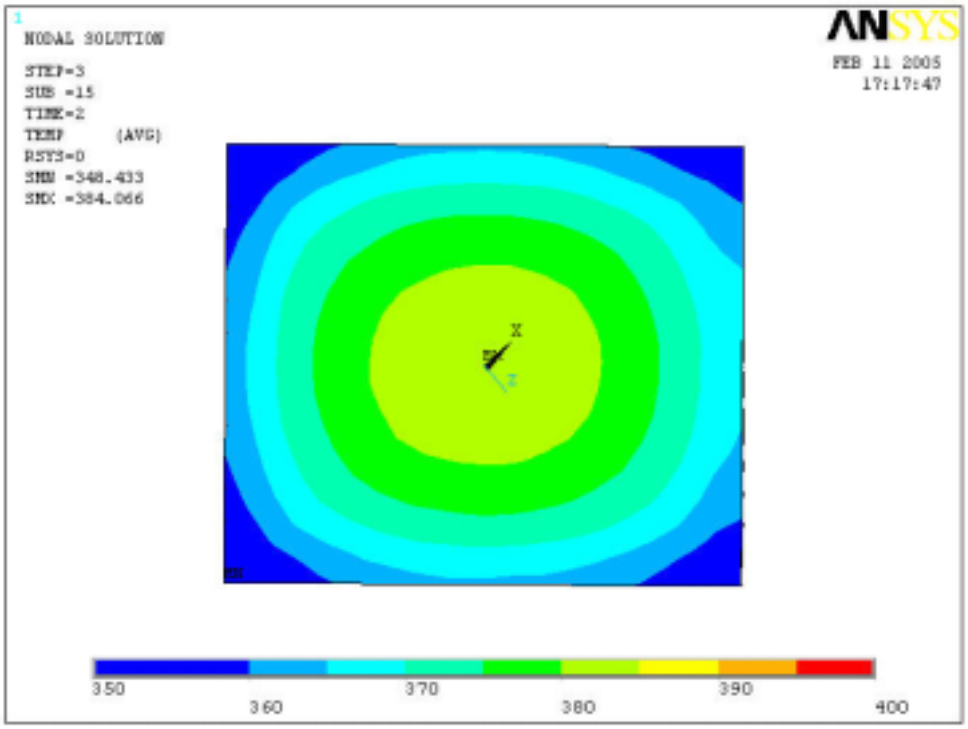


Figure 4. 10 Temperature distribution on top die surface with 5% crack at the right side at 2s

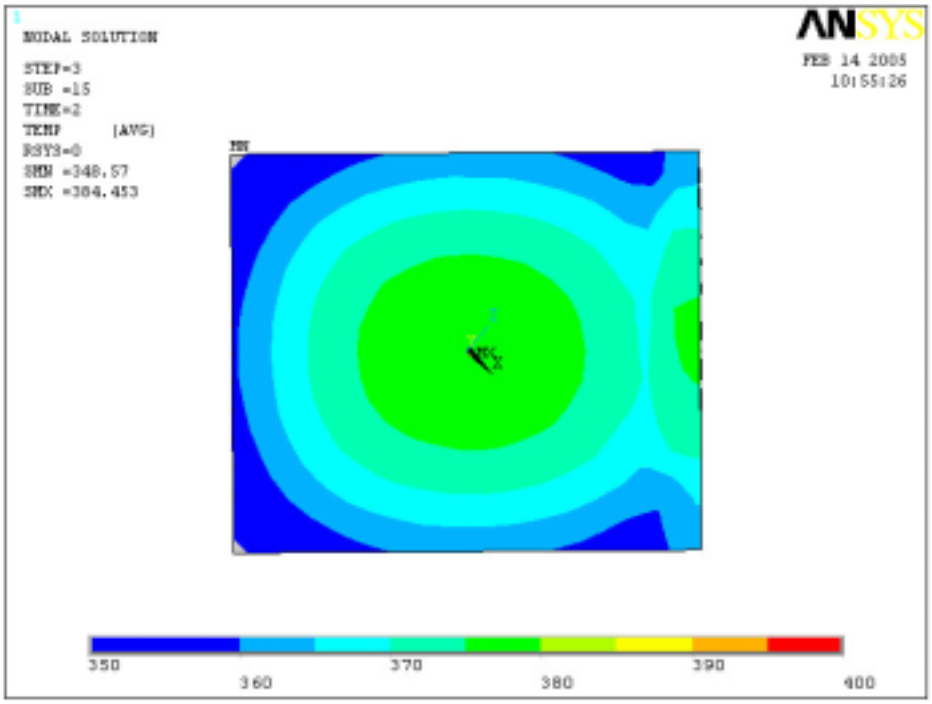


Figure 4. 11 Temperature distribution on top die surface with 10% crack at the right side at 2s

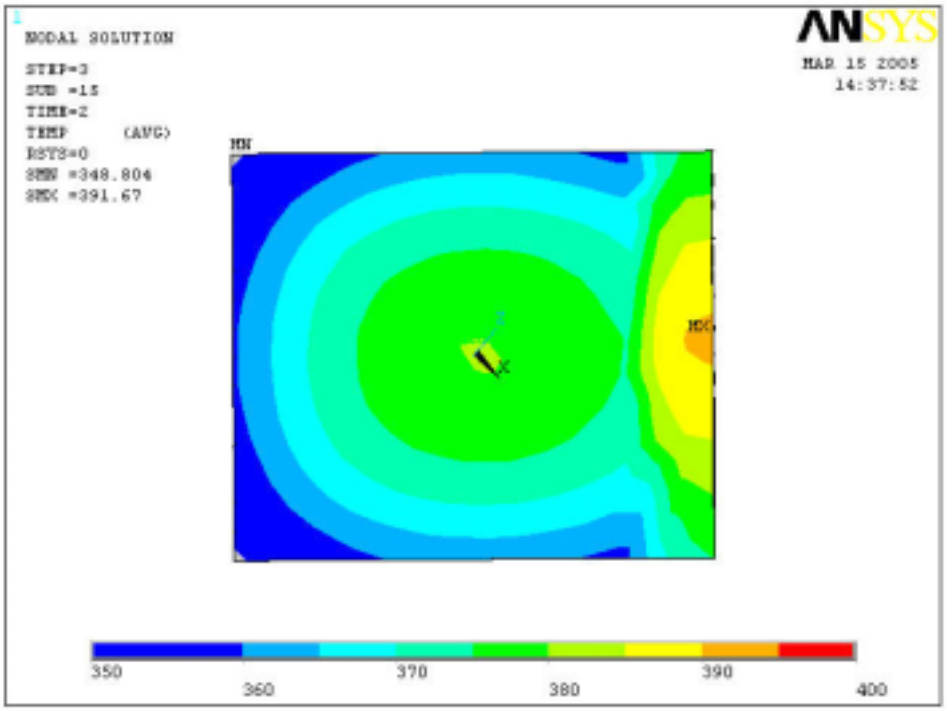


Figure 4. 12 Temperature distribution on top die surface with 15% crack at the right side at 2s

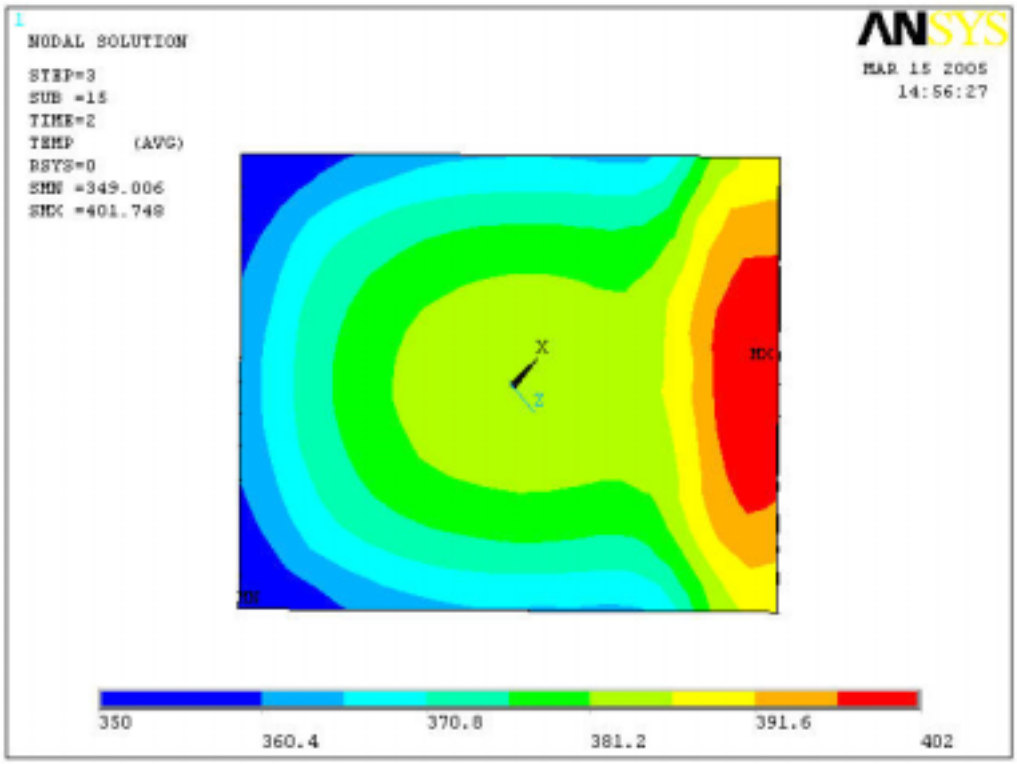


Figure 4. 13 Temperature distribution on top die surface with 20% crack at the right side at 2s

In the second case, the thickness of thermal grease is set to be 80μm. Thermal impedance at both 80ms and 2s are compared with the first case where the thickness of the grease was 51μm. The results show that Z_{jc} at 2s is very sensitive to the thickness of the thermal grease. The grease has little effect on Z_{jc} at 80ms and the increase due to crack propagation is more stable. So Z_{jc} at 80ms is a better criterion to monitor die attach cracking.

Before crack reaches 10% of the die attach area, the increase in the thermal impedance is very small (<5%). After the crack exceeds 10%, the increase in the crack area results in a large increase in the thermal impedance. 10% and 16.6% increase in Z_{jc} at 80ms

corresponds to about 15% and 20% crack respectively. This is also confirmed by failure analysis on the failed sample.

4.2.4 Discussion

Through thermal transient analysis, we have correlated die attach crack with thermal impedance increases. Generally, die attach crack propagation increases thermal impedance; causing the temperature of the die especially in the region above the crack to increase. As the crack initiates from the edge, it has little influence on the average junction temperature. Simulation shows 5% and 10% side crack will only cause thermal impedance at 80ms to increase 0.95% and 3.65% respectively. Thus the thermal impedance tester can hardly detect the crack until it occupies about 10% of the area.

At the same time, experiments have indicated that thermal impedances are stable as power cycling starts. The measurements may increase or decrease within ±2%, which are probably the noise and not the actual change. However, as the thermal impedance starts to increase, the increase is dramatic. After correlating this dramatic increase with die attach cracking, we can conclude that dramatic increase happens before thermal impedance reach 5%, which corresponds to about 10% crack. However, we were unable to determine the exact stage when this rapid increase starts experimentally. This rapid increase happened is due to the following:

1. Under power cycling, once the die attach crack initiate, the propagation is fast. This has been reported by other studies [103]
2. Die attach cracks create a localized temperature increase around the crack that served to increase the thermo-mechanical stress near the crack and accelerate

crack propagation. The temperature increase near the crack is around 10~20°C for a crack area of 10%. It is suspected that the temperature increase of the die due to the crack will decrease extent of the C.T.E. mismatch between the die and the substrate. As a result, this will decelerate the crack propagation. However, the portion of the die that contribute to the C.T.E. mismatch is the die above the un-cracked die attach. For this portion, the temperature increase is negligible even for 10% crack (shown in Figure 4. 11). So this deceleration does not seem to be an issue here.

Although we could not determine when the dramatic increase in the thermal impedance starts, crack initiation is very likely to be the limiting process. As a result, the crack-initiation based fatigue model without considering crack propagation is expected to provide a good estimation.

4.3 Preliminary non-linear structural analysis

Nonlinear 2D plain strain finite element analysis is conducted for the case where die tilt exists. The objective is to examine the stresses/strains at the thick and thin side under power cycling and determine the cause for cracking at the thick side.

4.3.1 Development of stress model

A 2D diagonal plain-strain model is adopted for the stress analysis. The dimensions of the die and DBC substrate are the same as described in the thermal transient analysis. It is assumed that both thermal grease and heat sink are decoupled from the rest of the stack and are therefore not included in the module. Only the die, die attach and DBC substrate are modeled. From destructive physical analysis, we have found that the thickness of the die attach varies across the module. This variation in thickness is considered in both thermal and stress analysis. The edges of die attach are simplified as being perpendicular to the substrate in the model although they may be sloped with a fillet sometimes. Displacement of the bottom of the DBC substrate in the thickness direction is fixed. Quadratic plane42 elements are used and the mesh density is increased near the edges of the die attach. There are 4 rows of elements across the die attach thickness. (Figure 4. 14)

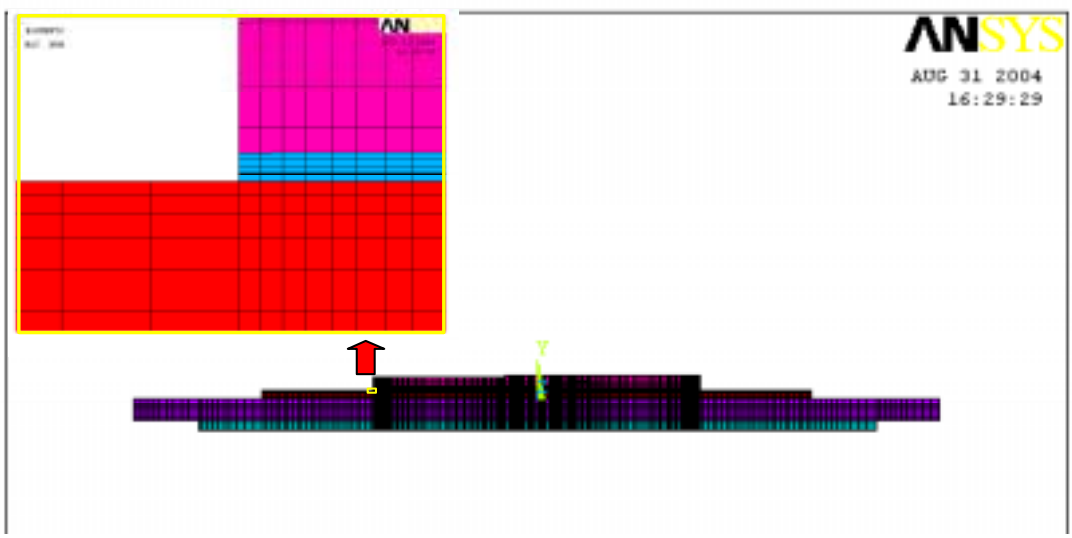


Figure 4. 14 Mesh assigned in the structural model

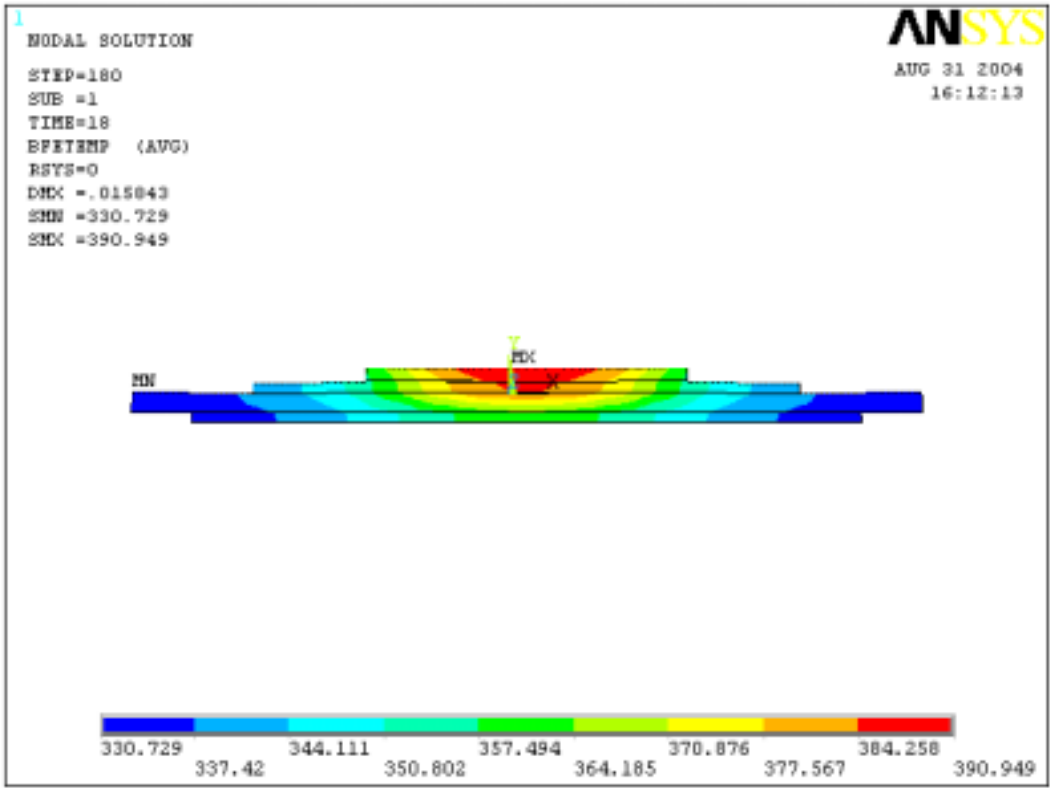


Figure 4. 15 Temperature loading at one step used 2D structural analysis, which is transferred from 3D thermal transient analysis

The temperature loading is caused by the power cycling applied to the active region inside the die. In the 2D structural analysis, the temperature loading will be transferred from the 3D thermal transient analysis. (See Figure 4. 15) However, ANSYS does not provide a function to directly transfer temperature loading at each time step during power cycling from 3D to 2D diagonal cross-section. ANSYS codes (See Appendix F) were developed to automatically read the temperature from thermal analysis results and transfer them as the load in the stress analysis. The input code also includes all the information for the modeling in order to the simulation. Any change in the geometry, mesh specification, material properties and loading profile can be updated in the input code. First, 3D thermal transient analysis is conducted for 3 power cycles (2 seconds on and 2 seconds off) and the temperature loading is transferred from the 3rd cycle.

Homogeneous properties are assumed for all materials. Elastic properties are assigned to the die and DBC substrates. (See Table 4. 3) Elastic, plastic and creep properties are assigned to the solder based on the test data on Sn3.8Ag0.7Cu solder by Zhang [39].

Table 4. 3 Elastic properties used in the simulation

	E (GPa)	η	C.T.E. (10^{-6})
Si	112	0.28	2.5
SnAgCu		0.34	17.6
Cu	110	0.33	17
Al_2O_3	300	0.21	7.5

Table 4. 4 Elastic modulus of SnAgCu[39].

Temperature (K)	298	348	398
Elastic modulus (MPa)	18367	16484	16304

Table 4. 5 Elastic modulus of SnAgCu[39].

C_1	C_2	C_3	C_4
1500	0.19	4.0	8176.9

$$\dot{\varepsilon}_{creep} = C_1[\sinh(C_2\sigma)]^{C_3} \exp(-C_4 T)$$

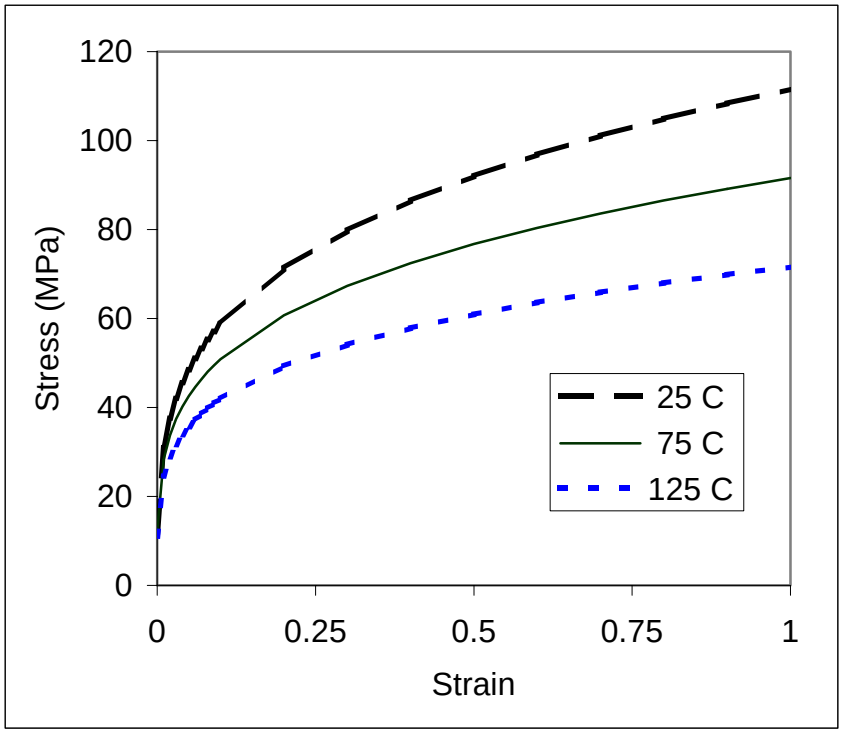


Figure 4. 16 Temperature dependent plasticity of SnAgCu[39].
(multilinear isotropic in ANSYS)

4.3.2 Effect of die tilt

From measurements on the cross-section images, the thickness of die attach is not uniform (die tilt). Usually, one side is thicker than the other side. Even if the thicker side is twice as thick as the thinner side, the resultant tilt angle is still very small (less than 0.4°) due to a very low ratio of the thickness to the length. Nevertheless, it is important to investigate the effect of die tilt on the stress/strain distribution in the die attach, since in experiments, the die attach crack always occurred at the thicker side.

The first simulation was based on the experimental results from sample 48, where die attach thickness was set to be 44μm on one side and 63μm on the other side. (Tilt angle is 0.14°). Thermal grease thickness was calculated to be 61μm. Average junction temperature at 2s was determined to be 379.66K, which matched with thermal impedance measurements.

Next, the thickness of die attach was assumed to be uniform and equal to the average thickness of the first case (thickness =(44+63)/2.0= 53.5 μm). Other parameters were kept the same.

The thermal analyses show that the differences in the die attach thickness have a negligible effect on temperature distribution, especially between the thick and thin side.

In thermal transient analysis, the distribution became stable at 3rd cycle and the temperature profile for this cycle was transferred to the 2D structure as the power cycle. 5 power cycles were applied in the structural analysis and the deformation reached stable at 5th cycle. So stress and strain was evaluated at 2S, the end of the power “on” segment of this cycle.

The stress and strain distribution is plotted across the diagonal length in the middle of the die attach thickness, where crack is usually located. Figure 4. 17 shows the shear stress, Von-Mises stress and hydrostatic stress distribution across the middle of the bondline. Here, the left end is thinner (tilt) and the right end is thicker.

The results show that stress (Figure 4. 17) and strain (Figure 4. 19) are the lowest in the center and reach a maximum at the two ends in the middle of the bondline. This is why the die attach cracks typically start from the ends. Peeling stress (stress Y in the figure) is almost zero inside the die attach and dramatically increases near the two ends. This is likely to be one important factor to accelerate the crack failure and its effect should not be neglected. So the V-M component instead of the shear component is going to be used to evaluate the fatigue life of die attach.

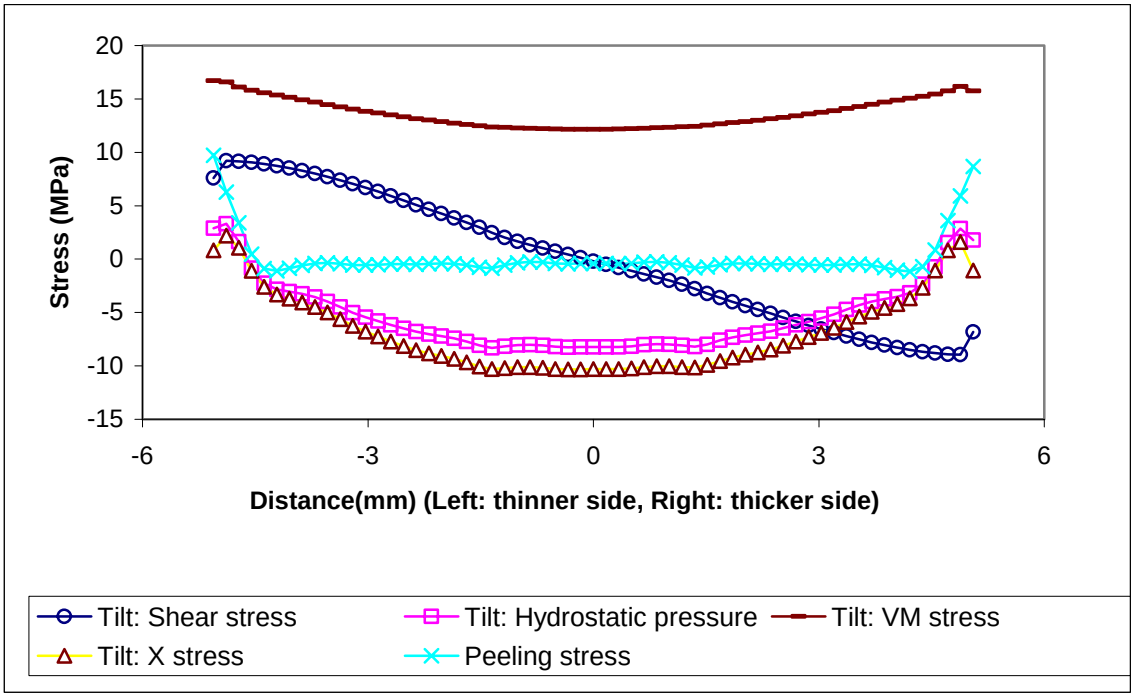


Figure 4. 17 Stress distribution along the middle of the bondline of die attach (Thickness at left end: 44μm; thickness at right end: 63μm)

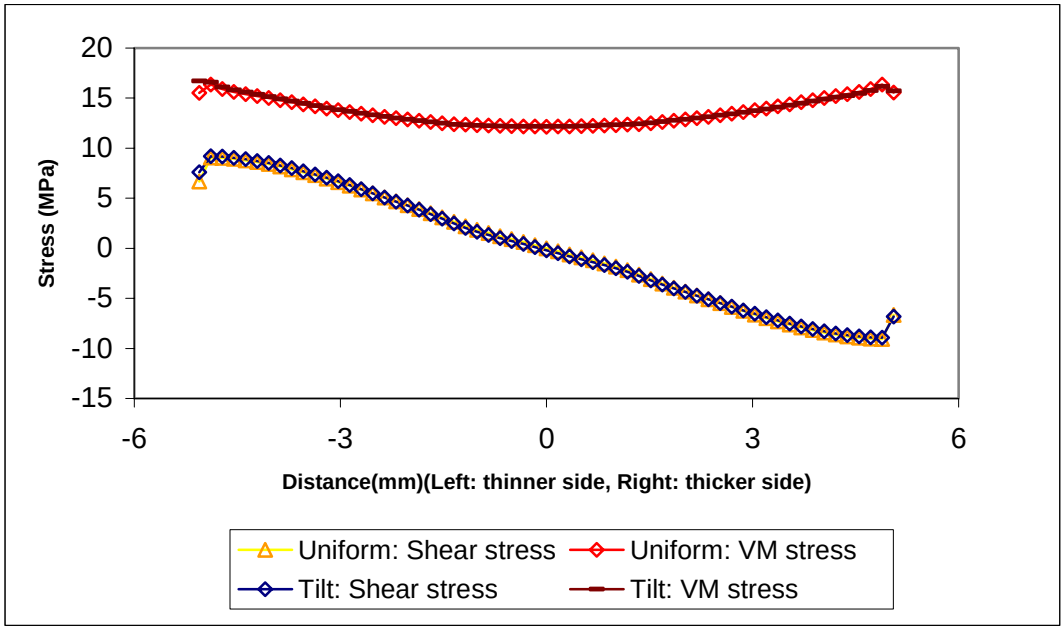


Figure 4. 18 Stress distribution along the middle of the bondline of die attach of tilt case (thickness at left end: 44μm; thickness at right end: 63μm) and uniform thickness case (thickness 53.5μm)

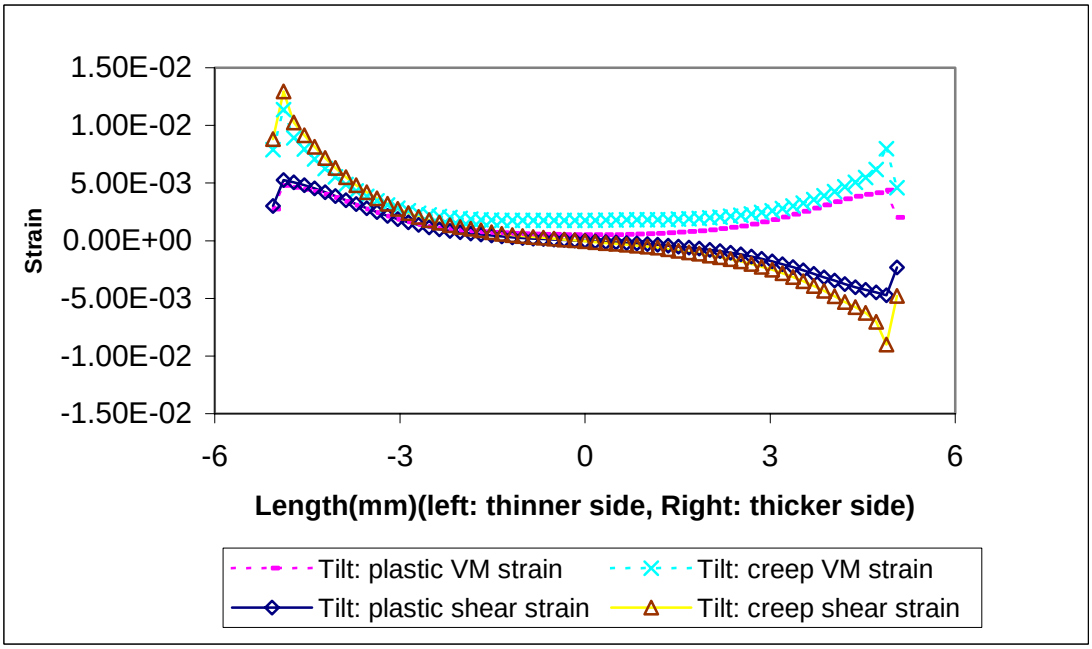


Figure 4. 19 Strain distribution along the middle of the bondline of die attach (Thickness at left end: 44μm; thickness at right end: 63μm

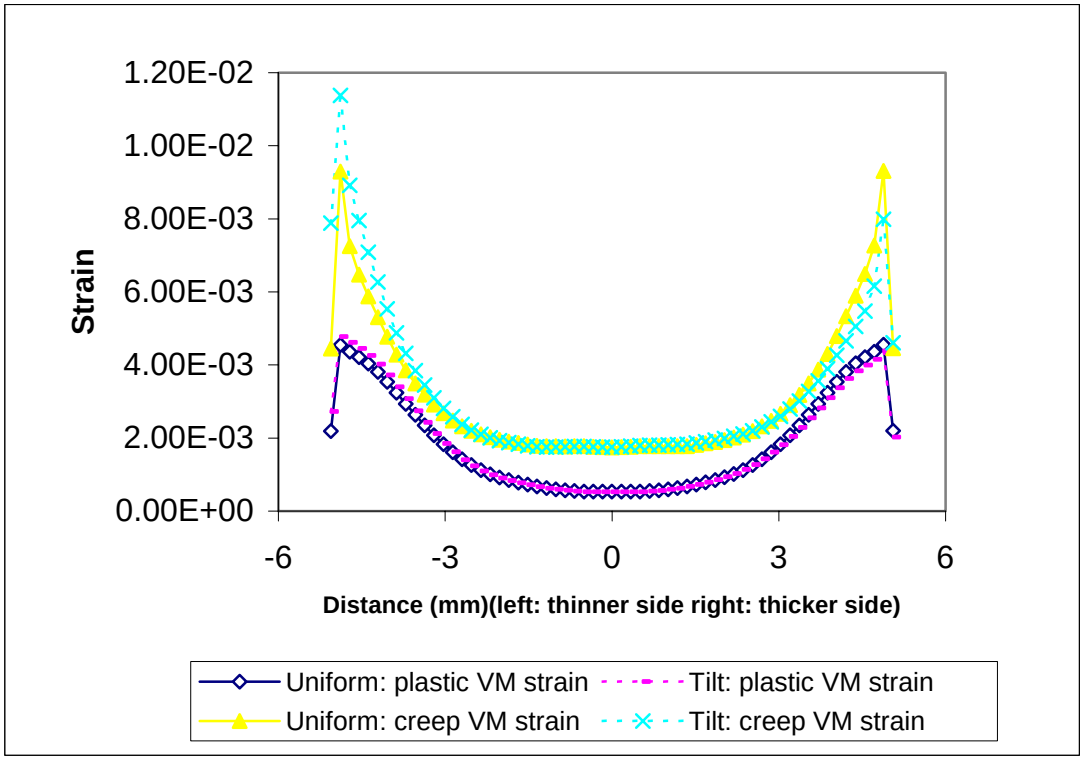


Figure 4. 20 Strain distribution along the middle of the bondline of die attach of tilt case (thickness at left end: 44μm; thickness at right end: 63μm) and uniform thickness case (thickness 53.5μm)

Furthermore, both shear stress and Von-Mises stress at thinner end are slightly higher than at the thicker end. Similar trends are also indicated by plastic and creep strains. The differences in the strains between thin and thick ends are larger than the corresponding stress, especially for the shear creep strain. (See Figure 4. 19) At the same time, deformation under tilt condition is also compared to the uniform bondline thickness condition. It is clear that the magnitude of stress/strain for uniform bondline thickness fall into the range between the thicker and the thinner side. (See Figure 4. 18 & Figure 4. 20)

4.3.3 Discussion

From the simulation, it is clear that under the tilt condition, stress and strain are always higher at the thinner end. So the crack might be expected to occur at the thinner side. However, this is the opposite of what was observed in the experiments where cracking occurred at the thicker side.

4.3.3.1 Effect of wetting angle

One possible cause for cracking at the thick side is that the wetting angle at the thick end might induce a higher stress concentration. In the experiments, the wetting angle at the ends of the die attach was investigated based cross-section results. The shape of the ends varies from one location to another and there are no clear correlations between the wetting angle and the thickness. It is concluded that wetting is not the root cause.

4.3.3.2 Effect of hydrostatic stress (σ_H)

Second, the effect of hydrostatic stress on the fatigue behavior of die attach has also emerged as a potential cause. Studies[118] have found a negative compressive (negative σ_H), retarding the crack growth, and thus making die attach less likely to fail.

From the simulation, it is clear that there is a compressive stress (negative σ_H) (see Figure 4. 17) inside the die attach. However, its magnitude decreases towards the ends to around zero and the differences in σ_H between the thick and thin end are negligible. Therefore, the effect of hydrostatic stress can be excluded as the cause.

4.3.3.3 Effect of microstructure

At the same time, it is possible that the mechanical properties of the solder die attach could change with the thickness due to microstructure variation. From the microstructure characterization, it appears that the dissolution of Ag from the die finishes and difference in the cooling rate could contribute to variation in the microstructure across the length of the die attach. This is another factor that needs to be included in the modeling in the future and is discussed in the next chapter.

Chapter 5 Microstructure characterization

5.1 Introduction

In this chapter, effects of die attach thickness and the surface finishes on the microstructure will be discussed. Metallurgical studies will also be conducted to investigate die attach cracking. Difference in the microstructure between the thick and thin side under tilt affecting die attach cracks at the thick side is also examined.

The samples are cross-sectioned, ground and polished to reveal the microstructure. The polished surfaces are etched by HCl vapor to better reveal the microstructure. Sometimes, an etchant with 93 vol% CH_3OH, 5 vol% HCL, 2 vol% HNO_3 is also applied. The samples can be divided to the following categories:

1. Fresh samples that have not been power cycled
2. Cycled samples with die attach cracking
3. Cycled Samples without die attac h cracking

5.2 Microstructure of SnAgCu die attach

SnAgCu solder is usually composed of Sn dendrites and a Sn matrix with Ag_3Sn and Cu_6Sn_5 intermetallics. The distribution of Ag_3Sn and Cu_6Sn_5, determines the microstructure of the die attach. As a result, the distribution of Ag_3Sn plays an important role in influencing the thermo-mechanical properties of the solder attach and is the focus of the microstructure characterization in the study.

At the same time, the extremely rapid growth of the crystalline Sn phase (>20 cm/s) from the under-cooled Sn metal suppresses nucleation of other Sn crystals.[121][122][123]] As a result, very few grains can be expected within a typical SnAgCu solder ball of a few hundred micrometers in diameter. Since the thickness of the SnAgCu die attach is less than 100μm, few grains are expected to appear across the thickness of the die attach. As a result, the effect of grains on the mechanical properties of the die attach isn't important and won't be discussed here.

The eutectic structure of SnAgCu will be laminar shape. And Ag_3Sn particles have a specific orientation relationship with the Sn matrix: {012} Ag_3Sn//{111} Sn and <100>Ag3Sn//<110>Sn[107]. As a result, it has been widely reported that the morphology of Ag_3Sn is needle-like.[125]

5.2.1 Dissolution of Ag from die finishes

Ag_3Sn precipitates have been detected in the samples just after soldering. It is clear that those Ag_3Sn are formed during soldering. WDX mapping of the die attach (nominal thickness about 40μm) have also revealed that little Ag is left at the die/die attach interface. Most of them have dissolved into the bulk after soldering. (See Figure 5. 1& Figure 5. 2) Dissolution of Ag from the die finishes contributed to the formation of Ag_3Sn intermetallics in the die attach.

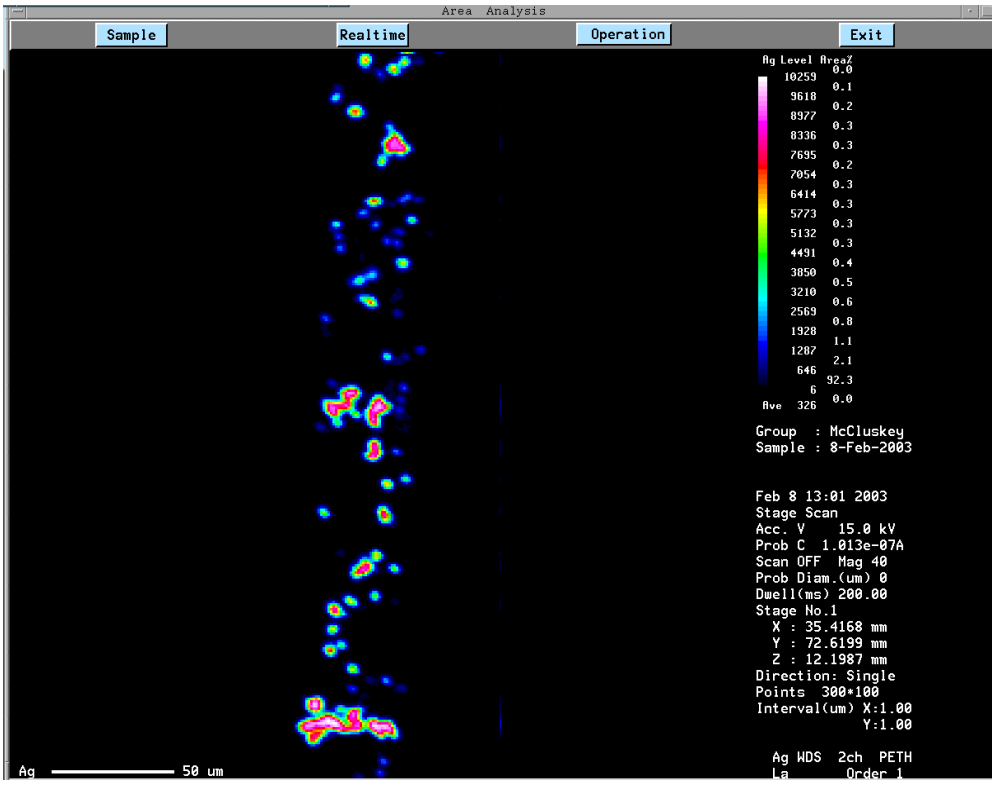


Figure 5. 1 WDX mapping of silver in the SnAgCu die attach

Table 5. 1 wt% of Ag in the die attach due to dissolution of Ag from die finish

Thickness	12µm	24µm	42µm	68µm
Ag wt% increase	2.83%	1.44%	0.83%	0.51%

Density is 10490kg/m^3 for Ag and 7500 Kg/m^3 for SnAgCu

The dissolution of silver from the die finishes increases the concentration of Ag_3Sn in the die attach. Since the amount of Ag from the finish is fixed and Ag from die finishes is completely dissolved into the die attach, the resulting Ag_3Sn concentration due to the dissolution is smaller for the thicker die attach. (Table 5. 1) There is a increase of 0.99wt% in Ag for 35µm-thick SnAgCu die attach and 0.46wt% for 75µm-thick die attach. This increase is considerable comparing to the original 3.5 wt% Ag in the solder and should not be neglected.

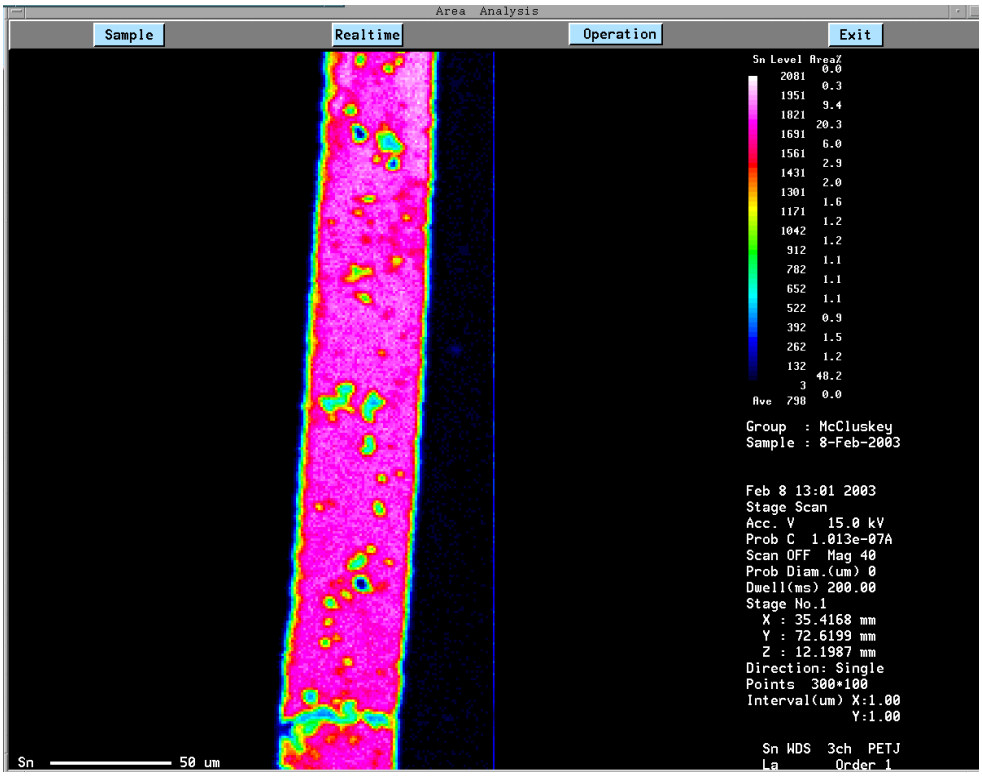


Figure 5. 2 WDX mapping of Sn in the same location as Ag mapping

5.2.2 Morphology of Ag_3Sn intermetallics

The size of Ag_3Sn in SnAgCu die attach varies from tens of microns to sub-microns.

At first, the appearance of Ag_3Sn with sizes larger than several microns is investigated for samples with various nominal thicknesses.

For die attach with thickness of 20 μm, Ag_3Sn particles with sizes normally less than several micrometers are distributed around interfaces.and occupy a large portion of the thickness.(See Figure 5. 3) Those are mostly in the shape of needles (shown in Figure 5. 4), perpendicular to the interfaces.

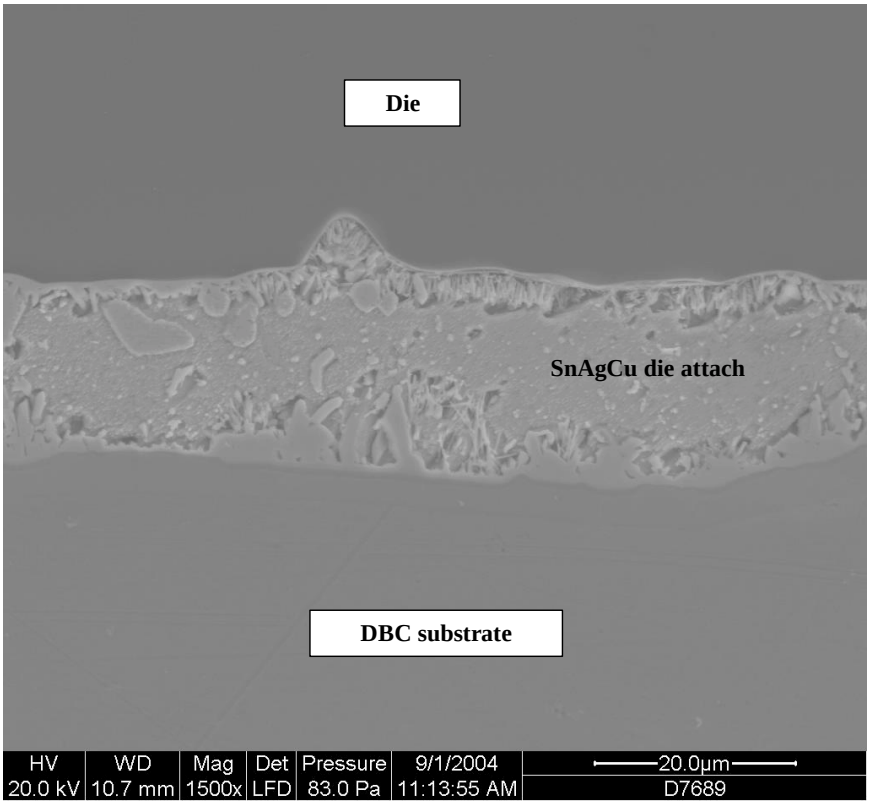


Figure 5. 3 SEM image of die attach with die attach thickness around 20 μm (Sample has been etched with HCL vapor)

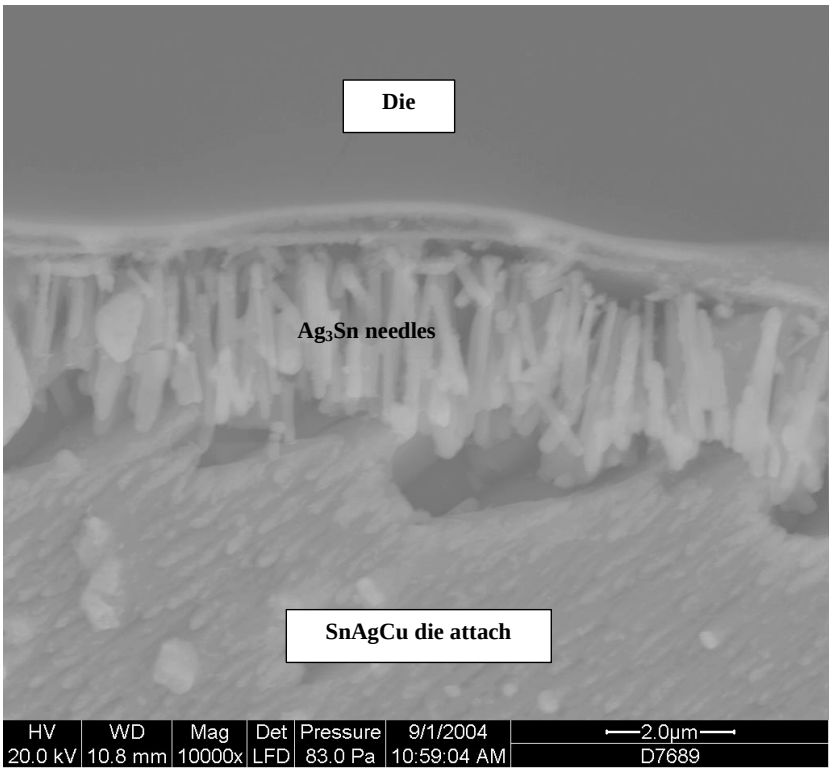


Figure 5. 4 SEM images of Ag_3Sn needles located at die/die attach interface with die attach thickness around 20 µm (sample has been etched with HCL vapor)

For the samples with die attach thickness around 40μm(Figure 5. 5), Needlelike Ag_3Sn is rarely detected. Ag_3Sn particles in the shape of blocks with sizes around 10μm are detected.

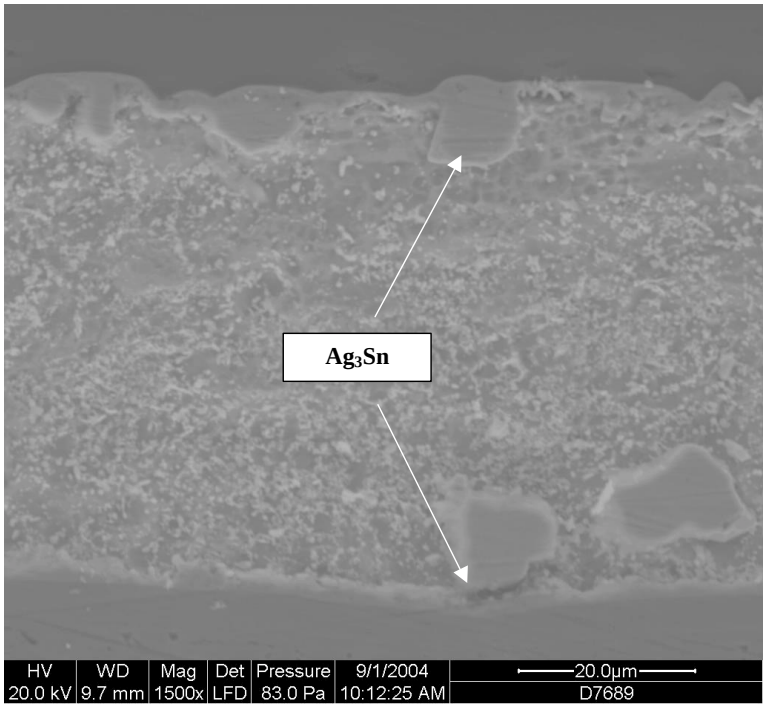


Figure 5. 5 SEM image of Ag_3Sn precipitates at interfaces for die attach with thickness around 40 μm (sample has been etched with 93 vol% CH_3OH, 5 vol% HCL, 2 vol% HNO_3)

For the samples with die attach thickness more than 60μm, Ag_3Sn are detected in the shape of blocks (Figure 5. 6) with sizes around 10μm. Large Ag_3Sn needles (Figure 5. 7) with length higher than 40μm have also been detected in those samples.

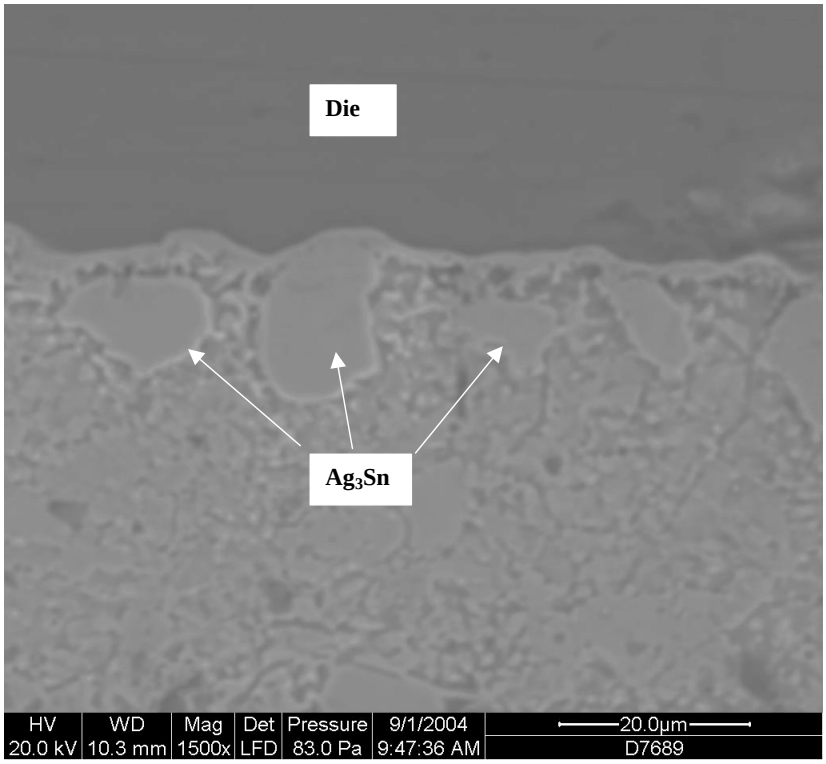


Figure 5. 6 SEM image of SnAgCu die attach with large Ag_3Sn near the die/die attach interface

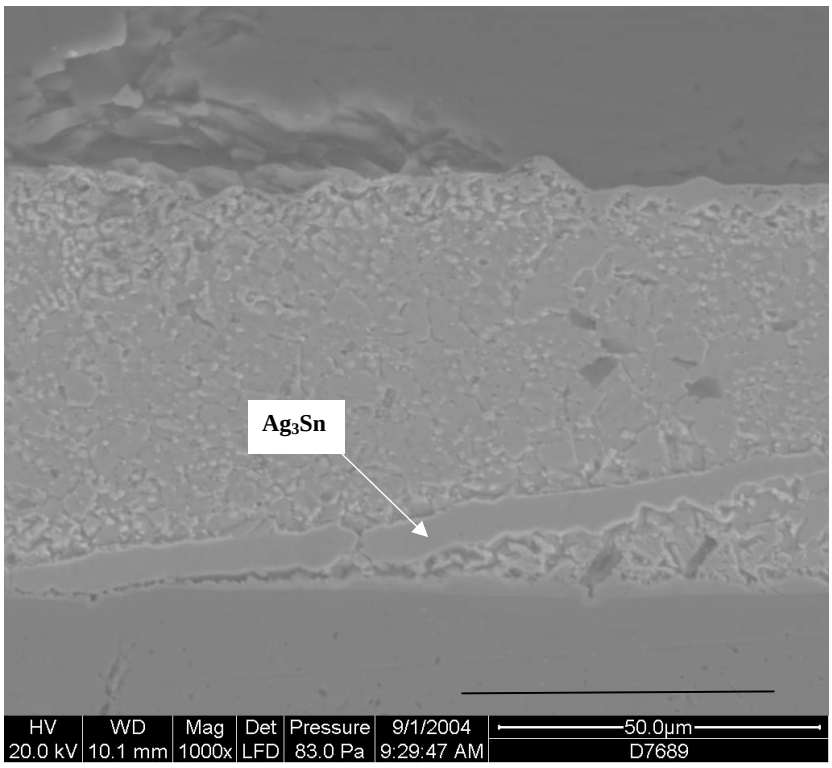


Figure 5. 7 SEM image of large Ag_3Sn needles in the die attach with nominal thickness of 80 micron (sample has been etched with 93 vol% CH_3OH, 5 vol% HCL, 2 vol% HNO_3)

5.2.3 Interfacial intermetallics

At both die/die attach and die attach/DBC substrate interface, Ni-Sn is formed. At die/die attach interfaces, Ag finish dissolved into die attach and exposed Ni in the die finish to form a thin layer of Ni-Sn intermetallics.(Figure 5. 8)

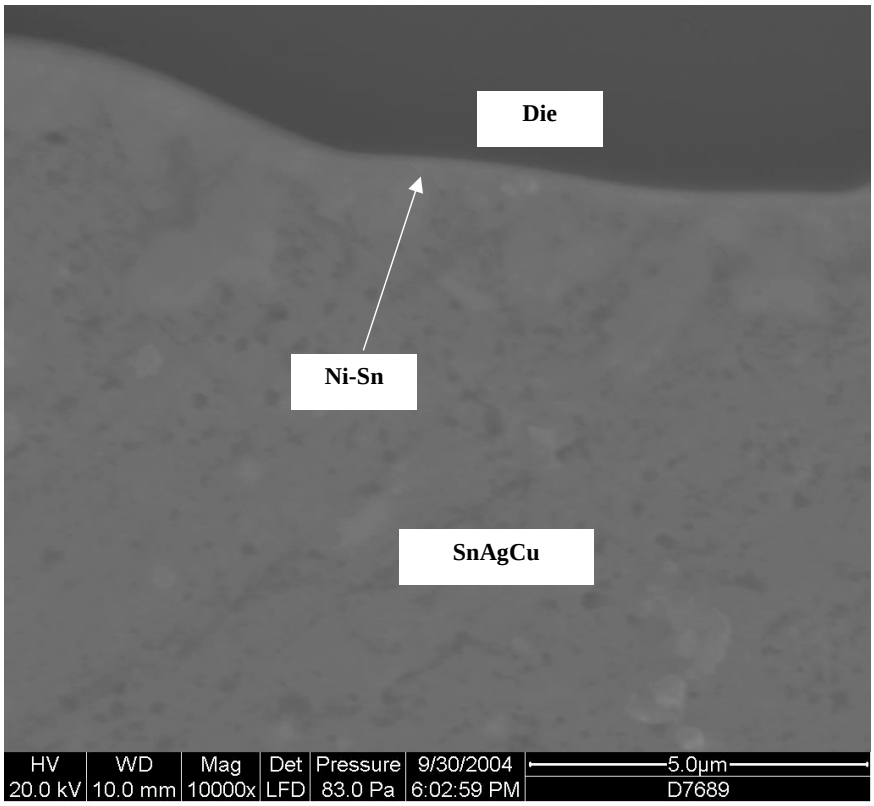


Figure 5. 8 ESEM image of SnAgCu die attach at die side

The results show that although thicker die attach has a lower concentration of Ag_3Sn due to the dissolution, the thicker die attach has more tendency to form larger Ag_3Sn precipitates. Those large precipitates could affect the thermo-mechanical properties of the die attach in three aspects: First, it decreases the concentration of small and fine Ag_3Sn precipitates, that serve to strengthen the solder die attach, making the die attach less uniform and more likely to fail; Second, it may provide a preferential path for die attach

cracking, thus decreasing the reliability of die attach; Third, those brittle Ag_3Sn may introduce brittle failure in the die attach.

5.3 Effect of die tilt on die attach side cracking

In this section, metallurgical analysis is performed on the die attach in order to understand the mechanisms that cause cracking at the thick side. The differences in the microstructure between thin side and thick side of the die attach under tilted conditions is investigated.

First, die attach with cracking at the thick side is analyzed. At the thick end, normally there is one major crack propagation path around the middle of the die attach (Figure 5. 9)(See more results in Appendix D). Large Ag_3Sn appears at the thick side, either around

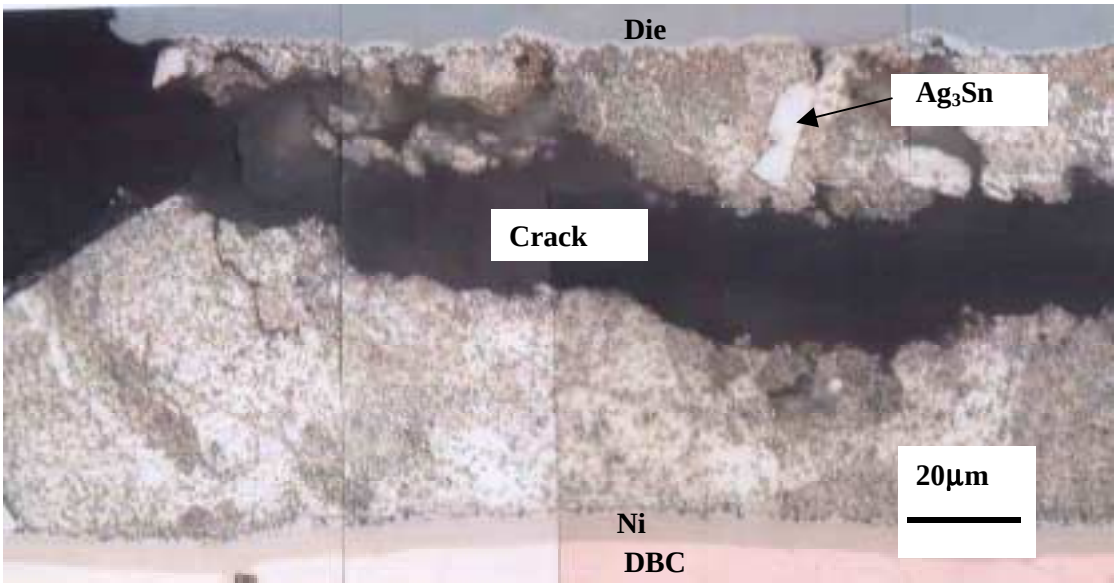


Figure 5. 9 Optical image of SnAgCu die attach cracking at the thick side

the crack or away from the crack (Figure 5. 9). So those large precipitates do not determine the crack path. Nor are there the cracks across the Ag_3Sn precipitates,

excluding the possibility of intermetallic brittle failure. Instead, the cracking seems to be contained to the tin matrix around the middle.

At the thin side, Ag_3Sn (shown in Figure 5. 10) have also been detected with sizes less than a few microns.

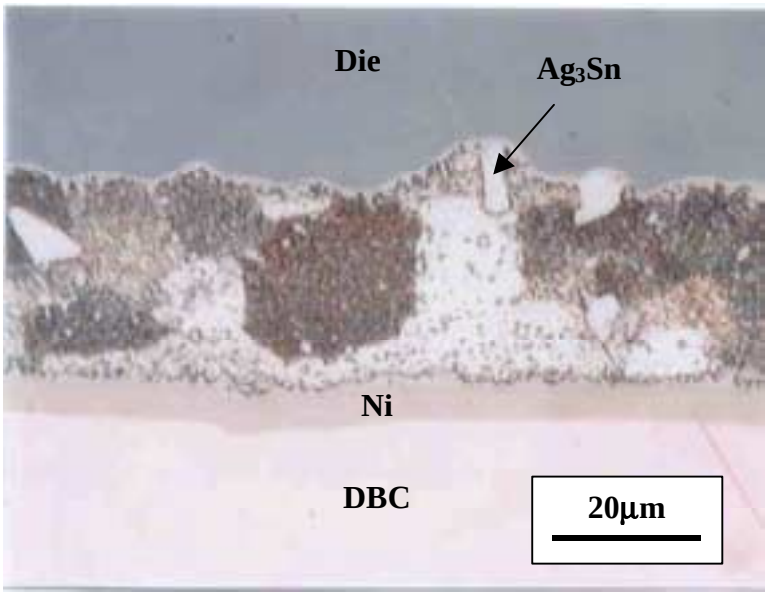


Figure 5. 10 Optical image of SnAgCu die attach at the thin side after etching

The difference in the distribution of Ag between the thick and thin side is investigated through EDX mapping. Here, one sample with similar extent of tilt (33μm at thin side and 58μm at the thick side) is analyzed. This sample didn't exhibit not die attach cracking, so the effect of the crack on the mapping results is avoided.

EDX mapping is then performed on two areas (20μmx20μm) near the thick ends and two areas near the thin ends (20μmx20μm) in the middle of the die attach. Those areas are randomly chosen with only small Ag_3Sn. (Areas with presence of large Ag_3Sn are not adopted.)

Table 5. 2 Results of EDX mapping between thin and thick ends for the tilted sample

	Thick end (58μm)		Thin end (33μm)	
	Thick area 1	Thick area 2	Thin area 1	Thin area 2
Measured Ag (wt%)	2.08	2.04	2.50	2.47
Measured Sn (wt%)	64.40	64.78	61.49	62.09
Adjusted Ag (wt%)*	3.07	2.99	3.86	3.78
Adjusted avg. Ag (wt%)	3.03		3.82	
Theoretical. Ag (wt%)	4.08		4.53	

* Adjusted Ag wt% is calculated based the on the assumption that Sn wt% is 95%. This is because during EDX mapping, other elements such as O, Si have also been included.

Although the results show that the value of Ag wt% is smaller than theoretical value. It is because of the following reasons:

1. Medium and large Ag_3Sn is not included.
2. Measurement errors

The result (shown in Table 5. 2) confirmed that thinner side does have a higher concentration of dissolved Ag and small Ag_3Sn particles. This makes the thin side stronger than the thick side.

5.4 Discussions & Conclusions

This chapter has investigated the microstructure of SnAgCu die attach, which is largely determined by the soldering process, with little influence from the subsequent power cycling.

First, microstructures at various die attach thickness from 20 μm to 80 μm were examined. The study has found that microstructure changes with thickness, especially the size and distribution of Ag_3Sn intermetallics. It is related to the dissolution of Ag from the die finishes. Ag from the die finishes plays an important role in forming Ag_3Sn intermetallics in the bulk. This has been proven by the study of microstructure of Sn3.8Ag0.7Cu on various PCB finishes (including immersion Ag finish). (Detailed in Chapter 2) Since the thickness of Ag finishes is fixed, for the samples (20 μm ~ 80 μm) that have Ag completely dissolved into the bulk, the thinner die attach is expected to have a higher concentration of Ag_3Sn. At the same time, this study has confirmed that the thicker the die attach, the larger the Ag_3Sn appears.

Microstructural causes for the die attach cracking at the thick side are then investigated. The large Ag_3Sn precipitates don't initiate the cracking, instead they decrease the percentage of small precipitates and lower the strength of Sn phases. Therefore, the thinner die attach will have smaller and higher percentage of Ag_3Sn precipitate distributed in the bulk.

EDX mapping on the tilt sample (58μm on the thick side and 33μm on the thin side) have further confirmed that a higher percentage of small Ag_3Sn intermetallics exists at the thin side of the joint. The presence of small Ag_3Sn strengthen the die attach. Kang[124] has found that a lower hardness for SnAgCu solder is generally related to a lower Ag content (Ag varies from 2.1 wt% to 3.8 wt%). Since for the same type of materials, higher hardness leads to higher yield strength, a higher Ag content in SnAgCu solders is

expected to have higher yield strength. As a result, die attach at the thin side is stronger than the thick side under tilt conditions. It is a critical factor that resulted in the die attach cracks at the thick side (>60μm) instead of the thin side (<45μm) even thought the thin side is under nominally high thermo-mechanical stress.

Another important mechanism that causes thinner die attach to be more resistant to the fatigue failure than thicker die attach is likely related to the cooling rate during solidification. During soldering, the cooling of the die attach occurs from both the die/die attach and die attach/substrate interfaces to the middle. Thus, under the same soldering profile, the actual average cooling rate is higher for thinner die attach, especially for die attach that is just tens of microns thick. As a result, a more uniform distribution of Ag_3Sn appears in the thinner die attach, leading to stronger die attach. Certainly, this difference is going to be negligible as the die attach becomes thicker, as is the effect due to Ag finishes dissolution.

Under the same loading conditions, the thermo-mechanical stress under power cycling increases with thickness, therefore, thicker die attach is normally expected to have a longer fatigue life. However, as thickness decreases to less than 60 μm for SnAgCu die attach, dissolution of Ag surface finishes as well as cooling rate difference have an important effect to the microstructure of the die attach, resulting in fatigue strength of the die attach increasing with decreasing thickness. Therefore, it is possible that thinner die attach is more resistant to fatigue failure even under higher thermo-mechanical stress (Figure 5. 11).

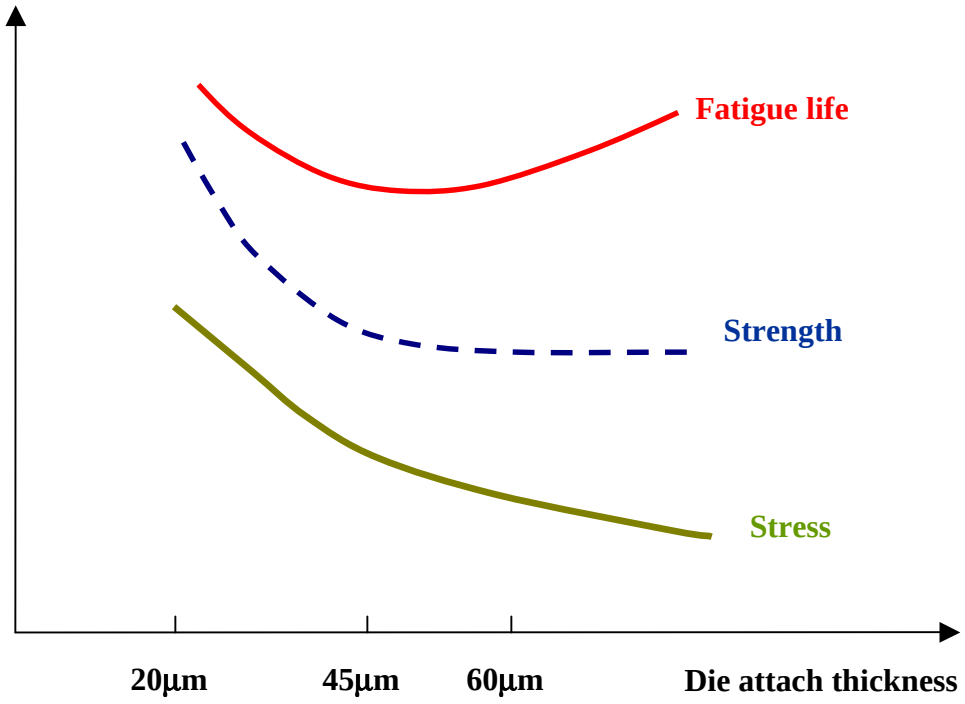


Figure 5. 11 The relationship between thermo-mechanical stress, fatigue strength and the resultant fatigue life for various thickness for SnAgCu die attach (Trend line of the fatigue life is indicated by experiments, trend line for stress is estimated by thermo-mechanical simulations, and trend line for strength is speculated based on microstructure characterization)

Chapter 6 Summary, Contributions and Suggestions for Future Work

6.1 Summary of results

The first part of the study investigated the effect of PCB surface finishes (OSP, ImAg, ImSn, ENIG and HASL) and high temperature aging ($0.8T_m$~$0.9T_m$) on the intermetallic growth and shear strength of Sn3.8Ag0.7Cu solder joints. Intermetallic growth at the interfaces and in the bulk with temperature aging has been characterized. Shear testing has also been performed to evaluate the influence of temperature aging and surface finishes on the shear strength and the failure modes. The study has determined that intermetallic won't cause interfacial failure when SnAgCu solder joints are soldered on lead-free finishes (ImAg, ImSn, ENIG, and OSP) even after long-term high temperature aging. Neither does the dissolution of Ag or Cu have a obvious influence to the shear strength of the Sn3.8Ag0.7 solder joint due to its limited availability compared to the large volume of the joint (700μm). However, interfacial weakening could happen after high temperature aging when HASL (PbSn) finish is used.

The second part is the main part of the thesis, which focused on the power cycling reliability of Sn3.5Ag0.8Cu die attach in actual power MOSFET devices. Extensive power cycling testing, failure analysis, microstructure characterization, and thermo-mechanical analysis are conducted. Power cycling has been performed at various power levels and different die attach thicknesses. Failure is detected by monitoring the increase in the thermal impedance. Failure analysis and microstructure characterization are performed to determine the failure mechanisms and important factors influencing the die

attach cracking. The effect of thickness on the microstructure of SnAgCu die attach, especially intermetallics, has been investigated.

At the same time, transient thermal analysis using ANSYS was performed to obtain the temperature profile of the power module under the power cycling. Transient thermal analysis has also helped to determine the time to measure the thermal impedance during experiments to differentiate die attach cracking and thermal impedance degradation. Thermal transient analysis has also correlated the extent of die attach cracking with the increase in the thermal impedance. Finally, 2D plain strain analysis was performed to evaluate the Von-Mises and shear stress/strain distribution in the die attach, especially the difference between thick and thin side of the die attach under die tilt conditions. Effect of hydrostatic stress was also investigated. The study has determined that under the same power cycling loading conditions, the thermo-mechanical stress under power cycling increases with decreasing die attach thickness and thinner die attach is expected to fail earlier than thicker ones. However, as the thickness decrease to around 60 μm for SnAgCu die attach, dissolution of Ag surface finishes as well as cooling rate difference have an important effect to the microstructure of the die attach, resulting in a higher fatigue strength for thinner die attach. Therefore, thinner die attach is more resistant to fatigue failure even under higher thermo-mechanical stress.

6.2 Contributions of the dissertation

1. Under the same power cycling conditions, a thinner die attach will experience higher thermo-mechanical stress. Therefore, thinner die attach generally leads to a

shorter fatigue life. However, the study have found that a thinner die attach (thickness around 20~45 μm) is more resistant to fatigue failure than thick ones (thickness higher than 60 μm) and leads to a longer fatigue life even under lower stresses.

2. It has been long been suspected that for die attach used in power semiconductor packages, interfaces will have an important effect on the thermo-mechanical behavior of the die attach since its thickness is less than 100μm[4][20]. The study has confirmed that the concentration of Ag in the SnAgCu die attach increases with thinner die attach due to dissolution of Ag finishes. At the same time, a thinner die attach is likely to have a faster average cooling rate. Therefore, thinner die attaches have a higher and more uniform intermetallic distribution, resulting in a higher fatigue strength.

3. This is the first study to confirm the important effect of Ag finishes on the microstructure and thermo-mechanical properties of SnAgCu die attach. Since the original content of Ag in the Sn3.5Ag0.7Cu is small (3.5wt %), the effect of dissolution of Ag finishes (0.25μm) is significant to the microstructure of SnAgCu die attaches (for example, 1.46 wt% increase for a 20 μm Sn3.5Ag0.8Cu die attach).

4. The thesis proposed a method to determine the time to measure the thermal impedance that could differentiate die attach cracking with thermal grease

degradation based on the 3D thermal transient analysis. There have been other methods[112] generally based on a RC network to determine the time, which is usually a 1D simplification on the power modules. The method proposed here is based on a 3D thermal transient analysis and is thus more accurate.

5. The thesis proposed a method to correlate die attach crack propagation to the increase in the thermal impedance based on the 3D thermal transient analysis. The increase in the thermal impedance further leads to the drop in the forward voltage (or increase in the electrical resistance between source and drain) for power MOSFETs. This makes it possible to determine the crack propagation behavior during power cycling experiments, where forward voltage drop (or increase in the electrical resistance) is usually used to monitor the die attach cracking indirectly.

6. The thesis systematically studied the influence of various lead-free surface finishes (ENIG, ImSn, ImAg, OSP) on the microstructure as well as the shear strength of the Sn3.8Ag0.7Cu balls (diameter around 700μm). For those large solder balls, dissolution of Ag (from Ag fishes) and Cu (non-Ni finishes) does not have an obvious influence on the shear strength, nor will the interfacial intermetallic formation cause intermetallic failure even after high temperature aging.

6.3 Suggestions for future work

- A thermo-mechanical fatigue model that incorporates the effect of thickness, especially as thickness decreases to tens of microns.
- More parametric power cycling (size of the die, different dwelling time and frequency) tests should be conducted.
- More experiments should be performed to differentiate the effect of different microstructure features. For example, a comparison study should be performed on the same power module without Ag die finishes to separate the effect due to dissolution of silver finishes from other thickness effects.
- Further studies on thermal grease degradation and wire-bonds lift off are necessary to better evaluate the reliability of power modules.

Appendix A Shear strength results

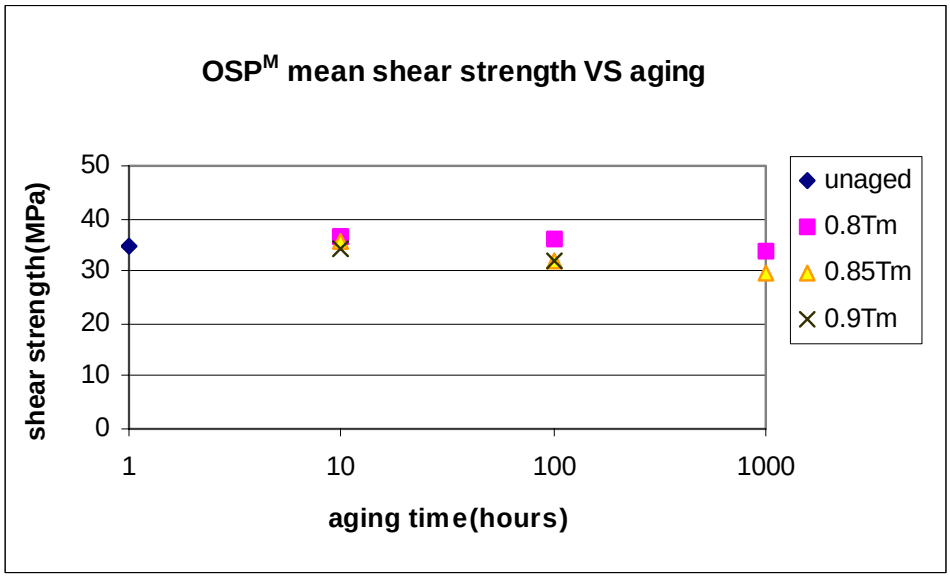


Figure A. 1 Mean shear strength of Sn3.8Ag0.7Cu solder on OSP^M surface finishes under high temperature aging.

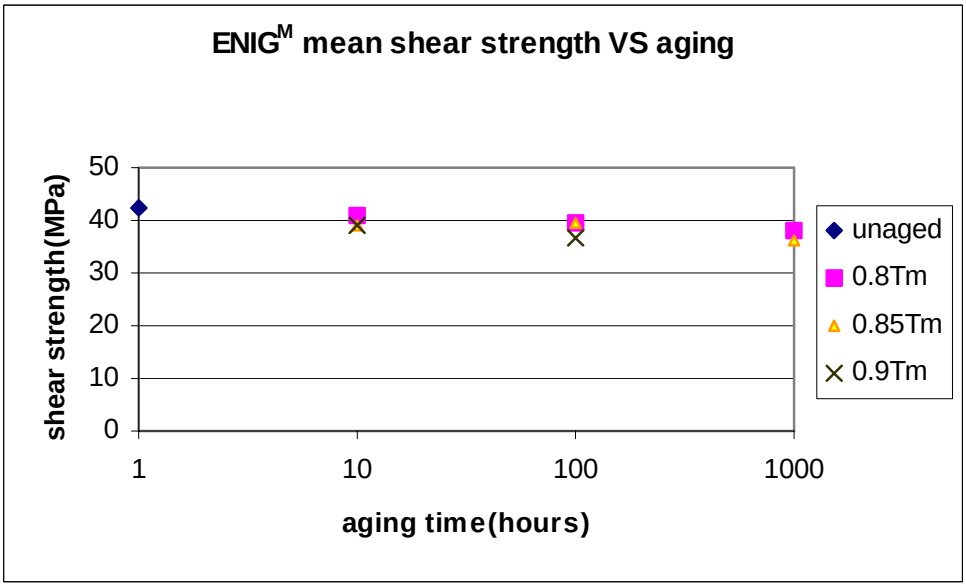


Figure A. 2 Mean shear strength of Sn3.8Ag0.7Cu solder on ENIG^M surface finishes under high temperature aging.

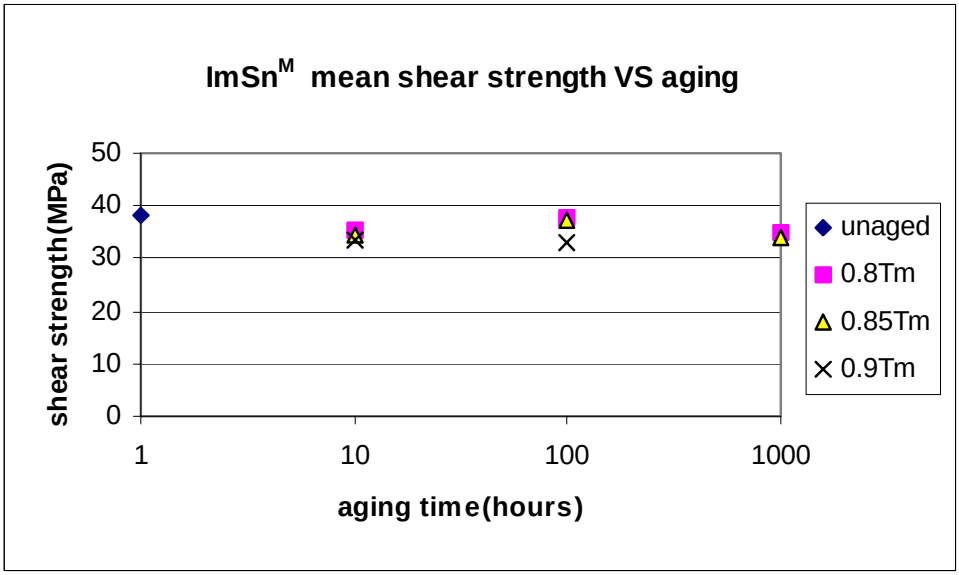


Figure A. 3 Mean shear strength of Sn3.8Ag0.7Cu solder on ImSn^{M} surface finishes under high temperature aging.

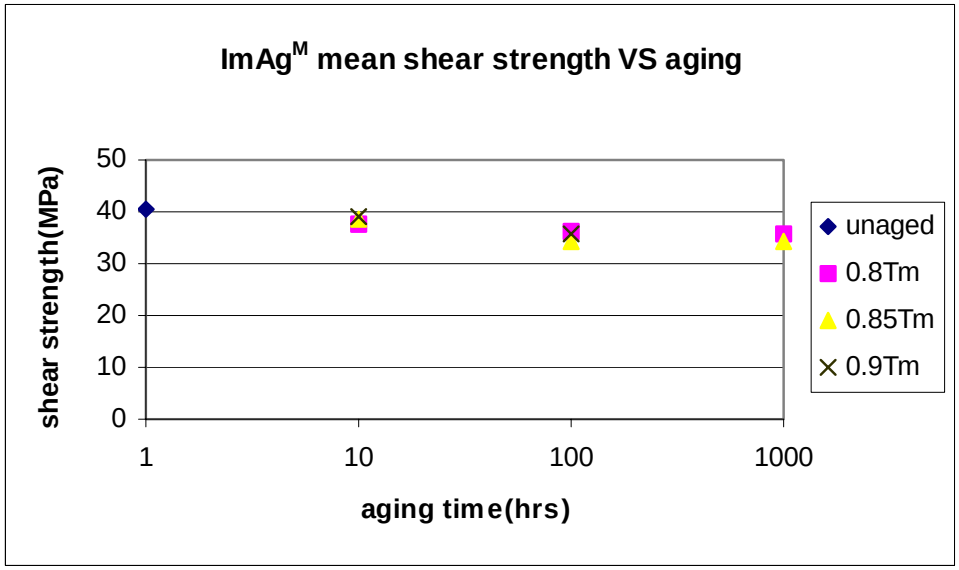


Figure A. 4 Mean shear strength of Sn3.8Ag0.7Cu solder on ImAg^{M} surface finishes under high temperature aging.

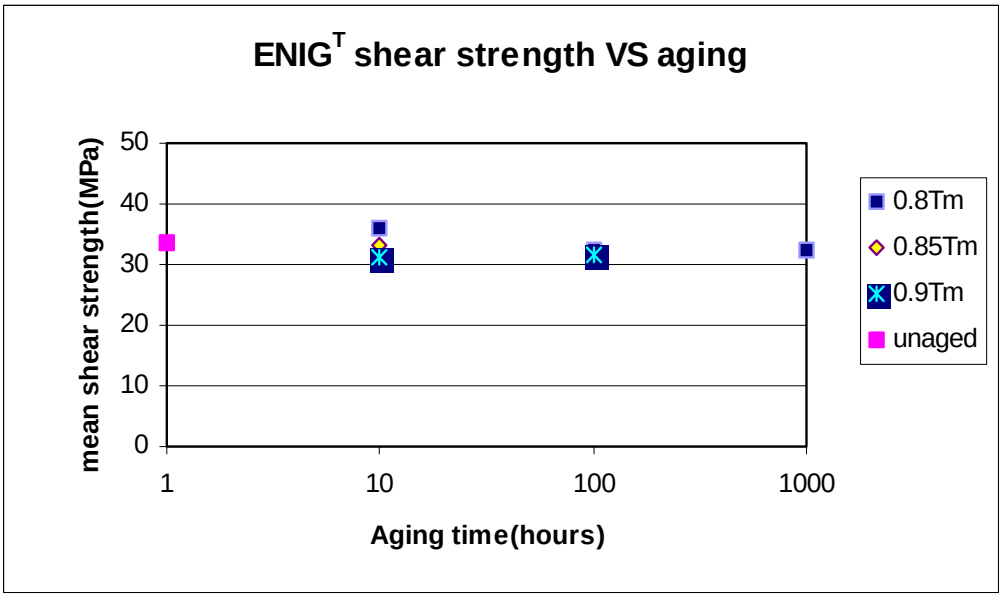


Figure A. 6 Mean shear strength of Sn3.8Ag0.7Cu solder on ENIG^T surface finishes under high temperature aging.

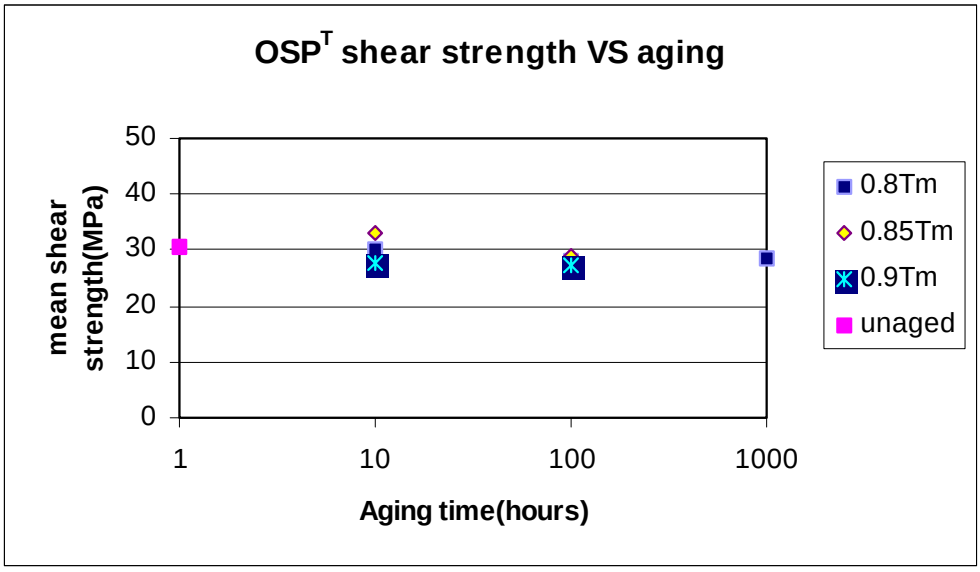


Figure A. 5 Mean shear strength of Sn3.8Ag0.7Cu solder on OSP^T surface finishes under high temperature aging.

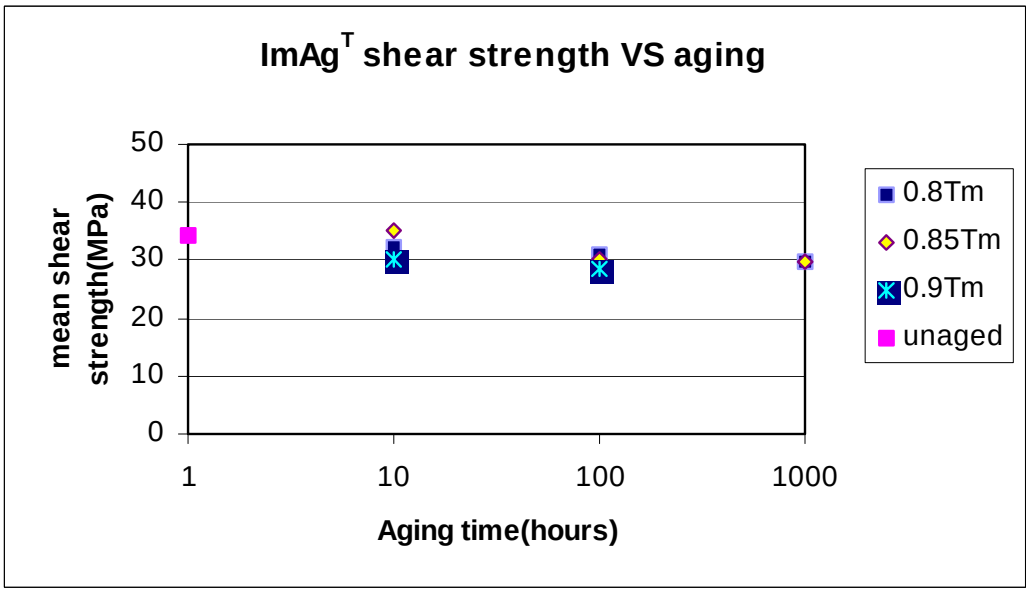


Figure A. 8 Mean shear strength of Sn3.8Ag0.7Cu solder on ImAg^{T} surface finishes under high temperature aging.

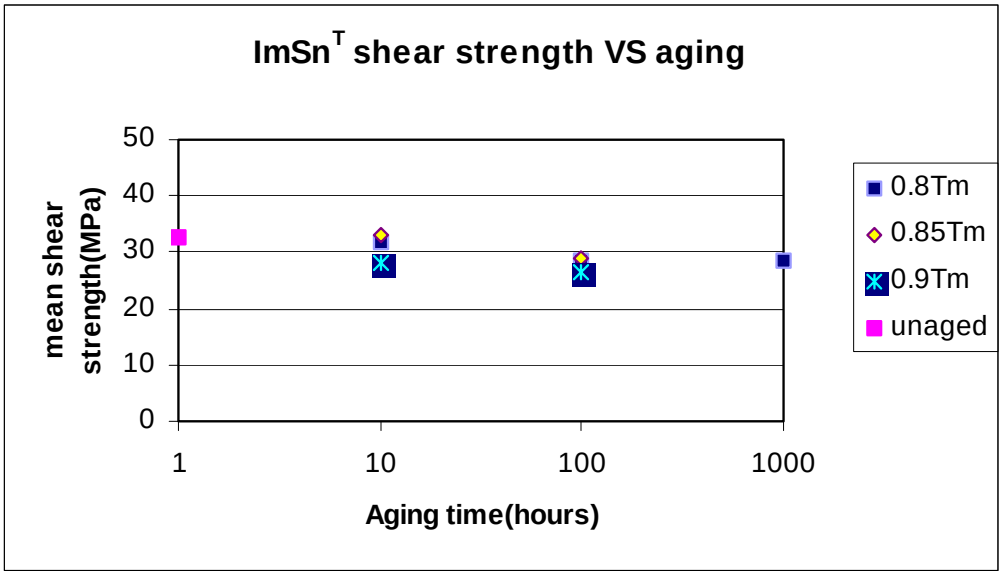


Figure A. 7 Mean shear strength of Sn3.8Ag0.7Cu solder on ImSn^{T} surface finishes under high temperature aging.

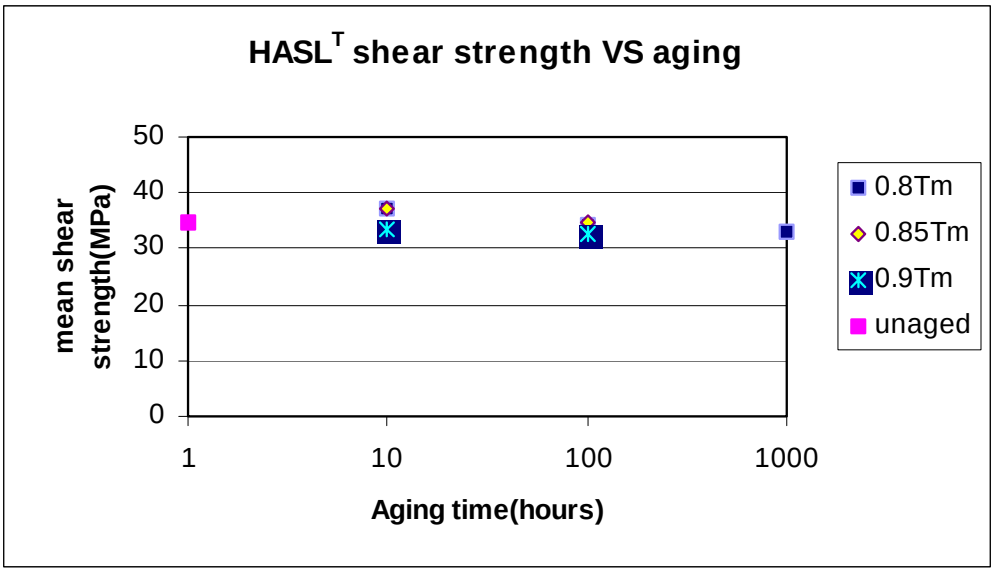


Figure A. 9 Mean shear strength of Sn3.8Ag0.7Cu solder on ImSn^T surface finishes under high temperature aging.

Appendix B Thermal impedance method

Transient thermal behavior of power modules

When a power device is in operation, heat is generated within its junction. The rate of the heat generation depends on the power. Heat is transmitted from the junction to die attach, substrate, heat sink and finally to the ambient. The junction temperature (T_j) will rise until the equilibrium is reached when the rate of the heat generated is equal to the rate of heat dissipated. Transient thermal behavior of a power module can be characterized by thermal impedance. It determines how fast and how high T_j rises.

In analogy to an electrical circuit, thermal impedance can be calculated by temperature difference between the chip and bottom of the heat sink divided by the dissipation power during power cycling

$$Z_{jc}(t) = \frac{\left(T_j(t) - T_{base}\right)}{P}$$

where $T_j(t)$ is the transient junction temperature and T_c is the bottom temperature of the heat sink and could be treated as constant in this study. Thermal impedance is usually determined by measuring junction temperature $T_j(t)$.

Introduction to thermal impedance tester

Both IR camera and thermo-couple can be used to measure temperature. However, neither IR camera nor thermocouple is used to measure the junction temperature of the power module due to the following reasons:

IR camera is used to determine the temperature distribution of an exposed surface by measuring the infrared energy emitted from the surface and the response is fast. The emissivity(μ) of the surface should be available to determine the temperature. So the surface is painted usually black ink (μ≈1) to get the accurate measurements. However, the top surfaces of the devices are usually encapsulated with silicon gel and IR camera could not be used.

Thermocouple is created based on the principle that whenever two dissimilar metals touch and the contact point produces a small open-circuit voltage as a function of temperature. This thermoelectric voltage is known as the Seebeck voltage. Within the application temperature range specified by the manufacturer, the voltage is approximately linear with respect to temperature. So temperature is determined once thermal couple is directly attached to the object and the Seebeck voltage is measured. However, this method is not appropriate to measure the junction temperature: first, it will introduce additional thermal conduct path by attaching to the die surface and obviously change the junction temperature, considering the small heat capacity of the die; Second, its response to the temperature is not fast. Thermocouple is more feasible to measure the temperature of big bulk material.

For power MOSFET, junction temperature T_j can be determined by measuring forward voltage drop. It is based on the principle that forward voltage drop of the device has a linear relationship with junction temperature. The temperature obtained is the average junction temperature. This method is quick and can be used to measure the junction

temperature of encapsulated devices. In the experiment, a thermal impedance tester based on this principle is used to measure the junction temperature at different time.

Both IR camera and thermocouple are also used in the experiments. IR camera is used to measure the junction temperature of without silicon gel and helps to determine the relationship between junction temperature and forward voltage drop of the thermal impedance tester. It has been used in the experiments to measure the temperature of the heat sink, which has a large heat capacity.[109]

Procedure

For power MOSFETs, forward voltage drop(ΔV) decreases linearly with the junction temperature(T_j).

$$\Delta V = KT_j$$

Determining this ratio (K) is necessary to get the absolute value of thermal impedance. In the study, K is determined by measuring forward voltage drop at two different defined temperatures. The temperatures are reached by a controlled heat sink

After power cycling load is suspended, thermal impedance tester is connected to power modules. A constant test power (70w) is applied for a well-defined heat dissipation period. At the same time, a small current (I1) will be applied just before and after the test power is applied and corresponding forward voltage (V1, V2) are measured. So forward voltage drop is determined.

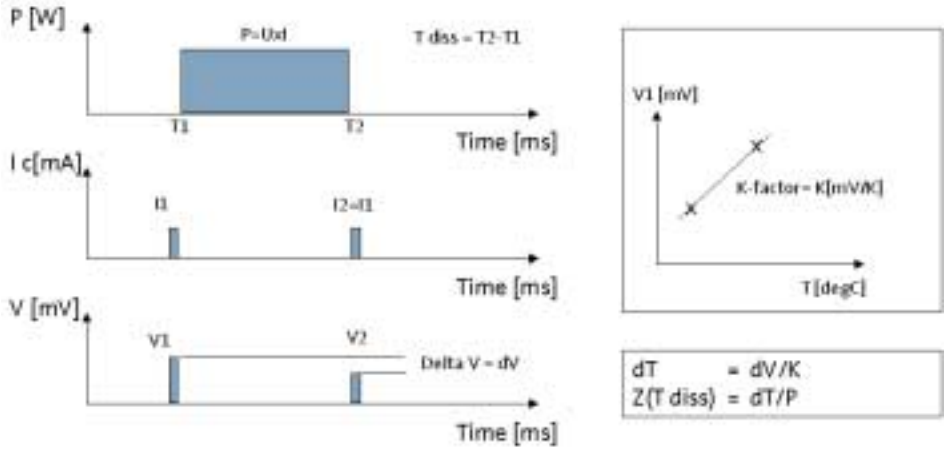


Figure B. 1 Operational principle of thermal impedance tester

Verification

In order to make sure the junction temperature measured by Thermal impedance thermal tester is accurate, one sample from each group under test is chosen. Gel is removed and the die surface is covered by black ink. Then the peak junction temperature is measured using IR camera. The figure below shows the comparison between peak junction temperature measured by IR camera and average junction temperature measured by Thermal impedance tester. The peak junction temperature by IR camera is about 10% higher than average junction temperature by thermal impedance tester, which is verified by simulation.(Figure B. 2) [110][111]

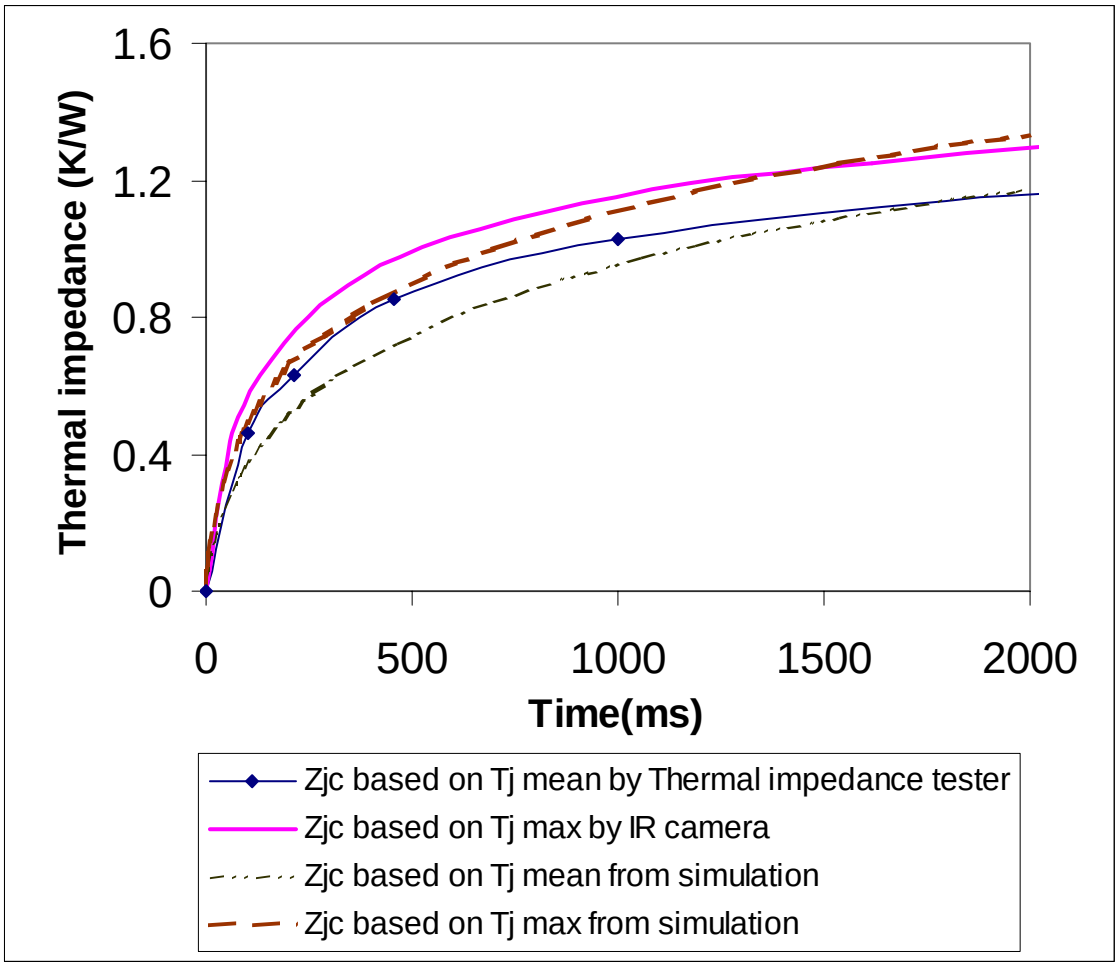


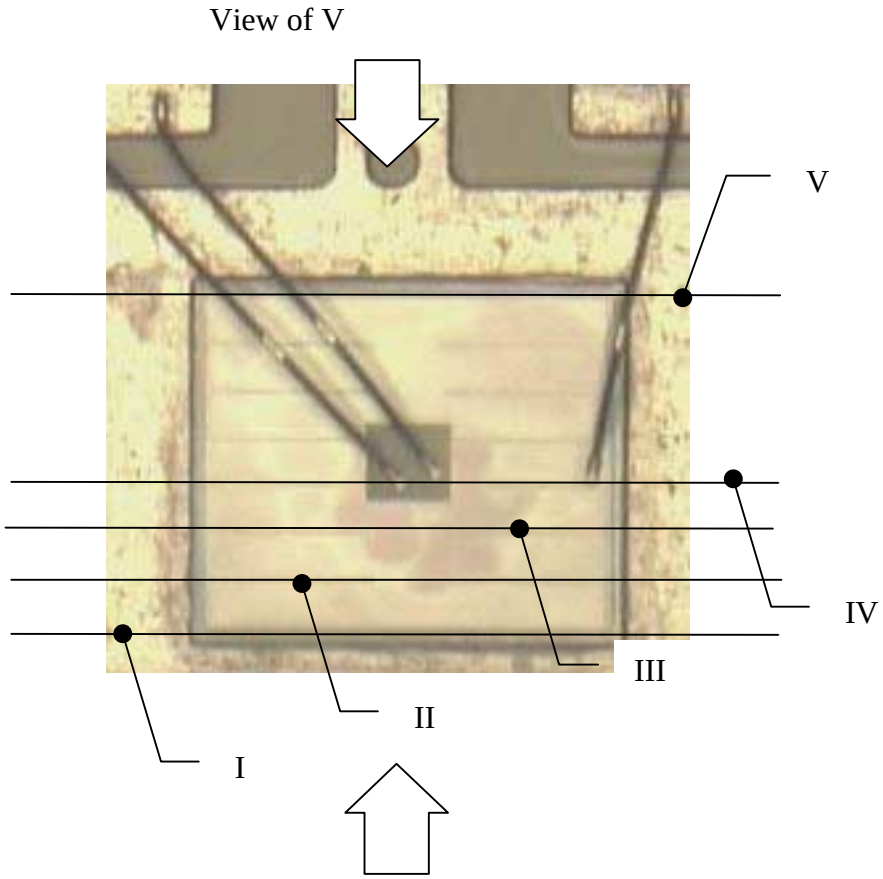
Figure B. 2 Comparison of thermal impedance between simulation and experimental results

Appendix C Thermal impedance results

Table B. 1 Thermal impedance measured during power cycling experiments

Sample #	Group#	Zjc at 80ms		Zjc at 2s	
		Initial(K/W)	Final(K/W)	Initial(K/W)	Final(K/W)
21	(30w,40μm)	0.40	0.40	0.82	0.89
22	(30w,40μm)	0.39	0.41	1.06	1.10
41	(30w,40μm)	0.39	0.40	1.07	1.10
42	(30w,40μm)	0.40	0.41	0.87	0.95
66	(30w,40μm)	0.40	0.42	0.94	1.05
23	(50w,40μm)	0.40	0.41	0.91	1.02
24	(50w,40μm)	0.40	0.41	0.84	0.92
43	(50w,40μm)	0.40	0.40	0.82	0.90
44	(50w,40μm)	0.39	0.41	0.91	1.05
67	(50w,40μm)	0.41	0.42	0.96	1.06
25	(70w,40μm)	0.39	0.66	1.10	2.07
26	(70w,40μm)	0.39	0.44	1.05	1.17
45	(70w,40μm)	0.40	0.54	1.13	1.60
46	(70w,40μm)	0.38	0.42	0.96	1.07
69	(70w,40μm)	0.41	0.52	1.17	1.55
27	(90w,40μm)	0.39	0.52	0.94	1.32
28	(90w,40μm)	0.40	0.45	0.99	1.11
47	(90w,40μm)	0.39	0.45	1.01	1.17
48	(90w,40μm)	0.40	0.50	1.27	1.57
70	(90w,40μm)	0.40	0.41	1.33	
13	(70w,20μm)	0.45	0.46	0.86	0.93
14	(70w,20μm)	0.46	0.45	0.87	0.91
15	(70w,20μm)	0.45	0.45	0.81	0.97
12	(70w,20μm)	0.45	0.46	0.83	0.92
17	(70w,20μm)	0.47	0.48	0.84	0.92
73	(70w,80μm)	0.43	0.43	0.77	0.89
72	(70w,80μm)	0.48	0.46	0.81	0.93
75	(70w,80μm)	0.43	0.44	0.74	0.88
71	(70w,80μm)	0.44	0.45	0.79	0.81
77	(70w,80μm)	0.45	0.46	0.74	0.85

Appendix D Stepped cross-section images

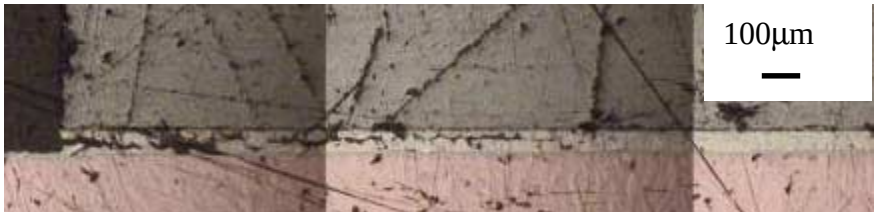


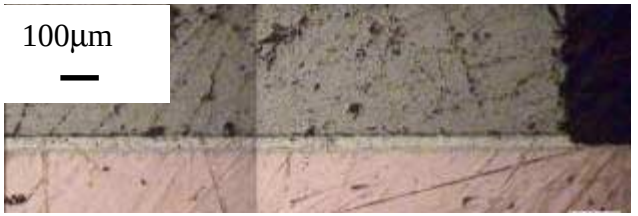
Description of the cross-section plan

Sample 27 (Only two sides are shown due to the paper constraint)

27- I

27- II





27- III

100µm

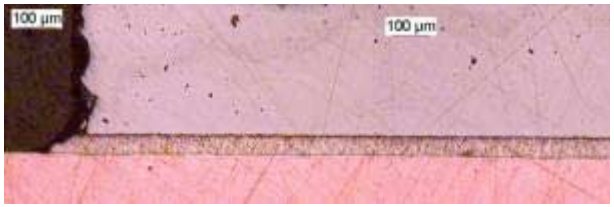
100µm

27- IV

100µm

100µm

27- V



100µm

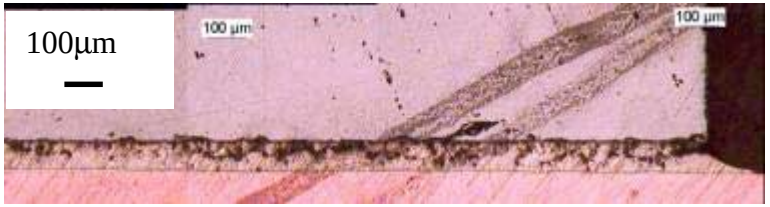


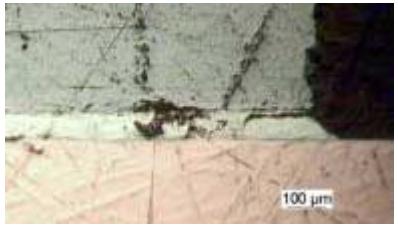
Image of V is from the opposite direction

Sample 28

28- I

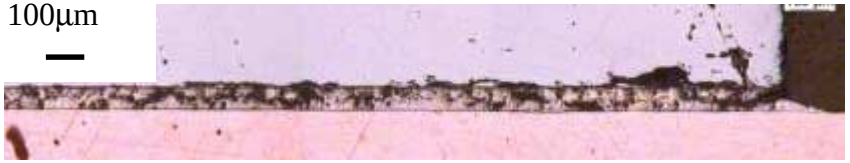
28- II

28- III



28- IV

28- V

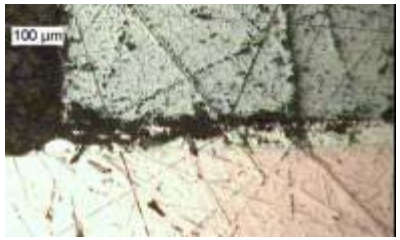


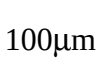
Sample 48

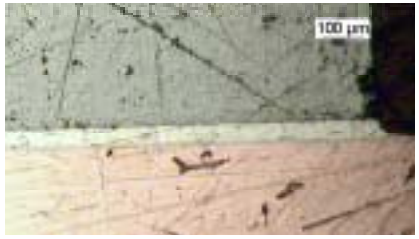
48- I

48- II

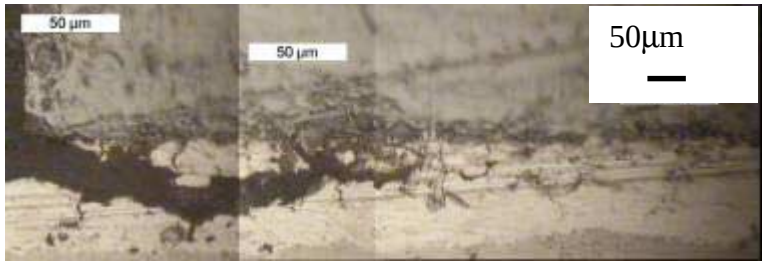
48- III







48- IV



48- V

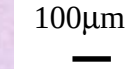


Image of V is from the opposite direction

Sample 69

69- I

69- II

69- III

69- IV

69- V

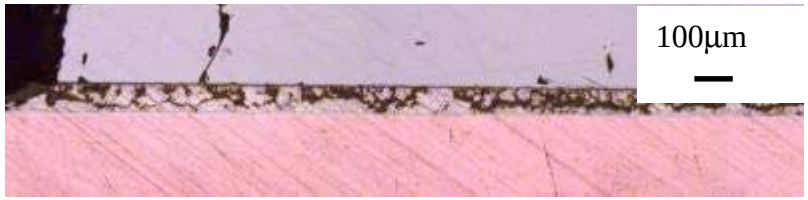


Image of V is from the opposite direction (crack on the die is caused by grinding)

Appendix E Determination of transition region

As power is turned on, there will be propagating delay as heat flow from the device junction toward the base of the heat sink. So both thermal impedance and junction temperature will gradually increase.

Chan Su Yun has investigated the transient thermal response of IGBT as power is applied. [112]In his simulation, at first, it takes 300us(1st transition time) for the silicon devices to be initially heated and no heat be transferred to the other parts of the module. After second transition time (80ms), the heat flux begin to reach the attach layer between DBC and heat sink. So thermal impedance measured between the 1st and the 2nd transition time won't influenced by the thermal grease. The exact value for the transition time varies with different module and usually requires complex thermal analytical impedance calculation based on 1-dimensional model, which neglect the spreading effect in the module that is also an important part of the heat dissipation.

Here, a simple method using ANSYS is proposed to determine the 1st and 2nd transition time by conducting three 3-dimensional thermal transient simulations. The first one is the same as what has been conducted before. It is a complete power module under a constant power of 70w. The only changes that the second case and third case have is that die attach has completely delaminated in the second case and thermal grease has completed delaminated in the third case.

The peak junction temperature is compared for those three cases. (Shown in Figure E. 1) Initially, the temperature follows the same curve. After the first transition time, junction

temperature for the second case (die attach crack) starts to divert and increase dramatically. The first transition happens around 4ms. At this time, the first case and the second case still stay the same. As heat reaches the thermal grease layer, the crack in the grease makes temperature of the third case start to divert from the first case. This happens around 200ms.

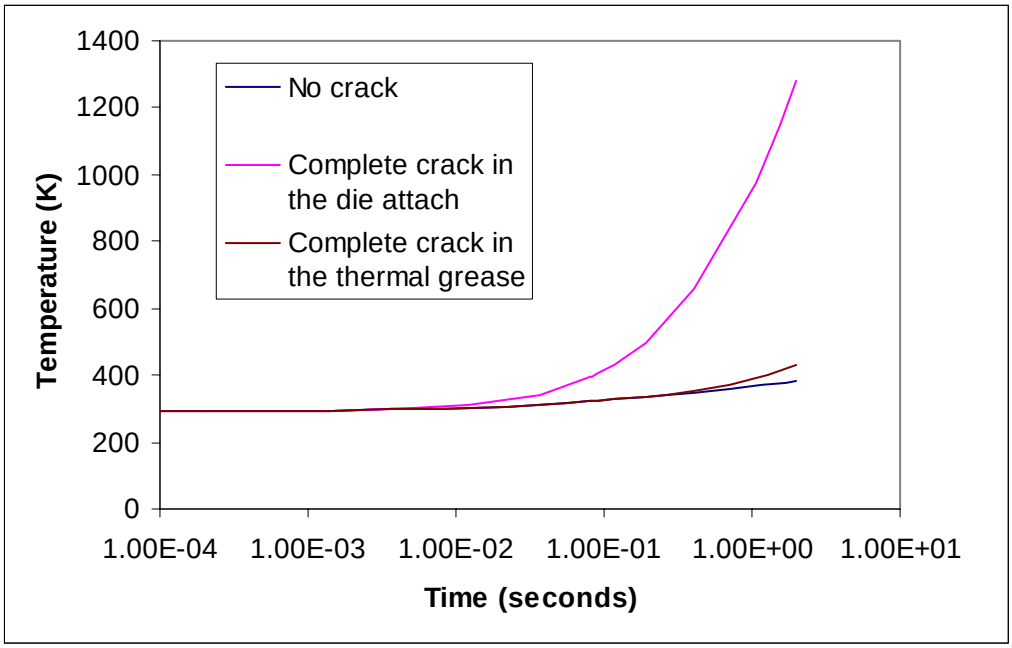


Figure E. 1 Effect of crack location on the transition time

Appendix F ANSYS input files

Input file for thermal transient analysis

```
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% Objective:3D diagonal tranisent state thermal analysis for 2D structural analysis
!% INFO:
!% Date:Sep. 22,2003
!% Place:     CALCE, University of maryland
!%    1.    Tilt is considered here(only two thickness)
!%    3.    Crack estimation needed to change accordingly!!!
!%    6.
!% Author:              Yunqi Zheng
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

/config, nproc,2
!setproc,2

!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% power cycling information
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!power(watt)
power=90
!Base Temp (K)
T_base=293
!cycles applied
Ncycle=3

!power on and off time(second)
t_poweron=2
t_poweroff=2
!time that measure the transient thermal resistance during power on(< t_poweron)
t_measure=0.08

!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% Geometry of the power module
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
! unit: mm
! Thickness:            th_
! Length:               l_
! Width: w_

!%--- Die ---
th_die=0.375
l_die=6.55
w_die=7.70

!%--- solder joint--- thick on the left
th_solmax=0.063
th_solmin=0.044

!% width and length of solder joint are defined as the same as die
!tilt of the die
delta_sol=(th_solmax-th_solmin)
th_sol=(th_solmax+th_solmin)/2.0
*AFUN,DEG
l_sol=l_die
w_sol=sqrt(w_die*w_die-delta_sol*delta_sol)
rot_sol=ASIN((th_solmax-th_solmin)/w_sol)

!% power generation region(assume the region is 5um thick)
th_p=0.040
l_p=5.79
w_p=6.94
d_p=0.015
!the power generation region will be slightly changed for later convenient mesh
area_p=l_p*w_p
l_p=sqrt(area_p*l_sol/w_sol)
w_p=sqrt(area_p*w_sol/l_sol)

!%--- Cu layer under solder joint---
th_Cu1=0.3
l_Cu1=13
w_Cu1=13

!%--- Cu layer above grease---
th_Cu2=0.3
l_Cu2=14
```

```
w_Cu2=16

!%--- Ceramic layer---
th_cer=0.635
l_cer=17
w_cer=19

!%--- Gel ---
!% width and length of gel are defined as the same as DBC ceramic
th_gel=7
l_gel=l_cer
w_gel=w_cer

!%--- grease ---
!% width and length of the grease are defined as the same as Cu layer above
th_gre=0.064
l_gre=l_Cu2
w_gre=w_Cu2

!%--- Heat base---
th_base=4
l_base=21
w_base=39


!+++check with analystical results++++
!l_Cu2=l_die
!w_Cu2=w_die
!l_Cu1=l_die
!w_Cu1=w_die
!l_cer=l_die
!w_cer=w_die
!l_gre=l_die
!w_gre=w_die
!l_base=l_die
!w_base=w_die
!l_p=l_die
!w_p=w_die
!d_p=0.0

!volume for the power region
Vpower=l_p*w_p*th_p

!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%
!% crack area distribution
!
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%
!crack edge points
!points number
N_crack=3

! location of the crack line in the old coordinates
! cracked area is on the left side

!ratio_x is the ratio of the crack region to the whole region in X0 direction
!ratio_y is the ratio of the crack region to the whole region in Y0 direction

*dim,ratio_x,array,N_crack
*dim,ratio_y,array,N_crack
ratio_x(1)=0.0
ratio_y(1)=0.0
ratio_x(2)=0.0
ratio_y(2)=0.42
ratio_x(3)=0.0
ratio_y(3)=1.0

*dim,lcrack_x,array,N_crack
*dim,lcrack_y,array,N_crack

*do,ii,1,N_crack
 lcrack_x(ii)=ratio_x(ii)*l_sol-l_sol/2.0
 lcrack_y(ii)=ratio_y(ii)*w_sol-w_sol/2.0
*enddo

!++++++++++++++++++++++++++++++++++++++

!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% Enter the preprosesser
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
/prep7
```

```
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% geometry
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% Define the element types
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!using solid70
et,1,70

!die: Volume 1
xtemp=l_sol/2
ytemp=w_sol/2
ztemp=th_Cu1
diez=th_die/cos(rot_sol)

k,1,-xtemp,ytemp,(ztemp+th_solmin)
k,2,-xtemp,-ytemp,(ztemp+th_solmax)
k,3,xtemp,ytemp,(ztemp+th_solmin)
k,4,xtemp,-ytemp,(ztemp+th_solmax)

k,5,-xtemp,-ytemp,(ztemp+th_solmax)+diez
k,6,xtemp,-ytemp,(ztemp+th_solmax)+diez
k,7,xtemp,ytemp,(ztemp+th_solmin)+diez
k,8,-xtemp,ytemp,(ztemp+th_solmin)+diez
v,8,7,6,5,1,3,4,2
! solder joints: Volume 2

k,100,xtemp,-ytemp,ztemp
k,101,xtemp,ytemp,ztemp
k,102,-xtemp,ytemp,ztemp
k,103,-xtemp,-ytemp,ztemp
V,1,3,4,2,102,101,100,103

! Cu1: Volume 3
BLOCK,-l_Cu1/2,l_Cu1/2,-w_Cu1/2,w_Cu1/2,0,th_Cu1

! ceramic: Volume 4
BLOCK,-l_cer/2,l_cer/2,-w_cer/2,w_cer/2,-th_cer,0

! Cu2: Volume 5
BLOCK,-l_Cu2/2,l_Cu2/2,-w_Cu2/2,w_Cu2/2,-th_Cu2-th_cer,-th_cer

! grease: Volume 6
BLOCK,-l_gre/2,l_gre/2,-w_gre/2,w_gre/2,-th_Cu2-th_cer-th_gre,-th_Cu2-th_cer

! heat base: Volume 7
BLOCK,-l_base/2,l_base/2,-w_base/2,w_base/2,-th_Cu2-th_cer-th_gre-th_base,-th_Cu2-th_cer-th_gre

! gel: Volume 8
BLC4,-l_gel/2.0,-w_gel/2.0,l_gel,w_gel,th_gel

!substract die from gel
VSBV,8,1,,delete,KEEP

!substract solder joint from gel
VSBV,9,2,,delete,KEEP

!substract Cu1 from gel
VSBV,8,3,,delete,KEEP
! Now gel is volume 9

!create the region where power is generated and substract it from the die
!power generation region: Volume 8
xtemp=l_p/2
ytemp=w_p/2
ztemp=th_Cu1+th_solmin+(th_die-th_p-d_p)/cos(rot_sol)
diez=th_p/cos(rot_sol)
!die: volume1
k,201,-xtemp,ytemp,(th_Cu1+th_solmin+(th_die-th_p-d_p)/cos(rot_sol))
k,202,-xtemp,-ytemp,(th_Cu1+th_solmax+(th_die-th_p-d_p)/cos(rot_sol))
k,203,xtemp,ytemp,(th_Cu1+th_solmin+(th_die-th_p-d_p)/cos(rot_sol))
k,204,xtemp,-ytemp,(th_Cu1+th_solmax+(th_die-th_p-d_p)/cos(rot_sol))

k,205,-xtemp,-ytemp,(th_Cu1+th_solmax+(th_die-th_p-d_p)/cos(rot_sol))+diez
k,206,xtemp,-ytemp,(th_Cu1+th_solmax+(th_die-th_p-d_p)/cos(rot_sol))+diez
k,207,xtemp,ytemp,(th_Cu1+th_solmin+(th_die-th_p-d_p)/cos(rot_sol))+diez
k,208,-xtemp,ytemp,(th_Cu1+th_solmin+(th_die-th_p-d_p)/cos(rot_sol))+diez
v,208,207,206,205,201,203,204,202

VSBV,1,8,,delete,KEEP
!left die: volume 10
```

```
/TRLCY,VOLU,0.5,ALL
csys,1

VGEN,1,all,,,0,atan(w_sol/l_sol),0, , ,1
wprota,0,90,0

csys,0

blc4,-50,-50,100,100
!area 55: the cutting area is different when it is 1D

VSBA,all,55,,delete,delete
vsel,all
save


!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% move the diagnal from X-Z plane to X-Y plane to match with
!% 2D structure analysis coordinates
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
wprota,,,90.000000
csys,4
wpstyl,,,,,,1
vGEN,,all, , , ,-90, , , ,1
csys,0

!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% thermal properties of the power module material used in material models
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
! Thermal conductivity(w/mm*K):      K_
! Mass density(kg/mm^3):             m_
! Specific heat(J/kg*K):             Cp_

!%---1. Die ---
!% thermal conductivity is temperature dependent(need to check
k_die1=0.1595
k_die2=0.1175
m_die=2.33E-06
Cp_die=700
mat,1
mp,c,,Cp_die
mp,dens,,m_die
MPTEMP,1, 0.273E+03, 0.373E+03
MPDATA,kxx,1,k_die1,k_die2

!%---2. solder joint---
k_sol=0.075
m_sol=7.40E-06
Cp_sol=213
mat,2
mp,kxx,,k_sol
mp,c,,Cp_sol
mp,dens,,m_sol

!%---3. Cu up---
k_Cu=0.385
m_Cu=8.93E-06
Cp_Cu=385
mat,3
mp,kxx,,k_Cu
mp,c,,Cp_Cu
mp,dens,,m_Cu

!%---4. Ceramic layer---
!% thermal conductivity is temperature dependent
k_cer1=0.02681
k_cer2=0.01978
Cp_cer=765
m_cer=3.97E-06
mat,4
mp,c,,Cp_cer
mp,dens,,m_cer
MPTEMP,1,0.273E+03, 0.373E+03
MPDATA,kxx,4,1,k_cer1,k_cer2

!%---5. Cu bottom---
mat,5
mp,kxx,,k_Cu
mp,c,,Cp_Cu
mp,dens,,m_Cu
```

```
!%---6. grease ---
k_gre=0.0003
m_gre=1.0E-09
Cp_gre=1
mat,6
mp,kxx,,k_gre
mp,c,,Cp_gre
mp,dens,,m_gre

!%---7. Cu baseplate ---
mat,7
mp,kxx,,k_Cu
mp,c,,Cp_Cu
mp,dens,,m_Cu

!%---8. Gel ---
!!!####m_gel need to check####!!!
k_gel=0.00019
m_gel=0.96E-06
!gel check
Cp_gel=1400
mat,8
mp,kxx,,k_gel
mp,c,,Cp_gel
mp,dens,,m_gel

!%---9. crack ---
!properties is air at 30 C from Flotherm
!k=2.49E-2 w/m*K
!Density 1.23kg/m^3
!specific heat 1.007E+3J/kg*K
k_crack=0.0000249
m_crack=1.23E-09
Cp_crack=1007
mat,9
mp,kxx,,k_crack
mp,c,,Cp_crack
mp,dens,,m_crack

SAVE
!volume number change after glue


vglue,25,11
vglue,11,14
vglue,2,16
vglue,3,18
vglue,18,20
vglue,3,22


vglue,24,1
vglue,1,15
vglue,6,17
vglue,7,19
vglue,19,21
vglue,7,23

!assign properties

!-- die: mat 1 --
Vsel,s,volu,,12
Vsel,a,volu,,13
!volume 12,13 is the power region
Vsel,a,volu,,24
Vsel,a,volu,,25
VATT,1,,1,0

!-- solder joints --
Vsel,s,volu,,1
Vsel,a,volu,,11
VATT,2,,1,0

!-- Cu up --
Vsel,s,volu,,2
Vsel,a,volu,,6
VATT,3,,1,0

!-- ceramic --
Vsel,s,volu,,4
Vsel,a,volu,,8
VATT,4,,1,0
```

```
!-- Cu bottom --
Vsel,s,volu,,18
Vsel,a,volu,,19
VATT,5,,1,0

!-- grease --
Vsel,s,volu,,7
Vsel,a,volu,,3
VATT,6,,1,0

!-- Cu base --
Vsel,s,volu,,5
Vsel,a,volu,,9
VATT,7,,1,0

!-- gel --
Vsel,s,volu,,26
Vsel,a,volu,,27
VATT,8,,1,0n

!***
!mesh power generation region from line mesh
vsel,all
lsel,s,line,,111
lsel,a,line,,112
LESIZE,all, , ,30, , , , ,0

lsel,s,line,,95
lsel,a,line,,96
lsel,a,line,,102
lsel,a,line,,104
LESIZE,all, , ,20, , , , ,0

lsel,s,line,,93
lsel,a,line,,94
lsel,a,line,,98
lsel,a,line,,100
LESIZE,all, , ,20, , , , ,0

lsel,s,line,,97
lsel,a,line,,99
lsel,a,line,,101
lsel,a,line,,103
LESIZE,all, , ,1, , , , ,0

!power region
MSHAPE,1
vmesh,12,13,1
ESIZE,0.5,0,
MSHAPE,1,3D
MSHKEY,0
!***

!die
ESIZE,1.0,0,
MSHAPE,1,3D
MSHKEY,0

vmesh,24
Vmesh,25

!solder
vmesh,11
vmesh,1

!other layers
ESIZE,1.5,0,
MSHAPE,1,3D
MSHKEY,0

!mesh Cu up
VMESH,2
Vmesh,6

!mesh ceramic
vmesh,4
vmesh,8

!mesh Cu bottom
vmesh,18
vmesh,19
```

```
!mesh grease
vmesh,3
vmesh,7

!mesh Cu base and gel
ESIZE,2.5,0,
MSHAPE,1,3D
MSHKEY,0
vmesh,5
vmesh,9
vmesh,27
vmesh,26

!###change the properties of the element in the crack region from solder(Mat:2) to air(Mat:9)##########

! select all the element from die attach
esel,s,mat,,2
!### get all the elements in die attach layer ###
*get,NEtotal,ELEM,0,COUNT
*get,NE_max,ELEM,0,NUM,MAX
*get,NE_min,ELEM,0,NUM,MIN


!### change the thermal ###

*do,i,NE_min,NE_max
!i=1254
 xa=CENTRX(i)
 ya=CENTRY(i)
 za=CENTRZ(i)

 !convert the coordinate to the old system
 x0=xa*0.648+za*(-0.762)
 y0=xa*(-0.762)+za*(-0.648)
 z0=ya*1.0
 *IF,z0,GT,th_Cu1,THEN
   *IF,z0,LT,(th_Cu1+th_sol),THEN
     !count the location of the element
     kk=0
     *do,j,1,N_crack
       *IF,y0,GT,lcrack_y(j),THEN
         KK=KK+1
       *ENDIF
     *enddo
     *IF,kk,GT,0,THEN
       *IF,kk,lT,N_crack,THEN
         xcrack=(lcrack_x(kk+1)-lcrack_x(kk))*(y0-lcrack_y(kk))/(lcrack_y(kk+1)-lcrack_y(kk))+lcrack_x(kk)
           *IF,x0,lt,xcrack,THEN
           !in the crack region
            emodif,i,mat,9
           *ENDIF
       *ENDIF
     *ENDIF
   *ENDIF
 *ENDIF
*enddo

vsel,,,,all,,,1


!#### solution start ####
/solu
outres,all,all

ANTYPE,TRANS
antype,0

!#####initial conditions:T_base K#####
TIMINT,OFF
TIME,1E-6
CNVTOL,TEMP
D,T_base
!bottom temperature 20C
DA,107,temp,T_base
DA,102,temp,T_base
outres,all,all
LSWRITE

!####Transient portion:####
*do,i,1,Ncycle
```

```
!step 1: power on from off to t_measure
TIMINT,ON
deltim,1e-4,5e-15,1
autots,on
kbc,1
!apply power
BFV,12,hgen,power/Vpower
BFV,13,hgen,power/Vpower
time,t_measure+(i-1)*(t_poweron+t_poweroff)
outres,all,all
lswrite

!step 2: power on from Transient1 to t_poweroff
TIMINT,ON
deltim,1e-4,5e-15,1
autots,on
kbc,1
!apply power
BFV,12,hgen,power/Vpower
BFV,13,hgen,power/Vpower
time,t_poweron+(i-1)*(t_poweron+t_poweroff)
outres,all,all
lswrite

!step 3: power off
TIMINT,ON
deltim,1e-4,5e-15,1
autots,on
kbc,1
!apply power
BFV,12,hgen,0
BFV,13,hgen,0
time,(t_poweron+t_poweroff)+(i-1)*(t_poweron+t_poweroff)
outres,all,all
lswrite
*enddo

lssolve,1,1+Ncycle*3
save
FINISH
!/EXIT,ALL

/post1
!######## calculate the average temperature and peak temperature of the die ########
vsel,s,mat,,1,1,1,1
!### get information of the nodes in die ###
*get,Node_diemax,NODE,0,NUM,MAX
*get,Node_diemin,NODE,0,NUM,MIN
*get,Y_topdie,NODE,0,MXLOC,Y

*set,AvgT_topdie,0.0
*set,MaxT_topdie,0.0
*set,Node_topdie,0

!######## calculate the average temperature and peak temperature of the junction########
/post1
vsel,s,,,12,13,,1
!### get information of the Nodes in die ###
*get,Node_juncmax,Node,0,NUM,MAX
*get,Node_juncmin,Node,0,NUM,MIN
*get,Node_juncnum,Node,0,COUNT


!#####step that average the temperature #####
set,4
*get,N_lastthermstep,active,0,set,lstp
*get,N_subthermstepoff,active,0,set,sbst

set,3
*get,N_stepson2s,active,0,set,sbst

set,2
*get,N_steps80ms,active,0,set,sbst
*get,T_cyclestart,active,0,set,time

!get the average and max temperature @80ms

set,(Ncycle-1)*3+2,N_stepson80ms

*set,AvgT_junction,0.0
*set,MaxT_junction,0.0
*set,Node_junction,0
```

```
*do,i,Node_juncmin,Node_juncmax
    *IF,NSEL(i),eq,1,then
        *get,eee,node,i,TEMP
        AvgT_junction=AvgT_junction+eee
        Node_junction=Node_junction+1
        *IF,eee,GT,MaxT_junction,THEN
          MaxT_junction=eee
        *ENDIF
    *ENDIF
*enddo
  AvgT_junction=AvgT_junction/Node_junction

AvgT_junction80ms=AvgT_junction
MaxT_junction80ms=MaxT_junction

!get the average and max temperature @2s(poweron)

set,(Ncycle-1)*3+3,N_stepson2s

*set,AvgT_junction,0.0
*set,MaxT_junction,0.0
*set,Node_junction,0

*do,i,Node_juncmin,Node_juncmax
    *IF,NSEL(i),eq,1,then
        *get,eee,node,i,TEMP
        AvgT_junction=AvgT_junction+eee
        Node_junction=Node_junction+1
        *IF,eee,GT,MaxT_junction,THEN
          MaxT_junction=eee
        *ENDIF
    *ENDIF
*enddo
  AvgT_junction=AvgT_junction/Node_junction

AvgT_junction2s=AvgT_junction
MaxT_junction2s=MaxT_junction

allsel,all

!!%%%%%%%%%%%%%%%% END OF PROGRAM   %%%%%%%%%%
```

Input file for structural analysis

```
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% Objective:        To develop 2D structural analysis on the power module with one side tilt
!%            under power cycling (input: thermaltilt.rth)
!%
!% Date:May 13th,2003
!%     1. properties updated based on Qian's thesis
!%       2. Problem: If using element 182 instead of 42 for die attach, there will be no result for creep strain
!%     3. relax the creep ratio to 0.15
!%  NEED TO do later:
!%     1.  Use a matrix to replace N_substeps80ms,N_substepspoweron,N_substepspoweroff
!%            together with its power level in thermal tilt
!%         2.  just bfin once and repeat lswrite
!%         3.
!% correction of movevoid0 :
!%     1. thermal input file is thermaltilt(.rth,.db..), jut replace the name for other thermal transient analysis
!%     2. temperary backup file is struct2D.db(do not use the same name)
!%     3. 3 steps per cycle in the thermaltransient
!%     4. TILT
!%     5.
!%     5.
!% Author:           Yunqi Zheng
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% Geometry of the power module
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
! unit: mm
! Thickness:                  th_
! Length:                     l_
! Width:             w_
! Diagnonal Length:  d_

!%--- Die ---
th_die=0.375
l_die=6.55
w_die=7.70

!%--- solder joint---
th_solmax=0.063
th_solmin=0.044
l_sol=l_die
w_sol=w_die
!% width and length of solder joint are defined as the same as die
th_sol=th_solmin

!%--- Cu layer under solder joint---
th_Cu1=0.3
l_Cu1=13
w_Cu1=13

!%--- Ceramic layer---
th_cer=0.635
l_cer=17
w_cer=19

!%--- Cu layer above grease---
th_Cu2=0.3
l_Cu2=14
w_Cu2=16

!determine the diagonal length

d_die=sqrt(l_die**2+w_die**2)

!Cu1
*if,l_Cu1/w_Cu1,gt,l_die/w_die,THEN
    d_Cu1=d_die*w_Cu1/w_die
*else
    d_Cu1=d_die*l_Cu1/l_die
*endif

!cer
*if,l_cer/w_cer,gt,l_die/w_die,THEN
    d_cer=d_die*w_cer/w_die
*else
```

```
     d_cer=d_die*l_cer/l_die
*endif

!Cu2
*if,l_Cu2/w_Cu2,gt,l_die/w_die,THEN
     d_Cu2=d_die*w_Cu2/w_die
*else
     d_Cu2=d_die*l_Cu2/l_die
*endif

!Use dual processor
/config,nproc,2
!SRthproc,2
!L: Length(mm)
!Th: Thickness(mm)
!N,S:division and space ratio for mesh generation

!arrays to form keypoint
ny1=6
nx1=12

*dim,nylayer,array,ny1-1
*dim,sylayer,array,ny1-1
*dim,nxlayer,array,nx1-1
*dim,sxlayer,array,nx1-1

*dim,ylayer,array,ny1
*dim,xlayer,array,nx1

!!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% void (void region is occupied with solder when there is no void
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!center
c_void=0.0
!diameter of the void
d_void=0.0

!void is not considered if the diameter is below evoid
evoid=0.5*th_sol

no_void=100

*if,d_void,lt,evoid,THEN
 no_void=-100
 d_void=d_die/8.0
 c_void=0.0
*endif

NXv=20                                  !Mesh division
SXv=1.0                                 !Mesh space ratio
nxlayer(6)=NXv
Sxlayer(6)=SXv                          !radius of the void

Lm1=(d_die/2.0+c_void-d_void/2.0)/2.0
!Lm1:left 1 for mesh (mm) left side of the die attach length: d_die/2.0+c_void-d_void/2.0
NLm1=30
SLm1=4.0
nxlayer(4)=NLm1
sxlayer(4)=SLm1

Lm2=d_die/2.0+c_void-d_void/2.0-Lm1
NLm2=30
SLm2=0.5
nxlayer(5)=NLm2
sxlayer(5)=SLm2

Rm1=(d_die/2.0-c_void-d_void/2.0)/2.0
NRm1=30
SRm1=2.0
nxlayer(7)=NRm1
sxlayer(7)=SRm1

Rm2=d_die/2.0-c_void-d_void/2.0-Rm1
NRm2=30
SRm2=0.25
nxlayer(8)=NRm2
sxlayer(8)=SRm2

!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% mesh specifications for layers
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Nth_die=4
```

```
Sth_die=4.0
nylayer(5)=Nth_die
sylayer(5)=Sth_die

Nth_sol=4
Sth_sol=1.0
nylayer(4)=Nth_sol
sylayer(4)=Sth_sol

!Cu1: up copper layer
Nd_Cu1=25
Sd_Cu1=1.0
nxlayer(3)=Nd_Cu1
sxlayer(3)=Sd_Cu1
nxlayer(9)=Nd_Cu1
sxlayer(9)=Sd_Cu1

Nth_Cu1=6
Sth_Cu1=0.25
nylayer(3)=Nth_Cu1
sylayer(3)=Sth_Cu1

!ceramic layer
Nth_cer=6
Sth_cer=1.0
nylayer(2)=Nth_cer
sylayer(2)=Sth_cer

Nd_cer=10
Sd_cer=2.0
nxlayer(1)=Nd_cer
sxlayer(1)=Sd_cer
nxlayer(11)=Nd_cer
sxlayer(11)=Sd_cer

!Cu2:Bottom copper layer
Nd_Cu2=10
Sd_Cu2=2.0
nxlayer(2)=Nd_Cu2
sxlayer(2)=Sd_Cu2
nxlayer(10)=Nd_Cu2
sxlayer(10)=Sd_Cu2

Nth_Cu2=3
Sth_Cu2=1.0
nylayer(1)=Nth_Cu2
sylayer(1)=Sth_Cu2

!coordinates for keypoints
ylayer(1)=-(th_Cu2+th_cer)
ylayer(2)=-th_cer
ylayer(3)=0
ylayer(4)=th_Cu1
ylayer(5)=th_Cu1+th_sol
ylayer(6)=th_Cu1+th_sol+th_die

xlayer(1)=-d_cer/2
xlayer(2)=-d_Cu2/2
xlayer(3)=-d_Cu1/2
xlayer(4)=-d_die/2
xlayer(5)=-d_die/2+Lm1
xlayer(6)=-d_die/2+Lm1+Lm2
xlayer(7)=d_die/2-Rm1-Rm2
xlayer(8)=d_die/2-Rm2
xlayer(9)=d_die/2.0
xlayer(10)=d_Cu1/2
xlayer(11)=d_Cu2/2
xlayer(12)=d_cer/2
SAVE

!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% Enter the preprosesser
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%/prep7


!%%%%%%%%%%%%%%%%
!% Define the element types, real constants and material models
!%%%%%%%

! Example of choise of element type and material models
!Die
mat,5
```

```
et,5,plane42,0,0,2,0,0
mp,ex,5,112000
mp,prxy,5,.28
mp,alpx,5,0.0000025

!Die attach
mat,4
et,4,PLANE42,0,0,2,0,0,0
!elastic
MPTEMP,     1, 0.2980000E+03, 0.3480000E+03, 0.3980000E+03,
MPDATA,EX ,       4,   1, 0.18075E+05, 0.17025E+05, 0.15975E+05,
MPTEMP
MPTEMP,     1, 0.2980000E+03, 0.3480000E+03, 0.3980000E+03,
MPDATA,NUXY,       4,   1, 0.400000E+00, 0.400000E+00, 0.400000E+00,
MPTEMP,     1, 0.2980000E+03, 0.3480000E+03, 0.3980000E+03,
MPDATA,ALPX,       4,   1,0.0000176,0.0000176,0.0000176

!plastic
TB,MISO,4,3,20,
!121.6,-0.4,0.29,-0.00046
!Temp(K),Temp (C),Cp,     n
!298,    25,     111.6,    0.2785
!348,    75,     91.6,     0.2555
!398,    125,    71.6,     0.2325
TBTEMP,298
TBPT,,0.000662,11.965
TBPT,,0.01,30.950
TBPT,,0.02,37.541
TBPT,,0.03,42.028
TBPT,,0.04,45.534
TBPT,,0.05,48.454
TBPT,,0.06,50.978
TBPT,,0.07,53.214
TBPT,,0.08,55.230
TBPT,,0.09,57.072
TBPT,,0.1,58.771
TBPT,,0.2,71.285
TBPT,,0.3,79.807
TBPT,,0.4,86.465
TBPT,,0.5,92.008
TBPT,,0.6,96.801
TBPT,,0.7,101.047
TBPT,,0.8,104.876
TBPT,,0.9,108.373
TBPT,,1,111.600
TBTEMP,348
TBPT,,0.000756,12.870
TBPT,,0.01,28.242
TBPT,,0.02,33.714
TBPT,,0.03,37.394
TBPT,,0.04,40.246
TBPT,,0.05,42.607
TBPT,,0.06,44.639
TBPT,,0.07,46.432
TBPT,,0.08,48.044
TBPT,,0.09,49.511
TBPT,,0.1,50.862
TBPT,,0.2,60.717
TBPT,,0.3,67.344
TBPT,,0.4,72.481
TBPT,,0.5,76.733
TBPT,,0.6,80.392
TBPT,,0.7,83.622
TBPT,,0.8,86.524
TBPT,,0.9,89.167
TBPT,,1,91.600
TBTEMP,398
TBPT,,0.000688,10.991
TBPT,,0.01,24.542
TBPT,,0.02,28.834
TBPT,,0.03,31.684
TBPT,,0.04,33.876
TBPT,,0.05,35.680
TBPT,,0.06,37.225
TBPT,,0.07,38.583
TBPT,,0.08,39.800
TBPT,,0.09,40.905
TBPT,,0.1,41.919
TBPT,,0.2,49.250
TBPT,,0.3,54.118
TBPT,,0.4,57.862
TBPT,,0.5,60.943
```

```
TBPT,,0.6,63.582
TBPT,,0.7,65.902
TBPT,,0.8,67.980
TBPT,,0.9,69.867
TBPT,,1,71.600

!creep
TBDE,CREE,4,,,
TB,CREE,4,1,4,8
TBTEMP,0
TBDATA,,1500,0.19,4.0,8580,,

!up copper
mat,3
et,3,PLANE42,0,0,2,0,0
mp,ex,3,110000
mp,prxy,3,.33
mp,alpx,3,0.000017

!Al2O3
mat,2
et,2,PLANE42,0,0,2,0,0
mp,ex,2,300000
mp,prxy,2,.21
mp,alpx,2,0.0000075

!bottom copper
mat,1
et,1,PLANE42,0,0,2,0,0
mp,ex,1,110000
mp,prxy,1,.33
mp,alpx,1,0.000017

! Creation of key points

*dim,tiltdY,array,nx1,ny1

*do,i,1,ny1
 *do,j,1,nx1
!++++++++++++++++++++++++++++++++++++
!+++ ----------tilt------------ +++
!++++++++++++++++++++++++++++++++++++
   tiltdY(j,i)=0
    *IF,i,GT,4,THEN
      *IF,j,GT,3,THEN
        *IF,j,LT,10,THEN
!         die bottom layer and top layer
          tiltdY(j,i)=(xlayer(j)-xlayer(4))*(th_solmax-th_solmin)/(xlayer(9)-xlayer(4))
        *endif
      *endif
    *endif
    k,,xlayer(j),(ylayer(i)+tiltdY(j,i))
 *enddo
*enddo

xx1=xlayer(6)-0.005
xx2=xlayer(7)+0.005
yy1=ylayer(4)/2+ylayer(5)/2
!additional key points for voids
k,,xx1,yy1
k,,xx2,yy1

! Creation of lines in x direction(length)
! Total lines:(nx1-1)*ny1
linecount1=0
*do,j,1,ny1
 *do,i,1,nx1-1
  l,i+nx1*(j-1),i+nx1*(j-1)+1,nxlayer(i),sxlayer(i)
  linecount1=linecount1+1
 *enddo
*enddo

! Creation of lines in y direction(length)
! Total lines: nx1*(ny-1)
*do,j,1,ny1-1
 *do,i,1,nx1
   *if,j,eq,4,THEN
     *if,i,eq,6,THEN
        bsplin,(j-1)*nx1+i,nx1*ny1+1,j*nx1+i
            linecount1=linecount1+1
        lesize,linecount1,,,nylayer(j),sylayer(j)
     *elseif,i,eq,7,THEN
```

```
        bsplin,(j-1)*nx1+i,nx1*ny1+2,j*nx1+i
              linecount1=linecount1+1
        lesize,linecount1,,,nylayer(j),sylayer(j)
     *else
        l,i+nx1*(j-1),i+nx1*j,nylayer(j),sylayer(j)
              linecount1=linecount1+1
     *endif
   *else
        l,i+nx1*(j-1),i+nx1*j,nylayer(j),sylayer(j)
              linecount1=linecount1+1
   *endif
 *enddo
*enddo

!creation of areas
*do,j,1,ny1-1
  *do,i,1,nx1-1
    line1=i+(j-1)*(nx1-1)
    delt=(nx1-1)*ny1
    al,line1,line1+delt+j,line1+(nx1-1),line1+delt+(j-1)
  *enddo
*enddo

!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% Mesh the geometry
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
*do,k,1,5,1
  type,k                                    !Activate element type
  mat,k                                     !Activate material
  amesh,1+(k-1)*(nx1-1),k*(nx1-1),1   !Area mesh
*enddo

!%%%%%%%%%%%
!% remove redundacy area
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

!clear mesh
aclear,1
aclear,11
aclear,23,24,1
aclear,32,36,1
aclear,42,47,1
aclear,53,55,1

!delete areas and related lines,keypoints

adele,1,,,1
adele,11,,,1
adele,23,24,1,1
adele,32,36,1,1
adele,42,47,1,1
adele,53,55,1,1

! for void case
*if,no_void,gt,evoid,THEN
  aclear,39
  adele,39,,,1
*endif

!%%%%%%%%
!% Apply boundary condition
!%%%
!bottom UY=0.0
*do,i,2,nx1-2
   DL,i,,UY,0.0
*enddo

DK,2,UX,0.0

!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% save all the nodes in file: temper.node

allsel
nwrite,temper,node
finish
save,struct2D,db
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
!% resume thermal transient 3D(thermaltilt.db&thermaltilt.rth) to get the temperature
!%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

!time per cycle(unit:second)
T_cycle=4
```

```
!cycles for structure analysis(unit: cycle)
N_structcycle=5

! get the steps of transient thermal analysis

!###cycle1: include T_Cycle, N_structcycle###
PARSAV, scalar,cycle1

resume,thermaltilt,db
/post1
file,thermaltilt,rth
! struct2D just need one stablized cycle(the last one in the trasient thermal analysis)!!
! in the transient thermal analysis, there are two steps for one cycle!!

set,last
*get,N_laststep,active,0,set,lstp
*get,N_substepoff,active,0,set,sbst

set,N_laststep-2
*get,N_substep80ms,active,0,set,sbst

set,N_laststep-1
*get,N_substepon,active,0,set,sbst

set,N_laststep-3
!Time associated with current results in the database
*get,T_cyclestart,active,0,set,time

!###cycle2: include N_laststep,N_substep2,T_substep1,T_cyclestart###
PARSAV,scalar,cycle2
PARRES,CHANGE,'cycle1',

/solu
outres,erase
antype,static,new          !specifies new static analysis
solcontrol,on              !turn on the optimized nonlinear solver
nlgeom,on                  !turn on the large deformation effect
lnsrch,auto                !Auto line search
rate,1                    !Turn on creep
cutcontrol,crplimit,0.15,1  !specifies cutcontrol of creep
deltim,1e-1,5e-2,1
autots,on
bfunif,temp,293            !specifies initial condition
lswrite,init               !reset load step file number


*do,icycle,1,N_structcycle

  *do,jcycle,1,N_substep80ms
!###save currentcycle: jcycle, icycle, kcycle###
    PARSAV,scalar,currentcycle
    resume,thermaltilt,db
    PARRES,change,cycle1
    PARRES,change,cycle2
    PARRES,change,currentcycle

    /post1
    file,thermaltilt,rth
    set,N_laststep-2,jcycle
    *get,ptime0,active,0,set,time
    ptime=T_cycle*(icycle-1)+ptime0-T_cyclestart
    bfint,temper,node,,temper,bfin,,0
    parsav,scalar,readtime
    finish

    resume,struct2D,db
    PARRES,change,cycle1
    PARRES,change,cycle2
    PARRES,change,currentcycle

    /solu
    parres,change,readtime
    time,ptime
!     nsubst,,1000
!     deltim,1e-4,5e-15,1
!     autots,on
    kbc,0
    tref,293
    /input,temper,bfin
    outres,esol,
    lswrite
  *enddo
```

```
 *do,kcycle,1,N_substepon

   PARSAV,scalar,currentcycle
   resume,thermaltilt,db
   PARRES,change,cycle1
   PARRES,change,cycle2
   PARRES,change,currentcycle


   /post1
   file,thermaltilt,rth
   set,N_laststep-1,kcycle
   *get,ptime0,active,0,set,time
   ptime=T_cycle*(icycle-1)+ptime0-T_cyclestart
   parsav,scalar,readtime
   bfint,temper,node,,temper,bfin,,0
   finish

   resume,struct2D,db
   PARRES,change,cycle1
   PARRES,change,cycle2
   PARRES,change,currentcycle

   /solu
   parres,change,readtime
!    nsubst,,1000
!    deltim,1e-4,5e-15,1
!    autots,on
   time,ptime
   kbc,0
   tref,293
   /input,temper,bfin
   outres,esol,
   lswrite
 *enddo

 *do,kcycle,1,N_substepoff

   PARSAV,scalar,currentcycle
   resume,thermaltilt,db
   PARRES,change,cycle1
   PARRES,change,cycle2
   PARRES,change,currentcycle


   /post1
   file,thermaltilt,rth
   set,N_laststep,kcycle
   *get,ptime0,active,0,set,time
   ptime=T_cycle*(icycle-1)+ptime0-T_cyclestart
   parsav,scalar,readtime
   bfint,temper,node,,temper,bfin,,0
   finish

   resume,struct2D,db
   PARRES,change,cycle1
   PARRES,change,cycle2
   PARRES,change,currentcycle

   /solu
   parres,change,readtime
!    nsubst,,1000
!    deltim,1e-4,5e-15,1
!    autots,on
   time,ptime
   kbc,0
   tref,293
   /input,temper,bfin
   outres,esol,
   lswrite
 *enddo
*enddo

save
!lssolve,1,40,1
!lssolve,1,1+N_structcycle*(N_substepoff+N_substepon+N_substep80ms),1

!%%%%%%% %%  END OF PROGRAM %%%%%%%%%%%%%%%%%%%%
```

Input file for calculating the average strain energy density over critical area

```
/post26
FILE,'stuct2Dtilt42','rst','.'
!##### !!!This need to change for different model!!! ####
!### the corner key points of the die attach layer help to locate the coordinates of the critical area ###
!lowest on the left end
kpoint1=40
!highest on the right end
kpoint2=57

! ### percentage of the critical area(total area,not just half) ###
! ### critical area is defined the right end in the middle half ###
Ap0=0.01
! percentage width of the critical area(y)
Apy=0.5
! percentage length of the critical area(x)
Apx=Ap0/Apy

Xmin1=KX(kpoint2)-(KX(kpoint2)-KX(kpoint1))/2*Apx
Xmax1=KX(kpoint2)
Ymin1=(KY(kpoint2)+KY(kpoint1))/2.0-(KY(kpoint2)-KY(kpoint1))/2.0*Apy
Ymax1=(KY(kpoint2)+KY(kpoint1))/2.0+(KY(kpoint2)-KY(kpoint1))/2.0*Apy

esel,s,mat,,4
!### get all the elements in die attach layer ###
*get,count1,ELEM,0,COUNT
*get,count11,ELEM,0,NUM,MAX
*get,count12,ELEM,0,NUM,MIN

*dim,tlist,array,count1

!### get all the elements(elist) whose center located in the critical area ###
kk=0
*do,i,count12,count11
 xa=CENTRX(i)
 ya=CENTRY(i)
 *IF,xa,LT,Xmax1,THEN
   *IF,xa,GT,Xmin1,THEN
      *IF,ya,LT,Ymax1,THEN
        *IF,ya,GT,Ymin1,THEN
          kk=kk+1
          tlist(kk+1)=i
        *ENDIF
      *ENDIF
   *ENDIF
 *ENDIF
*enddo

klist=kk+1
*dim,elist,array,kk+1
*do,i,2,klist
  elist(i)=tlist(i)
*enddo

nstep=n_structcycle*(N_SUBSTEP80MS+N_SUBSTEPOFF+N_SUBSTEPON)
!numvar,klist

*DIM,t_seconds,array,nstep,1
*DIM,XY_Wcr,array,nstep,1
*DIM,XY_Wpl,array,nstep,1
*DIM,VM_Wcr,array,nstep,1
*DIM,VM_Wpl,array,nstep,1

*dim,elemA,array,klist
*DIM,deltXY_Wcr,array,klist,1
*DIM,deltXY_Wpl,array,klist,1
*DIM,deltVM_Wcr,array,klist,1
*DIM,deltVM_Wpl,array,klist,1

!time step to caculate the strain energy change over one cycle
step_end=nstep-N_SUBSTEPOFF
step_start=step_end-(N_SUBSTEP80MS+N_SUBSTEPOFF+N_SUBSTEPON)

!### get the corresponding area for elements in the critical area ###
*do,k,2,klist
*VABS,1
```

```
*vget,elemA(k),ELEM,elist(k),GEOM
*enddo

*do,i,2,klist
 Eid=elist(i)
! get equivalent plastic energy

/POST26
FILE,'stuct2Dtilt42','rst','.'
/UI,COLL,1
!NUMVAR,200
SOLU,191,NCMIT
STORE,MERGE
FILLDATA,191,,,,1,1
REALVAR,191,191

esol,64,Eid,,eppl,x
esol,65,Eid,,eppl,y
esol,66,Eid,,eppl,z
esol,67,Eid,,eppl,xy
esol,68,Eid,,eppl,yz
esol,69,Eid,,eppl,xz
esol,74,Eid,,s,x
esol,75,Eid,,s,y
esol,76,Eid,,s,z
esol,77,Eid,,s,xy
esol,78,Eid,,s,yz
esol,79,Eid,,s,xz
 int1,80,74,64
 int1,81,75,65
 int1,82,76,66
 int1,83,77,67
 int1,84,78,68
 int1,85,79,69
 add,86,80,81,82
 add,87,83,84,85
 add,88,86,87,,Wpl_VM

! get Equivalent creep energy
 esol,164,Eid,,epcr,x
 esol,165,Eid,,epcr,y
 esol,166,Eid,,epcr,z
 esol,167,Eid,,epcr,xy
 esol,168,Eid,,epcr,yz
 esol,169,Eid,,epcr,xz
 esol,174,Eid,,s,x
 esol,175,Eid,,s,y
 esol,176,Eid,,s,z
 esol,177,Eid,,s,xy
 esol,178,Eid,,s,yz
 esol,179,Eid,,s,xz
 int1,180,174,164
 int1,181,175,165
 int1,182,176,166
 int1,183,177,167
 int1,184,178,168
 int1,185,179,169
 add,186,180,181,182
 add,187,183,184,185
 add,188,186,187,,Wcr_VM

 VGET,t_seconds,1
 VGET,XY_Wpl,83
 VGET,XY_Wcr,183
 VGET,VM_Wpl,88
 VGET,VM_Wcr,188

 deltXY_Wpl(i)=XY_Wpl(step_end)-XY_Wpl(step_start)
 deltXY_Wcr(i)=XY_Wcr(step_end)-XY_Wcr(step_start)
 deltVM_Wpl(i)=VM_Wpl(step_end)-VM_Wpl(step_start)
 deltVM_Wcr(i)=VM_Wcr(step_end)-VM_Wcr(step_start)

*enddo

!### calculate average strain energe ###
t1=t_seconds(step_end)
t2=t_seconds(step_start)
*cfopen,strainenergy,csv
*vwrite,Ap0,t1,t2
('% of crack,',F6.3,',end time,',F10.4,',start time,',F10.4)
*vwrite
('element #',1x,',element area',',deltXY_Wpl',1x,',deltXY_Wcr',1x,',deltVM_Wpl',1x,',deltVM_Wcr')
```

```
*vwrite,elist(1),elemA(1),deltXY_Wpl(1),deltXY_Wcr(1),deltVM_Wpl(1),deltVM_Wcr(1)
(f5.0,',',f13.9,',',4(f10.5,',',2x))
*cfclose
finish
```

Appendix G

Introduction

Solder joint used in electronic packages are under various loading conditions, where different strain rates are involved. Under temperature cycling, the strain rate is usually as low as 10^{-3}/sec. While under vibration or drop test, the strain rate could reach as high as 1~100/sec. (check) Former studies have found out that under different deformation rate conditions, failure modes could be different ([115]). So it is necessary to understand the difference in solder joints response under different strain rate testing.

In the study, Sn3.8Ag0.7Cu solder joints attached to copper pad at both sides has been studied under different strain rate conditions: 1μm/sec, 600 μm/sec and drop test. For each condition, failure modes have been detected and examined using optical microscope, scanning electron microscope (SEM) and EDX microprobe analysis. The mechanisms that cause the differences were also discussed.

Most of the studies on solder joint reliabilities have been concentrated on the solder properties. However, solder joints reliability involves the not only bulk solder but also interfaces, such as intermetallic such as CuSn or NiSn formed between solder and substrate metals.

A lot of studies have shown that under temperature cycling conditions, solder joint creep is the dominant failure mechanism and solder joint usually failed through the bulk solder, while initiation at the interface is also detected. On the other hand, under drop testing, studies ([116]) have found that the failure will always occurs at the interface between the

solder and substrate, more specifically, through intermetallics. However, more metallurgical studies are needed to confirm the results

The paper is going to concentrate on difference in failure modes of solder joints failure under various strain rate testing. Metallurgical analysis is conducted to determine root cause, thus supply physical evidence for further studies. It was concluded that interfacial microstructure plays an important role in the solder joint reliability especially under high strain rate testing.

Experiment setup

In this experiment, Sn3.8Ag0.7Cu has been soldered on copper pads using hot plate. The solder is reflowed at 250°C for 60 sec, the aging conditions is 100 hours at $0.82T_m$. Dimension of the joint is: $3x1x0.180mm^3$. Final intermetallic thickness at interfaces is around 4 ~ 5 μm.

In the test, Dage2400 shear testers were used to pull the sample at two constant speed: 1μm/sec (equivalent strain rate: 5.56E-3/s) and 600 μm/sec (equivalent strain rate: 3.33/s).(Figure G. 1) The loader kept moving at the constant speed until the sample has failed and maximum force were recorded. Drop test was conducted from 1m above to the ground several times until the sample was failed.

The fracture surfaces have also been examined using optical microscope and SEM/EDX. Both Secondary and Backscatter images were taken. Based on the microstructure

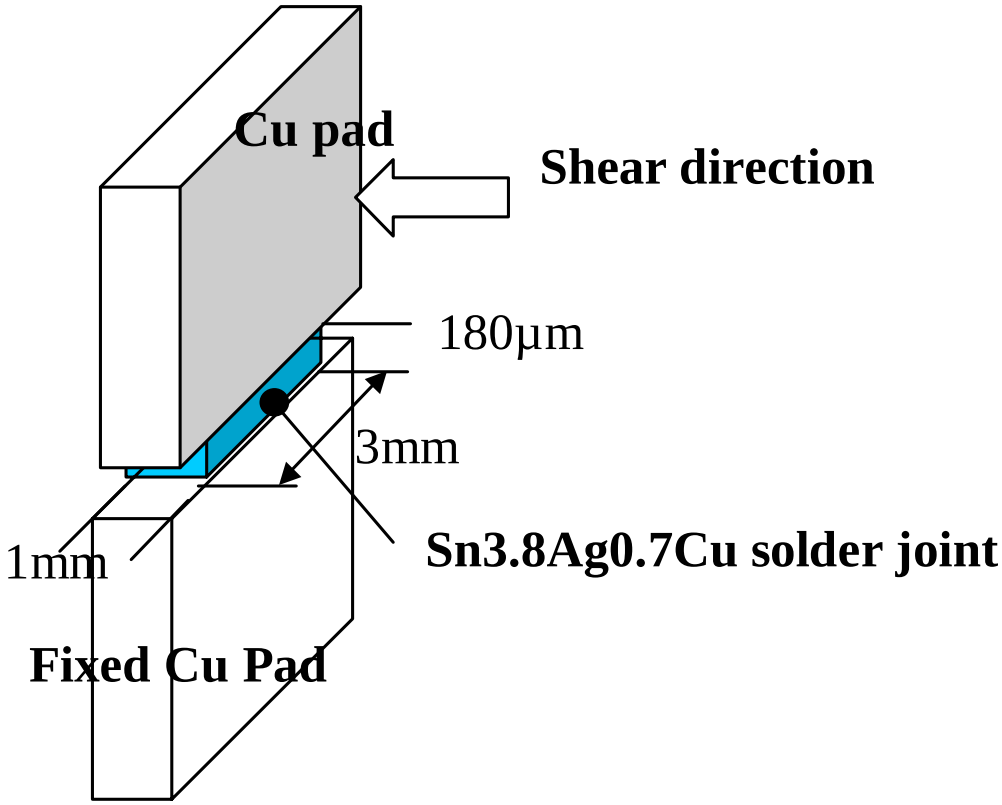


Figure G. 1 Strain rate shear testing setup

analysis, fracture modes have been determined and the mechanism has also been discussed.

Results

In the experiment, shear testing at low speed (1µm/sec), high speed (600 µm/sec) and drop test were conducted. For each loading condition, one typical sample with minimal voids was examined using SEM/EDX.

Failure under shear testing at 1 µm/s

In the experiment, a large amount of plastic deformation occurred to bulk solder. SEM/EDX analyses on both fracture surfaces, while fracture surface #1S is with the part that most solder is still attached and fracture surface #1(see Figure G. 2) is the opposite side with little solder attached. (S means the fracture surface with most solder attached

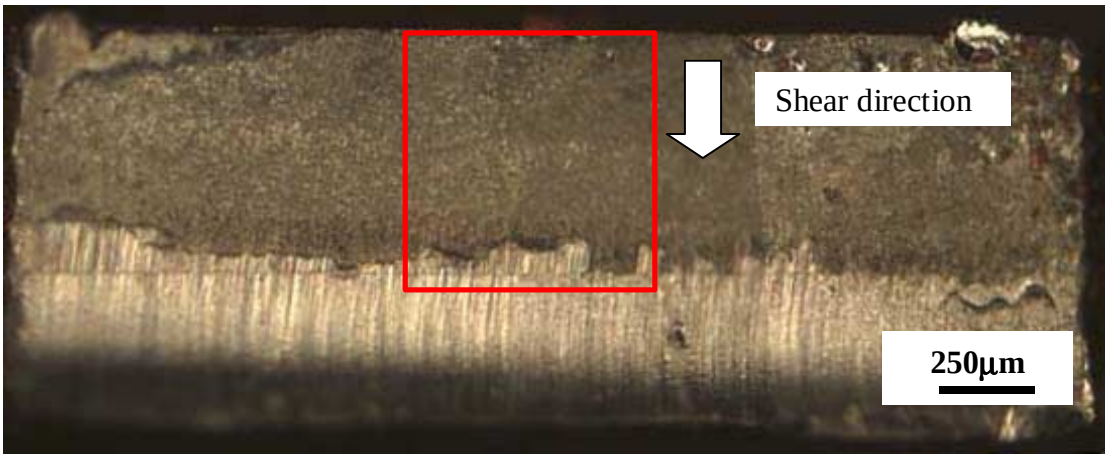


Figure G. 2 Optical image of the complete fracture surface #1 at 1µm/sec

after the failure, while without S means the fracture surface with less or no solder attached after the failure)

Through EDX analysis on area A, B, C on fracture surface #1(Figure G. 3) (see Fig. 3, it was determined that the relative dark area C, A on Fig. 3 are intermetallics. While the bright area B is solder.

Backscatter images on area A (see Figure G. 4) has also shown dimpled fracture surface. It indicated that ductile fracture occurred during shear testing at 1µm.

Table G. 1 EDX results on fracture surface#1

	Atomic ratio (%)			Results
	Cu	Sn	Ag	
B	0	100	0	Solder
C	58	41	0	Cu-Sn Intermetallic
A	51	49	0	Cu-Sn intermetallic

At the same time, EDX analysis on the other fracture surface #1S (See Figure G. 6&Figure G. 7) where most solder is attached have found that it is mostly solder at this side. (See Table G. 2) The fracture surface is characterized by dimpled surface with a large amount of small voids, a clear indication of ductile fracture. (See Figure G. 7)

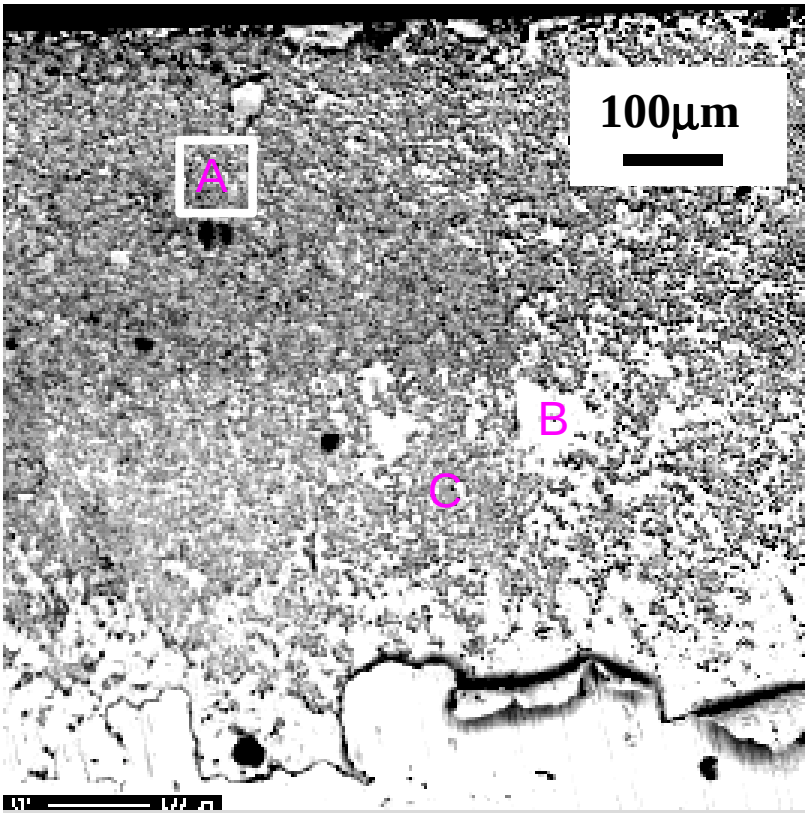


Figure G. 3 Backscatter images part of the fracture surface #1 (the area is inside red circle in Figure G. 2

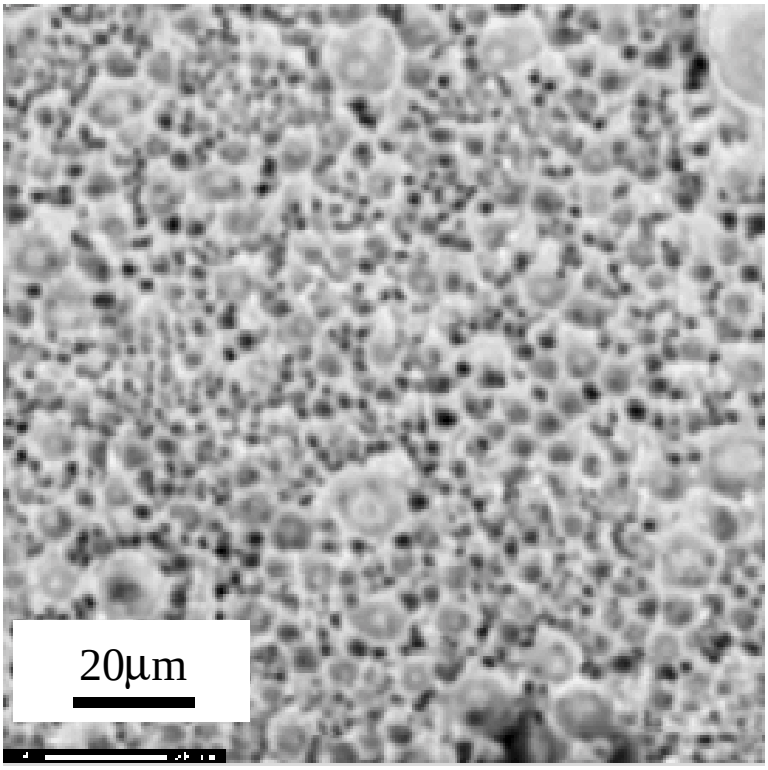


Figure G. 4 Backscatter image of area A on fracture surface #1, where dimpled surface is clearly shown.

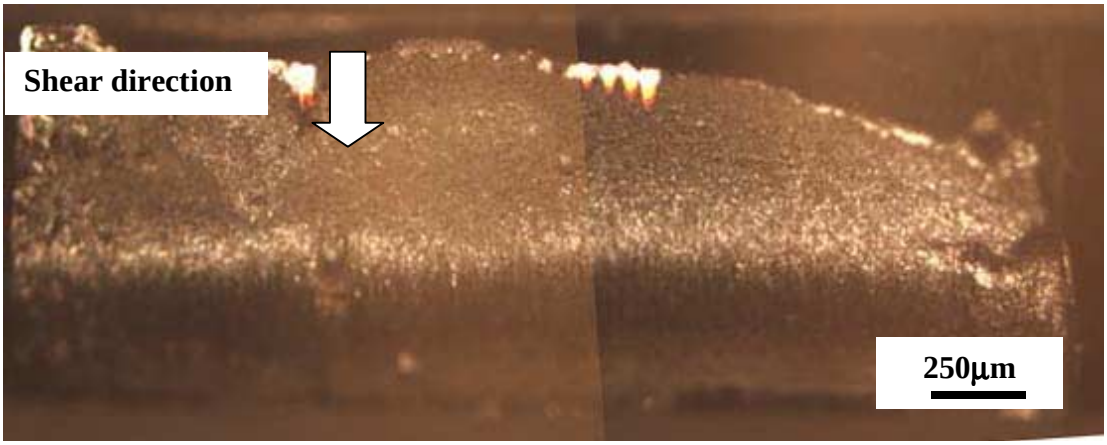


Figure G. 5 Optical image of fracture surface #1S (solder side) at 1µm/sec

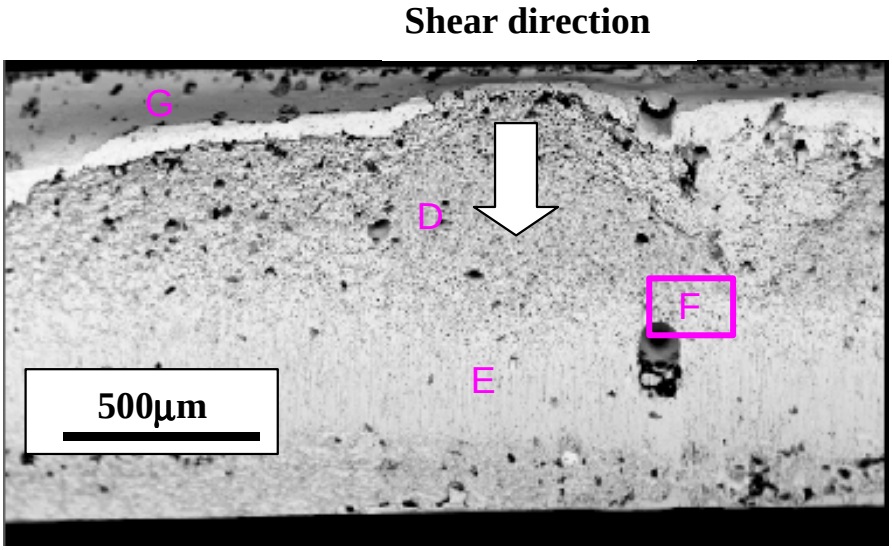


Figure G. 6 Backscatter image of fracture surface #1S (solder side) at 1µm/sec

Table G. 2 EDX results on fracture surface#1S

	Atomic ratio (%)			Results
	Cu	Sn	Ag	
D	16	80	4	Solder with some Cu-Sn
E	0	95	5	Solder
G	0	100	0	Solder

From analysis on both fracture surfaces which went through shear testing at 1μm/s, tt is clear that failure initiated in the solder, then propagated between solder and intermetallic and fail through the bulk solder at last. The fracture is ductile fracture and a lot of plastic deformation has occurred to the solder.

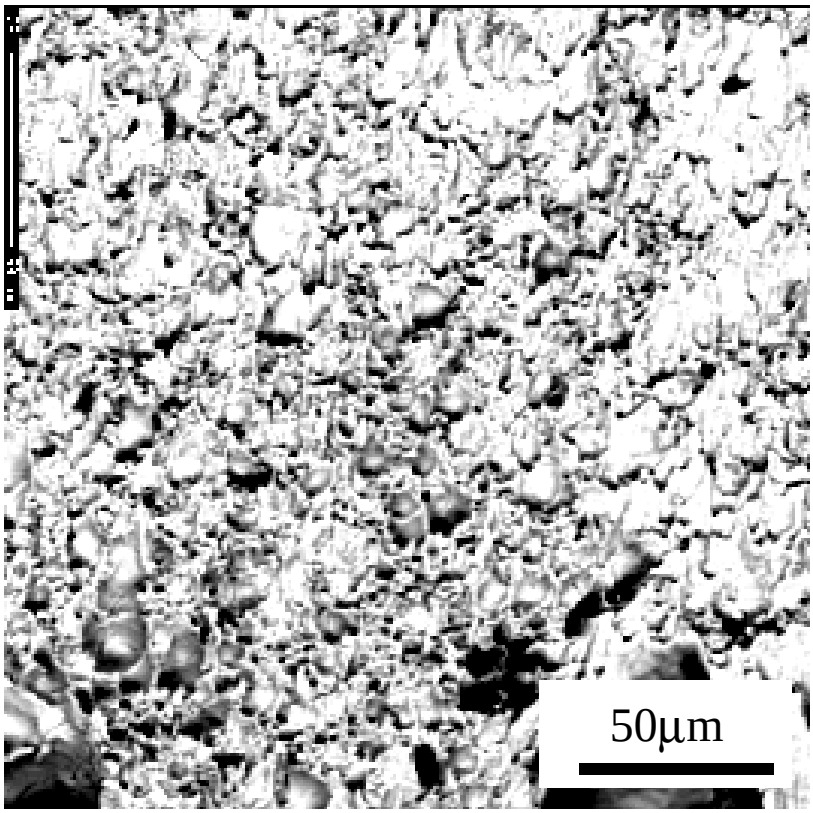


Figure G. 7 Backscatter image of fracture surface #1S at area F

Failure under shear testing at 600 μm/s

After 600μm/s speed shear testing, the bulk solder does not have obvious deformation (See Figure G. 8) The sample has been separated into half and crack was occurred at the interface.

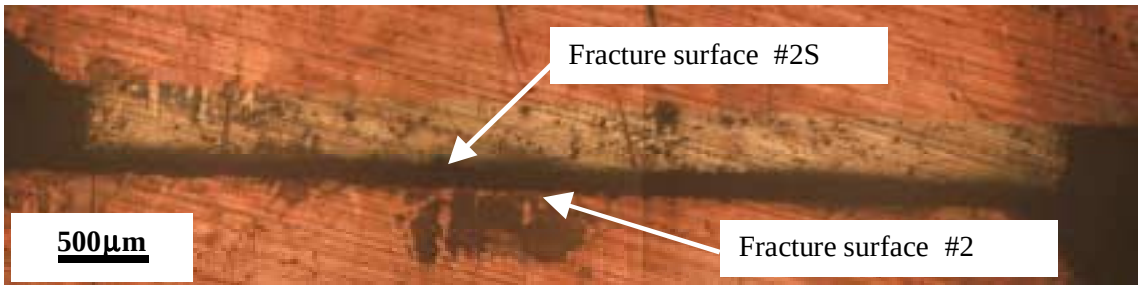


Figure G. 8 Optical microscopy of one failed sample after shear testing at 600µm/s

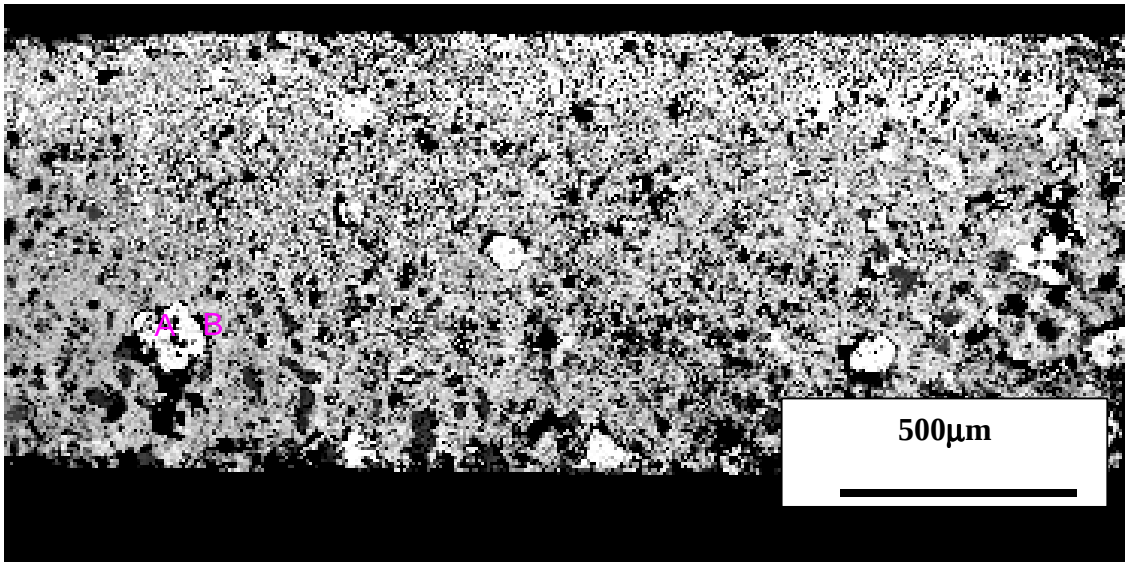


Figure G. 9 Backscatter image of fracture surface #2

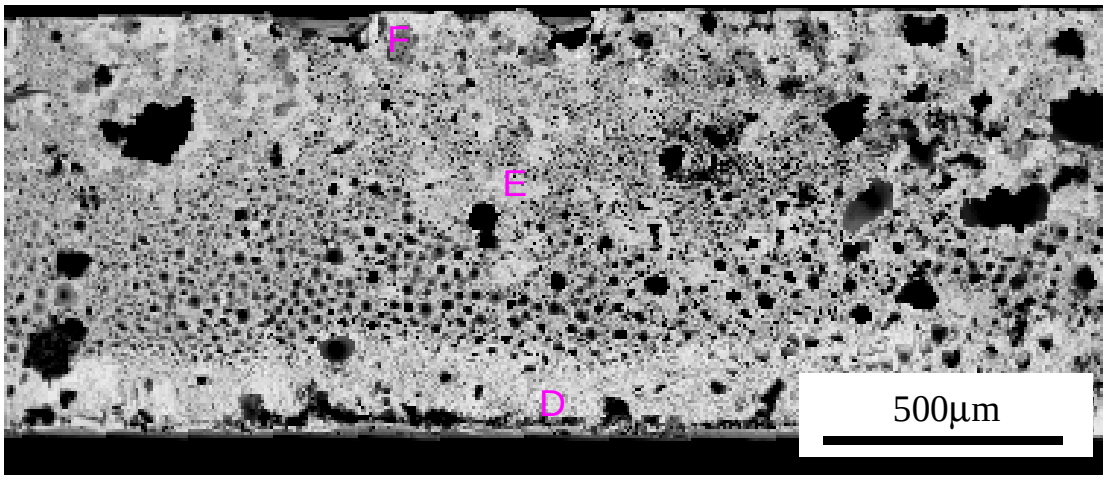


Figure G. 10 Backscatter image of fracture surface #2S

Table G. 3 EDX results on fracture surface#2S and #2

	Atomic ratio (%)			Results
	Cu	Sn	Ag	
A	20	75	5	Cu-Sn
B	75	25	0	Cu-Sn
D	25	75	0	CuSn
E	52	48	0	CuSn
F	97	3	0	Copper

Fracture surface#2 is mainly composed of Cu-Sn intermetallics (area B: Cu:Sn=75:25), Higher at% Cu is very likely due to the effect from the copper pad below. EDX on fracture surface#2S, the opposite side where most solder attached, clearly indicated the presence of Cu-Sn intermetallic at the surface as weel .It shows that fracture under high strain rate is at solder/copper pad interface. At the same time, little plastic deformation has occurred to the solder and it is a brittle failure. The fracture surfaces on the solder side show a lot of voids. Those voids might accelerate the failure.

Failure under drop testing

The failure under drop testing is similar to failure under 600μm/s, which has caused negligible deformation in the solder joints (see Figure G. 11). The sample has broken into half and the failure just went through solder joint/copper pad interface. EDX analysis on fracture surface #3S on solder side confirmed that the surface is composed of Cu-Sn intermetallics. (See Table G. 4)

From the enlarging image(Figure G. 14) on fracture surface on solder side, small voids with diameter around a few microns are distributed. However, this is not detected on the opposite fracture surfaces(Figure G. 15&Figure G. 16)

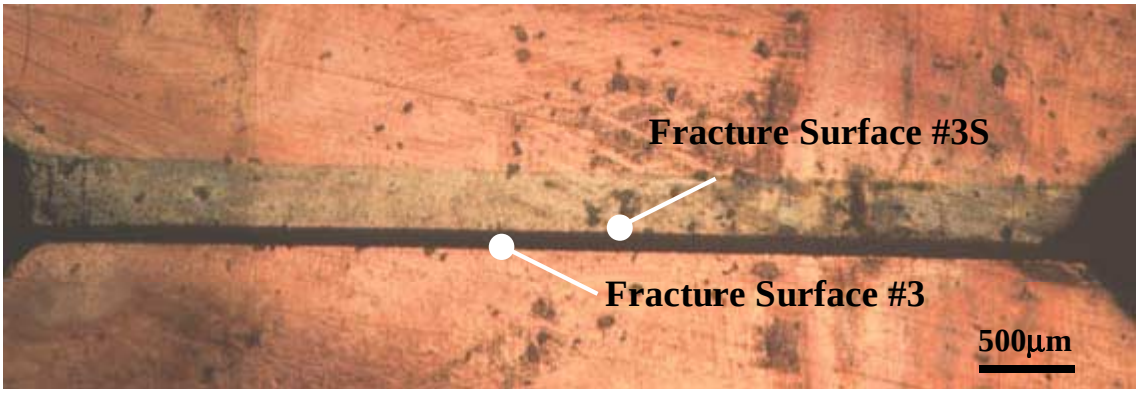


Figure G. 11 Optical microscopy of one failed sample after drop testing

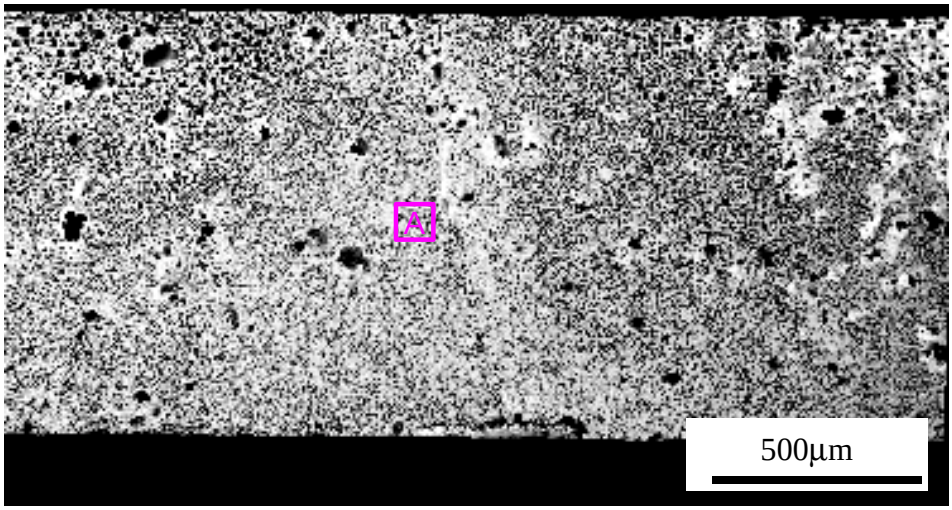


Figure G. 12 Backscatter image of fracture surface #3S

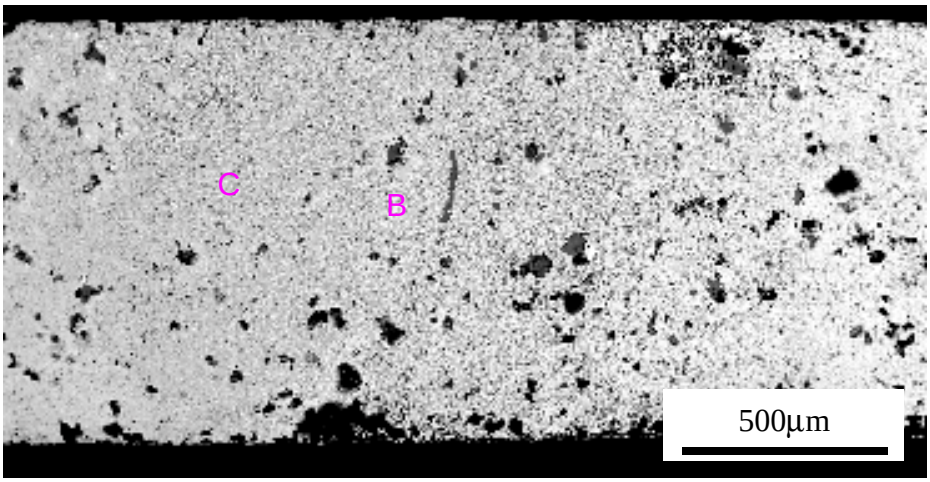


Figure G. 13 Backscatter image of fracture surface #3

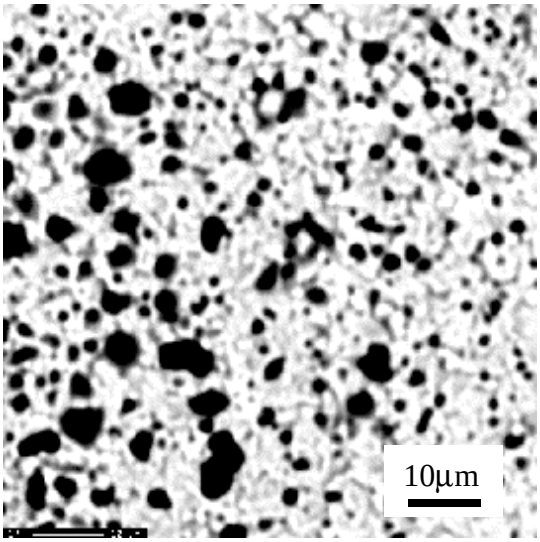


Figure G. 14 Backscatter image of A on fracture surface #3S, where voids of diameter around a few microns (dark) are distributed along the interfaces

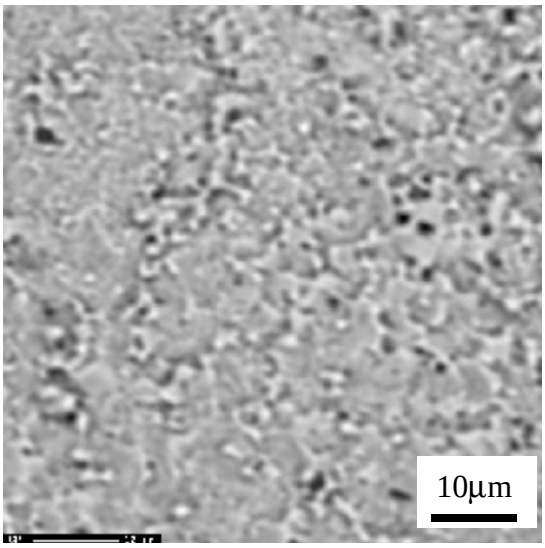


Figure G. 15 Backscatter image of B on fracture surface #3

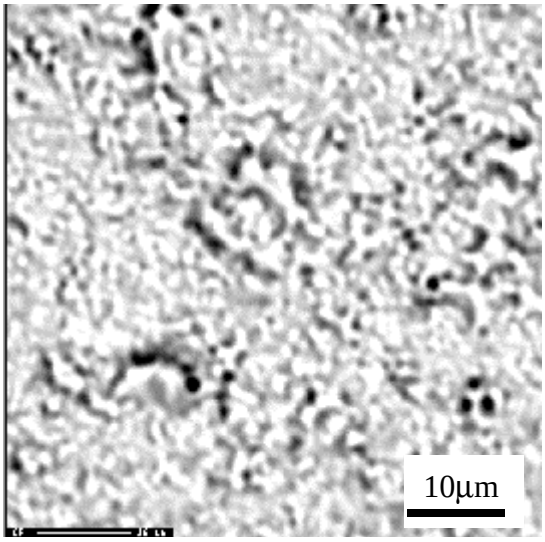


Figure G. 16 Backscatter image of C on fracture surface #3

Table G. 4 EDX results on fracture surface#3S and #3

	Atomic ratio (%)			Results
	Cu	Sn	Ag	
A	63	37	0	Cu-Sn
B	77	23	0	Cu-Sn
C	77	23	0	Cu-Sn

SEM/EDX result shows the fracture surface#3 at the solder side is composed of both Cu(77 at%) and Sn(23 at%).So this surface is definitely composed of CuSn intermetallics. At the same time, the atomic ration of Cu to Sn(77:23) under drop testing is very near to that(75:25) of fracture surface #2 under high strain rate loading(600μm/s). Which means that under drop testing, failure location is same to the location under high strain rate testing.

SEM/EDX analysis confirmed that failure under drop testing happens through intermetallic layer. It is brittle intermetallic failure.

Conclusions

In the experiment, we have testing the sample under three strain rates:

1. Low strain rate shear testing (≈5.56E-3/sec)
2. High strain rate shear testing (≈3.33/sec)\
3. Drop testing

Under low strain rate testing, the failure is initiated in the solder and going partly trough intermetallic, finally it break through the solder. Large amount of plastic deformation happens in the bulk solder and the fracture is ductile mode during the testing. It did not happen to the solder under high strain rate and drop testing, which has little bulk deformation, and the fracture is brittle mode.

So under the low strain rate, the failure is due to non-elastic deformation occurred to the solder and no intermetallic related failure has observed.

Under high speed shear testing and drop testing, while strain rate is much higher than under temperature cycling conditions, little plastic deformation has occurred to the joint. SEM/WDX analysis has confirmed that the failure happens through intermetallics at solder/copper pad interface, and is a brittle failure. Furthermore, the small defects such voids with several microns in diameter might also contribute to the failure and the effects should not be ignored.

Under high strain rate conditions, interfacial structures especially the intermetallics properties play an important role in the solder joint reliability. Under this condition, the effects of defects, such as voids due to reflow, kirkendal voids, could no longer be ignored.

However, for both high strain rate and low strain rate testing samples, failure happens at different locations at the interface even under similar amount of voids. So brittleness of the intermetallic layer definitely plays a dominant role in the failure under the high strain rate testing instead of the lower strain rate testing.

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