ABSTRACT

Title of Dissertation : LOW PHASE NOISE DESIGN TECHNIQUES FOR PHASE LOCKED LOOP BASED INTEGRATED RF FREQUENCY SYNTHESIZERS

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The explosive growth of wireless communication market today has brought an increasing demand for high performance radio-frequency integrated circuits (RFIC) at low cost. As a result, there is a great interest in integrating the various blocks of a communication system on a single chip transceiver. One of the most difficult components to integrate is the frequency synthesizer that generates the local oscillator (LO) carrier signal. The difficulty comes mostly from the very stringent phase noise performance requirements of the wireless application.

In this dissertation, we are interested in improving phase noise performance of integrated phase-locked-loop (PLL) based radio-frequency (RF) frequency synthesizers. The most important phase noise contributors in a PLL are voltage controlled oscillator (VCO) and Phase Frequency Detector/Charge Pump/Frequency Dividers (PFD/CP/Divider). In this dissertation, we focus on the analysis of the phase noise generation mechanism in these key building blocks and the derivation of the analytical relationship between their phase noise performance and circuit design parameters. For VCO, based on the understanding of phase noise generation process

in cross-coupled CMOS LC VCO, a simple yet accurate analytical phase noise model was proposed and a closed form formula for the fitting factor in Leeson's model is derived. For PFD/CP/Divider, due to the presence of many digital components, their phase noise model is studied from the point of view of timing jitter. The analytic equation that relates the PFD/CP/Divider 1Hz normalized phase noise floor and circuit parameters is derived. Based on the theoretical analysis, the design schemes for optimizing the phase noise performance are proposed and verified by simulation and experimental prototype measurement.

LOW PHASE NOISE DESIGN TECHNIQUES FOR PHASE LOCKED LOOP BASED INTEGRATED RF FREQUENCY SYNTHESIZERS

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Table of Contents

List of Abbreviations

AC	Alternating Current
AM	Amplitude Modulation
BER	Bit Error Rate
BPSK	Binary Phase shifted Keying
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
DC	Direct Current
EVM	Error Vector Magnitude
IC	Integrated Circuit
IF	Intermediate Frequency
ISF	Impulse Sensitivity Function
LC	Inductor Capacitor
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Loop Filter
NMF	Noise Modulation Function
NMOS	N-channel Metal Oxide Semiconductor
PA	Power Amplifier
PD	Phase Detector
PFD	Phase Frequency Detector
PSD	Power Spectral Density
PLL	Phase Locked Loop
PM	Phase Modulation
PMOS	P-channel Metal Oxide Semiconductor
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shifted Keying
RF	Radio Frequency
RMS	Root Mean Square
SNR	Signal to Noise Ratio
SSB	Single Side Band

VCO	Voltage Controlled Oscillator
VSA	Vector Signal Analyzer
WLAN	Wireless Local Area Network

Chapter 1: Introduction

1.1 Motivation

The wireless personal communication market has been growing explosively due to the ever emerging new applications and dropping prices. A low cost, small, long-battery-life solution has been the dream for decades. Many efforts have been devoted to the integration of such circuits in low-cost technology in order to reach the goal. Most of the baseband signal processing circuits use a CMOS process because of lower cost and higher integration capability. Recently research efforts are being made to integrate most RF functions in CMOS with the goal of realizing single-chip RF-to-baseband systems.

A PLL (Phase Locked Loop) based frequency synthesizer is one of the major building blocks for an RF transceiver. The role of a frequency synthesizer is to provide the reference frequency for frequency translation in wireless transceivers. An integrated frequency synthesizer in CMOS process that meets strict phase noise performance requirements of today's wireless communication standards remains a challenging problem due to both technology limitations on high quality on-chip passive components and lack of a proper and efficient optimization methodology.

This research focuses on the analysis and design techniques for low phase noise integrated phase-locked-loop (PLL) based radio-frequency (RF) frequency synthesizers in CMOS technology. In the dissertation, the phase noise generation mechanism in the key building blocks is analyzed and the analytical relationship between their phase noise performance and circuit design parameters is derived.

Based on the theoretical analysis, the design schemes for optimizing the phase noise performance are proposed and verified by simulation and experimental prototype measurement.

1.2 Organization of the dissertation

In Chapter 2, the fundamentals of frequency synthesizer and phase noise are reviewed. Various noise sources in PLL based frequency synthesizers are identified and their contributions to the overall closed loop phase noise are derived.

In Chapter 3, low phase noise design techniques for CMOS cross-coupled LC VCO are examined. A generalized linear phase noise model based on physical mechanism of phase noise is proposed and a closed form phase noise formula for LC cross-coupled VCO is derived.

In Chapter 4, low noise design techniques for other blocks in PLL are presented, including low noise frequency dividers, phase frequency detectors and charge pumps. Due to the presence of many digital components, their phase noise model is studied from the point of view of timing jitter. The analytic equation that relates the PFD/CP/Divider 1Hz normalized phase noise floor and circuit parameters is derived.

In Chapter 5, the design of an experimental prototype and the measurement results are presented.

Chapter 6 concludes the dissertation.

Chapter 2: Frequency Synthesizer and Phase Noise

2.1 Role of frequency synthesizer in a wireless transceiver

The role of a frequency synthesizer is to provide the reference frequency for frequency translation in wireless transceivers [Raza97]. Fig. 2.1 shows the block diagram of a typical super-heterodyne wireless transceiver RF section. A RF synthesizer is used to generate the local oscillator (LO) signals in down- and up-conversion mixers for the frequency translation.

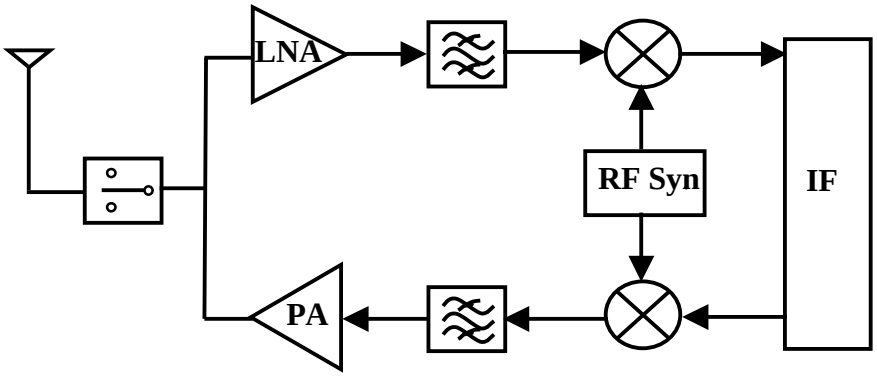


Figure 2.1 A typical wireless transceiver RF section

The function of frequency synthesizer is similar in receiver and transmitter path and generally the requirement of receiver is more stringent. So in the following discussion, we will focus on receiver path.

Considering the receiver path in the above diagram, there are several different channels being received at the antenna. The RF frequency synthesizer is tuned so that the output signal of the down-conversion mixer is at a constant IF frequency. The signal is then easier to filter and deal with because it is at a fixed and lower frequency from this point on.

As shown in Fig. 2.2, an ideal frequency synthesizer generates a single frequency tone. In the receiver case, it mixes with the received RF signal spectrum and shifts it down to IF. The output spectrum is the convolution result of the synthesizer tone with the received RF signal spectrum.

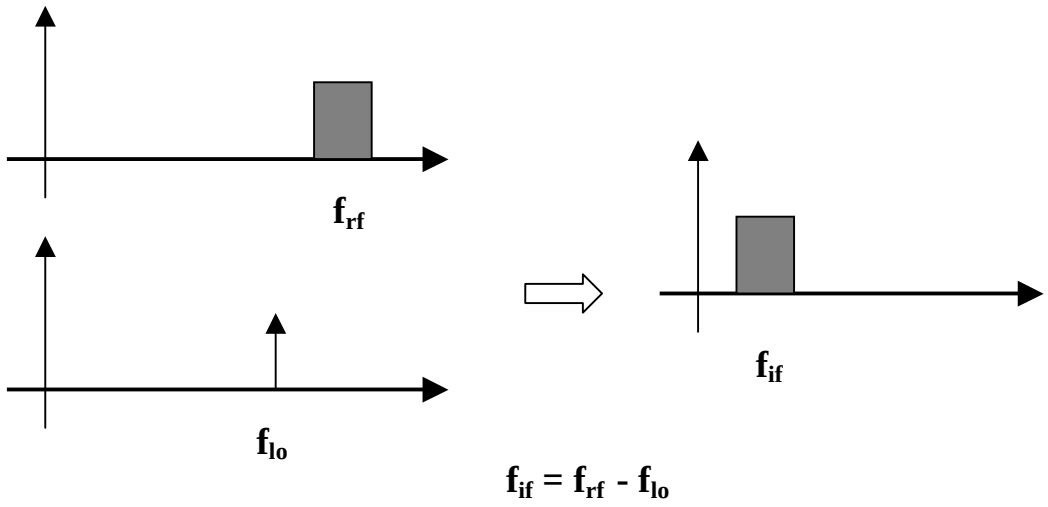


Figure 2.2 Role of frequency synthesizer in receiver path

2.2 Why phase noise is important?

2.2.1 The definition of phase noise

In section 2.1 we showed that the ideal output spectrum of a frequency synthesizer should be a single tone at the desired frequency in order to provide the reference frequency for accurate frequency translation. A single tone in the frequency domain is equivalent to a pure sinusoidal waveform in the time domain. In a practical frequency synthesizer, the random amplitude and phase deviations occur due to the inherent (*e.g.*, device thermal and shot noise) and external (*e.g.*, power line disturbance) noise sources. These deviations produce energy in the frequencies other than the desired

frequency. Figure 2.3 shows the spectrum of ideal and practical frequency synthesizer output signal. Phase noise is the parameter to measure the spectral purity of a frequency synthesizer output signal.

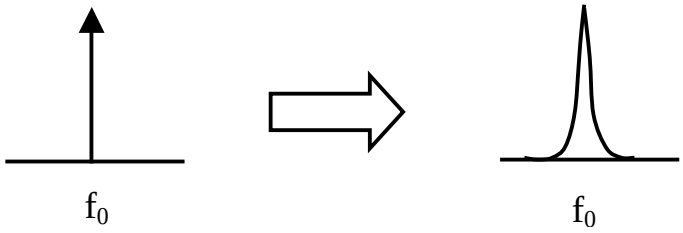


Figure 2.3 Spectrum of ideal and practical frequency synthesizer output

The ideal synthesizer output has a pure sinusoidal waveform

$$V(t) = A_0 \cos \omega_0 t \,, \tag{2.1}$$

where A_0 and ω_0 are nominal amplitude and angular frequency of the signal. When amplitude and phase fluctuations are included, the waveform becomes

$$V(t) = [A_0 + \varepsilon(t)]\cos[\omega_0 t + \phi(t)] \,, \tag{2.2}$$

where $\varepsilon(t)$ represents amplitude fluctuations and $\phi(t)$ represents phase fluctuations. Because amplitude fluctuations can be easily removed or greatly reduced by a limiter, we concentrate on phase fluctuations in a frequency synthesizer design. The $\phi(t)$ represents the random phase fluctuations. The spectral density of the phase fluctuations is

$$S_\phi(f) = \int_{-\infty}^{+\infty} R_\phi(\tau) e^{-j2\pi f\tau} d\tau \,, \tag{2.3}$$

where $R_\phi(\tau) = E[\phi(t)\phi(t-\tau)]$ is the auto-correlation function of the random phase changing process. When amplitude fluctuations are negligible and the root-mean-

square (RMS) value of $\phi(t)$ is much smaller than 1 radian, the frequency synthesizer output signal can be written as

$$V(t) = [A_0 + \varepsilon(t)]\cos[\omega_0 t + \phi(t)] \approx A_0 \cos[\omega_0 t + \phi(t)] \approx A_0 \cos[\omega_0 t] - A_0 \sin[\omega_0 t]\phi(t). \tag{2.4}$$

The spectral representation of $V(t)$ can be approximated as

$$S_V(f) = \frac{A_0^2}{2}\left[\delta(f - f_0) + S_\phi(f - f_0)\right], \tag{2.5}$$

where the first term represents our desired signal at nominal frequency f_0 and the second term represents the undesired noise components at frequency offset $\Delta f = f - f_0$.

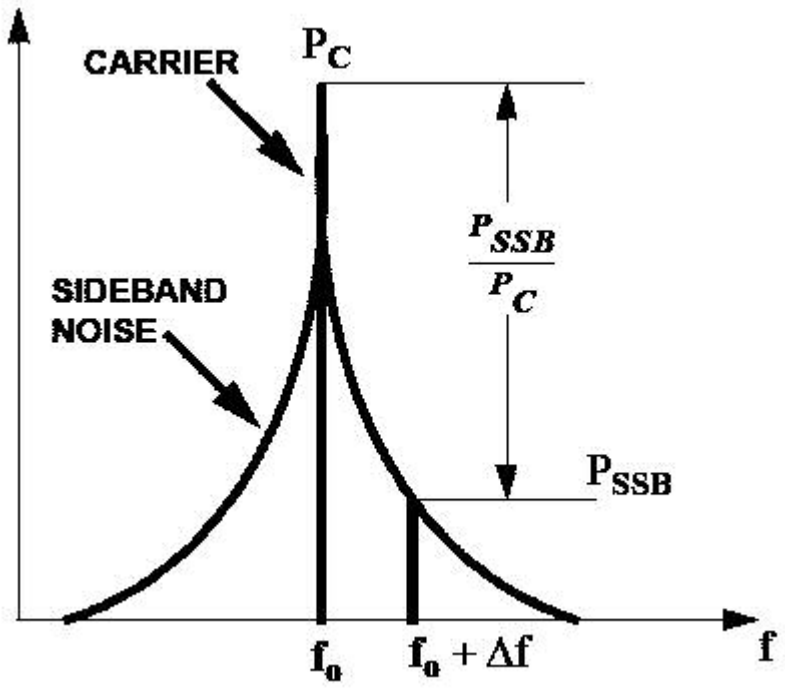


Figure 2.4 Definition of SSB phase noise

Phase noise is specified as the ratio of noise power in 1Hz bandwidth at a certain offset frequency from carrier to the carrier power [Bagh65], Figure 2.4. It is called

single side-band (SSB) phase noise and the unit is dBc/Hz. The SSB phase noise can be expressed as

$$L(\Delta f) = 10\log\frac{P_{SSB}(f_0 + \Delta f, 1Hz)}{P_{carrier}} \quad (dBc/Hz) \tag{2.6}$$

where $P_{SSB}(f_0 + \Delta f, 1Hz)$ is the noise power in 1Hz bandwidth at offset frequency Δf from carrier frequency f_0 and $P_{carrier}$ is the total carrier power.

2.2.2 Phase noise effect on receiver performance

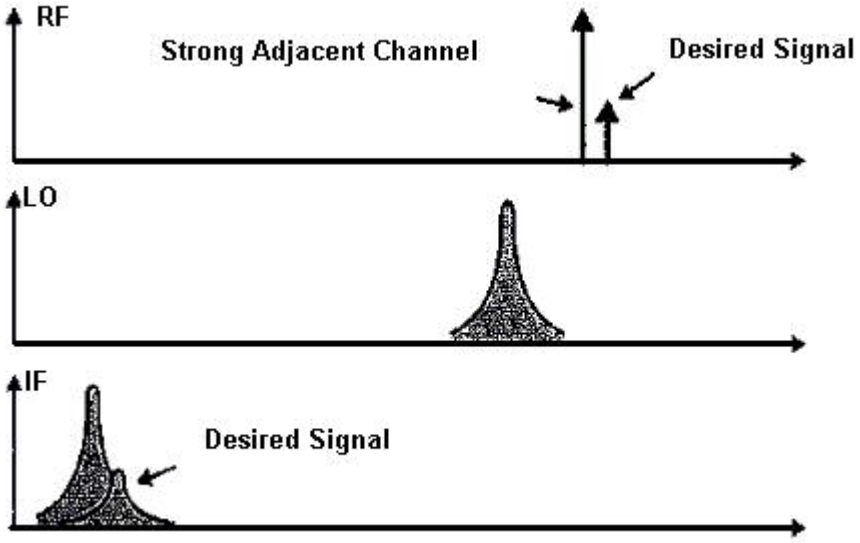


Figure 2.5 Reciprocal mixing effect on receiver performance

The phase noise has two independent impacts on the receiver front end's signal to noise ratio (SNR), hence bit error rate (BER). The first impairment is called **reciprocal mixing** [Raza96], coming out because of the presence of adjacent channel interference. To understand this impairment, consider the situation in Figure 2.5. The LO signal for down-conversion has a noisy spectrum as shown in Figure 2.3. The receiver sees two RF signals, one desired signal with small power level and one

interference signal at adjacent channel with large power level. The down-converted signal will consist of two overlapping spectra. The desired signal suffers from significant noise due to the tail of the interference signal.

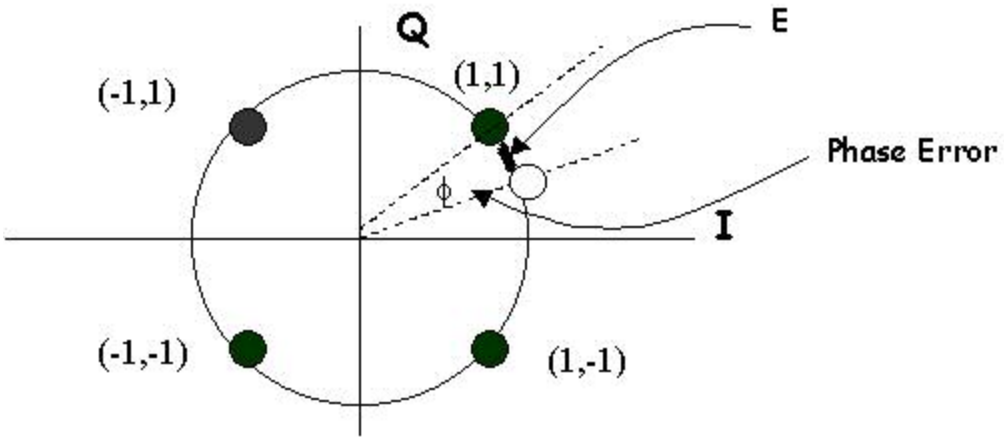


Figure 2.6 Phase impairment effect on QPSK signal demodulation

The second impact, called phase impairment [Leun02], is best understood in the phase domain. In the phase domain, the phase noise appears as phase error. Assume the frequency synthesizer is used to demodulate a phase-encoded signal, such as QPSK (Quadrature Phase Shifted Keying) signal. Figure 2.6 shows the constellation diagram of QPSK signal and the effect of phase noise on its demodulation. In the figure, the darkened circle at upper-right corner corresponds to the ideal signal for bits (1,1) if there is no phase error. Due to the phase noise of LO signal, the actual demodulated signal is the non-filled circle. The phase error between the ideal signal and the actual received signal is statistically distributed and typically modeled using Gaussian distribution with standard deviation equal to root-mean-square (RMS) phase error of the Local Oscillator. If the RMS phase error is large enough, it could cause

the signal to be mis-detected. Higher order modulation schemes, such as QAM16 and QAM64, have more compact constellation diagram than simple QPSK. They are more subject to Local Oscillator phase impairment effect.

The phase impairment effect is always there, with or without interference, whereas the reciprocal mixing effect is there only when there is adjacent channel interference. Which impact is more dominant depends mostly on the applications. Generally speaking, the reciprocal mixing is dominant in narrow band low data rate applications because of small channel spacing and simple modulation scheme, while the phase impairment effect is dominant in broad band high data rate applications because of large channel spacing and complex modulation scheme.

2.3 Architectures of frequency synthesizers

There are many ways to implement a frequency synthesizer. For an integrated radio transceiver, we want the synthesizer to be able to generate a tunable frequency in the gigahertz range with low phase noise using minimum power. A **direct digital frequency synthesizer** [Abid94] is best known for its fast switching and very fine frequency resolution. It can also easily be integrated because no off chip components are required. But due to technology limitations, it takes large power consumption to synthesize very high frequencies directly. A **phase-locked-loop-based indirect frequency synthesizer** [Egan81] is the most commonly used technique due to its high performance, namely, low phase noise and low power consumption. We will focus on PLL based frequency synthesizers in this dissertation.

2.4 Introduction to PLL based frequency synthesizers

2.4.1 What is PLL based frequency synthesizers?

A PLL based frequency synthesizer contains four basic components as shown below in Figure 2.7.

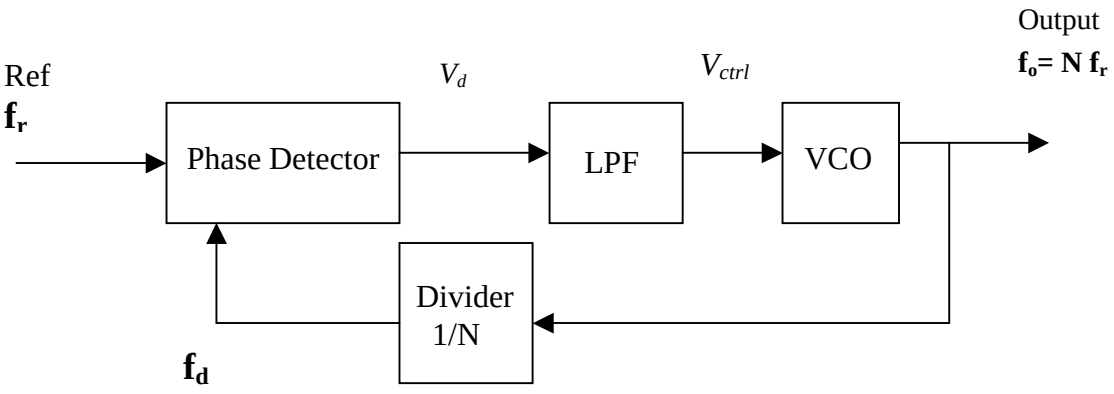


Figure 2.7 Typical PLL based frequency synthesizer block diagram

The Phase detector (PD) determines the difference between the phases of two signals and converts the difference to an error signal V_d. The loop filter (LPF) removes the high-frequency components from V_d and generates V_{ctl}, the voltage-controlled oscillator (VCO) controlling voltage. The VCO produces the output frequency. The frequency divider determines the ratio of the desired VCO frequency and the reference frequency.

A Phase-Locked-Loop locks the output phase or frequency to an accurate reference, which is usually implemented by a Crystal. When the loop is locked, the Phase Detector sees two in-phase waveforms f_r and f_d at its inputs and f_o equals to Nf_r. If for some reason $f_r > f_d$, Phase Detector generates positive V_d and V_{ctrl} goes up. So

the VCO output frequency increases. Vice versa, if $f_r < f_d$, V_{ctrl} goes down and the VCO output frequency decreases.

There are many different ways to implement the circuit blocks of a PLL. The PLLs can be roughly classified into two classes based on the implementation of phase detector, *i.e.* linear PLLs and digital PLLs. The linear PLLs (LPLL) use analog multiplier as phase detector. The digital PLLs use digital phase detectors such as EXOR gates, edge triggered JK flip flops, or tri-state phase-frequency detectors.

In a modern PLL, the phase detector is usually implemented by tri-state phase frequency detector combined with charge pump (PFD/CP). The PFD can detect both the phase and frequency difference between two signals. Consequently, the PFD/CP based PLL will have infinite pull-in range, irrespective of the type of loop filter used.

2.4.2 Linear model of PLL based frequency synthesizers

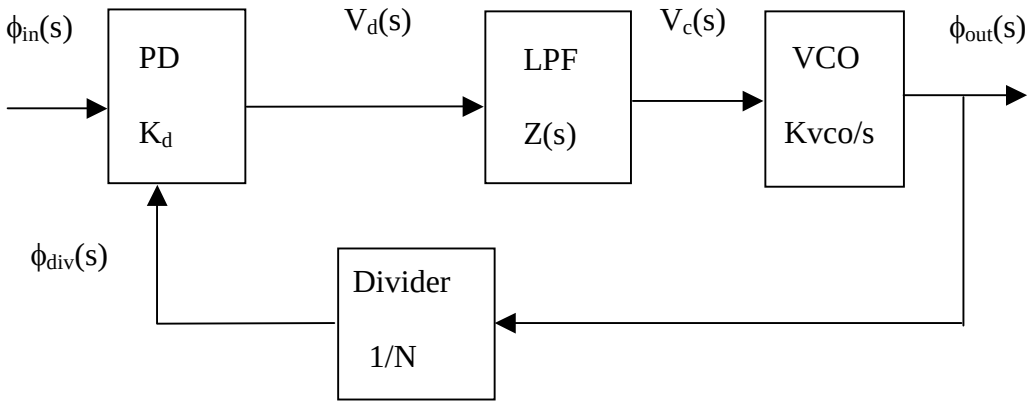


Figure 2.8 A linear model for PLL

Generally, a linearized model can be used to get more insight into the PLL design. Fig. 2.8 shows the linear model of a typical PLL. In the linear model, the PD has a gain of K_d (V/rads), the loop filter has a transfer function $Z(s)$, and the VCO has a

gain of *Kvco* (rads/sV). We use phase as the input and output variable in the model. Because phase is the integrated value of frequency, an integrator 1/*s* is included in the VCO block so that the VCO block has a gain of K_{vco} /s. The open loop transfer function *G(s)* can be written as

$$G(s) = K_d Z(s) \frac{K_{vco}}{s} \frac{1}{N} \tag{2.7}$$

Therefore the closed loop transfer function can be written as

$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = N \frac{G(s)}{1 + G(s)} \tag{2.8}$$

2.4.3 Type and order of PLL

The order of PLL is defined as the number of poles of the open loop transfer function G(s). The simplest PLL is a first order loop, in which loop filter is a simple gain block with gain K_p. Without loss of generality, let K_p equal to 1. The transfer function

$$G(s) = K_d \frac{K_{vco}}{s} \frac{1}{N} = \frac{K}{s}, \text{ where } K = \frac{K_d K_{vco}}{N} \tag{2.9}$$

$$H(s) = N \frac{G(s)}{1 + G(s)} = N \frac{K}{s + K} \tag{2.10}$$

The **loop bandwidth** ω_c is defined as the frequency where the open loop transfer function *G(s)* drops to unity. We can see that ω_c is always equal to the DC gain K for the first order PLL. The closed loop transfer function has only modest attenuation at the stop bands, *i.e.* -20dB/decade.

A simple RC based low pass filter creates a second order PLL if it is used as the loop filter. The loop filter transfer function Z(s) can be written as

$$Z(s) = \frac{1}{1 + sRC} = \frac{1}{1 + \frac{s}{\omega_{LPF}}} \tag{2.11}$$

Therefore the loop transfer function

$$G(s) = K_d Z(s) \frac{K_{vco}}{s} \frac{1}{N} = \frac{K\omega_{LPF}}{s^2 + \omega_{LPF} s}, \text{ where } K = \frac{K_d K_{vco}}{N} \tag{2.12}$$

$$H(s) = N \frac{G(s)}{1 + G(s)} = N \frac{K\omega_{LPF}}{s^2 + \omega_{LPF} s + K\omega_{LPF}} \tag{2.13}$$

The open loop transfer function G(s) has two poles, one at the origin and one at the loop filter 3dB cutoff frequency ω_{LPF} . The closed loop transfer function H(s) can be written as a familiar form that describes a second order feedback system

$$H(s) = N \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \tag{2.14}$$

$$\text{where} \quad \omega_n = \sqrt{K\omega_{LPF}} \;, \; \xi = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K}} .$$

ω_n and ζ are the natural frequency and damping factor of the system. The second order PLL gives us one more degree of freedom in setting the loop bandwidth. The loop bandwidth depends on both the DC gain K and the loop filter 3dB cutoff frequency ω_{LPF} . The closed loop transfer function has -40dB/decade attenuation at stop bands.

The first and second order PLL discussed above has only one pole at origin in their open loop transfer function G(s). The number of poles at origin in G(s) is defined as **the type of PLL**. The above PLLs are called type I PLL. One problem of the type I PLL based frequency synthesizers is their limited hold in and pull in range. **The hold in range** is the frequency range over which a PLL can statically maintain phase

tracking. **The pull-in range** is the range within which a PLL can get locked from unlocked state. These two parameters describe the PLL locking process. If the PLL is initially unlocked, the phase error, $\phi_e = \phi_{in} - \phi_{div}$, can take an arbitrarily large value and as a result, the linear model is no longer valid. The mathematics behind the unlocked state is beyond the scope of this dissertation. Please refer to [Gard79] for detail explanation.

The limited hold in and pull in range issue is solved in the type II PLL. The type II PLL has two poles at the origin in its open loop transfer function G(s). The type II PLL has infinite hold in and pull in range. The second pole at origin can be created by including an integrator in loop filter Z(s), which means we need an active loop filter for typical Phase Detector implementations. The active loop filters generate extra noise and consume more power. Another solution is to use a tri-state phase frequency detector (PFD) and charge pump. This charge pump based PLL (CPLL) can implement type II PLL using passive loop filter and is the most popular structure in modern PLL design. The CPLL will be discussed in next section.

2.4.4 Charge pump based PLL

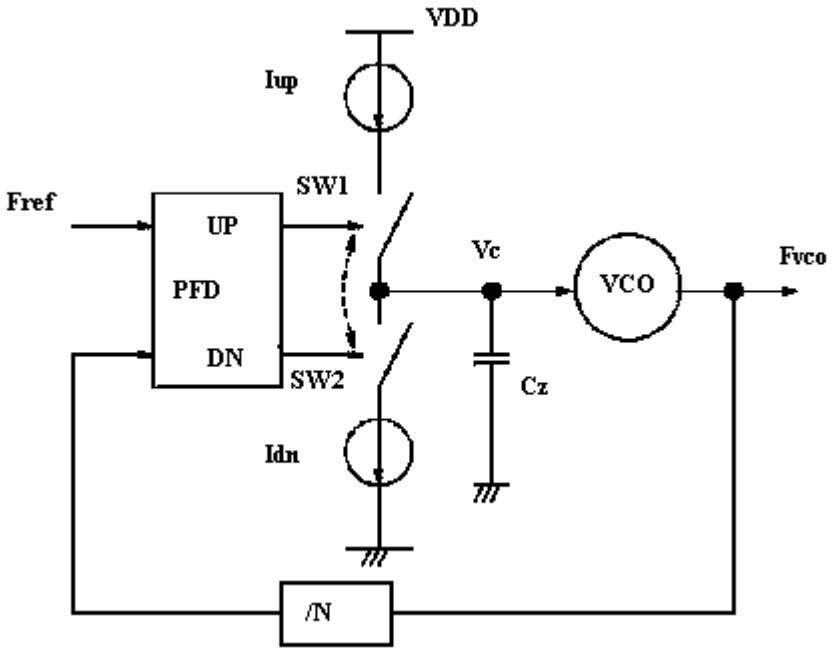


Figure 2.9 Block diagram of charge pump based PLL

Figure 2.9 shows a simplified charge pump based PLL (CPLL) block diagram. A phase frequency detector (PFD) is a digital phase detector having UP, DOWN, and high impedance, three states based on the phase and frequency relation of its input. A charge pump consists of two switched current sources which drive a combination of several resistors and capacitors to form a filter for the PLL with a pole at the origin. The switches of a charge pump are controlled by the PFD output signals UP and DOWN. Since the pulse width of the UP (DOWN) signal is proportional to the amount of phase error at the PFD input, the charge pump will charge (discharge) capacitor C_z accordingly while switch SW1 (SW2) is on. The VCO control voltage Vc is proportional to the integration of phase error ϕ_e and can be written as

$$V_c(s) = \frac{\phi_e I_{cp}}{2\pi} \frac{1}{sC_z}. \qquad (2.15)$$

The open loop transfer function G(s) becomes

$$G(s) = \frac{I_{cp}}{2\pi}\frac{1}{sC_z}\frac{K_{vco}}{s}\frac{1}{N} \tag{2.16}$$

This type II, second order loop is not stable since two poles are at the origin. To make the system stable, a zero is inserted by adding a resistor R_z in series with C_z as shown in Figure 2.10. Now the open loop transfer function G(s) becomes

$$G(s) = \frac{I_{cp}}{2\pi}\frac{1+sR_zC_z}{sC_z}\frac{K_{vco}}{s}\frac{1}{N}, \tag{2.17}$$

which contains a zero at $\omega_z = 1/R_zC_z$. In Figure 2.10, there is an additional capacitor C_p, which is commonly used to improve the stop band attenuation performance. The final open transfer function G(s) is

$$G(s) = \frac{I_{cp}K_{vco}}{2\pi N}\frac{1+sR_zC_z}{s^2(C_z+C_p)(1+sR_zC_1)}, \text{ where } C_1 = \left(\frac{1}{C_z}+\frac{1}{C_p}\right)^{-1}. \tag{2.18}$$

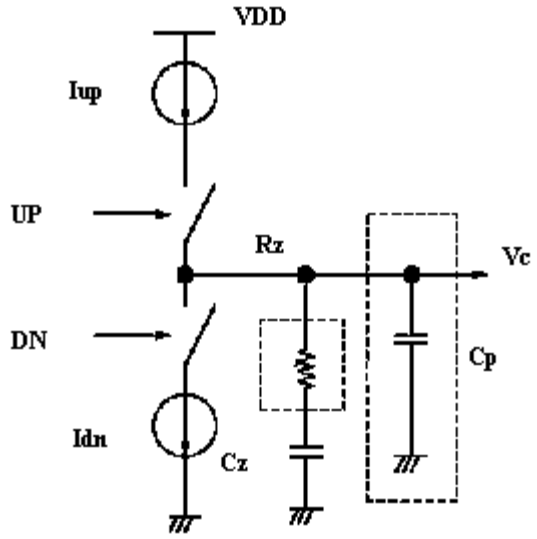


Figure 2.10 Loop filter with additional zero and pole

Figure 2.11 shows the Bode plot of a CPLL with the loop filter shown in Figure 2.10. This is a type II, third order loop with one zero at $\omega_z = 1/R_z C_z$ and one pole at $\omega_p = 1/R_z C_1$ in addition to two poles at the origin. To guarantee an enough phase margin, we usually place zero ω_z at α times below loop bandwidth ω_c and the third pole ω_p at β times above ω_c. The factors α and β are typically set to 3 ~ 4 to give a phase margin of approximately 45 ~ 60 degree. In the above case, it means $C_p << C_z$. The third pole $\omega_p = 1/R_z C_1 \approx 1/R_z C_p$. The loop bandwidth ω_c equals approximately

$$\omega_c \approx \frac{I_{cp} K_{vco} R_z}{2\pi N} \frac{C_z}{C_z + C_p} \approx \frac{I_{cp} K_{vco} R_z}{2\pi N}. \qquad (2.19)$$

This type II, third order CPLL is the most popular PLL architectures used in RF frequency synthesizers and is the focus of this dissertation. To improve further the stop band attenuation performance, it is possible to add the fourth pole in G(s) by

adding another resistor R_4 and capacitor C_4 in its loop filter, shown in Figure 2.12. The analysis of this type II, fourth order CPLL can be carried out similarly as above.

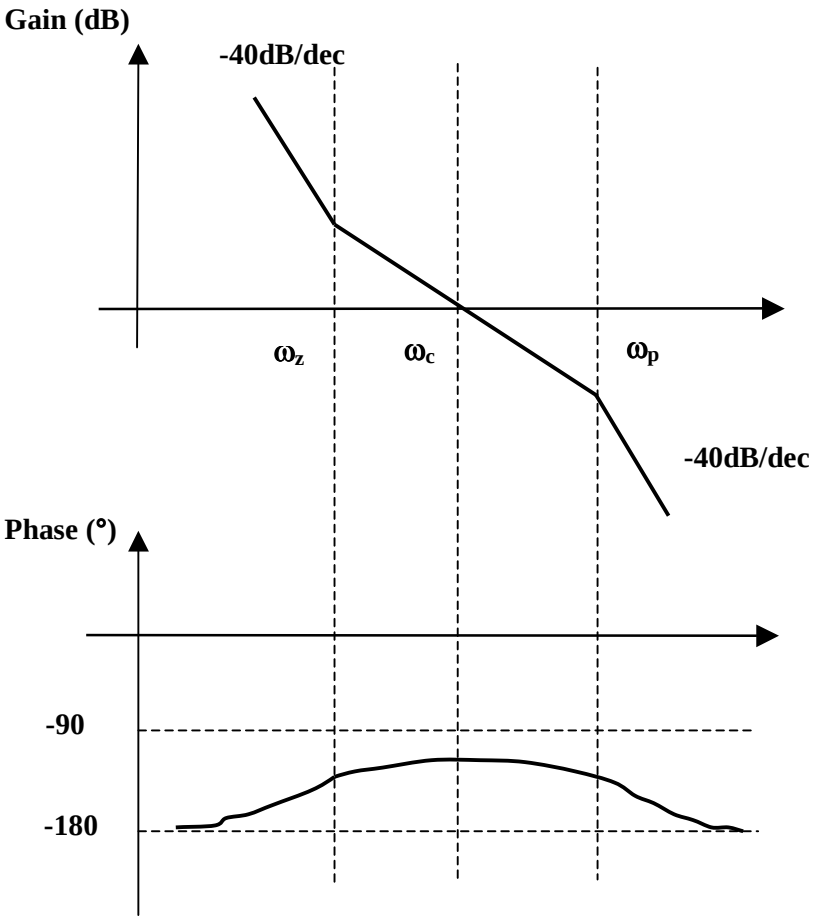


Figure 2.11 Bode plot of type II, third order PLL

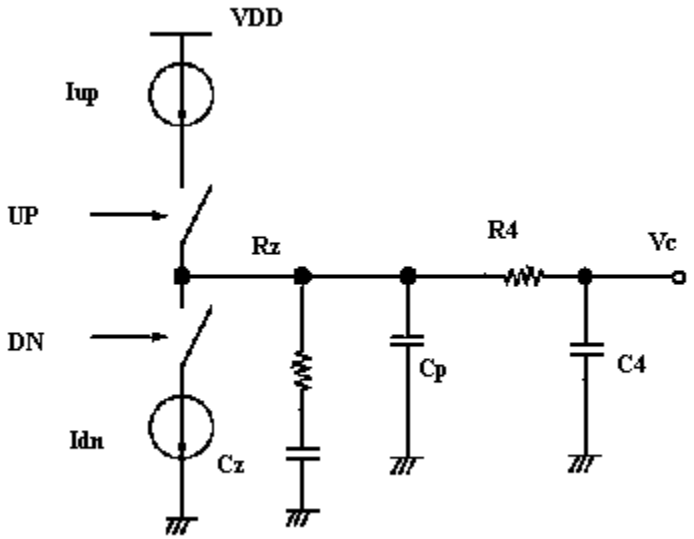


Figure 2.12 Loop filter with the fourth pole

2.5 Noise sources in PLL based frequency synthesizers

The focus of this dissertation is the phase noise performance of PLL based frequency synthesizers. The sources of phase noise within a PLL synthesizer include:

1. VCO phase noise
2. Reference oscillator phase noise
3. Noise from the PFD/CP and digital dividers
4. Noise from components in the loop filter

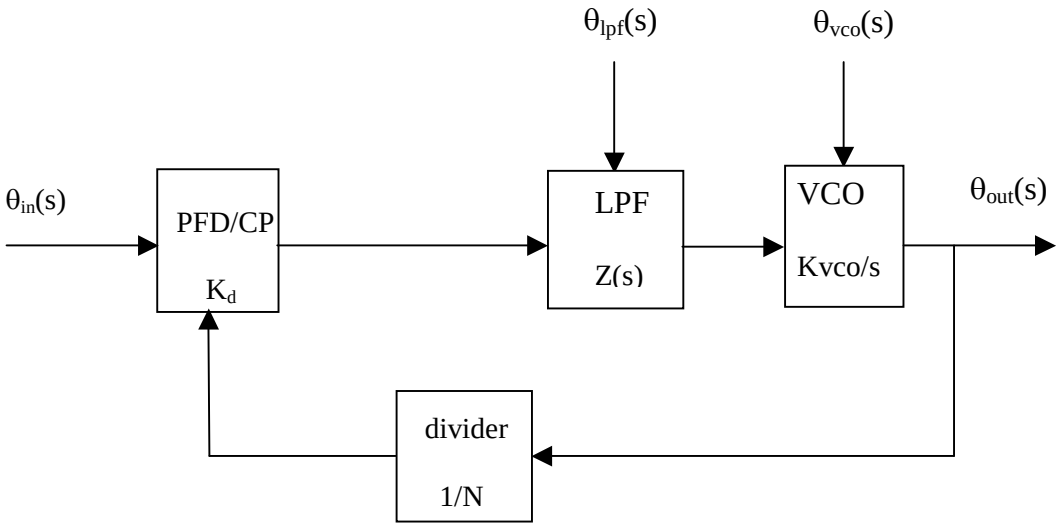


Figure 2.13 Noise sources in a PLL

These noise sources are grouped into three groups in Figure 2.13. Noise sources 2 and 3 are combined as one input phase noise $\theta_{in.}$ VCO phase noise is represented by θ_{vco} and loop filter phase noise is represented by $\theta_{lpf.}$ The three groups of noise sources experience different transfer functions to θ_{out}, as given in Table 2.1.

source	Transfer function
θ_{in}	$H_1(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = N\frac{G(s)}{1+G(s)}$
θ_{vco}	$H_2(s) = \frac{\theta_{out}(s)}{\theta_{vco}(s)} = \frac{1}{1+G(s)}$
θ_{lpf}	$H_3(s) = \frac{\theta_{out}(s)}{\theta_{lpf}(s)} = \frac{K_{vco}}{s}\frac{G(s)}{1+G(s)}$

Table 2.1 Noise transfer functions in a PLL

Notice that the transfer function for θ_{in} is a low-pass function with a gain of N at frequencies below the loop bandwidth. This means the noise contribution from the reference, PFD/CP, and divider is referred to the output enhanced in effect by *N* at low offset frequencies from the carrier, and suppressed at high offset frequencies from the carrier. The transfer function from the VCO to the synthesizer output is a high-pass function. It means the lower-frequency part of the noise from the VCO can be corrected by the relatively fast PLL. But for the higher-frequency part of the noise from VCO, the loop is not fast enough and is essentially an open loop. The response from the loop filter noise to the output depends on the loop filter. For example, the 3rd-order PLL has a loop filter with one zero and two poles, which gives the above transfer function a band-pass characteristics.

Among these noise sources, the dominant ones are VCO and PFD/CP/Divider. Also they are more difficult to predict in design because they are usually implemented on chip. The reference and loop filter are usually made from off-chip discrete components and can be modeled with good accuracy using measured phase noise data for the reference, and conventional noise models from circuit theory for the loop filter. The noise transfer functions from PFD/CP/Divider and VCO to the output are shown in Figure 2.14.

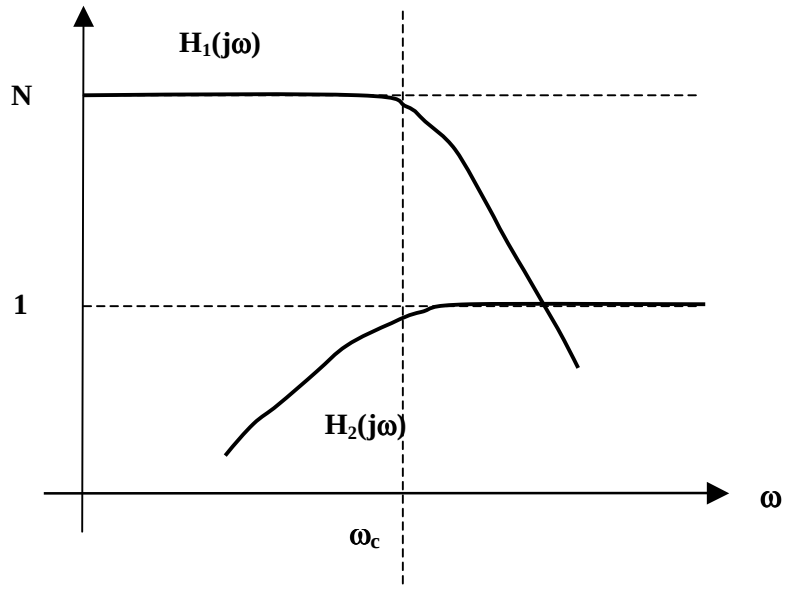


Figure 2.14 Noise transfer function for PFD/CP/Divider (H_1) and VCO (H_2)

2.6 Closed loop PLL output phase noise spectrum

The Noise sources described in section 2.5 experience different transfer functions and are combined at the PLL output. Figure 2.15 shows a typical frequency synthesizer output spectrum. Here we consider only the white noise dominated VCO and PFD/CP/Divider noise. In white noise dominated region, free running VCO phase noise has a –20dB/decade slope and PFD/CP/Divider noise is flat respected to frequency offset. After shaping by their respective transfer function, we can see there are two distinct regions in the output total phase noise spectrum. In the region where offset frequency is smaller than loop bandwidth, the phase noise flattens out as an in band phase noise floor. This noise floor is dominated by PFD/CP/Divider because VCO phase noise is suppressed in this region. In the region where offset frequency is larger than loop bandwidth, the phase noise declines in the slope of about -

20dB/decade. The phase noise in this region is dominated by VCO because PFD/CP/Divider noise is suppressed.

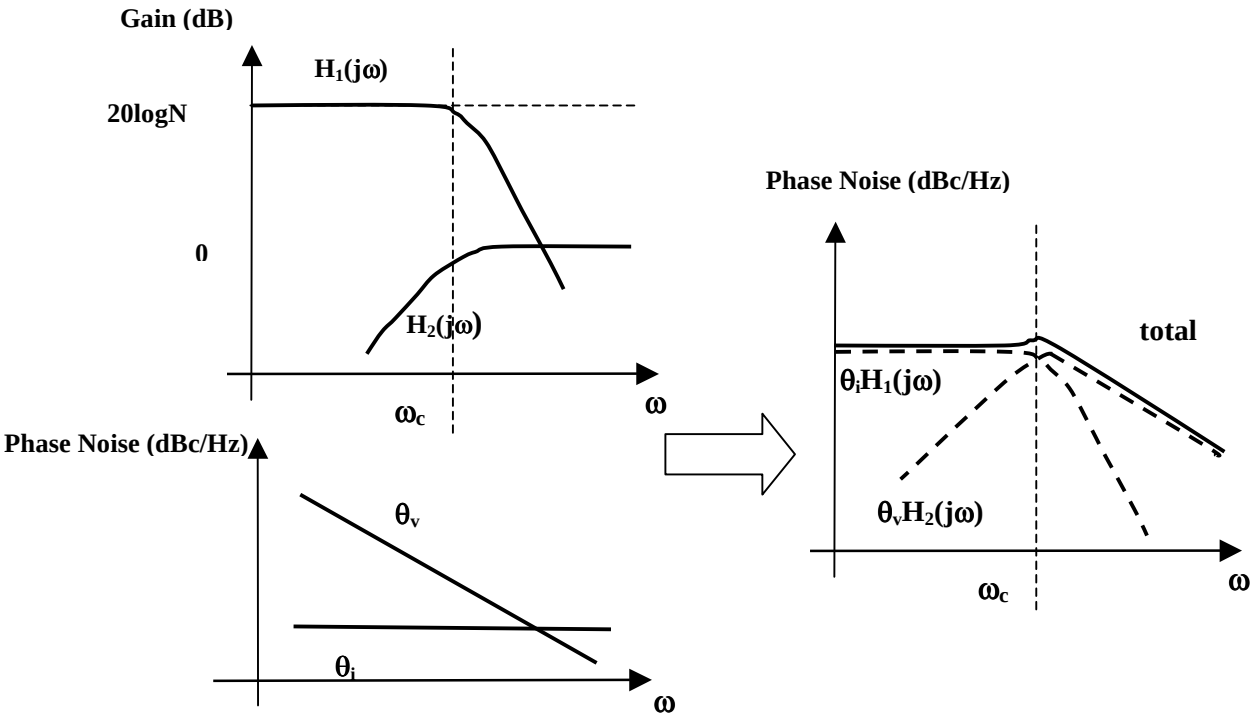


Figure 2.15 PLL output phase noise spectrum

One measure to characterize the PLL output phase noise spectrum is the integrated Root Mean Squared (RMS) phase error. Its definition is

$$\Delta\phi = \frac{180}{\pi}\sqrt{2\int_a^b L(f)df}\ , \tag{2.20}$$

where $\Delta\phi$ is the RMS phase error in degrees and $L(f)$ is the phase noise in dBc/Hz at frequency offset f. a and b are integration limits. Usually a is very close to carrier and b is selected to be the same as channel bandwidth. This RMS phase error degrades SNR in the following manner

$$SNR = \left(\frac{180}{\pi \bullet \Delta\phi}\right)^2. \tag{2.21}$$

The RMS phase error depends on the phase noise levels in the two distinct regions and the overall phase noise spectrum shape. To reduce this RMS phase error, we must

1. Reduce the out of band region phase noise,
2. Reduce the in band phase noise floor,
3. Optimize the phase noise spectrum shape to get the minimal integration value.

The items 1 and 2 are the focus of this dissertation and will be discussed in detail in the following two chapters. The item 3 is belong to the system level and will be discussed in the experimental prototype design in Chapter 5.

Chapter 3: Design Techniques for Low Phase Noise VCOs

VCO are key components in RF frequency synthesizers. It determines the out of band phase noise performance. The most popular integrated RF VCO architecture is a cross-coupled inductor-capacitor (LC) tank CMOS oscillator due to its relatively low phase noise, ease of implementation and differential operation. The implementation of the cross-coupled LC VCO has received lots of attention in recent years as evidenced by the large number of publications reporting improved phase noise performance [Cran97, Muer00] and higher operating frequency [Leva02, Tang02]. However lacking a clear understanding of the physical mechanism of phase noise generation in these VCOs is still a bottleneck for the circuit designer [Rael00]. This chapter will first briefly review the basics of oscillators in section 3.1. Then some popular CMOS cross-coupled LC VCO topologies are introduced in section 3.2. Section 3.3 presents two previous VCO phase noise models. Next a generalized linear phase noise model based on physical mechanism of phase noise is proposed and a closed form phase noise formula for LC cross-coupled VCO is derived in section 3.4. In section 3.5, a 2GHz VCO design example is described and the simulation and measurement results are compared to the theory prediction.

3.1 Introduction to oscillators

3.1.1 Feedback modeling and oscillation conditions

All oscillators can be analyzed by modeling them as feedback systems. Figure 3.1 shows a general block diagram of a linear feedback system with forward and feedback transfer functions represented by H(jω) and β(jω) respectively. The transfer function Y_{out} / X_{in} of the linear systems in Figure 3.1 is the general equation for a feedback system

$$\frac{Y_{out}(j\omega)}{X_{in}(j\omega)} = \frac{H(j\omega)}{1 + H(j\omega)\beta(j\omega)} \tag{3.1}$$

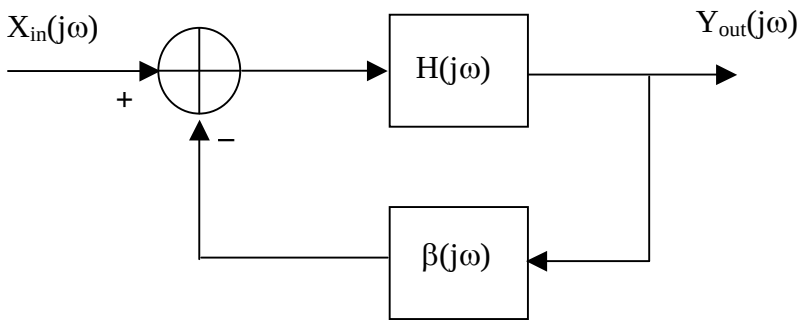


Figure 3.1 A linear feedback model for oscillators

The necessary conditions for steady state oscillation to occur are known as the Barkhausen criteria. These conditions require that the gain around the feedback loop equal to unity and the total phase shift around the loop equal to (2*m*+1) times 180 degrees where *m* is an integer value including zero. The gain and phase conditions are expressed as

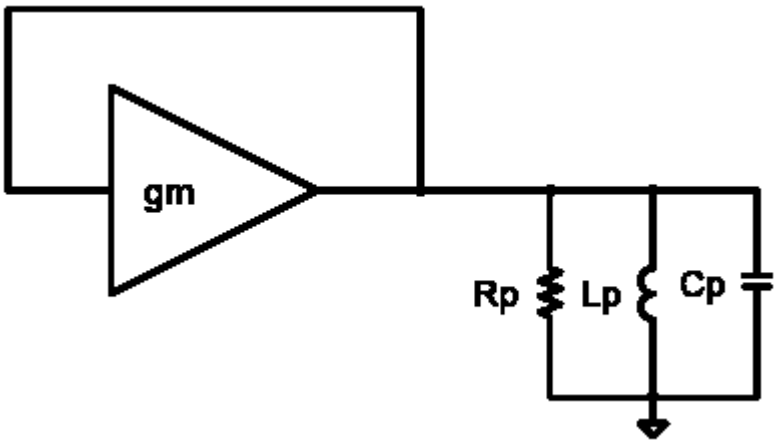
$$\left|H(j\omega)\beta(j\omega)\right| = 1, \tag{3.2}$$

and

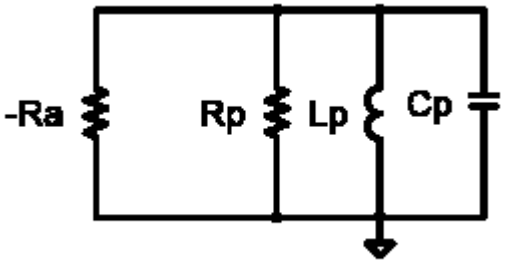
$$\angle H(j\omega)\beta(j\omega) = (2m+1)\bullet 180^{\circ}. \qquad (3.3)$$

When these conditions are satisfied, a signal at the input of the gain stage will be amplified and returned back to the input in phase resulting in a self-sustaining signal. This feedback loop viewpoint has been especially useful in describing the operation of traditional oscillators (based on single active devices) such as the Colpitts, Hartley, and Pierce oscillators, *etc*.

3.1.2 Negative resistance modeling



(a)



(b)

Figure 3.2 A negative resistance model for LC oscillators

An alternate way to describe the operation of oscillators involves the concept of negative resistance, Figure 3.2. Negative resistance modeling can be regarded as a special case of feedback modeling. Figure 3.2 shows a model of a simple negative resistance LC oscillator. In this figure the active device is a simple transconductance amplifier connected in positive feedback and is connected to a LC tank circuit. It is straightforward to show that the tank circuit sees a negative resistance of $-R_a = -\frac{1}{g_m}$ looking back into the transconductor output. It can be shown that this negative resistance will exactly cancel the equivalent parallel resistance of the tank circuit if the Barkhausen criteria are satisfied. The steady state oscillation condition for the negative registance model is expressed as

$$-R_a + R_p = 0 \tag{3.4}$$

This makes sense because the active device must add enough energy to the circuit to cancel the total losses of the tank circuit.

Negative resistance oscillators have the property that they continue to generate a negative resistance even when the tank circuit is removed. On the other hand, removing the tank circuit from a feedback oscillator breaks the feedback loop that creates the negative resistance and a negative resistance cannot be measured. Although both representations are equivalent, the negative resistance viewpoint will be utilized for the oscillator analyses of this dissertation.

3.1.3 Oscillator start-up conditions and amplitude stabilization

The previous two subsections discussed linear oscillator models and steady state oscillation conditions. In real oscillators, the analysis of the nonlinear effects can not

be done using small signal model. We first look at the oscillator start-up conditions using negative resistance model. In order for the circuit of Figure 3.2 to oscillate, the magnitude of the negative resistance Ra must be smaller than the parallel resistance of the tank circuit Rp. In other words, the transconductance g_m must be larger than the tank loss 1/Rp. The ratio of transconductance g_m to the equivalent LC tank conductance 1/Rp is referred to as the startup safety factor

$$\alpha = \frac{g_m}{1/R_p} = g_m R_p . \tag{3.5}$$

Integrated oscillators are usually designed with a startup safety factor of at least 2. When this start-up condition is met, the oscillator output will be an exponentially growing sine wave according to the small signal linear model.

It should be noted that the excess negative resistance for start-up does not result in an exponentially growing oscillation amplitude since nonlinear effects ultimately limit the maximum voltage swing. To help understand the non-linear amplitude stabilization effect, we assume the transconductor g_m in Figure 3.2 has the following nonlinear relationship to voltage

. $$I_{out} = g_m V - bV^3 . \tag{3.6}$$

This is referred as "Van Der Pol" oscillator [Pol20]. The simplified form of this non-linearity allows us to get a closed form solution for the steady state peak voltage

$$V_{peak} = \sqrt{\frac{4}{3}\frac{\alpha - 1}{bR_p}} , \tag{3.7}$$

where $\alpha = g_m R_p$ is the startup safety factor. The startup process works as following. When the signal level is small, the system has two right-hand plane poles and its time

response is a growing sine wave. The increase of the signal level will reduce the effective negative transconductance due to the non-linear effect. Eventually the effective negative transconductance reduces to a value which exactly cancels 1/Rp and we get a steady state oscillation level in the time domain.

3.2 CMOS cross-coupled LC oscillator topologies

It is possible to implement an oscillator in CMOS technology using single active devices in traditional topologies such as the Hartley or Colpitts. However, most recent implementations of CMOS LC oscillators have utilized a differential topology. Differential topologies are advantageous in integrated circuits, since they are less susceptible to supply voltage noise that is often present in on-chip power rails. Furthermore, many integrated RF systems would benefit from the use of a differential local oscillator (LO) since typical integrated mixers are double-balanced Gilbert Cell topologies. In these cases, the use of a differential oscillator eliminates the need for single-ended to differential conversion circuitry.

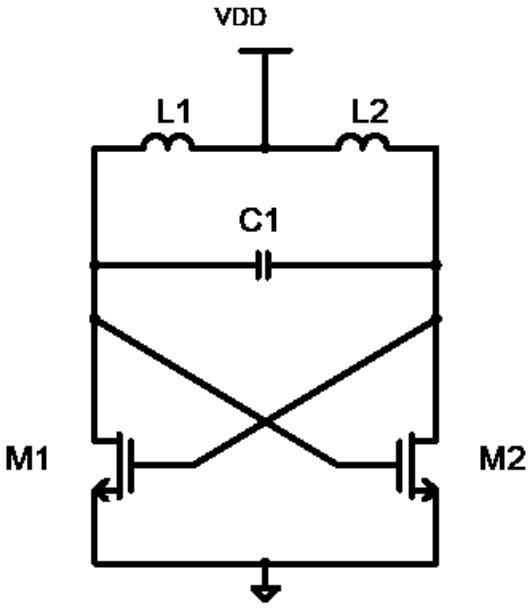


Figure 3.3 A simple NMOS cross-coupled LC oscillator

The most popular differential oscillator topologies are the cross-coupled LC oscillators, Figure 3.3, which utilize two cross-coupled transconductors (FETs) to produce a negative resistance similar to the transconductor of Figure 3.2.

The DC analysis of this circuit is simple since the inductors can be replaced by short circuits. The DC bias point is determined by $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}$. Assuming the cross coupled NMOS devices to be long channel FETs (for conceptual purposes only, short channel devices are actually used in the actual high frequency oscillator design), and neglecting the body effect, the drain current can be written as:

$$I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2, \tag{3.8}$$

where μ_n is the surface mobility of the electrons in the NMOS channel, C_{ox} is the oxide capacitance per unit area, and V_{th} is the device threshold voltage. The transconductance of one FET at this balance state is

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{GS}=V_{DS}=V_{DD}} = \mu_n C_{ox}(V_{DD} - V_{th)} \tag{3.9}$$

The input resistance seen looking into the cross-coupled NMOS transistors can therefore be shown to be $-\frac{2}{g_m}$. In order for the circuit of Figure 3.3 to oscillate, the magnitude of this negative resistance must be smaller than the equivalent parallel resistance of the tank circuit.

In the simple NMOS cross-coupled LC oscillator in Figure 3.3, the DC bias is set by the supply voltage and the size of the devices since V_{GS} and V_{DS} are both equal to V_{DD}. This severely limits the flexibility of the circuit since the negative resistance is effectively controlled by the power supply voltage. Varying the negative resistance will also vary the oscillation amplitude. This is an important fact since the phase noise performance (discussed in the next section) depends directly on the oscillation amplitude. For these reasons, it is desirable to have a means of controlling the negative resistance. This can be achieved by limiting the supply current. Figures 3.4 shows the NMOS versions of this circuit with a FET current mirror that is used to control the bias current, and therefore the negative resistance of the circuit. The bias current that flows through the mirror device is referred to as the tail current. The value of this tail current also sets the total power dissipation of the oscillator. Having a means of controlling the bias current allows the designer to make the best compromise between phase noise and power dissipation. Figure 3.4 also features two varactors instead of fixed capacitors to achieve voltage controlled frequency tuning function.

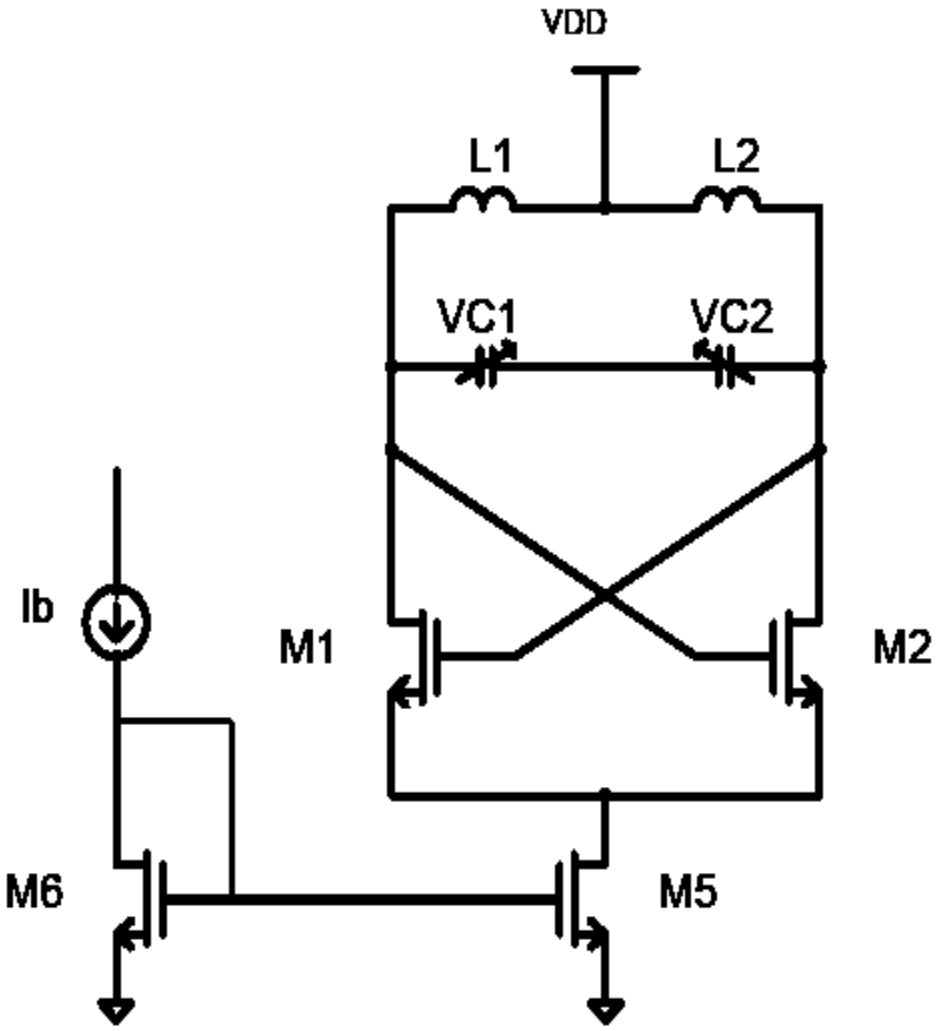


Figure 3.4 NMOS cross-coupled pair LC VCO with tail current

The N-PMOS complementary cross-coupled LC oscillator circuit is the result of using both PMOS and NMOS cross coupled pairs in parallel to generate the negative resistance. Figure 3.5 shows a simple complementary cross-coupled LC VCO. Since the same bias current flows through both the PMOS and NMOS devices, the negative resistance can be twice as large for the same power consumption. Viewing the negative resistance generated by the PMOS and NMOS devices in the same manner as discussed above, the total negative resistance of this circuit is the parallel

combination of the two individual cross-coupled FET circuits. The negative resistance is given by

$$R_{negative} = -\frac{2}{g_{mn} + g_{mp}}. \tag{3.10}$$

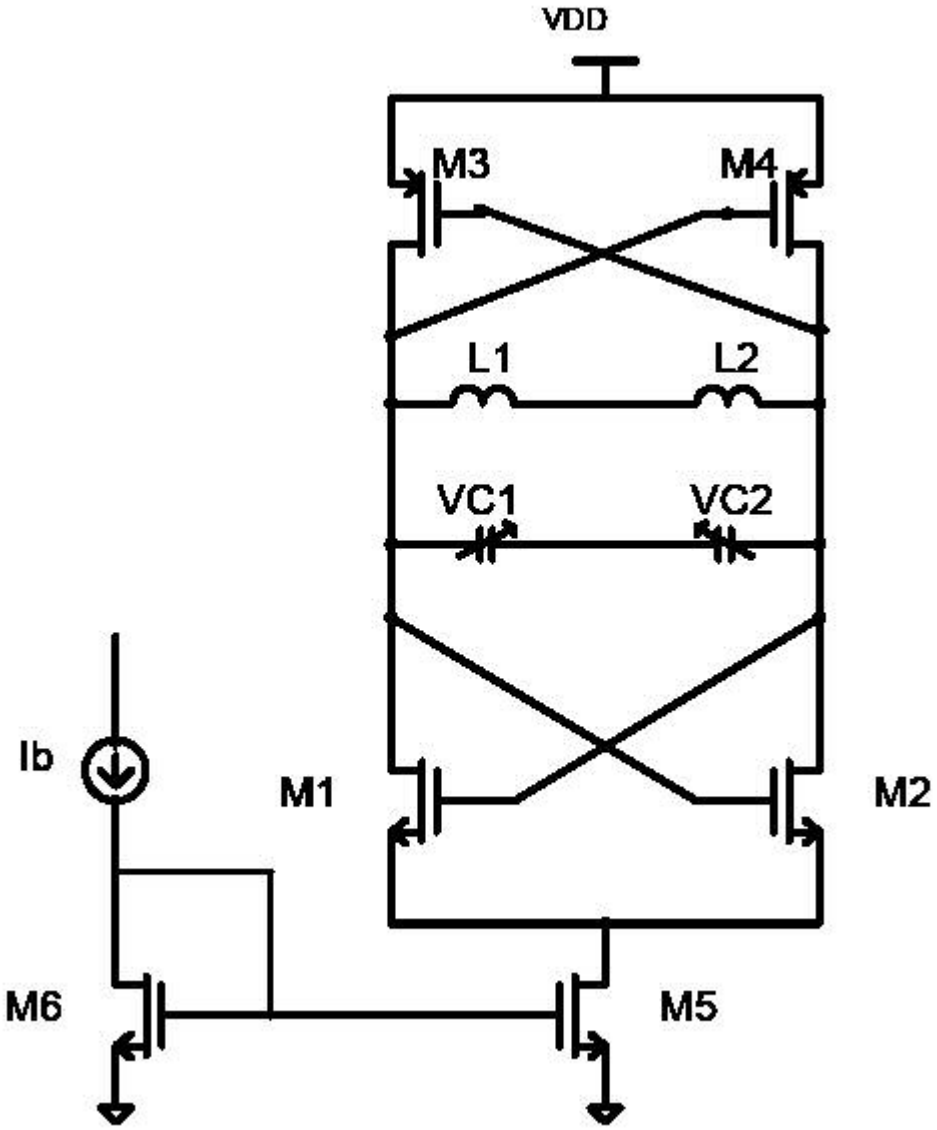
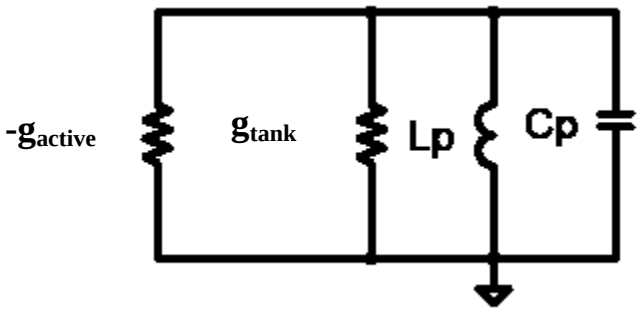


Figure 3.5 N-PMOS complementary cross-coupled pair LC VCO with tail current

This complementary pair topology has some advantages: (i) It gives doubled output amplitude if both topologies work in current-limited region at the same bias current; (ii) It can be optimized to have more symmetric output waveforms leading to smaller 1/f noise up-conversion [Haji99]. We will analyze and optimize the phase noise performance of this topology in the following sections.



3.3 Related work on LC VCO phase noise model

Figure 3.6 Equivalent circuits of cross-coupled LC VCO

Leeson's model: The first and still widely used VCO phase noise model is Leeson's linear model [Lees66]. It will be beneficial to briefly derive the linear noise model for cross-coupled LC tank VCO. We redraw the negative model in Figure 3.6 using conductance representation. In Figure 3.6, g_{tank} models the loss of the LC tank due to inductor and varactor parasitics and g_{active} models the negative conductance provided by the cross-coupled N-PMOS pair. We now can get the impedance of the LC tank at some small frequency displacement $\Delta\omega$ from center frequency ω_0 expressed as

$$Z(\omega_0 + \Delta\omega) = \frac{1}{g_{\tan k} + \frac{1}{j(\omega_0 + \Delta\omega)L)} + j(\omega_0 + \Delta\omega)C}$$
$$\approx j\frac{\omega_0 L}{2\Delta\omega/\omega_0} = jR_p\frac{\omega_0}{2Q\Delta\omega}, \tag{3.11}$$

where Q is the quality factor of the LC tank while $R_p=1/g_{tank}$ is the total equivalent parallel resistance of the LC tank. The PSD (Power Spectrum Density) of current noise due to tank loss can be written as

$$i_n^{\,2}/\Delta f = 4kT/R_p, \tag{3.12}$$

where *T* is the temperature while *k* is Boltzemann's constant. The phase noise due to tank thermal noise is

$$L(\Delta\omega) = \frac{1}{2}\left(\frac{\overline{v}^{2}_{noise}}{\overline{v}^{2}_{signal}}\right) = \frac{1}{2}\left(\frac{\left|Z(\omega_0 + \Delta\omega\right|^2 i_n^{\,2}/\Delta f}{V_0^2/2}\right)$$
$$= \frac{kTR_p}{V_0^2}\left(\frac{\omega_0}{Q\Delta\omega}\right)^2. \tag{3.13}$$

V_0 is the differential output voltage peak amplitude and depends on bias current. For N-PMOS complementary cross-coupled LC oscillator, $V_0=4/\pi I_{bias}R_p$ [Haji99]. The ½ before the parentheses in the derivation is based on the equal partition of the AM and PM noise. We are interested in phase noise (PM) only. To include the noise contribution of the active devices, Leeson introduced a heuristic parameter F. Total phase noise can be written as follows [Lees66],

$$L(\Delta\omega) = \frac{kTR_{eff}(1+F)}{V_0^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2. \tag{3.14}$$

$R_{eff} = R_p/Q^2$ is the total equivalent series resistance of the LC tank.

Hajimiri's model: Leeson's model is based linear time invariant analysis. But the oscillator is an autonomous non-linear circuit and the non-linearity and time variant is essential for its operation. Hajimiri's model [Haji98] first introduces a special function: **Impulse Sensitive Function** (**ISF**) which describes how much phase shift results from applying a unit impulse at any point in time, such that phase shift response to a unit impulse is expressed as

$$h_{\Phi}(t,\tau) = \frac{\Gamma(\omega_0 t)}{q_{\max}} u(t-\tau), \tag{3.15}$$

where $\Gamma(\omega_0 t)$ is the **ISF** function of the output waveform which represents the time-varying sensitivity of the oscillator's phase to perturbations and q_{max} is the maximum charge offset across the capacitor. The total excess phase due to a noise current can therefore be described by the expression:

$$\theta(t) = \int_{-\infty}^{+\infty} h_{\Phi}(t,\iota) i(\iota) d\iota = \int_{-\infty}^{t} \frac{\Gamma(\omega_0 \iota)}{q_{\max}} i(\iota) d\iota . \tag{3.16}$$

Then using phase modulation approach to convert phase to voltage and get the side band phase noise as follows:

$$L\{\Delta\omega\} = 10 \cdot \log\left(\frac{\dfrac{\overline{i_n^2}}{\Delta f} \sum_{n=0}^{+\infty} c_n^2}{8 q_{\max}^2 \Delta\omega^2} \right), \tag{3.17}$$

where $\overline{i_n^2} / \Delta f$ is the power spectral density of input noise current. c_n is the coefficient of Fourier transform of ISF function. $\Delta\omega$ is the frequency offset from carrier frequency.

3.4 A generalized linear phase noise model

The understanding of the phase noise mechanism and an appropriate phase noise model is very important in the design and optimization of cross-coupled pair LC VCOs. Various attempts for phase noise analysis have resulted in several phase noise models as discussed in section 3.3. But lacking of physical insight and simple yet accurate analysis makes these models difficult to use in the design.

The Leeson's model is based on a linear model of LC resonator. It correctly models the phase noise due to LC tank. But the noise factor F is empirical and the model does not give ways to predict it from circuit parameter. Without the knowledge of this noise factor, we can not use Leeson's model to optimize VCO phase noise performance. The Hajimiri's model uses linear time variant analysis to include noise due to active devices and the effect of non-linearity. It is inherently more accurate. But we need to calculate the ISF function for every noise source. These ISF functions are too complicated to get from hand calculation. Moreover, to include the effect of periodic varying noise sources, the Noise Modulation Function (NMF) is introduced [Apar02]. The NMF functions are also hard to get analytically. So in practice these ISF and NMF functions can only be gotten by simulation. Hence the Hajimiri's model is mostly simulation based and suitable more for verification than for design.

The difficulty of VCO phase noise analysis comes mostly from: (i) all oscillators are inherently nonlinear and traditional linear analysis is invalid; (ii) time variant of phase noise sensitivity to noise source; (iii) cyclostationary noise sources due to devices switching on and off. The general non-linear time variant analysis is too involved to be used in the design hand calculation. So in this dissertation, we propose

a generalized linear phase noise model [Kong03, Kong04-1]. The model combined linear small signal analysis and non-linear large signal concept. It is possible to predict the phase noise performance using the proposed model from circuit parameters known to designer.

3.4.1 Phasor representation of AM and PM noise

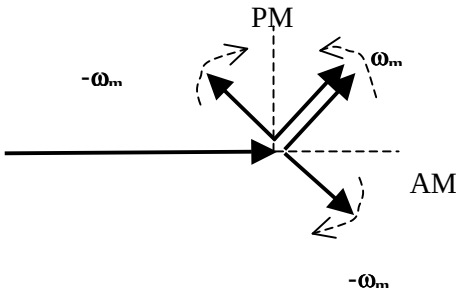


Figure 3.7 Phasor Representation of AM and PM noise

We can represent a perfect oscillation signal as a vector $\mathbf{V_0}$ rotating at frequency ω_0. In time domain, it is written as $V_0(t) = A_0 \cos \omega_0 t$. The noise produces amplitude and phase fluctuations when superimposed on the perfect oscillator signal. As shown in Figure 3.7, at frequency offset ω_m and $-\omega_m$, there are two noisy vector $\mathbf{V_m}$ and $\mathbf{V_{-m}}$ rotating relative to $\mathbf{V_0}$. It clearly shows that when the two vectors are in negative phase they produce AM (Amplitude Modulation) noise only while when the two vectors are anti-phase they produce PM (Phase Modulation) noise only. In time domain, the two cases are written as

1.AM noise

$$\begin{aligned} V_m(t) + V_{-m}(t) &= A_m \cos((\omega_0 + \omega_m)t + \phi) + A_m \cos((\omega_0 - \omega_m)t - \phi) \\ &= (2A_m \cos(\omega_m t + \phi)) \cos \omega_0 t. \end{aligned} \tag{3.18}$$

2. PM noise

$$V_m(t) + V_{-m}(t) = A_m \cos((\omega_0 + \omega_m)t + \phi) + A_m \cos[(\omega_0 - \omega_m)t + \pi - \phi] \\ = -(2A_m \sin(\omega_m t + \phi)) \sin \omega_0 t. \quad (3.19)$$

As can be seen later, this representation is especially useful in the analysis of biasing current source noise contribution.

3.4.2 Phase noise from LC tank

Phase noise from LC tank has been derived by Leeson's linear model as follows,

$$L(\Delta\omega) = \frac{kTR_{eff}}{V_0^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \quad (3.20)$$

$R_{eff} = R_p/Q^2$ is the total equivalent series resistance of the LC tank.

3.4.3 Phase noise from cross-coupled pair

Thermal noise of cross-coupled MOSFET's may significantly contribute to the output phase noise and must be modeled. In Leeson's model, it is represented as a fitting factor F. Our aim here is to derive its analytic expression represented by circuit parameters.

One popular method [Cran98, Ham01], though having no theory basis, is to evaluate the cross-coupled MOS current noise PSD at the completely balanced time (i.e., the zero-crossing of the differential tank voltage). We will first look at this method briefly. Suppose the transconductance of one side of MOS transistor is g_m. The differential total transconductance will be $g_m/2$. To ensure stable startup, $g_m/2$ is often designed greater than $1/R_p$. Let i_{n1} and i_{n2} be the current noise of the left and right MOSFET in cross-coupled pair. Their PSD will be

$$i_{n1}^2/\Delta f = i_{n2}^2/\Delta f = 4kT\gamma g_m.$$

γ is a device noise parameter depending on technology. For long channel device, γ=2/3. For short channel device, γ=2~5. Assume the two current noise sources are un-correlated, the total current noise PSD across the different LC tank is

$$i_n^2/\Delta f = \frac{1}{4}\left(i_{n1}^2/\Delta f + i_{n2}^2/\Delta f\right) = \frac{1}{2}4kT\gamma g_m = \frac{4kT\gamma\alpha}{R_p}. \quad (3.21)$$

Here we let $g_m/2=\alpha(1/R_p)$. Usually α is chosen between 3~5.

Since these noise current sources have the same effect as the noise source of the LC tank, the same transfer function can be used to obtain the output noise due to the active devices as

$$L\{\Delta\omega\} = kT\frac{R_p\gamma\alpha}{V_0^2}\left(\frac{\omega_o}{Q\Delta\omega}\right)^2. \quad (3.22)$$

It means that in Leesons' model the F factor due to cross-coupled pair will be F=$\gamma\alpha$. It is concluded from this analysis that using larger devices for cross-coupled pair will result in larger excess noise factor and will increase phase noise at a given bias current.

The drawback of this analysis is that it neglects the fact that the cross-coupled pair is always switching. The biasing point of the devices changes periodically with time. So the current noise PSD of cross-coupled pair has periodically time-varying statistics. It is not appropriate to model it as a stationary noise source. Fortunately, it can be shown that if the biasing point is changing with time, the resulting channel thermal noise is still white, with a time-varying PSD given by the same equation as for the time-invariant case if we replace the fixed transconductance with the time-varying one [Tria96]. In the following analysis, we will calculate the time average output noise and use it to evaluate phase noise.

We first note that the cross-coupled pair only contributes phase noise when they are both in saturation region. When one side is tuned off, the other side will be cascoded on the bias current source and the cross-coupled pair will contribute little to output noise [Terr99], as shown in Figure 3.8. During the time period of both sides are on, the total differential transconductance is

$$g(t) = \frac{g_{m1}(t)g_{m2}(t)}{g_{m1}(t) + g_{m2}(t)} \tag{3.23}$$

The corresponding current noise PSD is

$$i_n^2(t)/\Delta f = 4kT\gamma g(t) \tag{3.24}$$

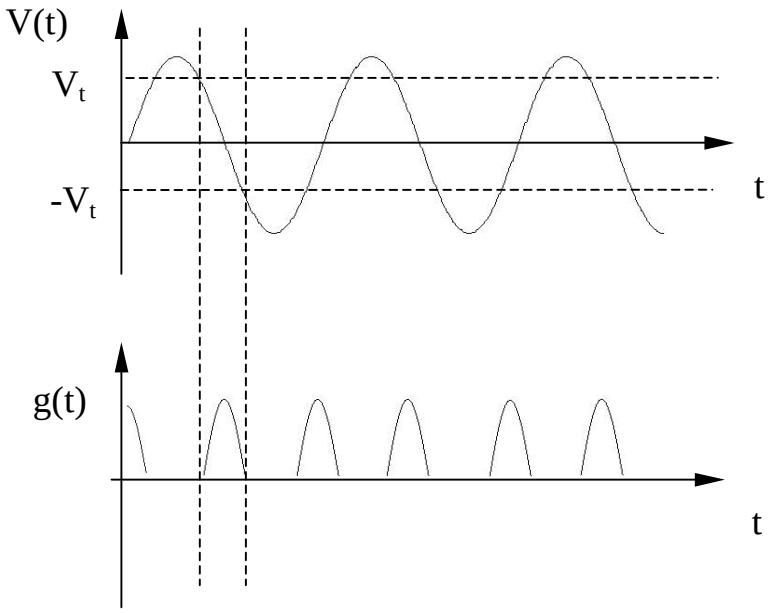


Figure 3.8 Time-varying transconductance of cross-coupled pair

The time average current noise PSD is

$$i_n^2 / \Delta f = 4kT\gamma\bar{g} \tag{3.25}$$

The time average transconductance must be equal to one over the total parallel tank resistance, or in equation form

$$\bar{g} = 1/R_p \tag{3.26}$$

We obtain the output phase noise due to the active devices as

$$L\{\Delta\omega\} = kT\frac{R_p\gamma}{V_0^2}\left(\frac{\omega_o}{Q\Delta\omega}\right)^2 \tag{3.27}$$

3.4.4 Phase noise from tail current source

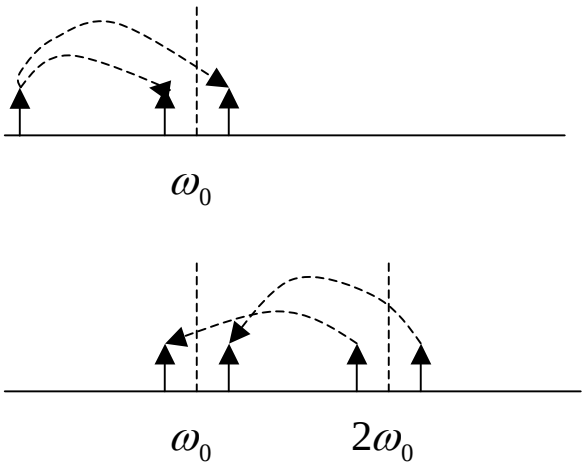


Figure 3.9 Tail noise up conversion and down conversion

For the bias current source, the cross-coupled pair acts as a single balanced mixer. So it will up-convert the low frequency noise and down-convert the noise at $2f_0$ to the fundamental frequency f_0, Figure 3.9. The conversion gain is in the form

$$G(\Delta\omega) = \frac{2}{\pi}R_p\frac{\omega_0}{2Q\Delta\omega} \tag{3.28}$$

Here we need to make a difference between up-converted low frequency noise and down-converted $2f_0$ noise.

For the low frequency noise, say at frequency ω_m, the up-converted noise at $\omega_0+\omega_m$ and $\omega_0-\omega_m$ is from the same source and in negative phase. This is shown by

$$\cos(\omega_m t+\phi)\cos\omega_0 t=\frac{1}{2}\left[\cos((\omega_0+\omega_m)t+\phi)+\cos((\omega_0-\omega_m)t-\phi)\right] \qquad (3.29)$$

So the up-converted noise will produce AM noise only. For the $2f_0$ noise, say at frequency $2\omega_0+\omega_m$ and $2\omega_0-\omega_m$, the down-converted noise at $\omega_0+\omega_m$ and $\omega_0-\omega_m$ is from different sources and in random phase. This is shown by

$$\cos((2\omega_0+\omega_m)t+\phi)\cos\omega_0 t=\frac{1}{2}\left[\cos((\omega_0+\omega_m)t+\phi)+\cos((3\omega_0+\omega_m)t+\phi)\right] \quad (3.30)$$

$$\cos[(2\omega_0-\omega_m)t+\gamma]\cos\omega_0 t=\frac{1}{2}\left[\cos((\omega_0-\omega_m)t+\gamma)+\cos((3\omega_0-\omega_m)t+\gamma)\right] \quad (3.31)$$

ϕ and γ are phases of different sources and not correlated. So the down-converted noise will produce one half AM noise and one half PM noise.

So phase noise due to bias current source will be

$$L\{\Delta\omega\}=4kT\gamma_{bias}g_{bias}\frac{R_p^2}{\pi^2Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\frac{1}{V_0^2/2} \qquad (3.32)$$

3.4.5 Total phase noise equation

Finally, combining each device noise with the tank output noise, the total excess output noise factor for the oscillator can be found.

$$F=\gamma+\frac{8}{\pi^2}\gamma_{bias}g_{bias}R_p \qquad (3.33)$$

3.4.6 Comparison with other models

We have reviewed Leeson's model and Hajimiri's model for oscillator phase noise modeling. Several numerical simulators [Cade01, Agil04] are now also available to assist the circuit designer to predict phase noise of integrated VCO. So what is the point of another phase noise model? The reason is that the previous models are either measurement based or simulation based. They can not give physical insight and simple yet accurate formula for the phase noise. At present, the situation of the oscillator designer is similar to the designer of amplifiers who has only SPICE simulator, but who lacks physical insight and methods for simple yet accurate analysis with which to optimize a circuit.

Leeson's classic model is based on a linear model of an LC resonator in steady-state oscillation through application of negative conductance concept. However, without knowing the excessive noise factor, which Leeson leaves as an unspecified measurement based factor, the actual phase noise cannot be predicted. Hajimiri's model uses linear time variant analysis to capture the effect of large signal periodic switching of oscillators. It is inherently more accurate. But the ISF functions and NMF functions are generally too complicated to get from hand calculation and can only be obtained by computer simulation. The commercial simulators, such as spectreRF from Cadence, use methods similar to Hajimiri's model and are usually more involved [Caden00]. Table 3.1 compares our proposed model with the other three phase noise models.

	Need Measurement?	Need Simulation?	Closed form formula?	Simplicity
Proposed	No	No	Yes	simple
Leeson's	Yes	No	No	simple
Hajimiri's	No	Yes	No	complex
SpectreRF	No	Yes	No	More complex

Table 3.1 Comparison of phase noise models

3.5 A low phase noise 2 GHz LC VCO design and analysis

3.5.1 Tank passive components design

Inductor design: From the phase noise equations from section 3.4, we can see that the tank quality factor Q strongly affects the phase noise of the oscillator. The inductor in a LC oscillator is usually the most critical circuit element in the design. Typically, the Q of the inductor dominates the total Q of the tank circuit. In addition, the tuning range of a VCO is strongly affected by the self-resonant frequency (f_{sr}) of an inductor. The self-resonant frequency is the frequency at which capacitive parasitics result in a zero net reactance; beyond this frequency the inductor becomes capacitive.

Traditionally, inductors have been incorporated as discrete components located off chip (often as small surface mounted parts). While off chip inductors can have extremely good performance, it is desirable to use on chip inductors and eliminate as many discrete components as possible. This reduces the board-level complexity and

component count, which in turn leads to a direct reduction in cost. As an alternative to off chip inductors, some RF integrated circuits have utilized bonding wires as inductors. While bonding wires can have a relatively high Q (on the order of 50), they can also suffer from large variations in inductance value since wire bonding is a mechanical process that cannot be as tightly controlled as photolithographic processes.

Monolithic inductors fabricated as simple planar spirals are now widely used on silicon based substrates. The inductance of a monolithic inductor is defined solely by its geometry. Modern photolithographic processes provide extremely tight geometric tolerances. For this reason monolithic inductors have very small variations in their performance. But their Qs are usually less than 10.

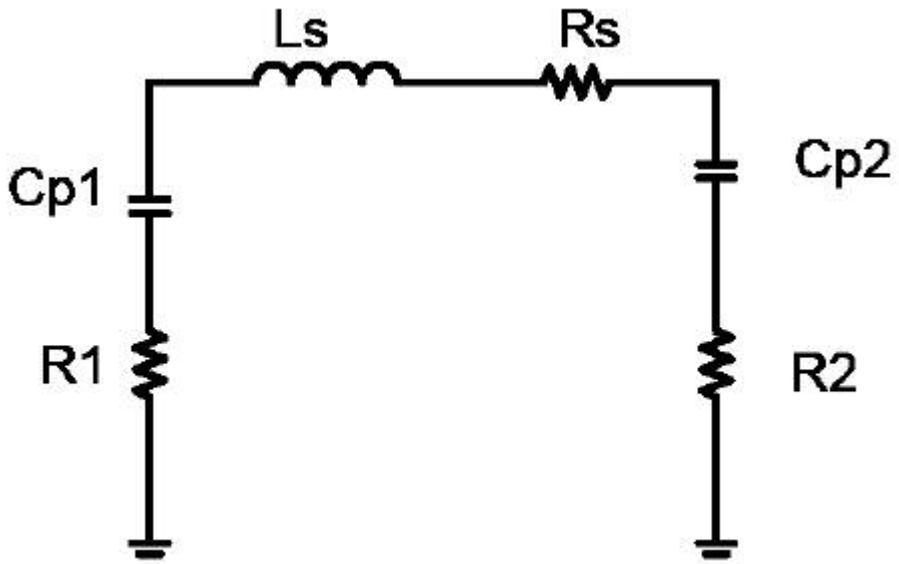
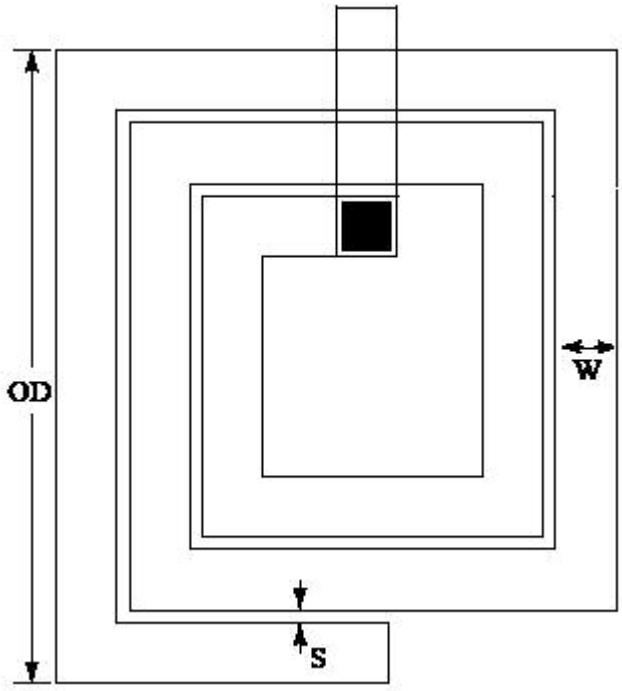


Figure 3.10 Equivalent lumped model for spiral inductor

In a standard CMOS process, metal layers can be used to construct on-chip spiral inductors. Several issues associated with the on-chip inductor need to be taken care of

to improve its performance. First, there is series resistance in the metal layers which reduces the quality factor of the inductor. Second, there is capacitive coupling from the metal to substrate which reduces the self-resonant frequency of the inductor. Third, there is resistance in the conducting substrate which also reduces the quality factor of the inductor. These non-idealities are modeled in the lumped pi model for the spiral inductor as shown in Figure 3.10. *Ls* models the series inductance and *Rs* models the series resistance of the metal. *Cp1* and *Cp2* model the capacitive coupling of the metal and the substrate. *R1* and *R2* model the resistive path in the substrate. The optimal layout of an inductor depends on the inductance value, the particular



process and the frequency of operation.

Figure 3.11 Geometry of square spiral inductor

The design of the planar inductor for high quality factor is not the focus of this dissertation. So the detailed inductor design process will not be described here. In this dissertation the inductors are designed primarily by iteration. 2GHz is the desired frequency of operation and we try to obtain oscillation near this frequency. Since a tank circuit with C = 1pF and L = 6nH resonated near 2GHz, this was the chosen as the starting point for the design. The final designed inductor geometry is a 2.5-turn square spiral shown in Figure 3.11. The final parameters are outside diameters (OD) 200um, tracewidths (W) 10um, and an interwinding spacing (S) 2um.

Varactor design: Although the quality factor of the tank circuit will be dominated by the inductor, the design of the varactor is also critical. If the varactor is not carefully designed its series resistance could signicantly lower the overall Q of the tank circuit, adversely impacting the phase noise of the oscillator.

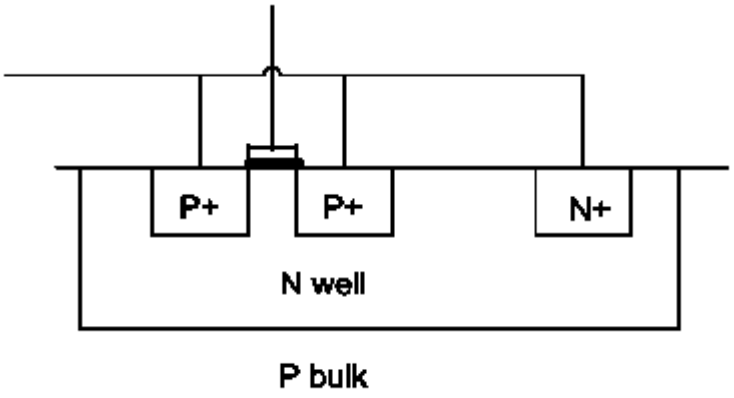
Traditionally, discrete VCO implementations have used junction varactor diodes. These diodes are operated under reverse bias and are designed to enhance the variability of their depletion capacitance with reverse bias voltage. In a monolithic environment designers are much more restricted in the choice of tuning elements. The junction diodes that are available in a standard silicon CMOS process are not optimized for use as varactors; still, many monolithic LC oscillators have used such diodes as tuning elements. In a typical n-well CMOS process there are three types of junction diode structures available: n+/p-bulk, p+/n-well, and n-well/p-bulk. The only suitable choice for a junction varactor diode is the p+/n-well junction. Since the pbulk is typically connected to ground, the other structures would require a negative bias voltage in order to be reverse biased. The p+/n-well structure also has a lower series

resistance due to the higher n-well doping level compared to the p-bulk. A p+/n-well structure can typically have a quality factor of 20 or better. One disadvantage of junction varactors is that they can become forward biased by large amplitude voltage swings.

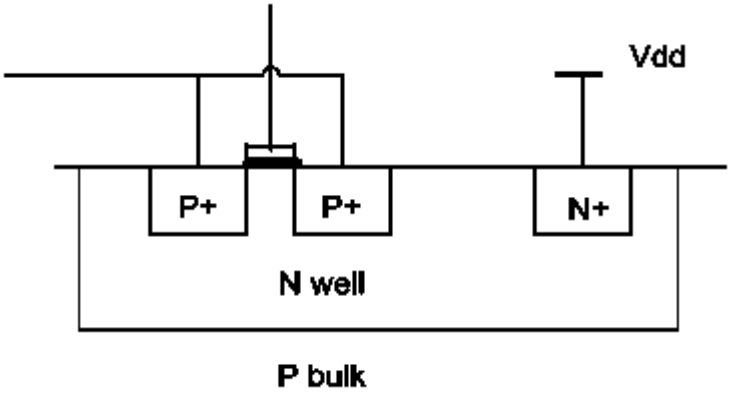
MOS capacitor, instead of a junction diode, can be used for the tuning element of the VCO. The MOS capacitor operates in a similar manner as a simple parallel plate capacitor in series with a depletion junction capacitance. In MOS capacitor the plates of the capacitor are formed by the polysilicon gate and the channel of a MOSFET. The capacitance of this MOS device varies nonlinearly as the DC gate bias of the MOSFET is varied through accumulation, depletion and inversion operation region.

There are three types of MOS structures suitable to be used as varactors. Figure 3.12 shows the cross sections for each of these three structures. Each structure shown is situated in an n-well; however, these devices could also be implemented in the p-bulk as well. N-well is preferred because the bulk terminal of an n-well can be biased at a variable voltage (in an n-well process), whereas the p-bulk must be at ground potential.

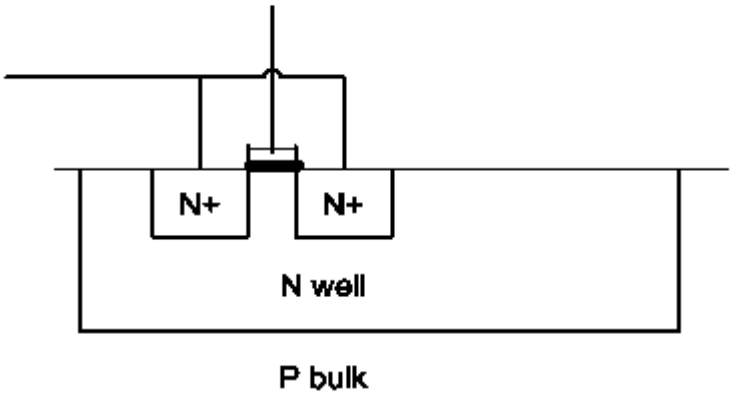
The first structure consists of a PMOS transistor with the drain, source and bulk connected together (D=S=B) to form one node of the capacitor, and with the polysilicon gate as the other node, Figure 3.12 (a). This structure has a DC capacitance that varies nonmonotonically, since the device can operate in inversion, depletion, and accumulation region. The DC capacitance in both inversion and accumulation is approximated by Cox, which can be calculated from the device dimensions as a simple parallel plate capacitor. If fringing effects are neglected,



(a)



(b)



(c)

Figure 3.12 MOS varactor structure (a) PMOS (b)I-MOS (c) A-MOS

$$C_{ox} = \frac{\varepsilon_{ox} WL}{t_{ox}}, \tag{3.34}$$

where tox is the gate oxide thickness. If a MOS varactor is to be used as the tuning element of a low frequency oscillator, then the non-monotonic characteristic can be problematic. At high frequency, the charge in the inversion layer does not change from the equilibrium state corresponding to the applied DC voltage. The high frequency capacitance therefore reflects only the charge variation in the depletion layer and the (rather small) movement of the inversion layer charge. The high frequency C-V characteristic of this structure becomes monotonic.

The second option is the inversion mode MOS capacitor, figure 3.12 (b). This structure is identical to a MOSFET. The drain and source are shorted together to form one capacitor terminal while the polysilicon gate forms the other. However, the bulk (n-well) of this structure is connected to the highest voltage available in the circuit, Vdd. Since the nwell connection of the device is always at a higher or equal potential with respect to the gate, the device can only operate in inversion. The C-V characteristic of this structure is monotonic and can be used as the tuning element in VCO. The capacitances of the D=S=B and Inversion mode capacitors can both be simulated by the BSIM3v3 models.

MOS capacitors can also be designed to operate in accumulation mode. Figure 3.12 (c) shows the structure of an accumulation mode MOS (A-MOS) capacitor. This structure departs somewhat from the standard PMOS transistor, since it replaces the p+ diffusions of the drain and source with n+ regions. This suppresses the injection of minority carriers (holes) into the channel and prevents it from inverting. The use of n+ regions also obviates the need for n+ ohmic contacts to bias the n-Well, so this

structure can be smaller than the other MOS capacitors. Since this device works in accumulation and depletion only, the capacitance characteristic of this structure is also monotonic. This structure typically has higher Q value compared with the previous two options due to the higher mobility of electron. The main drawback of this structure is its characteristics are not represented in the device models supplied by the vendor because this structure is no longer a MOS transistor. In order to simulate the behavior of this structure, a device simulator must be used, requiring detailed knowledge of process parameters such as doping concentrations.

The A-MOS varactor is selected in this design due to its higher quality factor. From the starting point of tank C = 1pF and L = 6nH resonating near 2GHz, the maximum capacitance value of the varactor is decided to be 1.8 pF considering the parasitic capacitors of inductor and cross-coupled MOS devices.

3.5.2 Circuit design

The np-Pair is chosen due to its lower power consumption and reduced 1/f noise up-conversion. The supply voltage we use is 2.7 V. To meet the power consumption constraint of specifications, we set I_{bias} = 2.5mA.

Each inductor has an inductance value of 2.7nH with quality factor 7.4 at 2GHz. The tank Reff = 9.2 ohm. Tank equivalent parallel resistance $R_p = R_{eff} Q^2$=503 ohm. Tank transconductance g_{tank} = 2mS. Let startup factor α =3.5. We need the sum transconductance of one NMOS and one PMOS to be $g_n+g_p = \alpha*2\ g_{tank}$ = 14mS. To reduce 1/f noise up-conversion, we choose $g_n = g_p$= 7mS. From these parameters and 0.25um CMOS technology parameters, we get NMOS size as W/L =40/0.25 and PMOS size as W/L=120/0.25.

From the phase noise model, we should have bias current source transconductance g_{bias} and γ_{bias} as small as possible. So we will choose large length and small width for the current source MOSFET. But transconductance g_{bias} must be large enough to ensure that the device works in saturation region. The final size we choose is W/L = 200/4.

3.5.3 Analysis and simulatiom

From the phase noise model, differential output amplitude

$$V_0 = 4/\pi I_{bias} R_p = 1.6V \tag{3.34}$$

When oscillation frequency is 2GHz, the predicted phase noise at 1MHz is

$$L(1MHz) = \frac{KTR_{eff}(1+\gamma+\frac{8}{\pi^2}\gamma_{bias}g_{bias}R_p)}{V_0^2}\left(\frac{2\times10^9}{10^6}\right)^2 = -127dBc/Hz \tag{3.35}$$

In the calculation, we choose $\gamma_{bias} = 2/3$ and $\gamma = 2.5$.

We simulated the phase noise and frequency tuning characteristics of the final circuit design using Agilent ADS. The simulation results are shown in Figure 3.13 and Figure 3.14. Figure 3.13 shows the phase noise v.s. frequency offset when the oscillation frequency is at 2GHz. The simulated phase noise at 1MHz offset is -126 dBc/Hz. It is in good agreement with our analysis result. Figure 3.13 (b) shows the simulated frequency tuning curve of the 2G VCO. When tuning voltage changes from 1~2.7 V, the oscillation frequency changes from 1.9~2.2GHz.

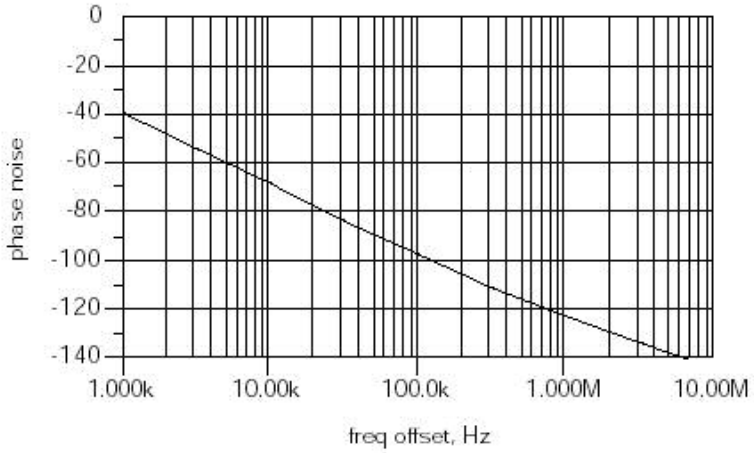


Figure 3.13 Simulated VCO phase noise v.s. frequency offset

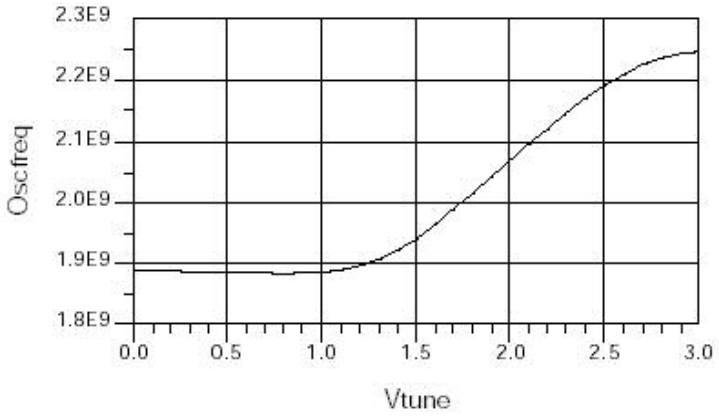


Figure 3.14 Simulated VCO frequency tuning curve

3.5.4 Measurement results

The 2GHz VCO is fabricated in TSMC CMOS 0.25um process. The die photograph is shown in Figure 3.15.

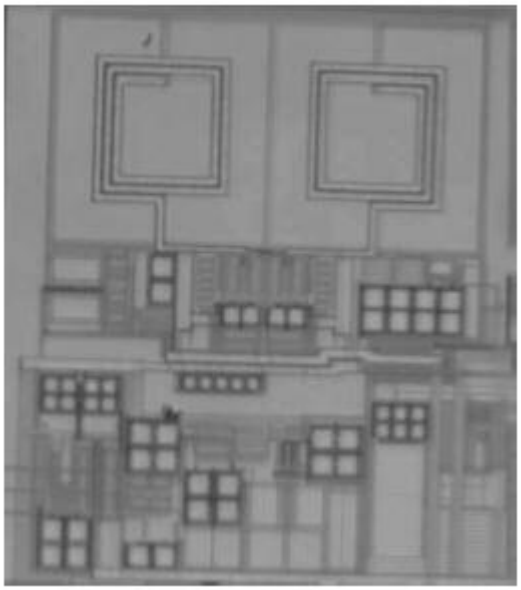


Figure 3.15 Die photograph of 2GHz VCO

The measurement results are shown in Figure 3.16. Figure 3.16 (a) shows the measured frequency tuning curve of the 2GHz VCO. When tuning voltage changes from 0.5~2.2 V, the oscillation frequency changes from 1.9~2.2GHz. It covers the 14 channels of 802.11b/g applications. The tuning range is about 15%. Figure 3.16 (b) shows the phase noise v.s. frequency offset when the oscillation frequency is at 2 GHz. The measured phase noise at 1MHz offset is -125 dBc/Hz. It is in good agreement with our analysis and simulation result.

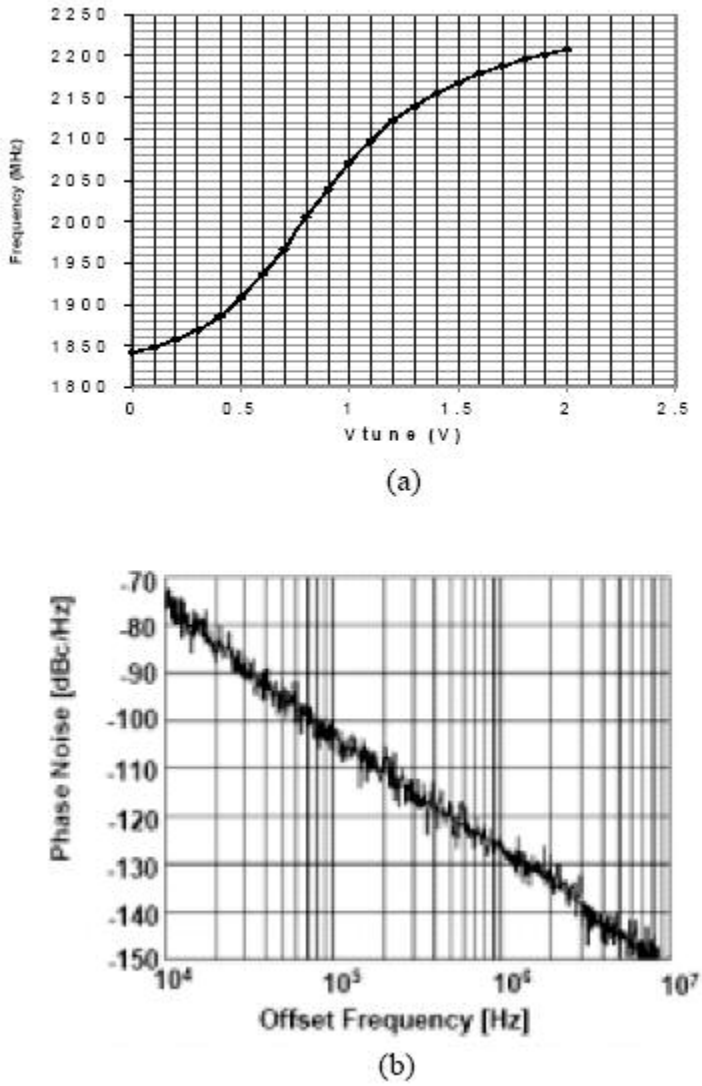


Figure 3.16 Measured 2GHz VCO performance (a) VCO frequency tuning curve (b) VCO phase noise v.s. offset frequency

Chapter 4: Low phase noise PFD/CP/Divider design

As discussed in section 2.6, PFD/CP/Divider determines the in-band phase noise floor of the closed loop PLL. As the wireless design evolves into higher operating frequency and higher data rate, PFD/CP/Divider becomes more important. High data rate is usually achieved by broad band operation and high order modulation scheme, such as QAM64. As shown in section 2.2, the phase impairment effect will dominate in this case. The measurement of phase impairment is RMS phase error which depends both on in-band and out of band phase noise. On the other hand, integrated VCO performance becomes worse at higher operating frequency. Thus, we have to use relatively noisy VCO to meet the strict RMS phase error specifications. So it is desirable to use a wide bandwidth PLL to suppress the VCO phase noise. More PFD/CP/Divider phase noise will contribute to the closed loop phase noise in a wide bandwidth PLL. Thus, optimization of PFD/CP/Divider phase noise becomes a very important issue.

4.1 Introduction to PFD/CP/Divider in PLL

4.1.1 PFD (Phase-Frequency Detector) and CP (Charge Pump)

In a PLL, the control voltage of the VCO comes from the filtered output of PFD (Phase-Frequency Detector) and CP (Charge Pump), which contains the information of how much the divided VCO signal leads or lags reference signal in terms of phase. Figure 4.1 shows a block diagram of a typical PFD/CP implementation.

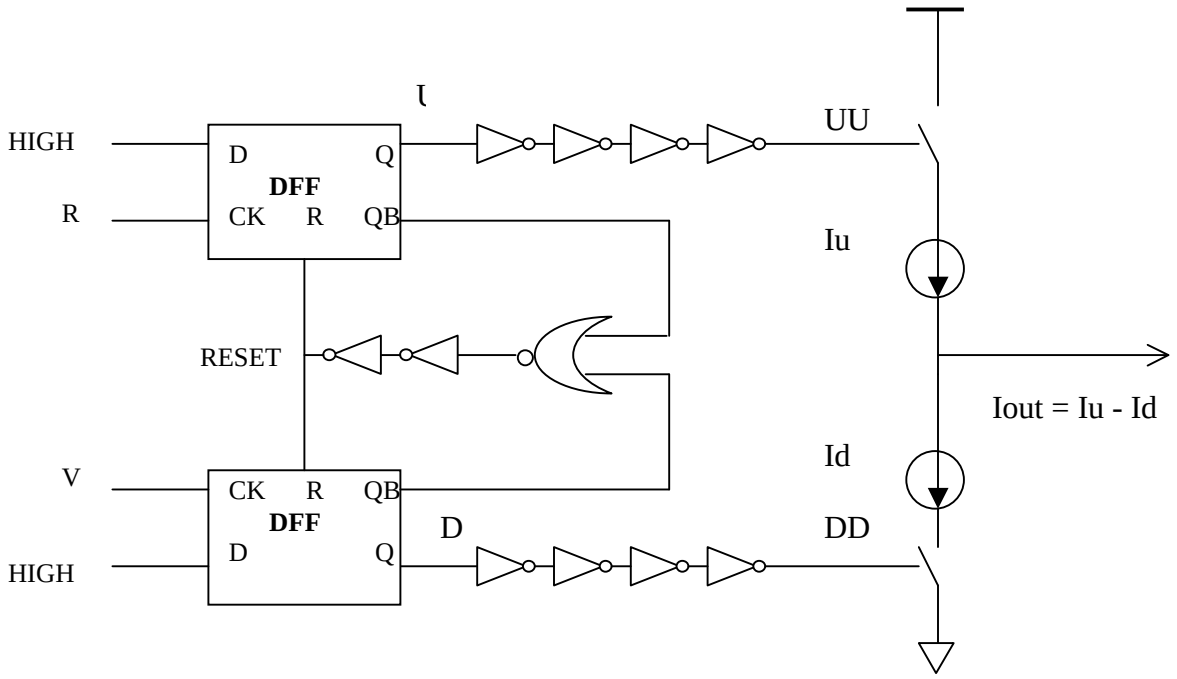


Figure 4.1 Block diagram of PFD/CP

The top DFF (D-type Flip-Flop) generates a high signal when a rising edge from reference signal (R) is received. This high signal will turn on the top switch and allow the current to charge the loop filter. The top switch will keep on until a rising edge from divided VCO (V) is received, which generates a high signal in the bottom DFF and resets both DFFs through the NOR gate in the reset path. When the rising edge of V is leading R, the operation is similar except that the down switch will turn on and the current will discharge the loop filter. The pulse width of the current waveform indicates the phase/frequency difference of R and V signal.

One important problem of PFD is its dead zone. The dead zone of the PLL is the region where the charge pump currents can not flow proportionally to the phase error

at the input of the PFD. The main reason of the dead zone is that the switching time of the charge pump currents is longer than reset delay of the PFD. In the dead zone, the PFD/CP will have no response even there is a small phase difference between the reference and divided VCO pulses. A timing diagram of the signals for the PFD/CP in Figure 4.1 is shown in Figure 4.2, where Tr is the delay in the PFD reset path, Te is a given phase error, Vth is the threshold voltage of the charge-pump current switch, and Tth is the time for the input voltage of the charge-pump switch to change from zero to Vth. Tth is defined as the switching time of the charge-pump currents. As shown in Figure 4.2, the PLL loop is effectively opened and the VCO phase noise can no longer be suppressed by the loop.

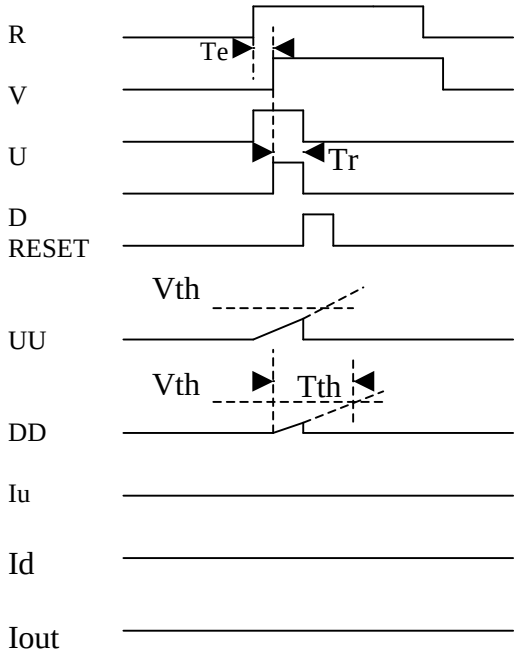


Figure 4.2 Dead zone of PFD

4.1.2 Divider

The divider in the feedback path of the PLL determines the output frequency of the VCO in locked state. Typically the divider sees the full range of frequencies in the loop (from several hundred kHz to several GHz). The divider must be programmable to select different channels for the desired application. Due to different speed requirement, the divider is usually implemented by a combination of different logic family circuits. In the low speed part, the full swing conventional CMOS logic is used for its low static power consumption. But the conventional CMOS logic has its speed limit. In the high speed part closer to VCO output, static logic, e.g. source coupled logic (SCL), must be used.

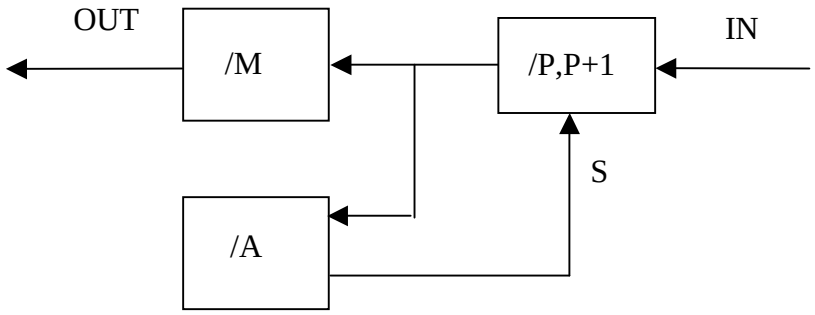


Figure 4.3 Programmable divider

A programmable divider usually consists of a prescaler and two counters in a pulse swallow architecture [Yan99], Figure 4.3. The dual modulus prescaler divides the input frequency by either *P* or *P*+1 depending on the setting signal S. The output of the prescaler serves as the input of counter **A** and counter **M**. At the beginning, the prescaler is in the divide by *P*+1 mode. When counter **A** reaches zero, the setting signal **S** sets the prescaler in the divide by *P* mode. This mode continues until counter

M reaches zero. For a complete cycle, it takes **MP+A** edges of the input to generate one edge at the divider output. This means that the divider divides the input by **MP+A**. Usually the prescaler is implemented by source coupled logic while the M and A counters are implemented by CMOS logic.

4.2 Related work on PFD/CP/Divider phase noise analysis

Unlike VCO, there is very little work on PFD/CP/Divider phase noise analysis in the circuit level. Several mathematical operators similar to the discussions in section 2.5 are offered to describe PFD/CP/Divider noise contributions in a PLL from the system level [Utsi90, Wils89]. But no physical insight and circuit level analysis is given.

In [Bane01], Banerjee proposed a simple empirical model for predicting the noise from the digital components in PLL with good accuracy. The model characterized a specific PFD/CP/Divider with a single parameter: the 1Hz normalized phase noise floor L_{1Hz}. The PLL in-band phase noise floor can be determined by

$$L_{floor} = L_{1Hz} + 20\lg N + 10\lg F_c \quad \text{(dBc/Hz)}, \tag{4.1}$$

Where N is the divider ratio and Fc is the PFD comparison frequency. The problem with this model when designing a PFD/CP/Divider is that 1Hz normalized phase noise floor is unknown at first and the model does not give methods to predict it directly from circuit parameters.

Besides the phase noise contribution in normal operation mode, it has long been observed that the dead zone of PFD/CP could greatly worsen its phase noise level [Cran98]. But there is no systemic design solution to combat their effects in the literature.

4.3 Organization of this chapter

To get optimal PFD/CP/Divider phase noise performance, we first need to make sure it works in the normal operation mode. A design scheme to eliminate the dead zone is desired. In section 4.4, we will propose a simple design scheme for eliminating the dead zone.

For the model of PFD/CP/Divider phase noise, the difficulty comes mostly from the digital components in PFD/CP/Divider. These digital components are more suitable to be modeled in the time domain. The noise in the time domain occurs as timing jitter. In section 4.5, we derive the relationship between the PFD/CP/Divider 1Hz normalized phase noise floor and the effective timing jitter referred to PFD input. The analysis of timing jitter for PFD/CP/Divider is presented in section 4.6. Based on the analysis, an analytic model for PFD/CP/Divider phase noise can be derived. Section 4.7 gives a design example and simulation results.

4.4 Dead zone free PFD/CP design

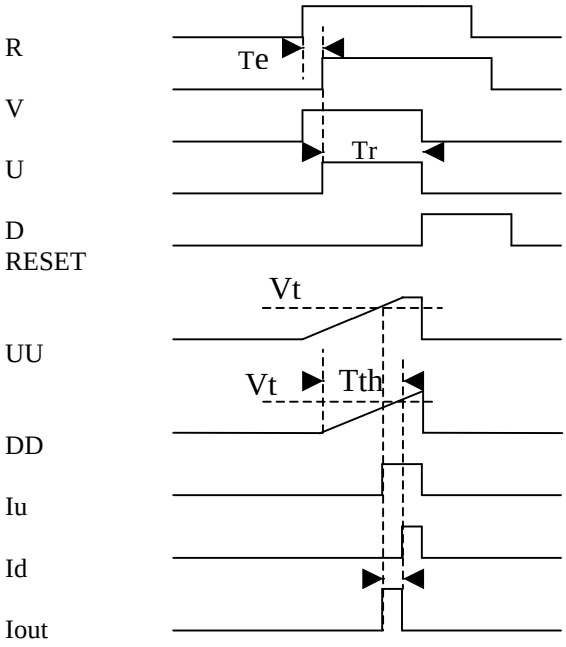


Figure 4.4 Dead zone free PFD

From Figure 4.2, we can see that the main reason of the dead zone is that the switching time of the charge pump currents is longer than reset delay of the PFD. So in PLL applications, an additional delay can be added in the PFD reset path to avoid the dead zone problem [Miju94]. When the reset delay is made longer than the switching time of the charge pump currents, even if the phase difference is very small the UP and DOWN signals are active during the reset delay period. Thus, the charge pump will not stay at its high impedance state and the loop is always locked, Figure 4.4. But the delay will cause both the UP and DOWN signals to appear even in the locked state. Thus, the charge pump current will switch on and off and the current pulses will appear on the charge pump output at every comparison cycle. This will

increase the phase noise contribution of charge pump, as will be explained in section 4.5.2. So the delay must be carefully designed to eliminate the dead zone while not causing too much phase noise increase.

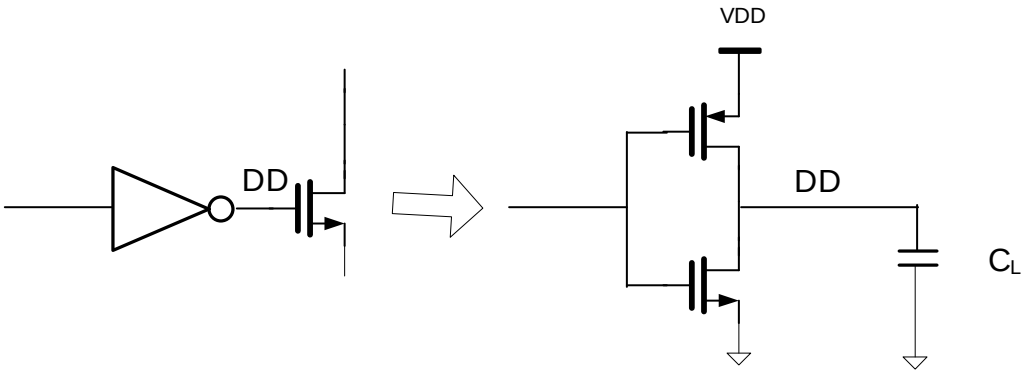


Figure 4.5 Modeling of inverter and charge pump switch

The switching time of the charge-pump is a function of the charge-pump current, the load capacitance from the CP switch, and the driving ability of the PFD output buffer. For the calculation of T_{th}, the last inverter of the charge-pump buffer and the charge-pump switch made of the MOS transistor in Fig. 4.1 are modeled as the inverter and a load capacitor (C_L), Figure 4.5. The charge-pump switching time (Tth) can be approximated by the rising (falling) time of the DD (UU) signal of Figure 4.1. The rising time (Tr) and the falling time (Tf) can be calculated as [Bake97]

$$T_r, T_f \approx \frac{2V_{DD}}{K_p \frac{W}{L}(V_{DD} - V_{TH})^2} C_L, \tag{4.2}$$

where K_p: the process transconductance constant (A/V^2).

W and L: the width and length of the device in inverter.

Vth: threshold voltage.

The equation for the minimum reset delay of the PFD in order to avoid dead-zone is given by

$$T_{th} = \frac{T_r + T_f}{2} \tag{4.3}$$

4.5 Timing jitter and phase noise

The ideal phase-frequency detector with current pump output produces a pulse of current for every phase comparison cycle. The duration of the pulse is proportional to the phase error $\phi_e = \phi_r - \phi_d$. We assume that the kth comparison cycle occurs at time *kTc*. Thus for phase error $\phi_e(kT_c)$ the ideal duration t_k of the current pulse is given by

$$t_k = \frac{\phi_e(kT_c)}{2\pi F_c}, \tag{4.4}$$

where F_c is the comparison frequency of PFD.

We can refer all noises in PFD/CP/Divider to the input of PFD. The noise effect can be characterized by the change of duration of the current pulse, i.e. timing jitter. We now include this timing jitter, so that at time *kTc* the current pulse has the ideal duration plus the timing jitter

$$t_k = \frac{\phi_e(kT_c)}{2\pi F_c} + \tau_k, \tag{4.5}$$

where the timing jitter is represented by τ_k, a random variable with zero mean and variance $\sigma^2 = \overline{\tau_k^2}$. It means that sometimes the pulses are longer, sometimes shorter. The rms variation of the pulse width is σ.

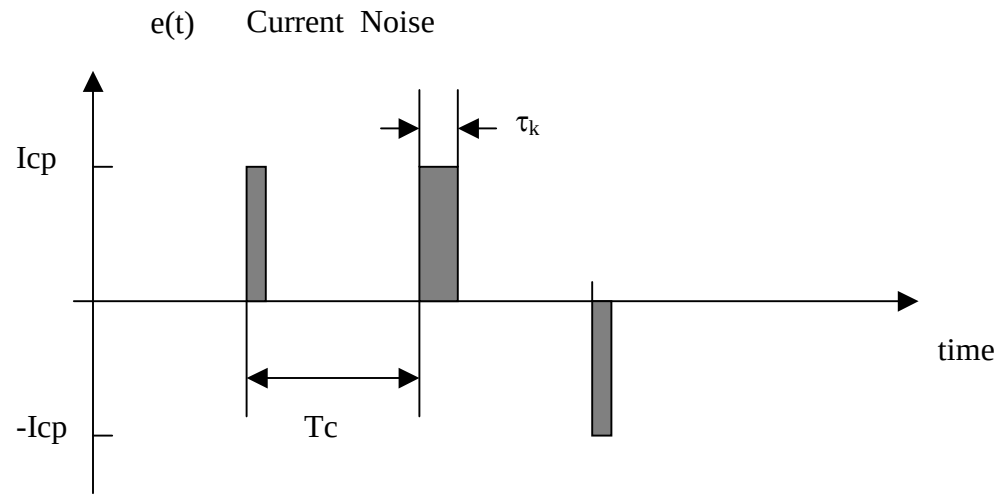


Figure 4.6 PFD/CP output current noise pulse

The noise waveform *e*(*t*) resulting from the timing jitter is shown in Figure 4.6. The power spectral density *E(f)* of a noise process *e(t)* is defined as

$$E(f) = \lim_{T\to\infty} \frac{1}{T} \overline{\left| \int_{-T/2}^{T/2} e(t) e^{-j2\pi ft} dt \right|^2} = \lim_{T\to\infty} \frac{1}{T} \overline{\left| \sum_{k=1}^{M} I_{cp} t_k e^{-j2\pi ft} \right|^2}, \qquad (4.6)$$

where $M=T F_c$ is the number of noise current pulse in the integration time T and I_{cp} is the charge pump current. We assume that the jitters are uncorrelated, then

$$E(f) = \lim_{T\to\infty} \frac{TF_c I_{cp}^2 \sigma^2}{T} = I_{cp}^2 \sigma^2 F_c \ . \qquad (4.7)$$

So the output SSB phase noise

$$L_\phi(f) = E(f) \frac{N^2}{K_D^2} \left(\frac{G(j2\pi ft)}{1+G(j2\pi ft)} \right)^2, \qquad (4.8)$$

where

$$G(s) = Z(s) \bullet \frac{Kvco}{s}.$$

$Z(s)$: transfer function of loop filter

K_{vco} :VCO gain (Hz/V)

N: divider ratio

$K_D = \frac{I_{cp}}{2\pi}$: gain of PFD/CP (A/rad)

Consider in-band phase noise where $|G(s)| >> 1$. Using $K_D = I_{cp}/2\pi$ gives an in band phase noise floor of

$$L_{floor} = E(f)\frac{N^2}{K_D^2} = 4\pi^2 F_c \sigma^2 N^2 \quad (4.9)$$

or

$$L_{floor} = 20\lg(2\pi\sigma) + 10\lg Fc + 20\lg N\,. \quad (4.10)$$

Comparing with Banerjee's measurement based model in section 4.2, we can get the relationship between 1Hz normalized phase noise floor and timing jitter as follows

$$L_{1Hz} = 20\lg(2\pi\sigma)\,. \quad (4.11)$$

4.6 PFD/CP/Divider phase noise model

4.6.1 PFD/Divider phase noise

The PFD and divider are digital blocks in the Phase Locked Loop. The noise generated by the PFD and divider can affect the closed loop synthesizer noise performance within the PLL bandwidth, especially if a high division ratio is used. In fact, the PFD/Divider noise power is multiplied by the square of the division ratio, when it is transferred to the PLL output. However, evaluation of the PFD/Divider noise is not straightforward. The various noise sources in the circuit affect the zero-crossing instants of the output signal and the resulting phase noise is a random process sampled at the output frequency. For this reason, only time-domain simulations can predict the digital block's jitter. Unfortunately, such simulations are

very time-consuming and provide little insight in the physical processes for the jitter generation. The literature offers only empirical models for classifying and describing the phase noise of digital blocks [Krou01]. These models do not account for the relative importance of the various noise sources and they do not identify the relationship between the noise and circuit design parameters.

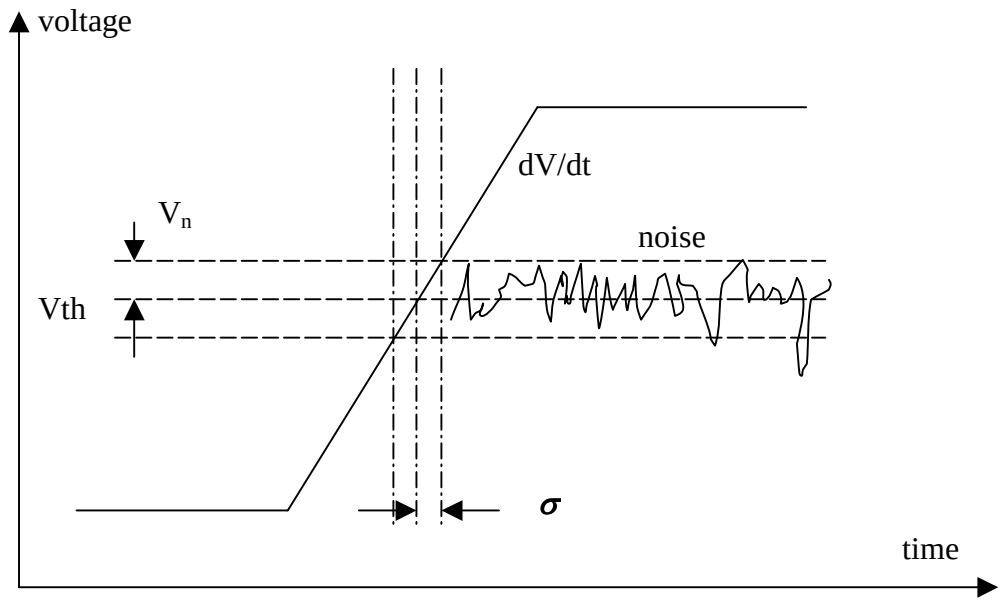


Figure 4.7 Conversion of noise to timing jitter

Additive noise, predominantly thermal, within the digital logic in the PFD/Divider gives rise to timing jitter. The jitter occurs because of an interaction of the noise and thresholds that are inherent to digital logic circuits. The threshold crossings of a noiseless periodic signal are precisely evenly spaced. However, when noise is added to the signal, each crossing is displaced slightly. Thus, a threshold converts additive noise to timing jitter. The conversion process is shown in Figure 4.7, where Vth, Vn, dV/dt and σ represent inverter threshold voltage, RMS value of thermal noise voltage,

incoming signal slope, and RMS value of timing jitter respectively. The amount of displacement of threshold crossing in time is determined by the amplitude of the noise signal $V_n(t)$ and the slew rate of the periodic signal $dV(t)/dt$ when the signal is crossing the threshold. The RMS value of timing jitter can be written as

$$\sigma = \left. \frac{V_n}{dV/dt} \right|_{V(t)=V_{th}} \tag{4.12}$$

As discussed in 4.1, there are different logics used for the digital blocks in PLL. We will discuss the method to derive expressions of the phase noise of two different logics, starting from the calculation of their timing jitter.

4.6.1.1 Source coupled logic

A frequency divider is typically implemented as an asynchronous cascade of D2 (divide by two) blocks, where each stage is clocked by the previous one. Therefore, the time jitter of any stage, defined as the variance of the instant of the output threshold crossing, is transferred to the following stage. Moreover, each stage adds its own jitter. The jitter at the output of the chain is the square root of quadratic sum of the jitters of each stage [Egan90].

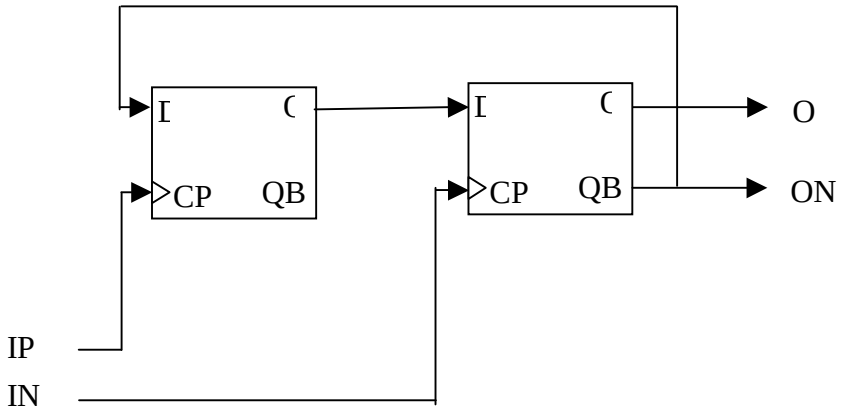


Figure 4.8 Block diagram of divide by two circuit

A common topology for the D2 is the one represented in Figure 4.8, where two D-latches are connected in master/slave configuration and the output of the second latch is fed back to the D input of the first latch. The jitter at the output of this divider is not affected by the noise of the first latch, since the latter has no control on the output switching. Thus, only the noise sources of the second latch need to be taken into account in the evaluation of the output jitter.

In the following, we will consider the latch implemented in static source-coupled logic (SCL) as the one shown in Figure 4.9, since they are very common in the design of dividers for gigahertz applications.

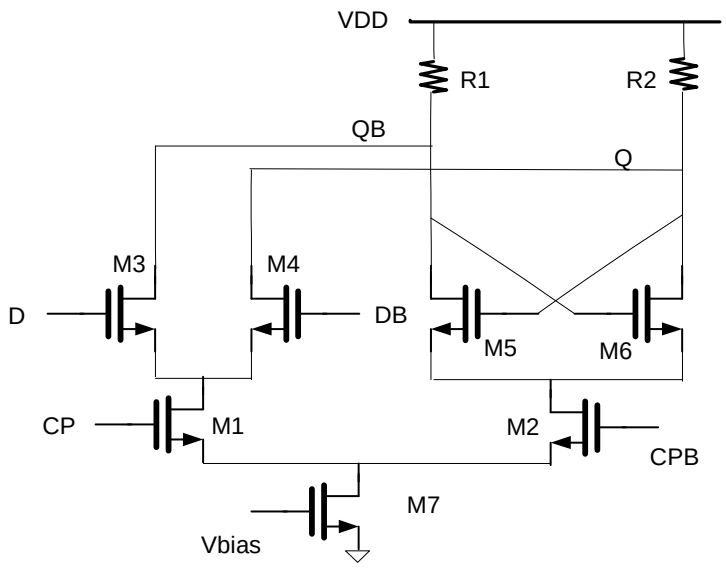


Figure 4.9 D latch in SCL logic

In the circuit show in Figure 4.9, R1 and R2 act as load resistors. Transistor M7 gives the biasing current. At the zero crossings of the inputs CP, differential stage M1 and M2 are balanced. For a proper operation of the divider, the D signals of the latch have already switched completely before CP starts to switch. Therefore, one of the transistors M3 and M4 is off and the other one is in triode region. The same happens to the transistors M5 and M6. So differential pairs M3, M4 and M5, M6 will not affect the output zero crossing point. The noise sources affecting the output zero crossings are the noise of differential pair M1 and M2, the noise of tail current transistor M7, and the noise of the load resistor R1 and R2.

A. Load resistor

The thermal noise of the resistors causes voltage noise at the differential output. The power spectral density of the noise voltage is

$$\overline{v}_n^2 = 4kTR_1 . \tag{4.13}$$

Let the capacitor C_L represents the total output capacitance, given by the transistors connected at the output nodes and by the interconnect capacitance. The output can be modeled as a first order low pass filter with 3dB cut off frequency of

$$f_c = \frac{1}{2\pi R_1 C_L} . \tag{4.14}$$

The noise bandwidth for a first order low pass filter is $\frac{\pi}{2} f_c$. The variance of the noise voltage can be written as

$$\sigma_V^2 = \overline{v}_n^2 \frac{\pi}{2} f_c = \frac{kT}{C_L} . \tag{4.15}$$

The slope of the waveform at the zero crossings is

$$\frac{dV}{dt} = \frac{I_B}{C_L} , \tag{4.16}$$

where I_B is the bias current given by M7. Considering the differential output, the resulting jitter is, therefore

$$\sigma_{t,load}^2 = \frac{2\sigma_v^2}{dV/dt} = \frac{2kTC_L}{I_B^2} \tag{4.17}$$

B. Tail current transistor M7

The tail current generator M7 represents another noise source in the circuit of Figure 4.9. Its current noise is alternatively injected into the nodes Q and QB. However, the effect of this noise on the two output nodes is different. Before the beginning of the switching process, one of the outputs is at VDD and the other one is at VDD - I_BR1.

Only the output at the lower voltage is affected by the tail noise. The noise voltage spectral density is

$$\bar{v}_n^2 = \bar{i}_{n,7}^2 R_1^2 , \tag{4.18}$$

where $\bar{i}_{n,7}^2$ is the noise current spectral density of transistor M7. The noise variance can be obtained by multiplying the voltage spectral density by the noise equivalent bandwidth $\frac{1}{4R_1C_L}$,

$$\sigma_V^2 = \bar{i}_{n,7}^2 \frac{R_1}{4C_L} . \tag{4.19}$$

$\bar{i}_{n,7}^2$ can be written as

$$\bar{i}_{n,7}^2 = 4kT\gamma_7 g_{m7} , \tag{4.20}$$

where γ_7 and g_{m7} are the noise factor and transconductance of the tail transistor M7 respectively. The above σ_V^2 is the voltage noise variance when the outputs are switched to one side completely. In the following, we will try to get the voltage noise variance at the time instant of output zero crossing.

After the beginning of the switching process, one output is pulled down and the other one is pulled up. The tail noise is not injected into the load for the pull-up node, thus its noise variance decreases exponentially with time constant of R_1C_L. The noise variance at the pull-up node changes with time according to the following equation,

$$\sigma_{V,up}^2(t) = \sigma_V^2(1 - e^{-\frac{2t}{R_1C_L}}) \tag{4.21}$$

At the same time, the tail noise flows toward the other output node, which is pulled down. The noise variance at this node increases exponentially. The noise variance at the pull-down node changes with time according to the following equation,

$$\sigma_{V,dn}^2(t) = \sigma_V^2 e^{-\frac{2t}{R_1 C_L}} \tag{4.22}$$

The noise variance of the differential output is the sum of the above noise variance at two nodes and can be calculated as

$$\sigma_{V,diff}^2(t) = \sigma_{V,up}^2(t) + \sigma_{V,dn}^2(t) = \sigma_V^2 . \tag{4.23}$$

So the noise variance of the differential output is independent of time and is always equal to σ_V^2. The timing jitter due to tail current noise is

$$\sigma_{t,tail}^2 = \frac{\bar{i}_{n,7}^2 R_1^2 \dfrac{1}{4R_1 C_L}}{\dfrac{I_B^2}{C_L^2}} = \frac{kT\gamma_7 g_{m7}}{I_B^2} R_1 C_L . \tag{4.24}$$

C. Differential pair M1 and M2

When the input signal switches completely the differential pair, none of the transistors contributes to noise. One of them is on, but fully degenerated, while the other one is off. As a result, noise is injected into the load only when the input waveform is within the linear range of operation of the differential stage, i.e. near the balanced state. The voltage noise variance due to one transistor M1 is

$$\sigma_{V1}^2 = 4kT\gamma_1 g_{m1} R_1^2 \frac{1}{4R_1 C_L} = \frac{kT\gamma_1 g_{m1} R_1}{C_L} , \tag{4.25}$$

where γ_1 and g_{m1} are the noise factor and transconductance of the tail transistor M1. Accounting for the noise of both transistors M1 and M2, the variance of the voltage noise can be written as

$$\sigma_V^2 = 2\sigma_{V1}^2 = 2\frac{kT\gamma_1 g_{m1} R_1}{C_L}. \tag{4.26}$$

But this voltage noise variance is for the static state at the zero crossing of the input signal. We need to find the variance of the voltage noise for the time instant of output zero crossing. Denoting the time duration of differential pair operating in linear region as Tw and the time delay between the input and output zero crossing point as T_0. Tw can be calculated from

$$T_w = \frac{2\sqrt{2}V_{od}}{dV/dt}, \tag{4.27}$$

where Vod is the overdrive voltage of the transistor M1 or M2, $V_{od} = \frac{2\frac{I_B}{2}}{g_{m1}} = \frac{I_B}{g_{m1}}$.

Transient responses of both output nodes (Q and QB) can be approximated by exponential waveforms with the same time constant $R_1 C_L$,

$$v_Q(t) = VDD - I_B R_1 (1 - e^{-\frac{t}{R_1 C_L}}), \tag{4.28}$$

$$v_{QB}(t) = (VDD - I_B R_1) + I_B R_1 (1 - e^{-\frac{t}{R_1 C_L}}). \tag{4.29}$$

It is easy to see that when $t = R_1 C_L \ln 2$, $v_Q(t) = v_{QB}(t) = VDD - \frac{1}{2} R_1 I_B$. So output zero crossing time

$$T_0 = R_1 C_L \ln 2. \tag{4.30}$$

The voltage noise variance changes according to the following equations,

$$\sigma_V^2(t) = \begin{cases} \sigma_V^2(1-e^{-\frac{2t}{R_1C_L}}), & t \le T_w \\ \sigma_V^2(T_W)e^{-\frac{2t}{R_1C_L}}, & t > T_w \end{cases}. \tag{4.31}$$

The first part of the above equation means that the variance of the voltage noise increases exponentially during the time window Tw and tends to an asymptotic value σ_V^2. The second part of the above equation means that after the time window, no noise is injected to the load and the voltage noise decays exponentially with time constant R_1C_L. At the output zero crossing time instant T0, the variance of the voltage noise will be

$$\sigma_V^2(T_0) = \sigma_V^2(1-e^{-\frac{2T_w}{R_1C_L}})e^{-\frac{2T_0}{R_1C_L}} \approx \sigma_V^2 \bullet \frac{2T_w}{R_1C_L} \bullet \frac{1}{4} = \sigma_V^2 \frac{T_w}{2R_1C_L}. \tag{4.32}$$

The timing jitter due to differential pair M1 and M2 is

$$\sigma_{t,diff}^2 = \frac{\sigma_V^2 \dfrac{T_w}{2R_1C_L}}{\dfrac{I_B^2}{C_L^2}} = \frac{2\dfrac{kT\gamma_1 g_{m1}R_1}{C_L}\dfrac{2\sqrt{2}\dfrac{I_B}{g_{m1}}}{\dfrac{I_B}{C_L}}\dfrac{1}{2R_1C_L}}{\dfrac{I_B^2}{C_L^2}} = \frac{2\sqrt{2}kT\gamma_1 C_L}{I_B^2} \tag{4.33}$$

D. Total timing jitter

Combined all the noise contributions, the total timing jitter for a SCL logic latch is

$$\sigma_{t,scl}^2 = \frac{2kTC_L}{I_B^2}(1+\sqrt{2}\gamma_1 + \frac{\gamma_7 g_{m7}R_1}{2}) \tag{4.34}$$

4.6.1.2 CMOS logic

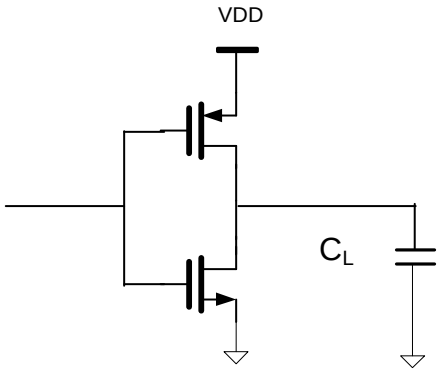


Figure 4.10 Inverter in CMOS logic

The basic building block of CMOS logic is an inverter. An estimate of the timing jitter from design parameters of an inverter can be obtained as follows. It assumes an inverter driving another identical inverter. Let the output impedance of the first inverter be R_o and the load capacitance be C_L. Then the input of the second inverter will be subjected to a first order low pass filter function with 3dB cut-off frequency $f_c = \frac{1}{2\pi R_o C_L}$. For first order low pass filter, the noise bandwidth is $\frac{\pi}{2} f_c$ .The RMS voltage noise

$$V_n = \sqrt{4kTR_o \frac{\pi}{2} f_c} = \sqrt{\frac{kT}{C_L}} . \tag{4.35}$$

The slew rate of the periodic signal when it crosses the threshold is approximated by

$$\frac{dV}{dt} = 2 f_c V_s = \frac{V_s}{\pi R_o C_L}, \tag{4.37}$$

where V_s is the logic signal swing. The jitter is

$$\sigma_{t,cmos} = V_n / \frac{dV}{dT} = \frac{\pi\sqrt{kTC_L}R_o}{V_s} \ . \tag{4.38}$$

For CMOS logic, we can get

$$R_o = \frac{V_{DD}}{\frac{K_p}{2}\frac{W}{L}(V_{DD} - V_{TH})^2}, \tag{4.39}$$

$$C_L = C_{ox}WL, \tag{4.40}$$

$$\sigma_{t,cmos} = \frac{\pi\sqrt{kTC_L}R_o}{V_{DD}} = \sqrt{kTC_{ox}\frac{L^3}{W}}\frac{2\pi}{K_p(V_{DD} - V_{TH})^2}, \tag{4.41}$$

where C_{ox}: process oxide capacitance,

K_p: the process transconductance constant (A/V^2)

W and L: the width and length of the device.

4.6.2 Charge pump phase noise

To eliminate the dead zone, many PFD/CP circuits enable both up and down current paths charge pumps briefly. This results in some feed-through of the charge pump current noise. CP generates noise only when it turns on. Let the duration of charge pump turning on time be τ. In average, the current noise at the output of charge pump is

$$I_{n,cp}^2 = \overline{I_n^2}\frac{\tau}{T} = 4kT\gamma g_m \frac{\tau}{T}, \tag{4.42}$$

where T is PFD comparison period, γ and g_m are the noise factor and transconductance of the charge pump transistor. Referring the noise back to the input of PFD, we get the effective jitter due to CP noise

$$\sigma_{CP}^2 = \frac{I_{n,cp}^2}{I_{cp}^2 F_c} = \frac{4kT\gamma g_m \tau}{I_{cp}^2}, \tag{4.43}$$

where Icp is the charge pump sinking or sourcing current.

4.7 Low phase noise PFD/CP/Divider design

4.7.1 Dead zone free PFD/CP

These equations derived from the analysis in section 4.4 are used for a PFD/CP design in TSMC 0.25um CMOS process. The chosen charge pump current is 1mA. From calculation, the CP switching time is about 2ns, the reset delay of PFD is set to be 3 ns to avoid dead zone. Figure 4.11 shows the simulated average charge pump current v.s. phase error for two different reset delays. Figure 4.7 shows that if the reset delay is longer than charge pump switching time, the dead zone does not appear.

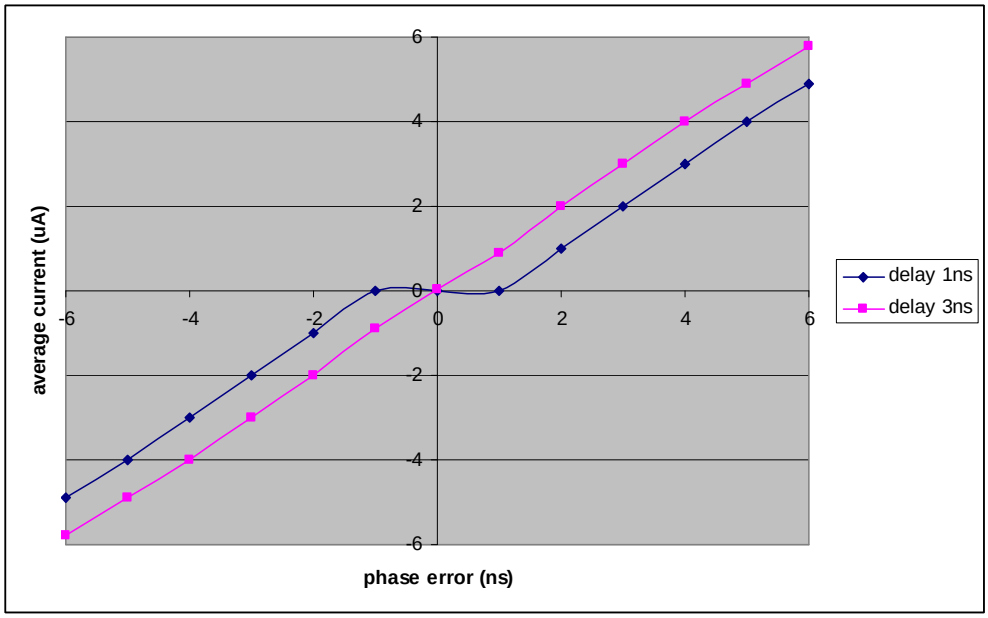


Figure 4.11 Simulated average charge pump current v.s. phase error for different reset delays

Based on the charge pump turning on time, we can predict the charge pump phase noise contribution. From equations in section 4.6.2, we get the timing jitter due to charge pump noise as

$$\sigma_{CP} = \sqrt{\frac{4kT\gamma g_m \tau T}{I_{cp}^2}} = 1.2\text{ps} . \quad (4.44)$$

In the calculation, we use the following circuit design parameter for the charge pump.

$\gamma = \frac{2}{3}$, noise parameter of current source transistor in charge pump

$g_m = 3mS$, transconductance of current source transistor in charge pump

$\tau = 3ns$, duration of charge pump turning on time

T = 1us, PFD comparison period

Icp =1mA, charge pump sinking or sourcing current.

The predicted 1Hz normalized phase noise floor due to charge pump is

$$L_{1Hz,CP} = 20\lg(2\pi\sigma_{CP}) = -223 \text{ dBc/Hz.} \quad (4.45)$$

4.7.2 Prescaler

The frequency divider design is targeted for the frequency synthesizer in WLAN 802.11b/g transceiver. In the design, the prescaler is a dual modulus divide by 32/33 analog divider. It consists of a divide by 4/5 synchronous counter followed by three asynchronous $\div 2$ counter. The prescaler is designed using Source Coupled Logic (SCL). The presence of interconnection stray capacitances requires a minimum bias current of the latches to be able to operate at high frequency. In order to guarantee a correct operation of the prescaler up to 2.5 GHz over process and temperature variations, the SCL latches of the $\div 4/5$ divider requires a minimum current of 750

uA. The differential peak voltage is limited to 600mV. The load capacitance is 120 fF, including the interconnection capacitance given by post-layout extraction. The second divider stage has an input frequency of at most 1.25 GHz, thus the speed requirements of this stage are relaxed and its power consumption can be reduced. This is obtained by biasing the latches at 250uA and maintaining the voltage peak at 600mV. Obviously, the transistor widths are scaled down. The resultant load capacitance is 60 fF. This scaling could be repeated theoretically at each following stage. However, the reduction of biasing current would deteriorate the prescaler noise performance, the bias current of the following $\div 2$-dividers have not been scaled further.

The estimation of the phase noise of the total prescaler has to take into account all the cascaded stages. The contribution of the first stage (i.e., the $\div 4/5$-divider) is estimated be be -235dBc/Hz. The contribution of the following three $\div 2$-dividers is higher, since their latches are biased at lower current (250 uA). Each one of $\div 2$-dividers contributes to the output phase noise for -230dBc/Hz. Summing contributions of all stages, we obtain the predicted 1Hz normalized phase noise floor due to SCL logic as

$$L_{1Hz,SCL} = -225\,\text{dBc/Hz}. \tag{4.46}$$

4.7.3 CMOS divider and PFD

The A counter is implemented by a 5-bit counter while M counter need to be 7 bit. The CMOS logic circuits in these counters and PFD contributes phase noise to the output according to the equations derived in 4.6.1.2. The design parameters that affect the CMOS logic phase noise are the sizes of the devices. It is easy to see a large W/L

ratio is beneficial for phase noise performance. So minimal length device is used for CMOS logic. The determination of device width depends also on the area and power consumption. The predicted 1Hz normalized phase noise floor due to CMOS logic is

$$L_{1Hz,SCL} = -228 \text{ dBc/Hz}. \quad (4.47)$$

4.7.4 Prediction of total phase noise from PFD/CP/Divider

Summing contributions from PFD, CP and divider, the predicted total 1Hz normalized phase noise floor is

$$L_{1Hz} = -219 \text{ dBc/Hz}. \quad (4.48)$$

This prediction will be compared with the measurement result in chapter 5.

Chapter 5: Experimental Prototype Design

5.1 Introduction to the WLAN 802.11b/g RF transceiver

The design techniques in the previous chapters are used in the design of a complete prototype RF synthesizer. The frequency synthesizer is to be embedded in a single chip transceiver for 2.4GHz ISM band WLAN 802.11b/g application.

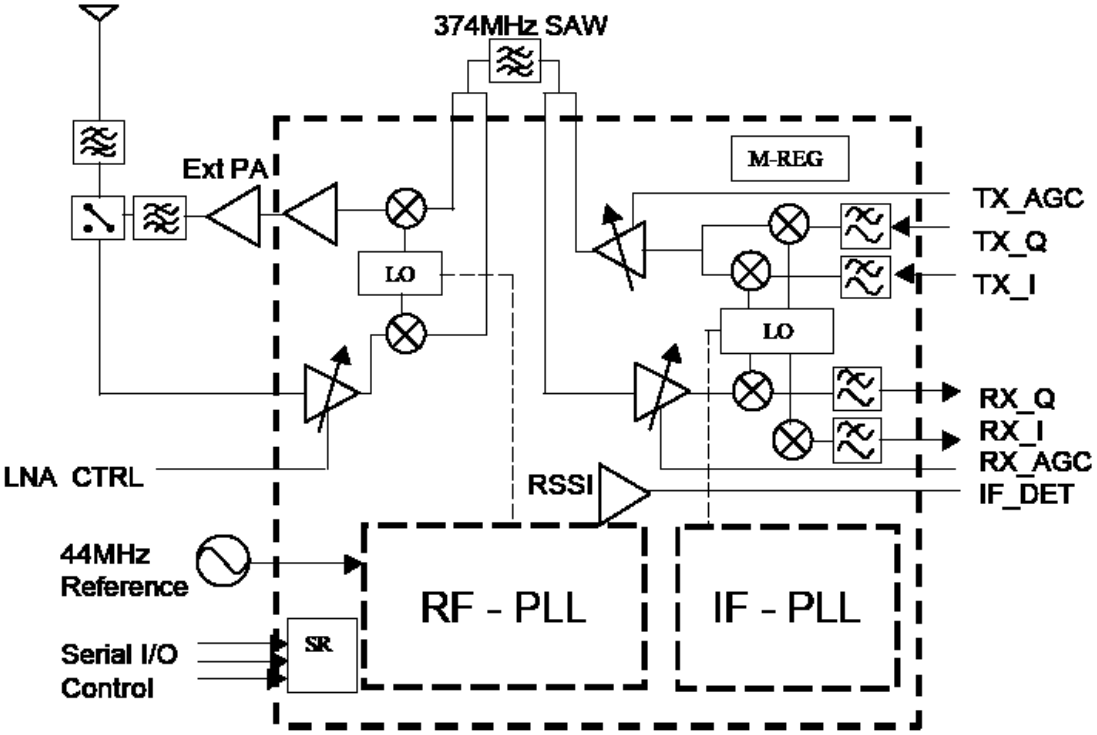


Figure 5.1. 802.11b/g RF transceiver block diagram

For 2.4GHz WLAN applications the super-heterodyne architecture has the potential to consume less power and have lower cost than a direct conversion transceiver [Kong04-2, Kong04-3]. The image problem can be solved using careful frequency planning and narrow band response of Low Noise Amplifier (LNA)

without the troublesome image rejection filter. Figure 5.1 shows the block diagram of the CMOS transceiver that employs the super-heterodyne architecture. The receiver down-converts the RF signal to baseband in two steps. The IF is chosen to make the image band falls in a quiet band. Then the image can be sufficiently rejected by external band selection filter and on chip narrow band LNA. With an IF of 374MHz and the implemented 2.4GHz LNA, the image at 1.7GHz is rejected by more than 50dB which is enough for this application.

5.2 Determining specifications of the frequency synthesizer

The RF and IF PLL are used to generated the LO signals for up and down conversion mixers. The design requirements for the PLL can be derived from the WLAN 802.11b/g system specifications. Channel selection is performed with the RF LO. The 14 channels in 802.11b/g span the frequency range from 2412MHz~2484MHz.

Tuning-range specification

With a fixed IF of 374MHz, the RF LO must cover 2038MHz~2110MHz. For 802.11b/g applications, the tuning range must cover the entire 72 MHz for the given band. The tuning range is determined by the VCO used in the PLL. The VCO described in chapter 3 has a tuning range of 1.9~2.2GHz. We will use the VCO described in chapter 3 in the prototype design.

Phase-noise specification

Because IEEE 802.11b/g specifies multiple data rates up to 54 Mbits per second, using BPSK, QPSK, 16-QAM and 64-QAM modulations, phase-noise requirements vary for each case. Phase noise is typically specified in terms of RMS phase error. A simplified method to approximate the LO phase noise requirements is as follows:

1. Identify the bit rate, modulation, coding rate.

2. Calculate maximum rms phase error per symbol allowed based on the maximum bit error rate (BER).

Data rate (Mbits/s)	Modulation	Coding rate
6	BPSK	1/2
9	BPSK	3/4
12	QPSK	1/2
18	QPSK	3/4
24	QAM16	1/2
36	QAM16	3/4
48	QAM64	2/3
54	QAM64	3/4

Table 5.1. Different data rates of 802.11g

Table 5.1 summarizes the bit rate, coding rate and modulation for 802.11g. The most phase noise sensitive case for 802.11g is 54M bits per second with 64-QAM, which has a minimum constellation angle difference of 9.5 degrees. Because 802.11g utilizes interleaving and forward error correction, acceptable channel BER is 10^{-4}. For 64-QAM, the total required carrier to noise ratio (C/N) at 10^{-4} BER is 17 dB. Although calculating the precise degradation due to phase error requires rigorous mathematical derivation and statistical analysis, a worst case limit can be estimated by assuming both local oscillator (LO) phase error and channel noise have a Gaussian

distribution and combine accordingly. Because LO phase noise will act as an irreducible noise floor, the carrier to noise ratio due to LO phase noise (C/N_{lo}), must be >> 17 dB for 64-QAM. This means total integrated phase noise over one symbol should be less than at least 27 dBc for negligible impact on the BER. This converts to the maximal RMS phase error of 3 degree.

Locking time specification

When the system changes its operating frequency to a different channel, frequency synthesizer must track the frequency change. The standard requires the PLL completes the frequency change in 150us.

The design specs are summarized in Table 5.2.

Operating Frequency	2038~2110MHz
Phase Noise	RMS phase error < 3°
Locking time	150 us

Table 5.2 802.11b/g RF synthesizer specifications

5.2 Prototype design

The synthesizer consists of phase/frequency detector, charge pump, loop filter, VCO, main divider and reference divider. The VCO and PFD/CP/Divider circuit design is covered in detail in chapter 3 and 4. Here we will briefly discuss the design in the system level.

5.2.1 Frequency plan

A good frequency plan is crucial to achieving all the specifications with a minimal amount of hardware and power consumption.

First we need to select reference frequency. It is desirable to develop a frequency plan where only one external crystal reference oscillator is used in the whole system including the baseband chip. Most available 802.11b/g baseband chips on the market use a clock of 44MHz. So a crystal oscillator of 44 MHz is used as the reference for both RF and IF frequency synthesizers.

Next we need to decide PFD comparison frequency. A higher comparison frequency has many benefits. With a higher comparison frequency, we could use a lower divider ratio in PLL and the in band phase noise floor could be reduced. A higher comparison frequency also enables a wider loop bandwidth which helps to achieve fast locking. But for PLLs of integer-N architecture, the comparison frequency is limited by the channel spacing of the target application. For our RF frequency synthesizers, the comparison frequency must be selected to cover all the 14 channels of 802.11b/g standard. We know that most channel spacings are 5MHz except that the last one is 12MHz. So the largest comparison frequency we could use is 1MHz. With 1MHz comparison frequency, the main divider ratio should be programmable as 2038, 2043,**…**, 2098, 2110. The reference divider ratio is fixed at 44.

For IF LO, we need 374MHz I/Q (In phase/Quadrature phase) signals. One simple method to generate I/Q signal is to use a divide by two circuit with an input signal of double frequency. So IF frequency synthesizer output should be fixed at 748MHz.

Here we can use a higher comparison frequency because the desired frequency is fixed. The comparison frequency is chosen to be 5.5MHz. Then the main divider ratio should be 136 while the reference divider ratio is 8.

In the following discussion, we will focus on the RF PLL. It must be programmable and is at higher frequency. Its design is more challenging and its performance determines the overall LO path performance for the transceiver.

5.2.2 Frequency divider programming

As discussed in section 4.1.2, the programmable divider in the RF frequency synthesizer consists of a dual modulus P/P+1 prescaler and M, A counters in a pulse swallow architecture. The divider ratio is determined by the M, A counter configuration and can be calculated as MP+A. With 32/33 prescaler, the configuration of the A and M counters for 14 channels of IEEE 802.11b/g is shown in Table 5.3.

Channel number	Channel Frequency (MHz)	A-counter	M-counter	Divider Ratio	RF VCO Frequency (MHz)
1	2412	22	63	2038	2038
2	2417	27	63	2043	2043
3	2422	0	64	2048	2048
4	2427	5	64	2053	2053
5	2432	10	64	2058	2058
6	2437	15	64	2063	2063
7	2442	20	64	2068	2068
8	2447	25	64	2073	2073
9	2452	30	64	2078	2078
10	2457	3	65	2083	2083
11	2462	8	65	2088	2088
12	2467	13	65	2093	2093
13	2472	18	65	2098	2098
14	2484	30	65	2110	2110

Table 5.3 Configuration of A and M counters

5.2.3 Loop filter design

The chosen loop filter is a second order passive network. There are several considerations in the selection of the loop bandwidth.

First, the loop bandwidth is usually chosen to be smaller than 1/10 of PFD comparison frequency to ensure the stability of the loop. Our analysis of the PLL is based on the continuous time linear model for the loop. But PLL with digital phase detector is a discrete time system in the strict sense. The continuous time approximation is valid only if the loop bandwidth is much smaller than PFD comparison frequency. When the loop bandwidth is more than 1/5 of PFD comparison frequency, there is a great risk of instability even when there is enough phase margin from continuous time analysis. The discrete time effect could easily

introduce additional delays and destroy the stability in reality. For our case, the comparison frequency is 1MHz. Then the loop bandwidth must be smaller than 100 kHz.

Second, the loop bandwidth must be large enough to meet the locking time requirement. The accurate locking time calculation is pretty complex. A rule of thumb equation for the estimation of locking time (LT) for a PLL is

$$LT \approx \frac{0.2}{F_c}\left(1 - \lg\frac{\varepsilon}{\Delta F}\right), \tag{5.1}$$

where Fc: loop bandwidth

ε: frequency tolerance, when the frequency difference is smaller than ε, the PLL is considered to be relocked

ΔF: frequency jump, equal to the difference of initial and final frequency

With the worst case of ΔF =72MHz and ε =100Hz, to meet the requirement of LT=150us, we get Fc = 10kHz. This is the minimal loop bandwidth to meet the locking time requirement.

Third, there is an optimal loop bandwidth to minimize the integrated RMS phase error. Figure 5.2 shows the simplified output phase noise spectrum for different loop bandwidth. As discussed in chapter 2, there are two distinct regions in the output total phase noise spectrum. In the region where offset frequency is smaller than loop bandwidth, the phase noise flattens out as an in band phase noise floor. In the region where offset frequency is larger than loop bandwidth, the phase noise declines in the slope of about -20dB/decade. The selection of the loop bandwidth will determine the PLL total phase noise for the given VCO and PFD/CP/Divider design. When the loop bandwidth is too small, the VCO phase noise is not suppressed enough, figure 5.2(b).

When the loop bandwidth is too large, the in band phase noise floor would contribute more noise to the output, figure 5.2 (c). The optimal loop bandwidth in terms of phase noise is at the intersection of in band phase noise floor and the out of band VCO phase noise. With this optimal loop bandwidth, the phase noise contributions of PFD/CP/Divider and VCO are balanced and the minimal RMS phase error is achieved, figure 5.2 (a).

The determination of the final loop bandwidth must take into account all the above considerations. The optimal loop bandwidth in terms of phase noise may not meet the stability or locking time requirement. In that case, phase noise performance must be traded off to meet the other two specifications. Fortunately in our design, the optimal loop bandwidth for minimal RMS phase error is 20 kHz. This loop bandwidth can meet both of the other requirements. So 20 kHz is selected to be the loop bandwidth. From the loop bandwidth of 20 kHz and phase margin of 60 degree, the R, C component values in the loop filter can be decided.

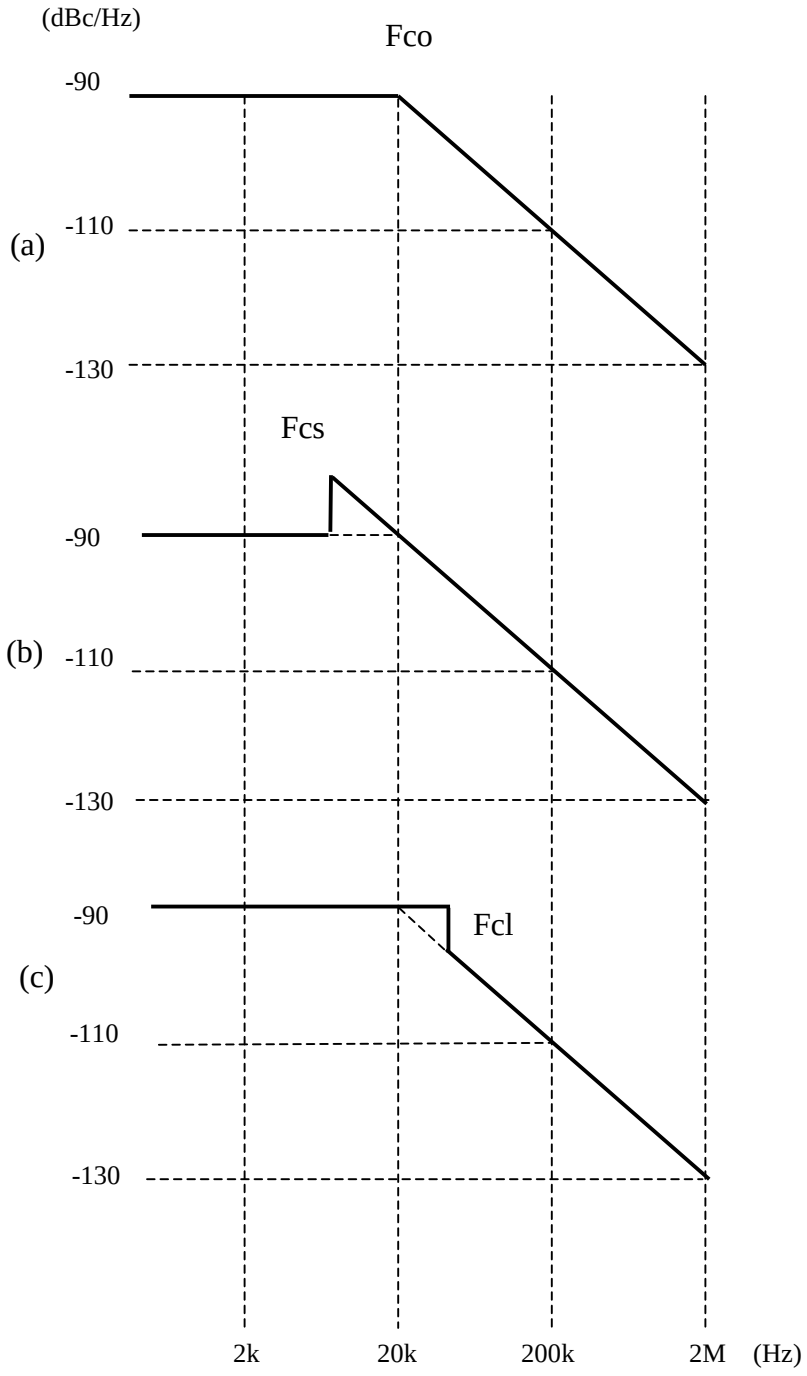


Figure 5.2 PLL output phase noise spectrum at different loop bandwidth.

(a) optimal loop bandwidth (b)loop bandwidth is small (c) loop bandwidth is large

5.3 Measurement results

The 802.11b/g transceiver described above is fabricated in TSMC 0.25um CMOS process. The die photograph of the entire chip is shown in figure 5.3.

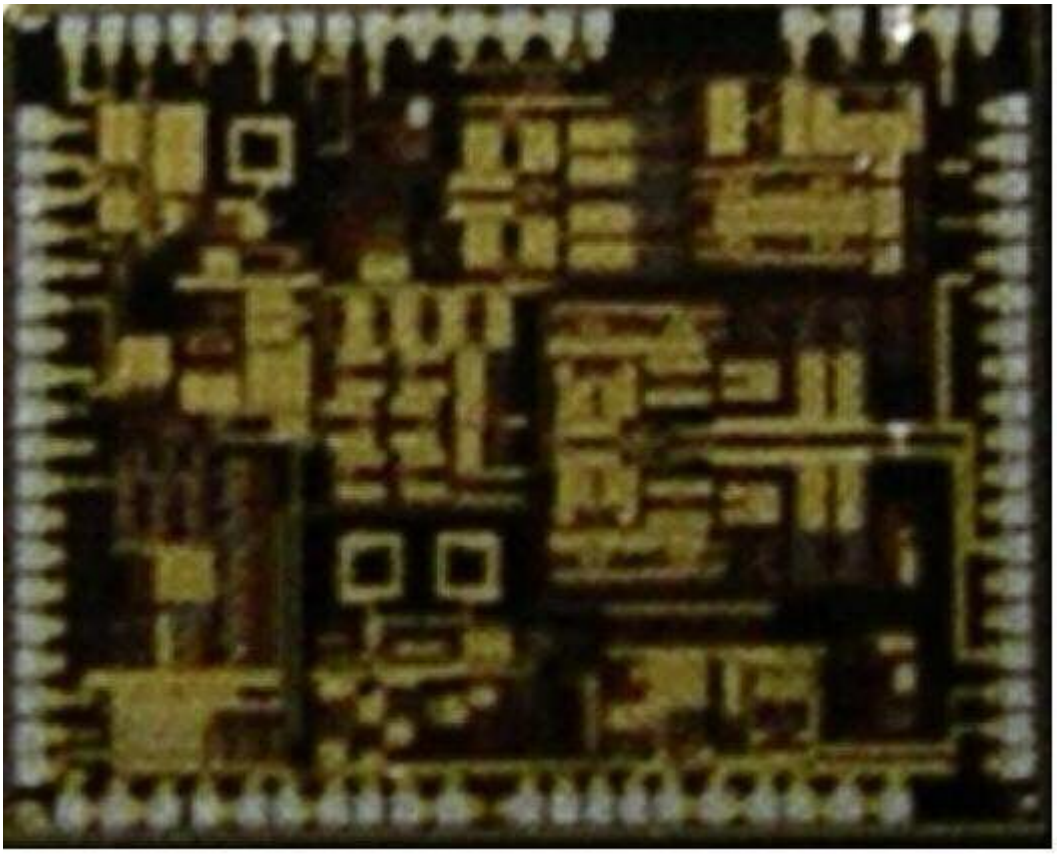


Figure 5.3 Photograph of the entire 802.11b/g transceiver IC.

The part including the frequency synthesizers is shown in figure 5.4.

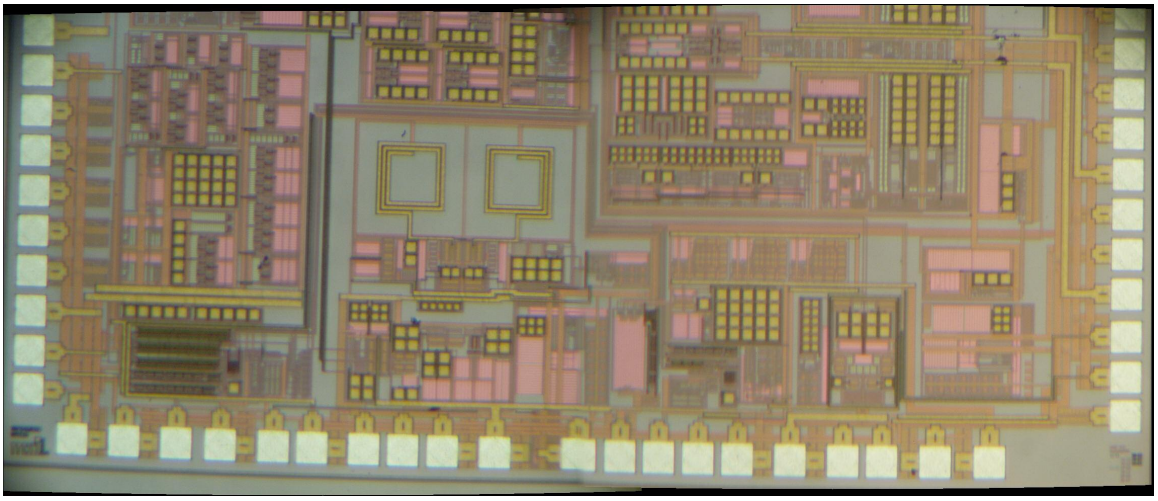


Figure 5.4 Part of the transceiver including frequency synthesizers.

The chip is packaged in a 64-pin TQFP package and tested on a FR-4 evaluation board. The evaluation PCB board is show in figure 5.5

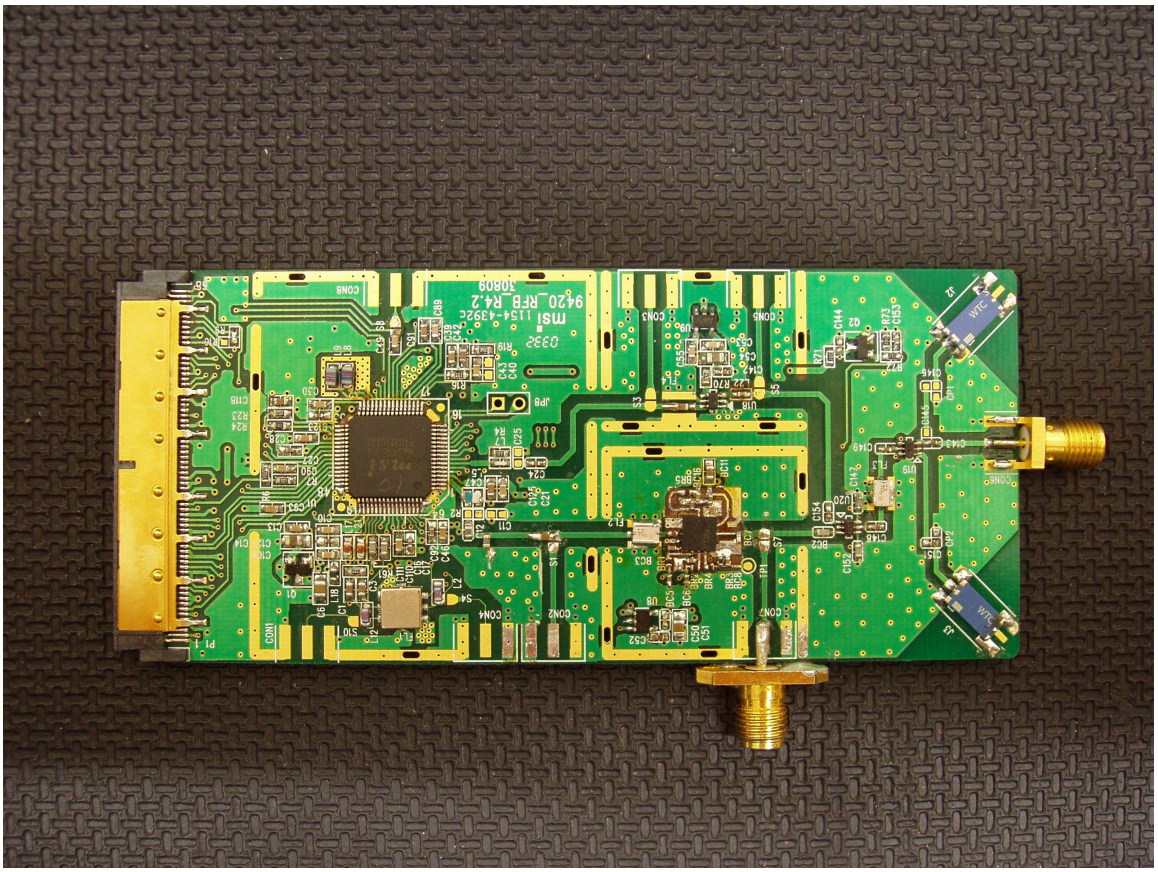


Figure 5.5 Evaluation PCB board.

Figure 5.6 shows the RF LO output spectrum when the chip is programmed to work in channel 1. For channel 1, the LO frequency should be at 2.038GHz.

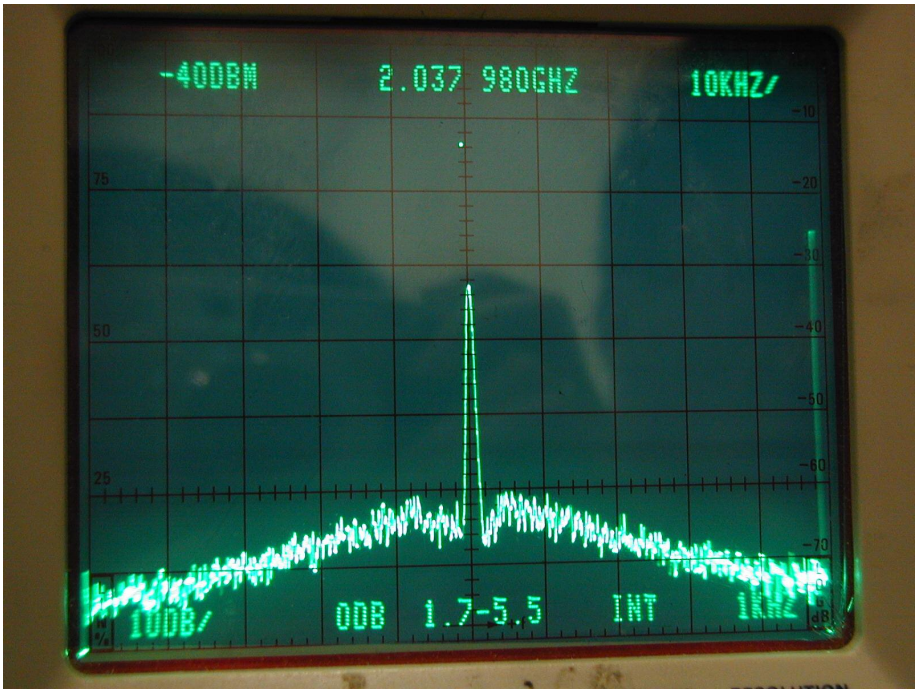


Figure 5.6 RF PLL output spectrum operating in channel 1

Because the PLL is embedded in the transceiver, we can access the LO signal only from the leakage to ground. The power level of the leakage signal is too low for the phase noise measurement. In stead of measuring the LO signal itself, we measure the phase noise of the signal at transmitter Power Amplifier (PA) output. The measured phase noise in this way is the combined result of RF and IF PLL. Because the RF PLL is dominant in terms of phase noise performance, the measured combined phase noise result should be close to the RF PLL phase noise.

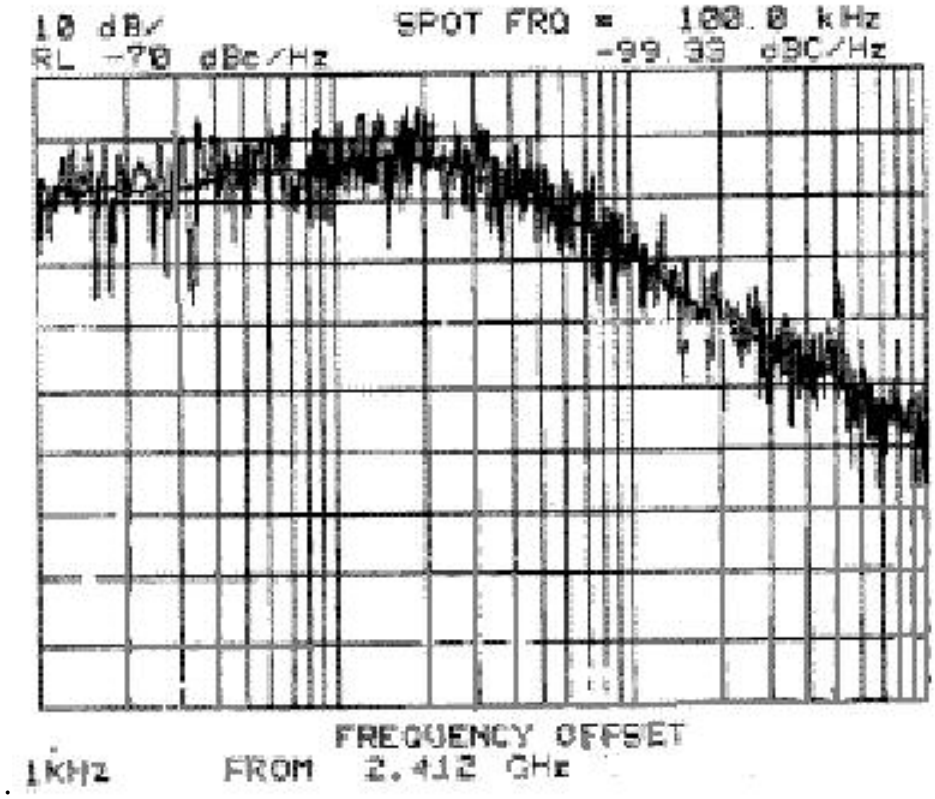


Figure 5.7 Phase noise measurement result at transmitter PA output

Figure 5.7 shows the phase noise measurement result at the transmitter output. The output signal is at 2.412GHz, the first channel in 802.11 b/g standard. The loop bandwidth is at 20 kHz. The out of band region has a slope of -20dB/decade. At 1MHz, the measured phase noise is about -125 dBc/Hz. It is the same as the free running VCO as show in chapter 3. The measured in band phase noise floor is at about -88dBc/Hz.

In chapter 4, the predicted 1Hz phase noise floor due to PFD/CP/Divider is -219dBc/Hz. The prediction of in band phase noise floor can be calculate as

$$L_{floor} = L_{1Hz} + 10\lg F_c + 20\lg N \qquad (5.2)$$

With Fc = 1MHz and N =2038, the predicted in band phase noise floor is -89dBc/Hz, which is very close to the measurement result.

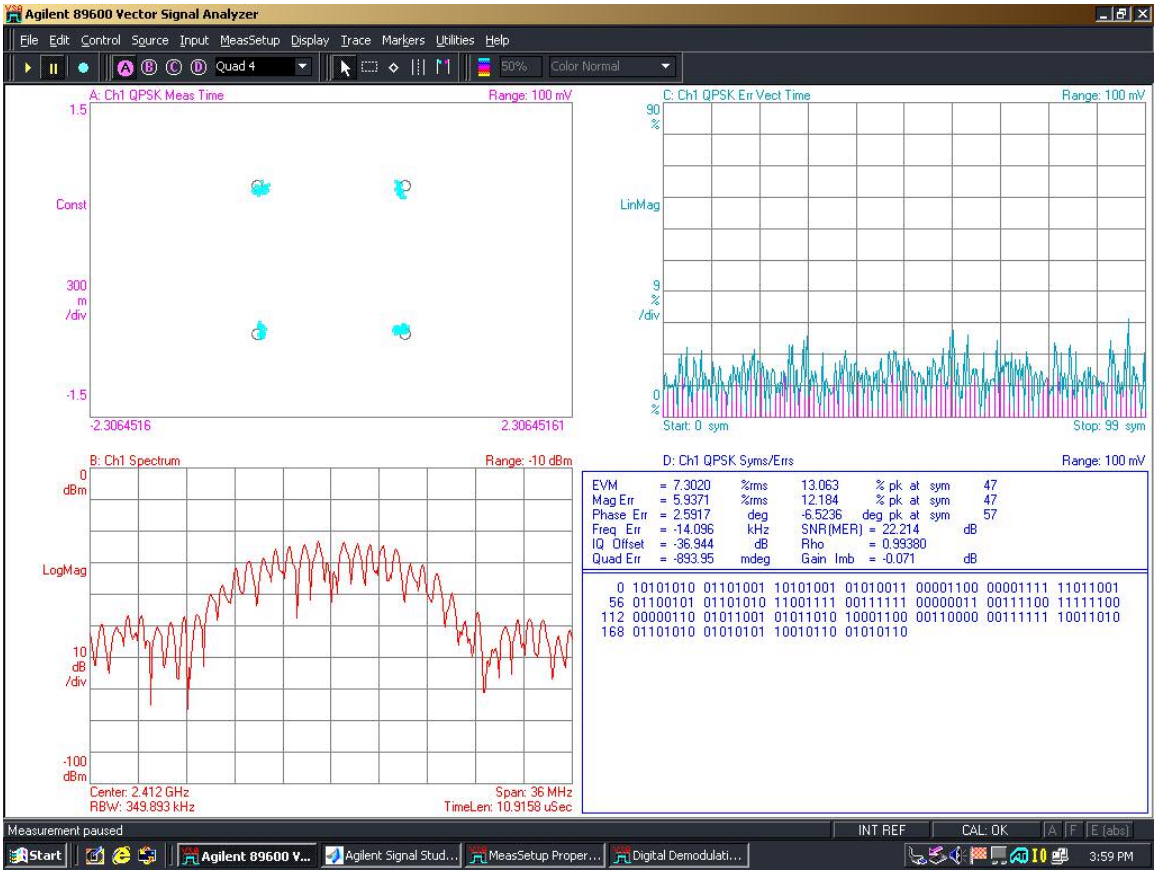


Figure 5.8 Transmitter EVM measurement result

Figure 5.8 shows Error Vector Magnitude (EVM) measurement result using Agilent 89600 Vector Signal Analyzer (VSA) at the transmitter output. The transceiver is working at QPSK modulation mode. The average EVM is less than 7.5% which is better than standard requirement of 15%. This measurement also gives

the RMS phase error of 2.6 degree, which meets our design targets of less than 3 degree.

Chapter 6: Conclusions

The goal of this Ph.D. research is to develop design techniques for low phase noise PLL based frequency synthesizers. As stated in chapter 2, the VCO and PFD/CP/Divider are the main phase noise contributors for out of band and in band regions of closed loop PLL respectively. The first part of this Ph.D. work is to study the VCO phase noise generation mechanism and design techniques for low phase noise VCO. Based on the understanding of phase noise generation process in cross-coupled CMOS LC VCO, a simple yet accurate analytical phase noise model was derived. A 2GHz low phase noise CMOS LC VCO was designed, simulated and measured. The simulation and measurement results confirm the proposed VCO phase noise model.

Next, the design scheme for low phase noise PFD/CP/Divider was investigated. The non-ideal operation, such as dead zone, could affect the PFD/CP phase noise performance a lot. A systemic design scheme for avoiding dead zone problems in PFD/CP was presented and verified by simulation. Due to the presence of many digital components in PFD/CP/Divider, its phase noise model was studied from the point of view of timing jitter. The analytic equation that relates the PFD/CP/Divider 1Hz normalized phase noise floor and circuit parameters was derived.

To experimentally confirm the developed design techniques, a complete PLL based frequency synthesizer prototype was designed and fabricated. The measurement results confirm the validity of theory analysis.

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