ABSTRACT

Dissertation Title: THE DEVELOPMENT OF COST AND SIZE ANALYSIS FOR THE ASSESSMENT OF EMBEDDED PASSIVES IN PRINTED CIRCUIT BOARDS

Bevin T. Etienne, Doctor of Philosophy, 2005

Dissertation directed by: Associate Professor Dr. Peter Sandborn
Department of Mechanical Engineering

Passive components are electrical components that do not provide amplification or gain. The primary functions of passive components are to manage buses, bias, decouple power and ground (bypass), filter, tune, convert, sense and protect. In 2001, passive devices accounted for 91% of all components, 41% of board area and 92% of all solder joints in an electronic system but only 2.6% were integrated in some fashion. The integrated circuit industry is achieving faster speeds by shrinking technology. This dictates that the passive solution must also shrink. In addition, the need to drive out every cent of costs, improve product reliability and the high passive to active ratios have motivated system manufacturers to consider higher levels of passive integration. These factors have increased interest in embedded passives.

This research examines the size and cost tradeoffs associated with the use of embedded passive technology for resistors and capacitors, and creates the models and methodology necessary to determine the coupled size/cost impact of embedding passives. It also examines the effects of embedding resistors on profit margin and throughput. A version of the model for performing tradeoff analyses is delivered via the CALCE Consortium and used by board manufacturers and system designers at this time. The

models developed have also been used to determine the optimal number of passive devices to embed in a given system by implementing them within a Multi-Population Genetic Algorithm (MPGA). Boards from several different applications are analyzed to demonstrate the applicability of the models and the optimization approach.

The effect of board size on the optimum embedded passive solution was studied and an assessment of whether better system solutions can be found was performed. The analysis has shown that the system size limitation when embedded passives are used is not only dependent on the quantity, type, and electrical properties of the embeddable components, but is, in fact, more dependent on layout constraints associated with the placement of the non-embeddable parts. Studies indicate that the higher the embeddable passive density, the greater the probability that placement can be improved when passives are embedded.

THE DEVELOPMENT OF COST AND SIZE ANALYSIS FOR THE ASSESSMENT OF EMBEDDED PASSIVES IN PRINTED CIRCUIT BOARDS

by

Bevin Thomson Etienne

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Advisory Committee:

Associate Professor Dr. Peter A. Sandborn, Chair (Advisor)
Professor Dr. Shapour Azarm
Associate Professor Dr. David Bigio
Associate Professor Dr. Jeffrey Hermann
Professor Dr. Vincent Brannigan

DEDICATION

To my parents

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CHAPTER 1 INTRODUCTION

1.1 Passive Components

By definition, passive components are devices that dissipate power or store energy, as opposed to active devices, such as transistors, that generate power gain [1]. Traditional passives are discrete devices, singular components enclosed in a single case, that are either through-hole or surface mounted onto a substrate. They are commonly referred to as "glue components" since they electrically "glue" integrated circuits (ICs) together to make the system. The most common examples of passive components are resistors, capacitors and inductors and their primary functions are to manage buses, bias, decouple power and ground (bypass), filter, tune, convert, sense and protect. Passive components are manufactured in many physical forms including discrete devices, integrated passive devices (arrays or networks), and embedded passives. Table 1-1 compares the various physical forms.

Table 1-1: Passive component's physical forms comparison [2]

	Discrete	Arrays and Networks	Integrated Passive Devices (IPD)	Embedded (Integral) Passives
Definition	A single passive element (capacitor, resistor or inductor) in a leaded or surface-mount case.	Passive arrays combine multiple passive elements of like function (e.g., all capacitors or all resistors) in a single surface-mount case. Networks combine passives or more than one function (e.g., capacitors + resistors) in a single surface-mount case. A network typically contains 4 to 12 elements.	Multiple passive elements of more than one function and possibly a few active elements (e.g., resistors + capacitors + diodes) in a single surface mount or ship scale package. Typically an IPD contains more than 20 elements. IPDs may also be referred to as "super components."	Passive devices that are buried in the substrate material rather than being mounted on top.
Cost	Good–The benchmark for all other technologies.	Better when local densities have 4 to 8 devices close together.	Better when high local densities are application specific	Better when average component density is above 3 devices/cm2 . Cost is panel size dependent.
Size	Good–Board area required for each and every device	Better–50% and greater board area savings over discretes.	Better–Application specific IPDs can replace dozens of components.	Best–No surface board area required because the devices are buried.
Performance	Good–Self-resonates at low frequencies.	Good–Self-resonates at low frequencies.	Better–Qualified out to several gigahertz (GHz).	Best–Ideal components; when buried underneath the integrated circuit (IC), it serves mainly to decrease lead length and avoid build up inductance of the connection loops.
Reliability	Good–Heavy use of solder joints	Better–Reduces solder joints slightly.	Better–Significantly reduces solder joints.	Best–Elimination of solder joints.
Flexibility	Best–Flexible for both design and manufacturing	Better than IPDs and embedded passives.	Better than embedded passives.	Good–Requires modeling and simulation.
Time to Market	Best–Flexibility allows quick turns.	Better–Simple quad and octal arrays can be designed in quickly	Good–IPDs require additional design iterations for wireability.	Fair–Most board shops require at least 5 to 7 days to fabricate an embedded passives board.
Availability	Best–Highly available from multiple sources.	Better–Standard parts from multiple suppliers.	Better–Non-standard parts from multiple suppliers.	Fair–Few suppliers.
Values	Best–All values available at commodity prices.	Better–Thick film arrays offer high values.	Good–Thin films have limited capacitor values.	Good–Currently limited to low values
Tolerances	Best–Tight tolerances at commodity prices.	Better–Both offer tight tolerances.	Better–Thin films offer tight tolerances.	Good–Loose tolerance, generally 5 to 10%.

1.2 Passive Growth

In 2000, the passive component market share in the US was estimated at $17.9 billion [3]. It is a huge, multi-billion dollar business, supporting electronic products in automotive, telecommunications, computer and consumer industries, for digital, analog and mixed signal applications. The resistor market in North America is expected to continue to be driven by the telecommunications and computer industries. Currently, Southeast Asia holds the largest share of the market at 47.1%, and it is driven by strong demand in the consumer electronics industry [4]. The US demand for passive components is forecast to increase 3.7 percent per year to $21.4 billion in 2005 [3].

Passive components are continuing to increase in use in electronic systems. There are a large number of passive components that are used in consumer electronic products such as VCRs, camcorders, television tuners, and other communication devices. Many analysts believed discrete passives would "integrate" away into integrated circuits, however, exactly the opposite has occurred [5]. In 1984, passive devices represented 25% of all components on printed circuit boards; by 1998 this fraction grew over 90% (Figure 1-1). In 2001, passive devices accounted for 91% of all components, 41% of the board area and 29% of all solder joints [6].

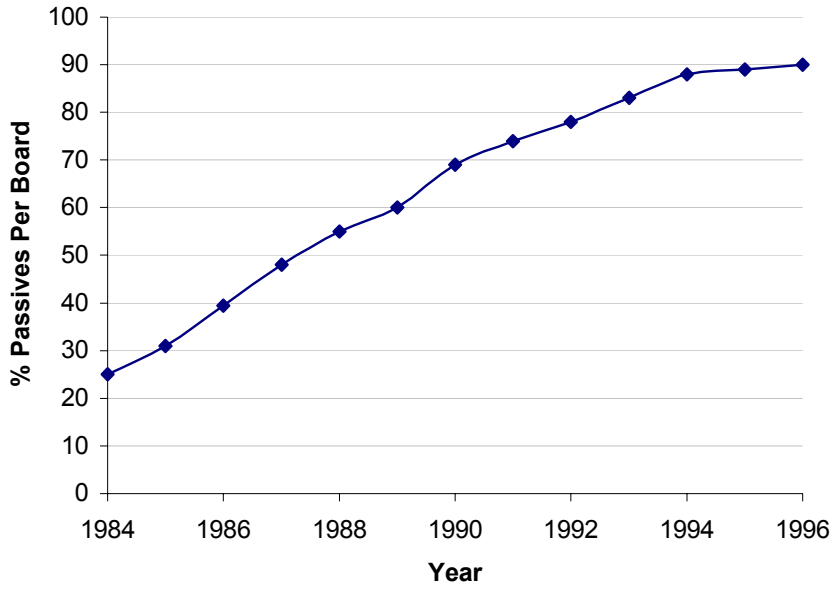


Figure 1-1: Growth of passive components in electronic systems [7]

Studies have shown that the number of passive components is still greater than 80% of the total part count (e.g., Figure 1-1) and the passive-to-active ratios continue to rise in applications like PDAs, cellular phone and other portable electronic devices [8]. Table 1-2 also illustrates the passive-to-active ratio in recent products.

Table 1-2: Passive-to-active ratio of recent products [9]

System	Total Passives	Total Ics	Ratio
Cellular Phones			
Ericsson DH338 Digital	359	25	14:1
Ericsson E237 Analog	243	14	17:1
Philips PR93 Analog	283	11	25:1
Nokia 2110 Digital	432	21	20:1
Motorola Mrl 1.8 GHz	389	27	14:1
Casio PH-250	373	29	13:1
Motorola StarTAC	993	45	22:1
Matsushita NTT DoCoMo	492	30	16:1
Consumer Portable			
Motorola Tango Pager	437	15	29:1
Casio QV10 Digital Camera	489	17	29:1
1990 Sony Camcorder	1226	14	33:1
Sony Handy Cam DCR-PC7	1329	43	31:1
Other Communication			
Motorola Pen Pager	142	3	47:1
Infotac Radio Modem	585	24	24:1
Data Race Fax-Modem	101	74	7:1
PDA			
Sony Magic Link	538	74	7:1

Given the steady growth of passive utilization, the drive for miniaturization of electronic systems, the electronics industry has been forced to seek innovative ways to satisfy demands to pack more functionality into less space and reduce costs. The industry has responded by developing smaller discrete passive components and improved efficiencies and automation in the assembly process. One of the solutions to accommodate passive growth is integrating multiple passives together within a single package as networks or arrays of passives. According to a study by Prismark Partners LLC in 1996, 880 billion passive components were built of which only 2.6%, (22.86 billion passive components) were integrated and a more recent study showed that in 2001 alone, approximately 1 trillion passive components were consumed with still only 26 billion, or 2.6%, passive devices integrated in some fashion [6]. This shows that although there has been an increase in the integration of passive the percentage of integration has remained the same over the years. Table 1-3 provides a market forecast for passive arrays through 2004.

Table 1-3: Passive array forecast [6]

	2000		2004	
	Units*	Value**	Units*	Value**
Resistor Chip Arrays	6.60	$99.0	10.8	$140.0
Capacitor Chip Arrays	1.47	$102.6	2.36	$145.0
R/C Networks and Arrays (Chips)	0.36	$33.0	0.58	$46.6
Total Chip Arrays (Chips)	8.43	$234.6	13.74	$331.6
Total Thin Film Arrays and Networks	0.85	$55.0	2.0	$105.0
Total Arrays (Thick and Thin Film)	9.28	$289.6	15.74	$436.6

* Billion
** Million

Integrating passives into arrays and networks can reduce assembly costs and free surface space on substrates, however, the per unit cost of integrated passives remains higher than the discrete passive components they replace. The needs to reduce cost, miniaturization, improved product reliability and the passive to active ratios have brought

about interest in embedded passives. Embedded passives (EPs) are buried inside the substrate material, and while EPs will never replace all passive components, they provide a potential advantage for many applications.

1.3 Embedded Passives (EPs)

Passives, embedded into a substrate, are considered the Holy Grail in terms of integration [10]. Embedded passives, also known as "integral" passives, are passive components buried within the layers of the interconnecting substrate (the substrate is the electrical interconnection between the components, e.g., a printed circuit board). The substrate could be ceramic, a laminate (e.g., printed circuit board), or a deposited thin film. As long as the passive elements are inside of the substrate, they are called embedded passives. The defining characteristic for embedded passives is the fact that the device does not need to be mounted on or connected to the exposed substrate surface [2]. It provides the ability to free surface space area to add more active devices and has the potential of increasing functionality in small electronic systems. Although capacitors, resistors and inductors are all candidates for embedding, current interests are focusing on capacitors and resistors since they represent the majority of passive devices used on a circuit board. Inductors are currently used in such low quantities, that the equivalent per part cost is too high to incorporate any special processes or materials to make embedding inductors economically viable. The generic single board computer is generally composed of 5% integrated circuits, 4% connectors, 40% capacitors, 33% resistors and 18% miscellaneous parts [12]. Both embedded resistors and capacitors can be fabricated in singulated value form while capacitors can also be manufactured in distributed planar form. Figure 1-2 shows a cross sectional view of a printed circuit board containing

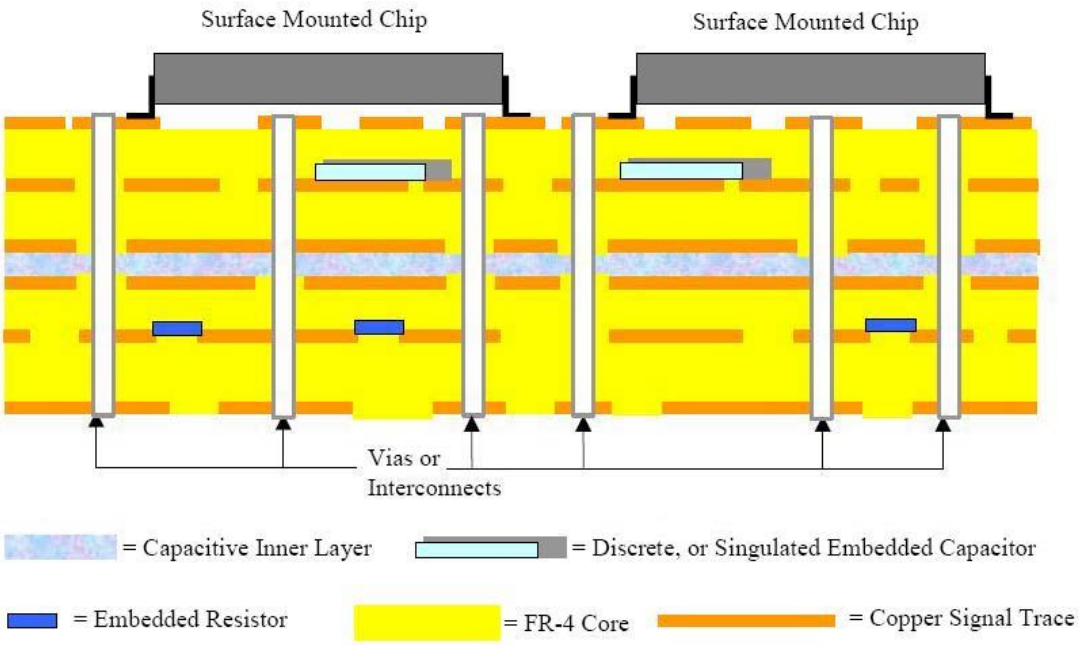


Figure 1-2: Cross-sectional view of a printed circuit board [11]

embedded passive components freeing up real estate on the substrate surface, which can be used for integrated circuits for added functionality or the board size can be decreased to obtain a smaller footprint.

Figure 1-3 shows the real estate savings and size reduction that is possible (in part) by embedding passives.

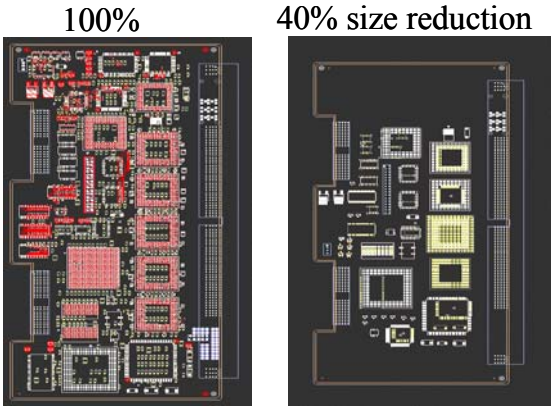


Figure 1-3: Real estate savings and size reduction by embedding passives (Nortel Networks)

1.3.1 Embedded Resistors

Thin and thick-film technologies are used to manufacture embedded resistors by depositing and pattering layers of resistive material in conjunction with an interconnect line within a substrate as shown in Figure 1-4. Replacing surface mount resistors with

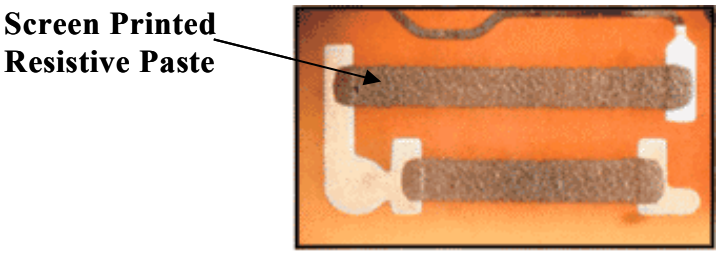


Figure 1-4: Embedded resistor (Ibiden Circuits of America)

embedded resistors aids in achieving faster bus speed by increasing transmission efficiencies. In addition to increasing transmission efficiencies and making available real estate on the board surface, embedded resistors also improve reliability through the elimination of the solder joints and plated through-hole connections.

There are two methods for implementing embedded resistors: the additive and the subtractive methods. In the additive method resistive material is either plated or screen-printed onto the inner layer of the substrate. In the subtractive method a layer pair in the printed circuit board is dedicated for the resistive material, material is removed from the layer to form individual resistors via an etching process. Figure 1-5 illustrates both the additive and subtractive resistor methods of fabrication. Table 1-4 highlights companies involved in embedded resistor technologies, the materials they use and their corresponding approach for fabrication.

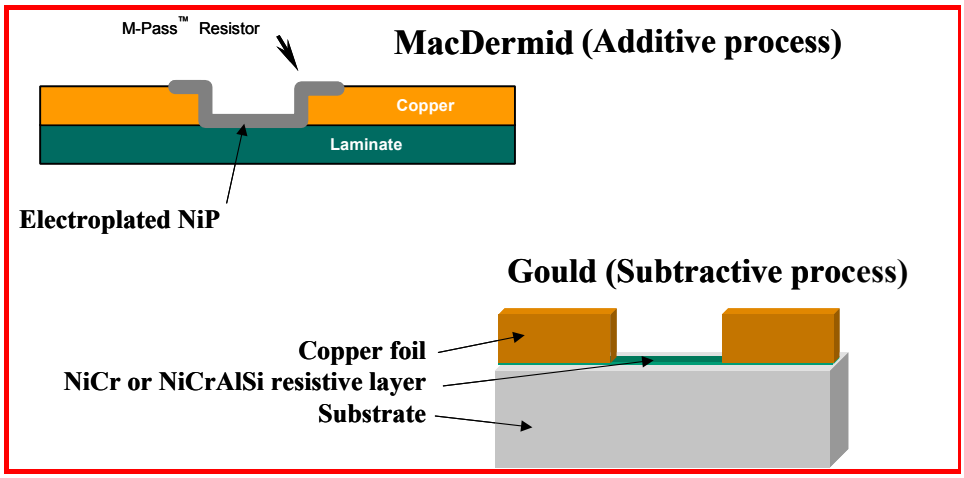


Figure 1-5: Additive and subtractive methods of embedded resistor fabrication

Table 1-4: Companies producing embedded resistor material technologies

Company	Technology	Approach
Asahi Kasei Corporation	Carbon paste (polymer thick film)	Subtractive
DuPont	Ceramic (polymer thick film)	Additive
Gould Electronics	Thin metal on copper	Subtractive
Ibiden	Unknown-internal development	
MacDermid	Plated nickel phosphorus	Additive
Multiline International Europea, LP	Carbon paste (polymer thick film)	Subtractive
Mitsui	Thin metal on copper	Subtractive
Ohmega Technologies	Nickel phosphorus on copper	Subtractive
Shipley	Thin metal on copper	Subtractive

Some embedded system applications may require tight design tolerances on embedded resistor values. Laser trimming of the resistive material on the layer pair achieves these tight tolerances. Figure 1-6 shows various types of laser cuts used to increase the value of embedded resistors and satisfy these tolerances.

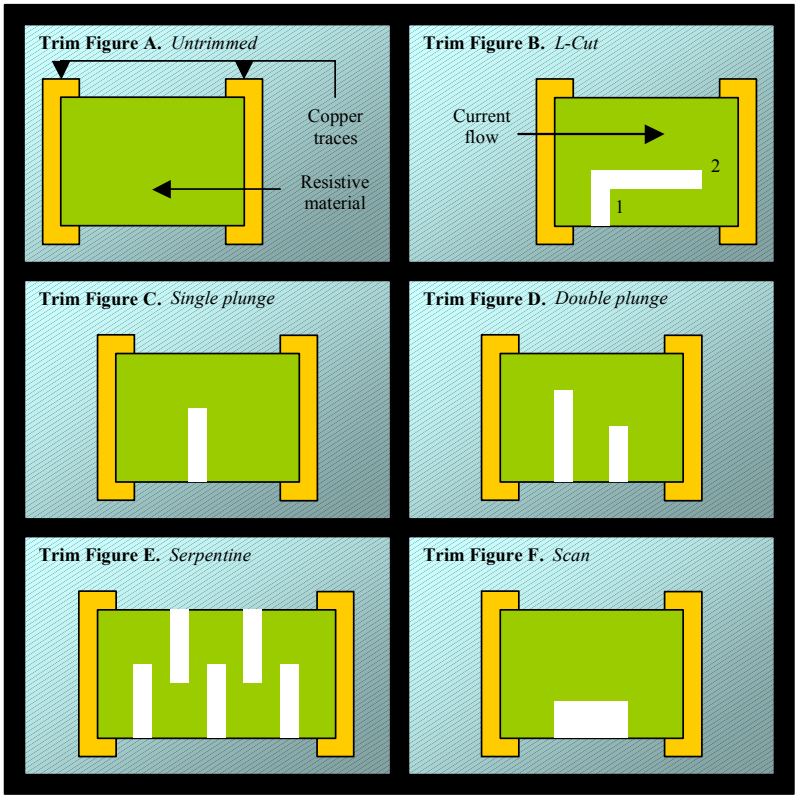


Figure 1-6: Various cuts used by industry for obtaining the resistor value [13]

1.3.2 Embedded Capacitors

Embedded capacitors are expected to provide faster clock speeds and manage switching noise in systems. Like embedded resistors they also contribute to the freeing up of real estate on the board surface, board size reduction and reduce signal-travel distances. Embedded capacitors are formed by inserting an insulating dielectric material between two conductive layers in the PCB as shown in Figure 1-7.

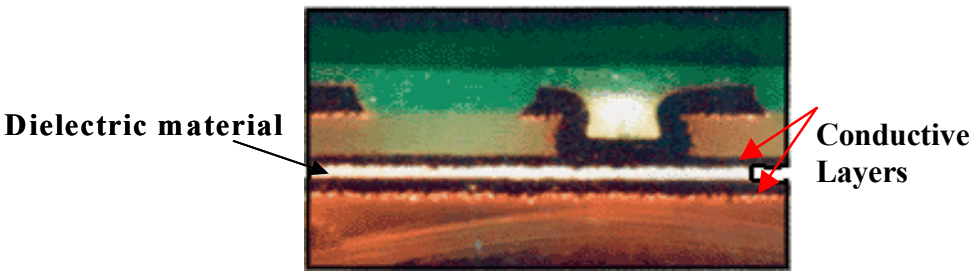


Figure 1-7: Embedded capacitor (Ibiden Circuits of America)

There are a wide variety of dielectric materials and technology providers available for embedded capacitor technology. Table 1-5 provides the names of various companies that are involved in embedded capacitor technologies and the materials they manufacture.

Table 1-5: Companies producing embedded capacitor material technologies [14]

Company	Technology
3M	Filled resin (sheet)
Asahi Chemical	Chemical filled paste
Dupont	Filled and unfilled polyimide film/copper
Dupont	Polymer thick film
Dupont	Filled polyimide paste
Hitachi	Chemical filled resin
Ibiden	Unknown-internal development
MicroCoatings	Thin film on dielectric/copper
Mitsui	
Nippon Paint	Filled resin (liquid and sheet)
Sanmina ZBC	Filled resin
Shipley	Thin film on dielectric/copper
Vantico	Filled liquid

1.3.3 Embedded Inductors

Embedded inductors are fabricated by forming a spiral out of an interconnect material with fine line capabilities (25-50 micron) small vias (25-50 micron) and thin dielectrics (25-50 microns) as shown in Figure 1-8. Although about 80% of the inductors used in hand-held products are low enough in value (less than 200 nH) and would be small enough in size (2 to 4 mm) that they could be embedded directly into the wiring of

Figure 1-8: Embedded inductor design

a suitable substrate they are not prime candidates for embedding [3]. This is due to the fact that inductors are used in such low quantities that the equivalent per component cost will be too high to incorporate any special processes or materials to embed them into the substrate manufacturing process [15].

Conventional surface mount technology will most likely remain the best design choice for inductors in the foreseeable future. Therefore, inductors are not considered within this research effort.

1.3.4 Embedded Passive Advantages

Driven by performance, size and economic concerns, embedded passives were introduced to the market in the early 1980s. The potential advantages offered as a result of embedded passives include:

- Increased circuit density through saving real-estate on PCB substrates
- Improved electrical properties through additional termination, filtering and shortening electrical connection opportunities
- Cost reduction through increased manufacturing automation
- Increased product quality through the elimination of incorrectly attached devices, and
- Improved reliability through eliminating solder joints

1.3.5 Specific Applications

Embedded passives are an attractive alternative for attaining higher passive integration in the telecommunications, automotive, avionics, medical equipment, and GPSs electronic industry. Embedded passive have been used in the following applications:

- Digital electronics for pull-up/pull-down on open collectors for gate inputs
- Line terminations
- LED current limiting
- Switch pad potentiometers and power dividers
- Microwave attenuators
- Parallel and series terminating resistors fabricated into voltage plans of emitter-coupled logic circuitry
- Series terminating resistors for high-speed CMOS applications, and
- Isolation resistors for burn-in boards

Companies currently making use of embedded passives include:

Alcatel	Bell
CTS Microelectronics	Cannon
Codex	Concurrent Computer
Control Data Corporation	Cray Research
Data General	Harris Computer
Hewlett Packard	IBM
Intel	Loral Defense
Loral Space	MIPS
Motorola	NCR
National Instruments	National Semiconductor
Nikon	Pentax
Raytheon	Seagate Technology
Sequent Computer	Siemens
Sun Microsystems	

An increase in the use of embedded passive technology is expected over the next few years which will further decrease the cost of implementing the technology in a fashion similar to what was witness by the PCB industry when the move was made from through hole assembly to surface mount assembly. In the early days, surface mount components were many times more expensive than through hole components and new surface mount assembly equipment costs were off the charts. As time went on, the cost of

the components, assembly equipment and all of the other infrastructure came down, so that today, in most cases, it is less expensive to build a surface mount assembly than a through hole assemble. Table 1-6 provides the projected market share for embedded resistors and capacitors in 2004.

Table 1-6: Projected market share of embedded resistors and capacitors in 2004 [16]

Type of Application	Projected Market Share for embedded passives in 2004	
	Resistors	Capacitors
Hand Held	64%	58%
High Performance	40%	40%
Cost/Performance	20%	20%
Low Cost	10%	10%
Harsh Environment	20%	20%

1.4 Embedded Passive Economics

Miniaturization is currently a major driver within the electronics industry. Passive components are under serious scrutiny because they constitute the vast majority of components placed on a PCB. The embedded passives technology presents the PCB manufacturing industry with an avenue to attain the miniaturization that they are after. There are several inhibitors that are likely to keep embedded passive components from reaching their full market potential including the following:

- Need to demonstrate the technical viability of embedded passive substrates, including materials, processes, design and test system;
- Need to demonstrate the value or economic justification for substituting embedded passive technology for discrete capacitor and resistors;
- Potential delay to the product development cycle. Designing substrates that include embedded passives takes longer and CAD software tools that support it are either not available or immature. The economic impact of a product delay

could easily out way any cost saving in size reduction or conversion costs;

- Embedded passives reduce engineering and manufacturing flexibility.
- Qualification - most of the processes, materials, vendors and products in this space are not yet qualified;
- Lack of availability from multiple suppliers;

Industry standards are required to capture the true market potential for this technology. However, the foremost concern of the embedded passive technology is whether the technology is economically feasible. Potentially the biggest single question about embedded passives is their cost, "…of all the inhibitors to achieving an acceptable market for integral substrates, the demonstration of cost savings is paramount" [9]. There is considerable controversy, however, as to whether the applications fabricated using embedded passives will be able to compete economically with discrete passive technology. On the bright side, the use of embedded passives reduces assembly costs, shrinks the required board size, and negates the cost of purchasing and handling discrete passive components. However, these economic advantages must be traded off against the increased cost (per unit area) of boards fabricated with embedded passives (a situation that will not disappear over time) and decreased throughput of the board fabrication process.

1.5 Dissertation Overview

The objective of this dissertation is to enable cost/size tradeoff analysis for the selective conversion of conventional passives to embedded passives. The cost/size tradeoff analysis capability will be used to determine the optimum set of conventional passives to replace with embedded passives on an application-specific basis. This

research provides a tool to determine the circumstances under which (and for what type of applications) it is economically viable to consider using the embedded passives technology. Only resistors and capacitors are considered herein (the quantities of inductors in systems are relatively small, and current methods of embedding inductors are not considered practical). This work will also only specifically consider embedding into Printed Circuit Boards (as opposed to ceramic or thin film substrates), however, the model and design methodology developed herein could be applied to other substrate types with very little or no modification. The specific tasks that have been completed to attain the objectives set forth above are:

Task 1: Develop a board sizing (including layer count prediction) model that accounts for routing changes due to embedding of passives.

Task 2: Develop a manufacturing cost model for embedded passive substrate fabrication and system manufacturing that can be integrated with the size analysis in Task 1.

Task 3: Implement a Multi-Population Genetic Algorithm optimization approach that allows the optimum mixture of discrete and embedded passives to be determined on an application-specific basis.

Task 4: Perform case studies to demonstrate and exercise the models and solution methodologies. The case studies demonstrate the applicability and limitations of existing modeling approaches as opposed to the new models developed in this dissertation, and the utility of optimizing the embedded passive content in systems.

Chapter 2 describes the approach to the development of the cost and size model

for embedding resistors and capacitors. Chapter 3 provides the results generated using the model developed in Chapter 2 for embedding resistors and capacitors in several different applications.

In Chapter 4, a Multi-Population Genetic Algorithm search is applied to the model developed in Chapter 2. An application from Chapter 3 is analyzed to obtain the optimal solution and demonstrate the approach. The results are also analyzed to study the sensitivity of the system cost to the design variables.

In Chapter 5, a real application, the SENDO M550 GSM cell phone main board, is analyzed to demonstrate the applicability of the model developed herein. Chapter 6 examines the effect of board size on the optimum solution (minimum cost solution) and assesses whether better system solutions can be found by varying or constraining the size of the board in different ways. Chapter 7 discuses the contributions of this research and conclude the dissertation.

CHAPTER 2 EMBEDDED PASSIVE COST/SIZE MODEL

As discussed in Chapter 1, although the embedded passive technology potentially offers many benefits to the electronics industry, in order to make it a viable widespread technology the cost has to be addressed. It will be extremely difficult for the embedded passive technology to compete with the existing surface mount technology (SMT) discrete passives if its economic impact is not fully understood. The motivation for this work is to explore the potential cost savings that are present in the embedded passive technology and to identify the system variables for which the system cost is most sensitive. The model developed in this chapter addresses Tasks 1 and 2, and represents the analysis engine around which an optimization methodology can be built (Chapter 4). The model in this chapter is expected to, by itself, result in a tool that enables tradeoff analysis between conventional discrete passive systems and systems with embedded passives technology at an application-specific level.

Currently there are two well-known methods for doing cost models in electronics manufacturing, namely, Bottoms-up and Top-down methods. Bottoms-up is the cost derived by accumulating detailed estimates from individual fabrication and manufacturing processes or process steps. Bottoms-up modeling allows the impacts of major and minor changes of processes to be quantified, minimizes the risk of missing significant contributor to system cost, and is often used to calibrate Top-down models. The difficulty with Bottoms-up models are that the input data required by the model may not be available and the models may never lead to a system-level answer since it gets stuck in component-level analysis. Alternatively, Top–down models cost is derived from major system attributes. Top-down models provide system-level answers with relatively

simple models that can be evolutionarily improved by adding more layers of detail. Top-down models ultimately yield more practical solutions for performing system-level tradeoffs on application-specific variations of the use of a technology than Bottoms-up and the data required by the model is usually readily available. The one potential problem with Top-down modeling is that the utility decreases when the technology varies widely, i.e., they work well as long as they contain the appropriate attributes of the technologies being considered. The cost model developed in this section employs a parametric Top-down approach.

2.1 Model Development

The model developed to analyze embedded passive cost trade off is summarized in Figure 2-1. Qualitatively the model in Figure 2-1 works in the following way:

1. Accumulate the area of the footprints of discrete passives to be embedded.
2. Reduce board area by the accumulated discrete passive area from step 1 maintaining the aspect ratio of the original board. This step is optional, i.e., the board area may be fixed.
3. Plated or Printed Resistors: Determine the area occupied by each plated or printed embedded resistor on wiring layers. Perform routing analysis removing nets and vias associated with resistors that are embedded and accounting for area blocked by embedded resistors on wiring layers. Routing is assumed to be unaffected by discrete resistors embedded using Ohmega-Ply® or similar dedicated layer subtractive approaches. Bypass Capacitors (distributed capacitors): All nets and vias associated with embedded bypass capacitors are removed from the routing problem. Singulated Capacitors: Assume that embedded singulated capacitors do

not affect routing analysis. Using these assumptions determine the relative change in routing resources due to embedding selected passives.

4. Using the layer requirements, the relative routing requirements for the embedded substrate and either a fixed measure of the routing efficiency associated with the conventional board or a range of possible efficiencies determined under the assumption that the conventional version of the board did not include any more layer pairs than it needed to route the problem, compute the number of required layer pairs for the embedded passive implementation.
5. Determine the yield of layer pairs that include embedded passives.
6. Determine the trimming cost for embedded resistors. The necessity of trimming is determined by the resistor's tolerance. The application-specific cost per trim is determined by modeling the throughput of a laser trimming process.
7. Compute the number of boards per panel from the board size (number-up) and the effective panel fabrication costs from the layer and material requirements, yields, and resistor trimming costs.
8. Determine the relative board fabrication profit margin from layer pair throughput modeling.
9. Accumulate assembly cost, test, rework, and board fabrication costs (with profit margin) to obtain total relative cost.

The analysis in Figure 2-1 focuses on generating the differences in system cost between embedded passive and discrete passive solutions, therefore all cost elements that are approximately equivalent for the embedded and conventional system are ignored, e.g., all functional testing of the system and, procurement and assembly costs associated

with non-embeddable parts. In the tradeoff analysis, accurately predicting differences in performance, size, cost, or reliability are more important than predicting accurately the actual properties.

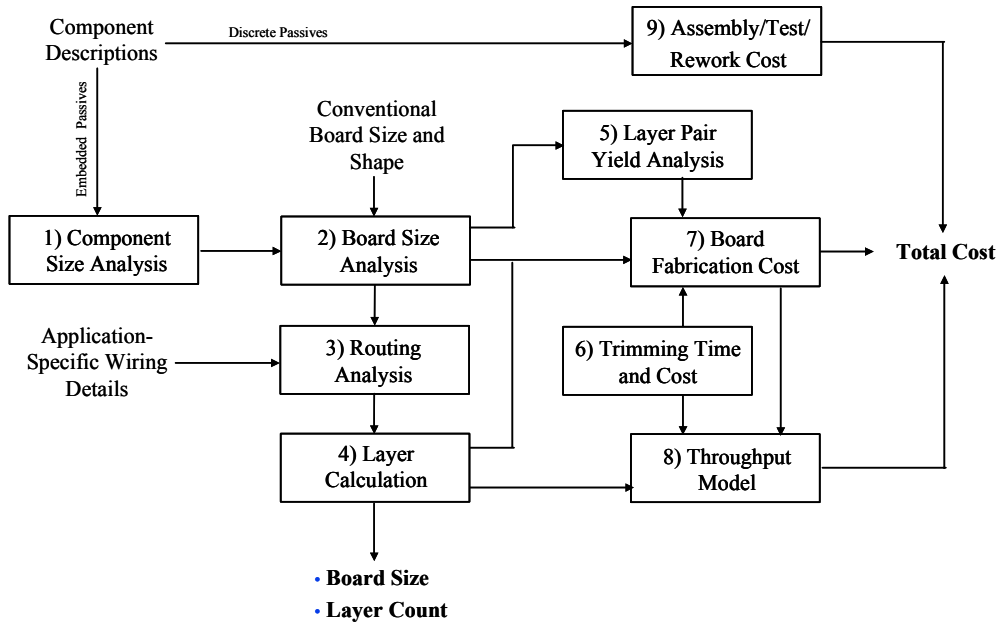


Figure 2-1: Model developed for the analysis of embedded passive cost and size impact on electronic systems

The objective of the model developed and demonstrated in this research is to capture the economic impact of the following competing effects when embedded passives are present in the board:

- Decreased board area due to a reduction in the number of discrete passive components
- Decreased wiring density requirements due to the embedding of resistors and bypass capacitors into the board
- Increased wiring density requirements due to the decreased size of the board
- Increased number of boards fabricated on a panel due to decreased board size
- Increased board cost per unit area

- Decreased board yield
- Decreased board fabrication throughput
- Decreased assembly costs
- Increased overall assembly yield
- Decreased assembly-level rework.

Due to the opposing nature of many of the effects listed above, the overall economic impact of replacing discrete passives with embedded passives is not trivial to determine and, in general, yields application-specific guidelines instead of general rules of thumb. In fact the very nature of tradeoff analysis is one in which *the greater the detail necessary to accurately model a system, the less general and more application-specific the result*.

2.1.1 Existing Embedded Passives Cost Modeling Work

Several authors have addressed cost analysis for embedded passives and thus provide varying degrees of insight into the economic impact of converting discrete passives to embed. The target of all these economic analyses is to determine the effective cost of converting selected discrete passive components to embedded components. The most common approach to economic analysis of embedded passives is to: 1) reduce the system cost by the purchase price and conversion costs[1] associated with the replaced discrete passives, 2) reduce the board size by the sum of the layout areas associated with the replaced discrete passives and determine the new number of boards on the panel, and 3) determine the new board cost based on a higher per unit area cost for the embedded passive panel fabrication and the new number-up computed in step 2. The results of these three steps determine the new system cost. The effects included in this first-order

approach are critical, however, the approach ignores several additional elements, most notably: decreased throughput for embedded passive board fabrication means that board fabricators will have to use higher profit margins for embedded passive boards to justify their production on lines that could otherwise be producing conventional boards; routing analysis of the board to determine not only what layers may be omitted, but what layers may have to be added to maintain sufficient wiring capacity as passives are embedded and the board is allowed to shrink; yield of both discrete passive components and the variation in board yield due to embedding passives; and potential reductions in rework costs (due to both assembly defects and intrinsic functional defects) associated with discrete passives.

Brown [17] presents an outline of all the potential contributions to the life cycle cost of embedded passives. Brown then provides a quantitative evaluation similar to the process outlined above for digital and RF applications. Brown concludes that the more you integrate at the design level, the higher the likely cost savings and that in the applications considered by Brown, embedded passive allowed a possible savings that ranged from 27 to 73% over conventional implementations. Rector [9] provided the economic analysis that appeared in the 1998 NEMI Passive Component Technology roadmap [18] using the first-order approach outlined above. Rector concludes that embedded passives can be economically feasible, but only if one considers more than the effects in the first-order model outlined above, but does not provide a quantitative analysis to support this supposition. Ohmega Technologies Inc. has also generated a cost model for assessing cost tradeoffs associated with it's Ohmega-Ply® embedded resistor material, [19]. The Ohmega cost model follows the first-order approach described above,

[1] Conversion costs are the handling, storage and assembly costs associated with a discrete component.

and includes yield and rework effects. Ohmega concludes that 2-4 embeddable resistors per square inch are required to make the use of the Ohmega-Ply material economically practical.

The most detailed analysis to date is from Realff and Power [20]. Realff and Power developed a technical cost model for board fabrication and assembly. The model includes test (board and assembly), yield, and rework. The focus of the model is on the equipment requirements, under the assumption that embedded resistors are fabricated using a dedicated resistor layer, they conclude that for embedded resistors to have a significant impact on the cost of a system, their use must allow the removal of equipment or in some other way fundamentally change the assembly process (e.g., changing from double to single sided assembly). Only embedded resistors are considered in [20]; Power *et al.* [20] extend the model in [21] to embedded capacitors and cast it in the form of an optimization problem targeted at choosing which discrete passives to embedded based on an assumption of assembly and substrate manufacturing process details, and material properties.

Another analysis that recently appeared focused on design tradeoffs for a GPS front end, [22]. This analysis includes detailed cost modeling of thin-film embedded resistors and capacitors performed using the Modular Optimization Environment software tool from ETH.

The model developed in this chapter incorporates quantitative routing estimation and assesses board fabrication throughput impacts for setting profit margins on board fabrication; these are effects that have not been included in previous models. Also, different technology assumptions than those used in the analyses discussed above were

made, i.e.,

1. Embedded resistors are fabricated directly on wiring layers via printing or plating a resistive material directly on a wiring layer only where an embedded resistor is required (e.g., [23], [24]) – as opposed to requiring dedicated embedded resistor layers as assumed previously, [19] and [20].
2. Bypass capacitors are embedded by dielectric substitution into an existing reference plane layer (as opposed to layer pair addition).
3. Singulated embedded capacitors if present are fabricated via dedicated layer pair addition.

2.1.2 Size/Cost Model Description

This section describes a new model that incorporates the additional effects discussed in Section 2.1.1 and allows size/cost tradeoff analysis for systems containing embedded resistors and capacitors (embedded inductors are not addressed in this work).

Board Size and Routing Calculations

As discrete passive components are converted to embedded passives, the physical size of the board can either remain fixed or is allowed to optionally decrease by the layout area associated with the discrete passives given by,

$$A_{new} = A_{conv} - \sum_{i=1}^{N} (l_i + S)(w_i + S) \qquad (1)$$

where S is the minimum assembly spacing, l_i and w_i are the length and width of the ith discrete passive, N is over all discrete passives that are converted to embedded passives, and A_{conv} is the conventional board area. It is assumed that if the board is allowed to shrink, its aspect ratio is preserved, thus, the new board length (L_{new}) and width (W_{new})

are given by,

$$L_{new} = \sqrt{\frac{A_{new} L_{conv}}{W_{conv}}} \tag{2a}$$

$$W_{new} = \frac{W_{conv}}{L_{conv}} L_{new} \tag{2b}$$

where L_{conv} and W_{conv} are the length and width of the conventional board. If the board is double sided, the calculation in (1) and (2) can be performed independently for each side of the board, the larger of the two sides determines the new board size.

The area consumed by the embedded passives on internal layers impacts the tradeoff analysis by decreasing the wiring available on internal layers. The area occupied by an embedded resistor on a board inner layer is given by,

$$A_R = \begin{cases} \frac{0.8R}{r} m^2 & \text{for } 0.75R > r \\ \frac{r}{0.8R} m^2 & \text{for } 0.75R \le r \end{cases} \tag{3}$$

where R is the value of the resistor, r is the resistivity of the resistor material (Ω/square), and m is the minimum feature size for embedded resistor fabrication. Since embedded resistors are designed and fabricated to smaller (resistance) values than required and trimmed, a factor of 0.8 is included in (3). The factor of 0.8 can be derived assuming a symmetric distribution of fabricated resistor values where the lowest trimmable resistor is 55% of the application target value, a 5% design tolerance on the resistors, and maximizing the number of resistors between the high specification limit and the lowest trimmable resistor, see [25].

There are two types of capacitors that must be considered - bypass (decoupling) capacitors, and non-bypass capacitors. It is assumed that bypass capacitors can be

absorbed into dedicated bypass layer pairs (planar distributed capacitance layers) and the non-bypass capacitors must be fabricated individually on a dedicated capacitor layer pair if they are to be embedded. The area occupied by an individual non-bypass embedded capacitor on a capacitor layer pair is,

$$A_C = \frac{C}{c} \tag{4}$$

where C is the value of the capacitor, and c is the capacitance per unit area of the capacitor layer pair. Assuming square capacitors, the number of embedded capacitor layer pairs (for non-bypass capacitors) required in the board is given by,

$$N_{\text{integral cap layers}} = \left\lceil \frac{\sum_{j=1}^{N_C} \left(\sqrt{A_{C_j}} + S_c \right)^2}{A_{\text{new}}} \right\rceil \tag{5}$$

where N_C is the total number of non-bypass capacitors that are converted from discrete to individual embedded capacitors, and S_c is the effective spacing between individual embedded capacitors on the embedded capacitor layer pair. S_c is usually set larger than the minimum spacing possible to allow for perforation of the embedded capacitor layer by vias and through holes, and to allow area for interconnection.

Besides estimating the physical size of the board after the embedding of selected discrete passive components, routing requirements also needs to be considered. The following routing assumptions are made with respect to embedded passives:

The IO (effectively the nets and vias) associated with discrete resistors that are embedded are effectively removed from the routing problem, i.e., the embedded resistors are fabricated in series with the nets they are attached to on the wiring layers, however, the area occupied by the embedded resistors blocks routing and is accounted for, see (7).

Non-bypass discrete capacitors converted to embedded capacitors have no effect on the routing problem. The IO (effectively the nets and vias) associated with discrete bypass capacitors converted to an embedded capacitor are effectively removed from the routing problem.

With these assumptions and the routing information from the conventional implementation, the routing requirements, and thereby the number of layers required, for an implementation that includes embedded passives can be determined. An estimation of the minimum number of layers required to route the application proceeds as follows,

$$N_{layers_{new}} = \frac{W_{used\,new} + W_{blocked}}{W_{layer\,new}} \left(\frac{U_{conv}}{U_{limit}} \right) \tag{6}$$

where U_{limit} is the maximum fraction of the theoretically available wiring in the board that can be used for routing, and U_{conv} is the fraction of that wiring that is actually used to route the conventional application. The ratio of U_{conv} and U_{limit} measures the routing efficiency of the conventional implementation. When the ratio is large (i.e., close to one), the implementation has effectively used all the wiring that is available and any additional wiring would require the addition of another layer pair or an increase in board area. At some smaller value, any decrease in wiring would allow the omission of a layer pair.

The wiring blocked ($W_{blocked}$) by embedded resistors (length of wiring that can not be used) is given by

$$W_{blocked} = \left(\frac{\sum_{i=1}^{N_R} A_{R_i}}{A_{new}} \right) \left(\frac{A_{new}}{A_{conv}} W_{layer\,conv} \right). \tag{7}$$

where, N_R is the number of embedded resistors, A_{new} is given by (1) and A_R is given by (3). The second multiplier is the wiring per layer in the embedded passive board with no

embedded resistors included (W_{layer}). The total length of wiring used for the new implementation is given by,

$$W_{used\,new} = f\left(W_{used\,conv}\right) \tag{8}$$

where, f is the fractional change in required total wiring length. The wiring used in the conventional implementation is found from,

$$W_{used\,conv} = W_{avail\,conv} \tag{9}$$

where, $W_{avail_{conv}}$ is the total length of wiring theoretically available in the conventional board ($W_{layer_{conv}}$ multiplied by the number of layers in the conventional board minus layers on which wiring is not done, e.g., reference planes). Assuming that the total wiring length required is proportional to the total number of system IO that require routing (a fundamental assumption in routing estimation approaches that compare requirements and resources, [26]), f is found from,

$$f = \frac{N_{IO_{new}}}{N_{IO_{conv}}} \tag{10}$$

where, $N_{IO\,new} = N_{IO\,conv} - 2N_R - 2N_{BC}$, the total number of system IO in the new implementation (assuming 2 IO per resistor and capacitor), assuming resistors are printed directly onto wiring layers

N_R = number of embedded resistors

N_{BC} = number of bypass capacitors absorbed into a bypass capacitance layer pairs

$N_{IO_{conv}}$ = total number of system IO in the conventional implementation.

Note, N in (1) is $N_R + N_C + N_{BC}$ where N_C is the number of non-bypass capacitors that are embedded into the board. The number of IO in the conventional implementation is given by,

$$N_{IO\,conv} = N_{nets\,conv}(\text{fanout} + 1) \tag{11}$$

where fanout = average number of IO that a net attaches together minus one (assumed to be the same for the conventional and embedded passives implementations)

$N_{nets\,conv}$ = number of nets in the conventional implementation.

Since layers occur in pairs in printed circuit board manufacturing, the result given by (6) is rounded up to the nearest multiple of two for use in the model. Note, the final value of $N_{layers_{new}}$ given by (6) is independent of $W_{layer_{conv}}$.

Cost Analysis

Using the size and routing relationships developed in the last section, we can predict the board fabrication costs. The price per conventional board is given by,

$$P_{conv} = (1 + M_{conv})\frac{C_{layer\,pair} A_{conv} N_{layers_{conv}}}{N_{up\,conv}} \tag{12}$$

where

M = profit margin (see throughput analysis below)

$C_{layer\,pair}$ = cost per unit area per layer pair

$N_{up_{conv}}$ = number up, number of boards that can be fabricated on a panel

$N_{layers_{conv}}$ = total number of layers (wiring and reference) in the conventional implementation of the board.

The $N_{up_{conv}}$ is computed from the board length and width, panel length and width, minimum spacing between boards, and the edge scrap allowance using the model in [27].

The price per embedded passives board is similar to (12), with the addition of the capacitor layer costs (if embedded bypass or non-bypass capacitors are present),

$$P_{new} = \frac{(1+M_{new})}{N_{up\,new}}\left[C_{layer\,pair_{new}} Area_{new} N_{layers_{new}} + N_{bypass\,cap\,layers} C_{bypass\,cap\,layer} + N_{integral\,cap\,layers} C_{integral\,cap\,layer}\right]$$

(13)

where

$N_{layers_{new}}$ = minimum number of layers required to route the application given by (6)

$N_{embedded\,cap\,layers}$ = number of embedded capacitor layers given by (5)

$N_{bypass\,cap\,layers}$ = number of bypass capacitor layers.

The new layer pair cost in (13) is given by,

$$C_{layer\,pair_{new}} = C_{layer\,pair} + (C_{resistor\,material})(N_{up_{new}})\sum_{i=1}^{N_{R'}} Area_{R_i} + N_{R'} C_{trim} N_{up_{new}} + C_{print} \quad (14)$$

where, the sum in (14) is taken over all embedded resistors in the particular layer pair of interest ($N_{R'}$), and

$C_{resistor\ material}$ = cost per unit area of the resistive material printed on the wiring layers to create embedded resistors

C_{trim} = the average cost of trimming one printed resistor

C_{print} = the average cost of printing or plating all embedded resistors onto one layer pair.

The board price is combined with component-specific assembly, test, and rework costs to determine the system cost. The average effective cost associated with a single instance of a discrete passive (after [28]) is computed as follows:

$$C_{discrete} = P_{discrete} + C_{handling} + C_{assembly} + C_{AOI} + (1 - Y_{assembly})(C_{assbly\ rework} + P_{discrete} + C_{handling}) + (1 - Y_{functional})(C_{func\ rework} + P_{discrete} + C_{handling}) \quad (15)$$

where,

$P_{discrete}$ = purchase price of a discrete passive component

$C_{handling}$ = storage and handling costs associated with a discrete passive component

$C_{assembly}$ = the cost of assembly of a discrete passive component (per site)

C_{AOI} = cost of inspecting a discrete passive component (per site)

$Y_{assembly}$ = assembly yield for discrete passive components

$Y_{functional}$ = functional yield of discrete passive components

$C_{assbly\ rework}$ = cost of reworking an assembly fault (per site)

$C_{func\ rework}$ = cost of diagnosing and reworking a functional fault.

The $(1\text{-}Y_{assembly})$ term in (15) represents the fraction of discrete passives requiring rework (replacement) due to assembly faults. The $(1\text{-}Y_{functional})$ term in (15) represents the fraction of discrete passives requiring rework (replacement) due to functional faults. Equation (15) assumes that all assembly and functional faults associated with discrete passives are diagnosable and reworkable.

The total system cost (for relative comparison purposes) is given by,

$$C_{system} = \sum_{i=1}^{N_{discrete}} C_{discrete_i} + P_{board} \quad (16)$$

where

$C_{discrete_i}$ = the cost associated with the i^{th} discrete passive component from (15)

P_{board} = the board price from (12) or (13)

$N_{discrete}$ = number of discrete passive components assembled on the board.

Note, the following costs are not included in the formulation because they are assumed to be the same whether or not the system contains embedded passives: all functional testing costs are ignored, all costs associated with other non-embeddable system components are ignored.

2.1.3 Profit Margin/Throughput Analysis

A fundamental issue that has not been addressed in previous cost analyses associated with embedded passives is the throughput of the process that is used to manufacture the embedded passive boards. Throughput is a measure of the number of products that can be produced in a given period of time, and is the inverse of the inter-departure time (the time elapsed between completed products). Throughput is key to understanding the profit margin that will be required to justify manufacturing embedded passive boards. The objective of this portion of the analysis is the computation of application-specific relative profit margin values for conventional and embedded passive versions of a board.

Embedded Passive Processing Time Model and Cycle Time Analysis

The processing time for the embedded passive boards is inherently longer than the processing time for the conventional boards since there are a number of additional process steps involve in the manufacture of embedded passive boards. The processing steps for the conventional and embedded passive board including processing time models for each process step are listed and discussed in [37]. At this point in time conventional and embedded passive board fabrication processes are both performed on the same line

with the only difference being additional process steps for the embedded passive process.

One additional significant process time model and process step included within the embedded passive process which was not considered in [37] is the processing time model for panel trim time associated with the embedding of resistors[2]. The processing time models discussed in [37] along with the panel trim time model discussed in [38] were used to determine the cycle time for processing both conventional and embedded passive bare boards.

Laser Trimming Resistors

To process a laser trim, the resistor of interest is connected to a high-speed measurement system via a suitable probe system, and a laser is directed to machine a cut through the resistor thickness in a direction generally orthogonal to the current flow Figure 2-2. As the laser cut forms, the measurement system detects a decreased current flow relative to applied potential, and interrupts the laser radiation when the desired resistor value has been reached.

A laser based resistor trimming system has several component processes contributing to the overall panel trim process time. These component processes are listed below [38]:

1. **Panel unload and load** – Time taken for a processed panel to be exchanged for an untrimmed panel.
2. **Panel alignment** – Time required to align the panel to maintain positional accuracy throughout the step and repeat trimming processes.

[2] Fabricated embedded resistors are usually targeted as resistance values that are lower than the values needed in the application and are trimmed by cutting out portions of the resistor to increase its value to the design target.

3. **Circuit[3] alignment** – Time required to align circuit to maintain probe to pad placement accuracy in a production application.
4. **Galvanometer resistor-to-resistor movement** – Time required to reposition the laser from the end of one cut to the start of next cut on sequential resistors (becomes very significant when the resistor count on the circuits increases).
5. **Resistor Trim** – Time required to trim a resistor (speed at which a laser cuts resistor material is determined by the laser repetition rate, the pulse bite size, and the trim length and shape).
6. **Panel movement** – Time for positioning circuits of a panel relative to the fixed lens and probe systems. This process requires exacting control of a large fast moving mass and the time required to change circuit position can be significant.

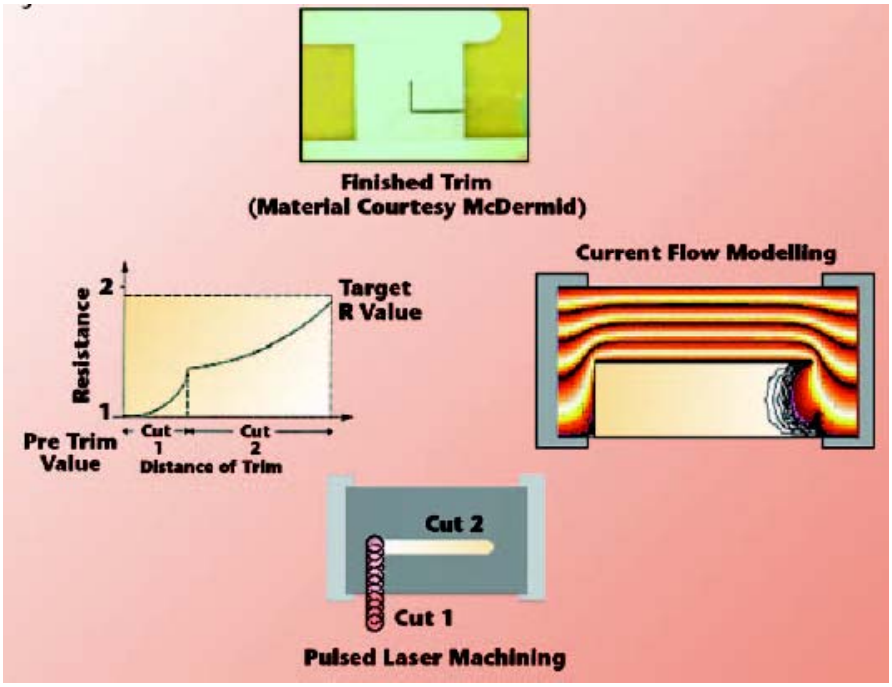


Figure 2-2: Basics of embedded resistor laser trimming process [38]

[3] A circuit is the connection of a measurement system to several resistors prior to laser trimming. The ultimate circuit size is largely dictated by the maximum scanning area available to the fixed laser lens.

The processing time for each component of panel trimming listed above was utilized to develop a panel trimming time model for trimming embedded resistors. The input and output variables along with the laser trimming machine capabilities of this model can be found in Appendix C. In this model it is assumed that all embedded resistors are visited and measured by the laser trimming machine even if they do not require trimming.

It is important to note that only the processing time models associated with the bare board manufacture are considered in this analysis. The processing time models were used to analyze the cycle time for the bare board manufacture of the SENDO M550 GSM cell phone and the NEMI Hand-Held product sector emulator (details of these boards are provided in Chapter 5 Table 5-1 and Chapter 3 Table 3-1). The results from this analysis are shown in Figures 2-3 and 2-4. In Figure 2-3 the cycle time for the embedded passive board design is double that of the conventional board design, 118.5 minutes and 58.7 minutes respectively.

This disparity in cycle time is due to the addition processing steps required for the design of the embedded passive bare board. This analysis also illustrates that the bottleneck in the design process is different for each process. For the embedded passive process the bottleneck process step is the panel trim step and for the conventional passive process it is the board inspection step. Figure 2-4 illustrates the cycle time analysis for the NEMI Hand-Held product sector emulator.

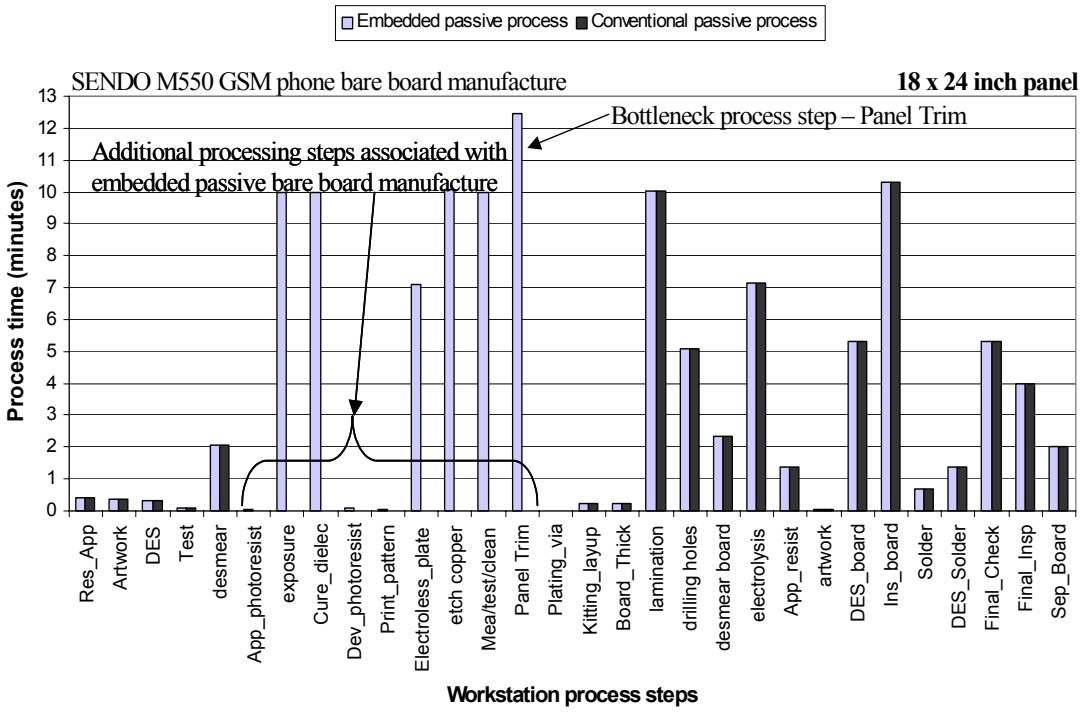


Figure 2-3: Cycle time for the SENDO M550 GSM cell phone bare board manufacture

In this case the cycle time for the embedded passive bare board design is more than twice that of the conventional bare board design, 131.8 minutes and 58.8 minutes respectively. Like in Figure 2-3 the increase in the embedded passive board design is due to the additional process steps required for the embedded passive process. However in Figure 2-4 the bottleneck process step time for the embedded passive process is much larger than the bottleneck process step time for the embedded passive process in Figure 23, 25.77 minutes and 12.44 minutes respectively. This is the primary difference between Figures 2-3 and 2-4 besides the increase in drill time (approximately 6 seconds) for the conventional passive drill time in the NEMI Hand-Held bare board product sector emulator. These differences are due to the larger number of embedded resistors in the NEMI Hand-Held product sector emulator, more than three times as many embedded

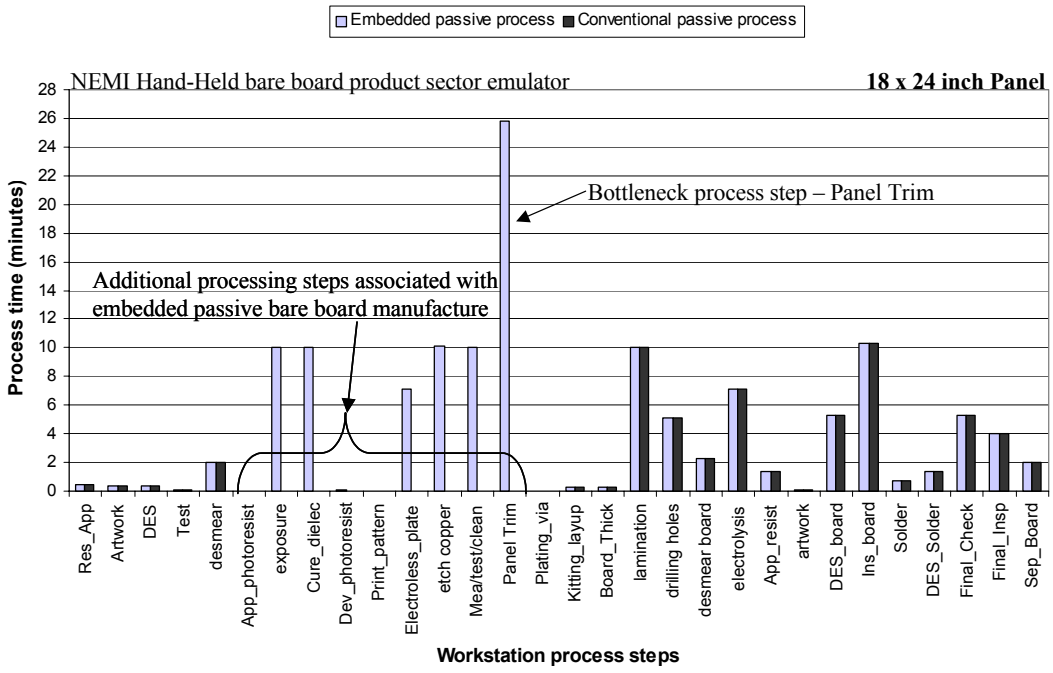


Figure 2-4: Cycle time for NEMI Hand-Held bare board product sector emulator

resistors than the SENDO M550 bare board. Figure 2-5 shows the effects of trimmed resistors on the panel trim time for both the NEMI Hand-Held and the SENDO M550 bare board manufacture. In this analysis the NEMI board contains 174 embedded resistors on a 2.17 x 2.17 inch board (12,180 embedded resistors per 18 x 24 inch panel) and the SENDO contains 54 embedded resistors on a 1.53 x 2.98 inch board (3,780 embedded resistors per 18 x 24 inch panel). The panel trim time becomes the global bottleneck of the process when approximately 46 percent of the embedded resistors are trimmed for the NEMI Hand-Held application and when approximately 88 percent of the embedded resistors are trimmed for the SENDO M550 cell phone application. The discontinuous "stair stepped" behavior of the panel trim time as resistors are trimmed is due to the number of resistors visited simultaneously per probe step; in this analysis there are seven resistors per probe step (see Appendix C).

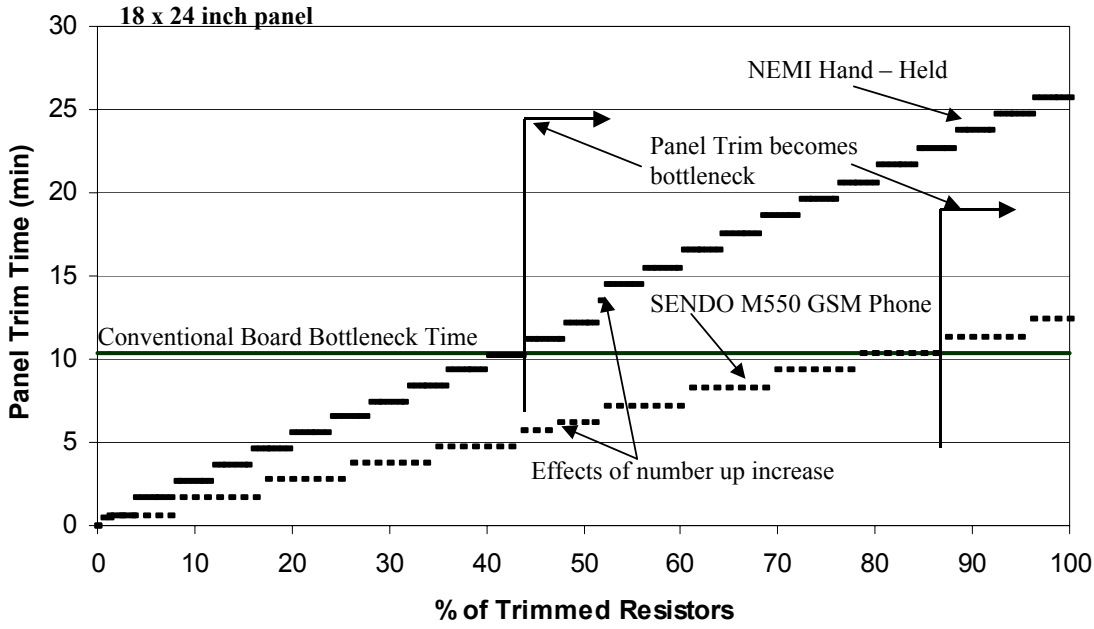


Figure 2-5: Effects of trimmed resistor on panel trim time for embedded passive bare board design

Figure 2-6 illustrates the percentage of time for the major components of the laser trimming process within the NEMI Hand-Held application on an 18 x 24 inch panel. This analysis demonstrates that the resistor trimming component only requires 0.41% of the panel trim time. Therefore whether the embedded resistors are trimmed or not, the visiting and measurement components would still render the panel trim process the bottleneck step in the manufacture of the embedded passive bare board.

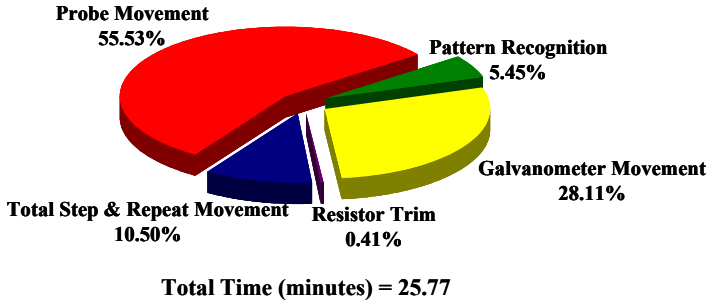


Figure 2-6: Laser trimming equipment utility distribution for the NEMI Hand-Held application on an 18 x 24 inch panel (see Appendix C)

The panel trim bottleneck of the embedded passive board manufacturing process means that there will be an increase in the inter-departure time for the embedded passive process which results in lower throughput for the embedded passive board process. This lowering in throughput will be used to determine the profit margin required for the embedded passive process in order to justify manufacturing embedded passive boards rather than conventional boards on a given manufacturing line.

The situation faced by the board manufacturer may be the following: assume that there are two types of boards that could be fabricated on a process line, one is a conventional board with a known profit margin and the other is an embedded passive board. To simplify the problem, assume that the number of boards to be manufactured will be the same for both types of board. The manufacturing cost of the embedded passive board will be larger. Knowing that the inter-departure time of the embedded passive process will be longer than that for conventional boards (due to the resistor trimming bottleneck discussed above), the manufacturer must decide what profit margin to use for the embedded passive board so that the total profit per unit time made by selling embedded passive boards equals or exceeds what can be made by selling the conventional boards. This is necessary to justify the use of a line to fabricate embedded passive boards when it would otherwise be producing conventional boards.

To explore throughput effects and determine the relative profit margins of the printed circuit boards, a model has been developed that is similar to cost of ownership models for capital equipment (e.g., [29]). The model captures the costs due to maintenance (scheduled and unscheduled), yield loss, inter-departure time variations, and changeovers.

The labor costs associated with scheduled and unscheduled maintenance, and changeovers are given by (17),

Scheduled Maintenance: $L_{sm} = N_{sm} T_{sm} R_L$ (17a)

Unscheduled Maintenance: $L_{usm} = \frac{MTTR}{MTBF}(T_{total})R_L$ (17b)

Changeovers: $L_{co} = N_{co} T_{co} R_L$ (17c)

where

N_{sm} = number of scheduled maintenance activities in a given period of time

T_{sm} = average labor time (touch time) associated with a scheduled maintenance activity

N_{co} = number of changeovers in a given period of time

T_{co} = average labor time (touch time) associated with a change over

R_L = labor rate

MTTR = Mean (labor) Time To Repair for an unscheduled maintenance event

MTBF = Mean Time Between Failures (unscheduled maintenance)

T_{total} = total time in the period of interest.

We must now evaluate the throughput impacts of various critical manufacturing events. Computed throughput loss is basically determining lost opportunity costs, i.e., how much good product does not get manufactured because the process has been slowed or stopped, or because defective product is produced instead. It is assumed that scheduled maintenance does not affect the throughput, i.e., it is performed during periods when the process would not be operational, therefore, only the cost of performing the

scheduled maintenance is important for our tradeoff, also it is assumed that the scheduled maintenance periods for lines producing conventional and embedded passive boards are of the same length and occur at the same frequency. Note, if there is no effective off-shift (i.e., no time when maintenance can be performed that does not affect the throughput), then N_{sm} is set to zero and all maintenance is treated as unscheduled maintenance.

The throughput impact of process yield can be computed from the number of multilayer panels lost in a fixed time period due to process yield losses,

$$\text{Lost}_{\text{yield}} = \left(1 - Y_{\text{ilp}}\right)\frac{N_{\text{inner layers}}}{N_{\text{inner layers per board}}} \tag{18}$$

where

Y_{ilp} = yield of the panel inner layer process

$N_{\text{inner layers}}$ = number of panel inner layers produced in a fixed time period

$N_{\text{inner layers per board}}$ = number of inner layer pairs in a single board.

Unscheduled maintenance, assuming it is performed during time when the process line would otherwise be producing good product contributes the following lost time,

$$\text{Lost}_{\text{usm}} = \left(\text{MTTR} + 2T_{\text{c/s}}\right)\frac{T_{\text{total}}}{\text{MTBF}} \tag{19}$$

where $T_{c/s}$ is the cool down/startup time associated with the line being stopped for the unscheduled maintenance activity. Similarly, the changeovers result in lost opportunity to produce products,

$$\text{Lost}_{\text{co}} = N_{\text{co}}\left(T_{\text{co}} + 2T_{\text{c/s}}\right) \tag{20}$$

Knowing the inter-departure, the average number of multilayer boards that can be obtained from the process line during the time period defined by T_{total} is given by,

$$N_{boards} = \left[\frac{T_{total}}{T_{inter} N_{inner\ layers\ per\ board}} \left(1 - \frac{Lost_{usm} + Lost_{co}}{T_{total}} \right) - Lost_{yield} \right] N_{boards\ per\ panel} \quad (21)$$

T_{inter} = inter-departure time of the inner layer process (time/inner layer pair)

$N_{boards\ per\ panel}$ = number up, i.e., the number of boards that can be fabricated on a panel.

The parameter that needs to be evaluated for comparison purposes is the total profit in a fixed period of time from fabricating a specific board type. Note, the profit per board is not a good comparison metric because it does not account for the number of boards that are produced. The average profit in the time period associated with the constituent variables is computed from,

$$Average\ Profit = N_{boards} V - \left(L_{sm} + L_{usm} + L_{co} \right) \quad (22)$$

where the value of a board (V) is given by,

$$V = \left(1 + M \right) C_{board} \quad (23)$$

where

M = profit margin

C_{board} = manufacturing cost per board.

The example results shown in Figure 2-7 was generated using the model described by (17)-(23). If inter-departure times of inner layer production for conventional and embedded passive layers, and the average profit margin for conventional boards are known, then the minimum required profit margin for embedded passive board fabrication can be determined. Note, this cost model must be repeated for each board manufacturing scenario since the number of layers in the multilayer board and the dimensions of the

individual board are application-specific.

The example shown in Figure 2-7 indicates that if, conventional boards have a 15.7% profit margin and 15 second inter-departure time (per layer pair), then 30 second per layer pair embedded passive board production is only feasible for profit margins of 26% or more. The most important property from this analysis is the difference between the profit margins; the tradeoff analysis results are much less dependent on the absolute values of the profit margins. Profit margin differences of ~10% was consistently observed. The analysis presented in Chapter 3 assumes profit margins that make the average profit per hour of each type of board fabrication equal.

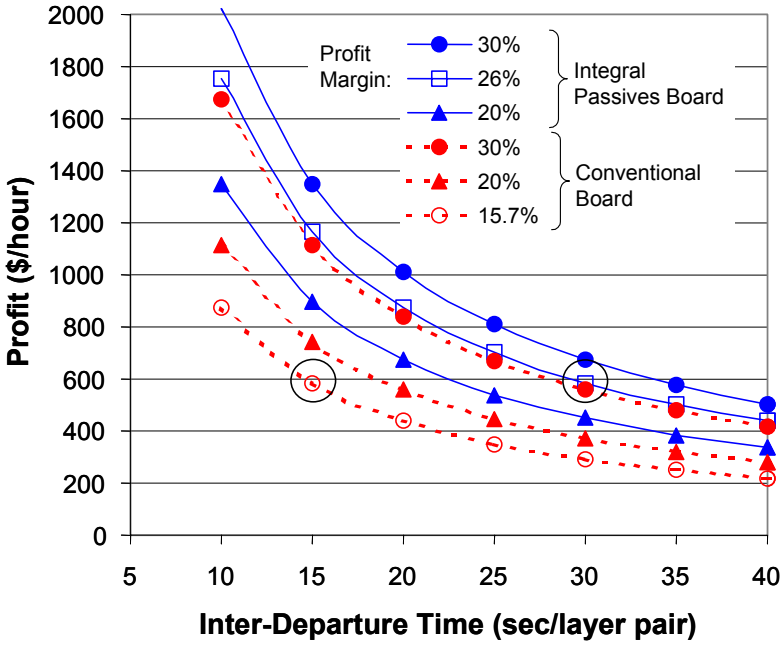


Figure 2-7: The relationship between profit margin and production inter-departure time for conventional and embedded passive board fabrication

Figure 2-8 shows the effects of embedding resistors for the NEMI Hand-Held application on the required embedded passive board profit margin. This figure shows that the profit margin required for the embedded passive board remains the same as that of the conventional passive board until the number of resistors embedded causes the panel trim

process to become the bottleneck of the system.

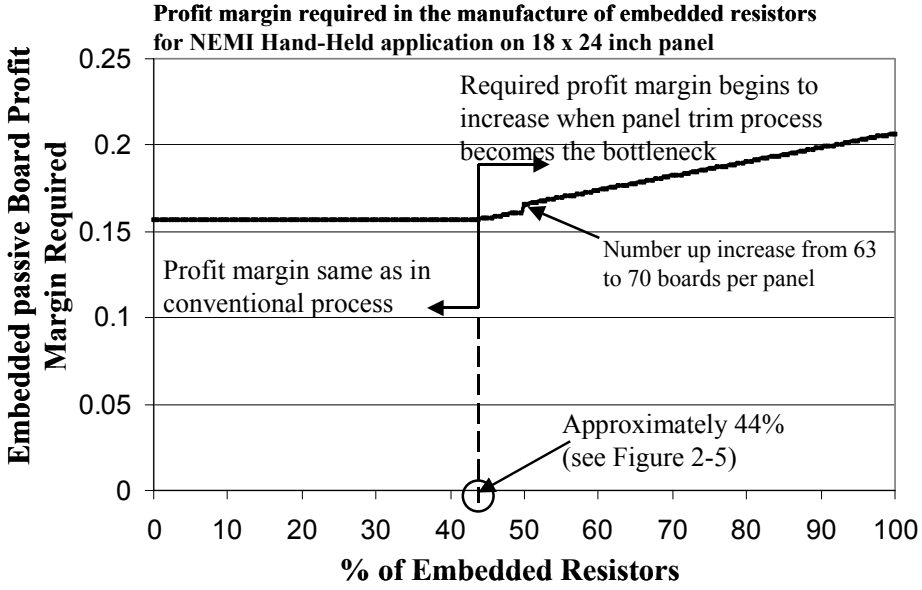


Figure 2-8: Effects of embedding resistor on profit margin for NEMI Hand-Held application. Conventional profit margin = 0.157 (15.7%)

2.2 Summary

This model developed in this chapter has been implemented in Java as a web base tool which has been used by the members of the Advanced Embedded Passive Technology Consortium to analyze the size/cost tradeoff that are present on various applications[4]. The implementation of the model is also fully instrumented for Monte Carlo analysis. Monte Carlo analysis methods involve simulating a design by sampling stochastic input variables to characterize output performance. Monte Carlo (random sampling) is the most straightforward sampling method and can be shown to appropriately represent the behavior of a response variable if an adequate number of samples are used. The implementation of the models allows any (or all) of the input

[4] The tool that implements the model developed in this chapter can be accessed at: http://www.calce.umd.edu/contracts/AEPT/restricted/EmbeddedPassivesTool.htm (note, access requires a CALCE login and password).

variables to be probability distributions and will produce system cost as a distribution.

The model described in this chapter characterizes all the size/cost tradeoffs elements that are inherent in the embedded passive technology when resistors and capacitors are embedded in PCBs. It emulates the manufacturing process by capturing the cost associated with embedding each embeddable discrete passive. The effect of the embedded passive technology on the cost of the system is presented in Chapter 3, which provides a detail analysis of the model results for 3 different applications. The cost/size models developed in this chapter are used as the analysis engine in the optimization methodology developed in Chapter 4.

CHAPTER 3 COST/SIZE ANALYSIS CASE STUDIES

In this chapter the results of cost/size tradeoff analyses performed using the model developed in Chapter 2 on several different single board applications, including a picocell board from Nortel Networks, the NEMI hand-held emulator and a fiber channel card from StorageTek. It is not the intent of these analyses to prove that embedded passives lead to less expensive systems, rather to understand the economic realities should one decide to use embedded passives. The following case studies only include manufacturing costs (no life cycle effects are included).

The relevant characteristics of the applications are given in Table 3-1. The common data assumptions for the 3 applications are shown in Table 3-2. The data in Table 3-2 comes from the sources referenced in the table, and was obtained from Merix (a printed circuit board fabricator who manufactures boards that include embedded passives) and from Nortel Networks.

Table 3-1: Picocell board, Hand-Held emulator and Fiber Channel Card application characteristics

	Picocell Board	Hand-Held [18]	Fiber Channel Card
Number of Embeddable Discrete Resistors	27 (< 100 Ω) 19 (100-1000 Ω) 22 (1 – 10 kΩ) 1 (10 – 100 kΩ) 1 (>100 kΩ)	40 (<100 Ω) 134 (0.1 – 1 kΩ)	210 (< 100 Ω) 181 (100-1000 Ω) 150 (1 – 10 kΩ) 63 (10 – 100 kΩ) 6 (>100 kΩ)
Size of Embeddable Discrete Resistors	69 0805 (80x50 mils) 1 1201 (120x100 mils)	0402 (40 x 20 mils)	561 0603 (60x30 mils) 10 0805 (80x50 mils) 31 120x60 mils 8 250x120 mils
Number of Embeddable Discrete Capacitors	1 (< 100 pF) 29 (100 – 1000 pF) 13 (1 – 10 nF)	69 (<100 pF) 40 (100 - 1000 pF)	88 (0.001μF) 38 (0.01μF) 116 (0.1μF)
Size of Embeddable Discrete Capacitors	0805 (80x50 mils)	0402 (40 x 20 mils)	159 0603 (60x30 mils) 82 0805 (80x50 mils)
Discrete Passive Cost	$0.0045 per part	$0.0045 per part	$0.0045 per part
Conversion Cost (excluding assembly)	$0.015 per part	$0.015 per part	$0.015 per part
Board Size	2.27 x 6.87 inches	30 cm^2 (square board assumed)	12 x 18 inches
Number of Board Layers	10	6	12

Table 3-2: Data assumptions used in the modeling

Panel Fabrication	Throughput Analysis	Embedded Passives
Panel size = 18 x 24 inches (except where otherwise noted)	Change overs = 4/week	Capacitance layer: 10 nF/cm^2
Edge scrap = 0.75 inches	Change over time = 15 minutes	Resistive material: 200 ohms/square
Min. spacing between boards = 0.15 inches	Cool down and start up = 30 minutes	Minimum feature size for embedded components = 15 mils
Cost per layer pair = $12.50/$ft^2$	MTBF = 200 hours (conventional) MTBF = 150 hours (embedded passive)	$C_{resistor\ material}$ = $0.08/$in^2$
	MTTR = 1 hour	C_{trim} = $0.002/embedded resistor
Assembly	Labor rate (repair) = $25/hour	C_{print} = $7.43/layer pair
Min. Assembly Spacing = 20 mils	Production hours = 5000/year	Cost of capacitor layer material = $14.40/$ft^2$ (>10 nF/in^2)
Yield = 0.992/discrete passive [19]		Spacing between non-bypass embedded capacitors (S_c) = 50 mils
Cost = $0.0045/discrete passive	**Routing Analysis**	
AOI = $0.0001/discrete passive	Average fanout = 2.1	
Assembly Rework = $4/site [19]		
Functional Rework = $4/site [19]		

3.1 Analysis of the Application Results

3.1.1 Picocell Board Application

Figure 3-1 shows analysis results for the picocell board as discrete resistors are replaced by embedded resistors (capacitors are not integrated in Figure 3-1). Relative system cost is plotted in Figure 3-1 and throughout this section indicating the system cost less the cost of all non-embeddable components and functional testing. The specific solution (data points) in Figure 3-1 indicate that the embedded passive board becomes economical when approximately 10% of the embeddable discrete resistors are embedded[5]. The data point at $18.30 when no resistors are embedded represents the board price increase due only to the need for a higher profit margin to justify embedded passive board fabrication (see Section 2.1.2). The next point on the vertical axis (~$19.00) is the relative cost of the system when the first resistor is embedded.

The resistor results appear as a "band" in Figure 3-1 due to the range of values that U_{conv}/U_{limit} can take on in (6). The upper edge of the band (the closed data points in Figure 3-1), represents the assumption that the conventional board used all available routing resources efficiently, i.e., U_{conv}/U_{limit} is close to 1.0. The lower edge of the band (the open data points in Figure 3-1), represents the assumption that the conventional board made poor use of the available routing resources, i.e., U_{conv}/U_{limit} is smaller[6]. Practically speaking, all solutions start at the top edge of the band (10 layers for the picocell board) and may step down to the lower edge of the band (8 layers for the picocell board) at some point depending on the actual value of U_{conv}/U_{limit} for the application.

[5] The embedded resistors considered in this study are considerably more economical than embedded resistors in previous studies due to the assumption of fabrication of the embedded resistors directly on wiring layers as opposed to dedicated embedded resistor layer.
[6] The minimum value is determined by finding the smallest value of U_{conv}/U_{limit} that predicts the correct number of layers in the conventional solution.

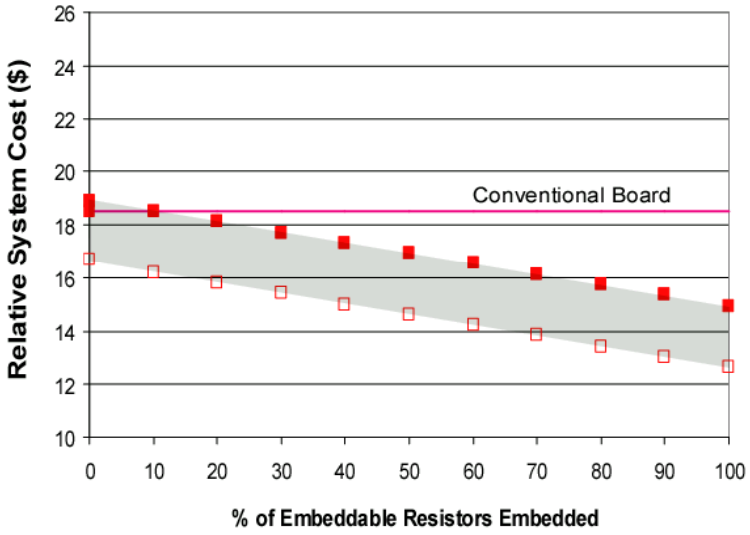


Figure 3-1: The economics of embedded resistors for the picocell board application. Each data point represents the embedded passive solution for a specific routing resource assumption (assumption of the ratio of resources actually used to route the conventional implementation of the board and the theoretical maximum amount of resources that could be used), the band represents all possible embedded passive solutions for this application; the solid horizontal line is the system cost of conventional implementations. Only resistors ≤ 10 Kohms were considered embeddable.

Another type of step discontinuity can also appear in the results if the board shrinks in size enough so that more boards can be fabricated on a panel. In the picocell board case, the board size never decreases sufficiently to allow more boards to be fabricated on an 18 x 24 inch panel, however, potential board size decreases are still important to the customer of this board and Figure 3-2 shows the board area change as fraction of embedded resistors is varied.

Next consider the integration of capacitors. Figure 3-3 shows the relative system costs as the embeddable capacitors are integrated (none of the embeddable discrete resistors are embedded in Figure 3-3). Since embedding of bypass capacitors requires material replacement and non-bypass capacitors requires the addition of an extra layer pair (for the technologies we assumed), the very first bypass capacitor embedded increases the cost of the board dramatically, but as more capacitors are embedded, the

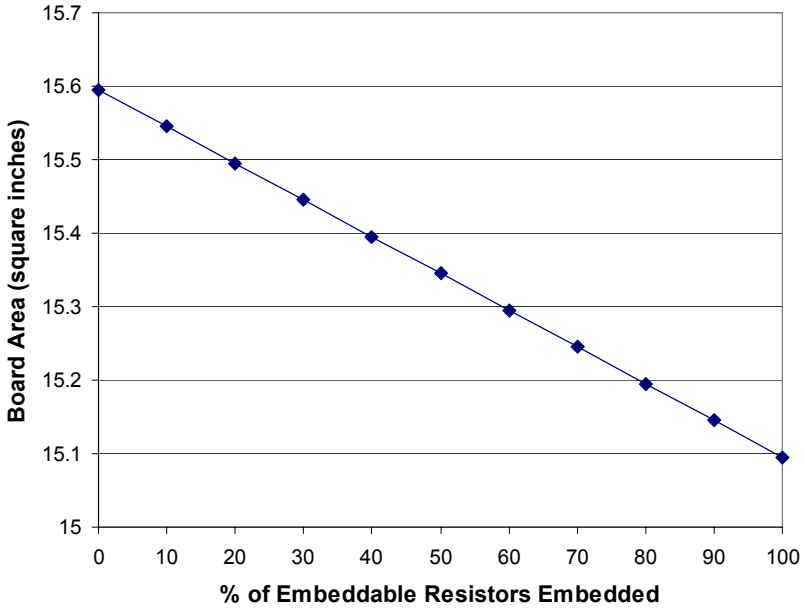


Figure 3-2: Board size decrease with resistor embedding for the picocell board application.

added cost of the replacement material layer is gradually offset by the avoidance of discrete capacitor part and assembly costs. It has also been assumed that when a bypass capacitance layer pair is added, less total bypass capacitance will be necessary[7], [31]. The driver that determines whether capacitor embedding is economical or not, is the density of embeddable discrete capacitors on the board. Figure 3-4 shows that if additional embeddable capacitors were added to the picocell board application (thus increasing the capacitor density), bypass embedded capacitors would become economically viable at approximately 6.9 capacitors/square inch, whereas the actual picocell board application has only 2.76 capacitors/square inch.

[7] At frequencies above a few MHz, the connection inductance of surface-mounted capacitors limits their effectiveness. For this reason, the amount of embedded capacitance required to achieve a given level of switching noise suppression may be significantly less than the total surface-mount capacitance it replaces.

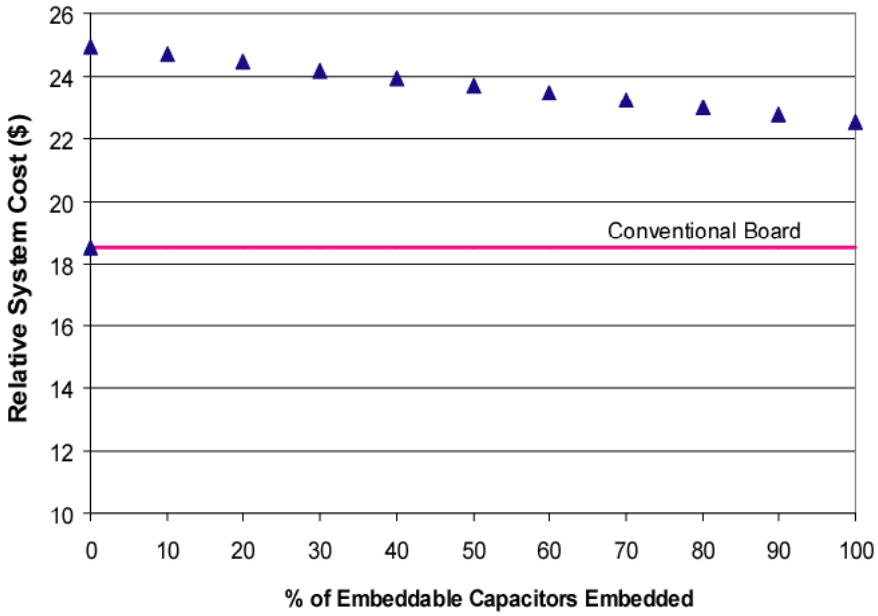


Figure 3-3: Capacitor embedding for the picocell board application. Only capacitors ≤ 100 nF were considered embeddable.

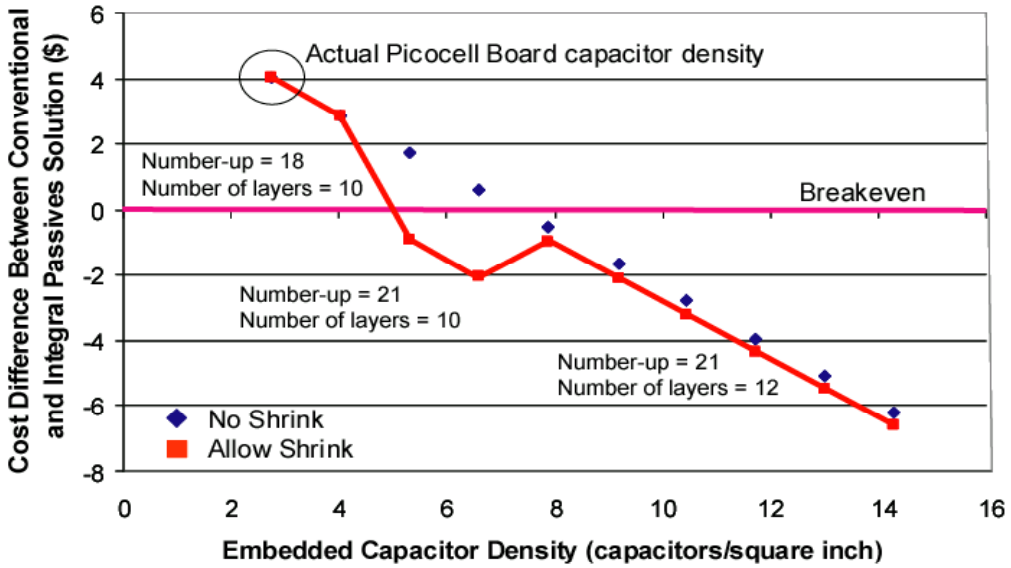


Figure 3-4: The impact of embeddable capacitor density on system cost for the picocell board application. When the density of embeddable bypass capacitors is increased, the number-up first decreases due to the decreased board size (if the size is allowed to change), and later (as density increases) a layer pair addition is required to support routing requirements of the application with the smaller board size.

3.1.2 NEMI Hand-Held Product Sector Emulator[8]

Analysis similar to those performed on the picocell board have been applied to the NEMI hand-held emulator described in Table 3-1. Figure 3-5 indicates that the embedded board becomes economical when approximately 3% of the embeddable discrete resistors are embedded[9]. A discontinuity in the embedded passive board data is labeled on the plot. The discontinuity appears when enough resistors have been embedded to sufficiently reduce the board size so that additional boards can be manufactured on the panel (number-up increases). In the hand-held emulator case, the boards are small (i.e., the number-up on the panel is large) and the overall price of the boards is low (under $2/board), therefore the effect of increasing the number-up has a minimal effect on the system cost.

Figure 3-6 shows the relative system costs as the embeddable capacitors are integrated (none of the embeddable discrete resistors are embedded in Figure 3-6). When bypass capacitors are embedded, the cost initially increased by the material replacement cost. We have assumed that when a bypass capacitance layer pair is added, less total bypass capacitance will be necessary[10]. Note, a much better economic case can be made for embedded bypass capacitors in the hand-held emulator than for the picocell board due to the larger embeddable bypass capacitor density (23.44 capacitors/square inch). Similar to the embedded resistor characteristics, eventually enough bypass capacitors are embedded to reduce the size sufficiently to allow a number-up increase (note, there are fewer embeddable capacitors than resistors, so the this discontinuity occurs later in the

[8] This application does not represent a real board, rather it is a generic emulator used to represent a hand-held electronic application.
[9] The embedded resistors considered in this study are considerably more economical than embedded resistors in previous studies due to the assumption of fabrication of the embedded resistors directly on wiring layers as opposed to dedicated embedded resistor layer.
[10] At frequencies above a few MHz, the connection inductance of surface-mounted capacitors limits their effectiveness. For this reason, the amount of embedded capacitance required to achieve a given level of switching noise suppression may be significantly less than the total surface-mount capacitance it replaces.

embedding process than for resistors). Also note that a second discontinuity appears in Figure 3-6 – a layer change. As board area decreased, so did the available wiring resources, eventually an additional layer pair had to be added to interconnect the system components.

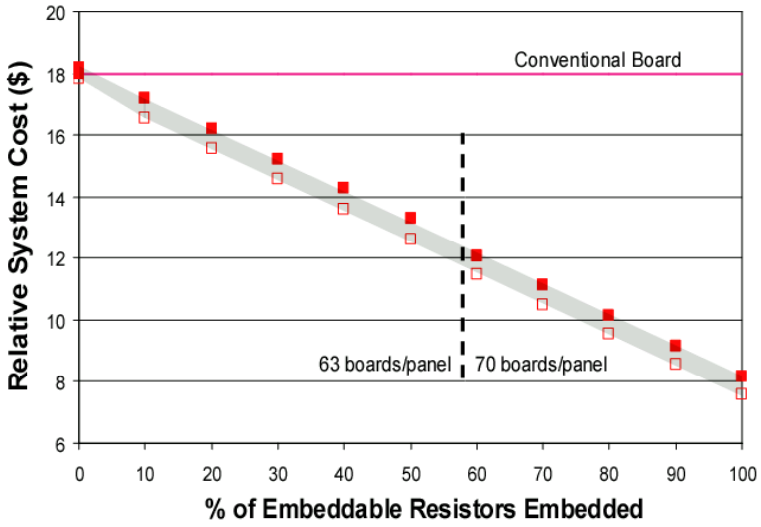


Figure 3-5: The economics of embedded resistors for the NEMI hand-held product sector emulator (5.5 x 5.5 cm board fabricated on an 18 x 24 inch panel). The data points represent specific embedded passive solutions; the solid horizontal line is the relative system cost of the conventional implementation.

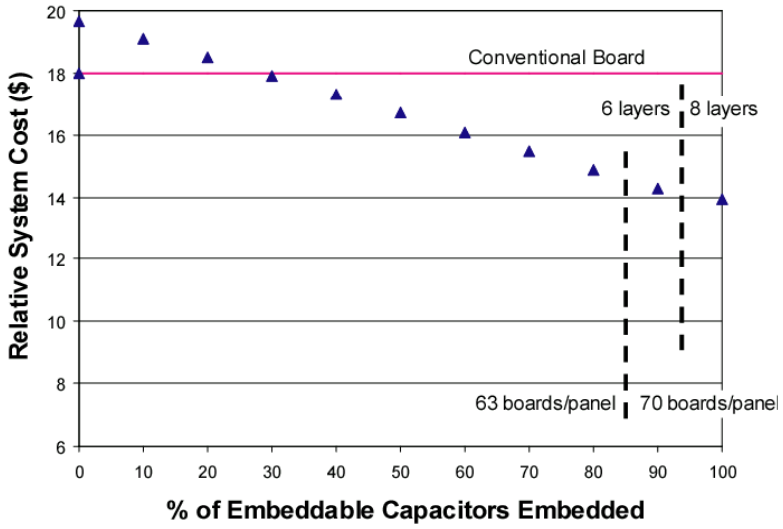


Figure 3-6: Capacitor embedding for the 5.5 x 5.5 cm NEMI hand-held product sector emulator. No embedded resistors are fabricated in this example. The baseline for this plot (the horizontal line) is the board with none of the embeddable capacitors embedded.

3.1.3 Fiber Channel Card

Figures 3-7 and 3-8 show the results of embedding resistors and bypass capacitors into the fiber channel card described in Table 3-1. In this case the board is large and only one can be fabricated per panel (results for two different panel sizes are considered in Figures 3-7 and 3-8). Because all the cost associated with fabricating embedded resistors on a panel has to be born by a single board, 25-35% of the 610 embeddable resistors need to be embedded to realize a cost savings. Figure 3-7 also shows that when there is less panel waste (i.e., when the board is fabricated on a smaller panel), embedded resistors become economical more quickly.

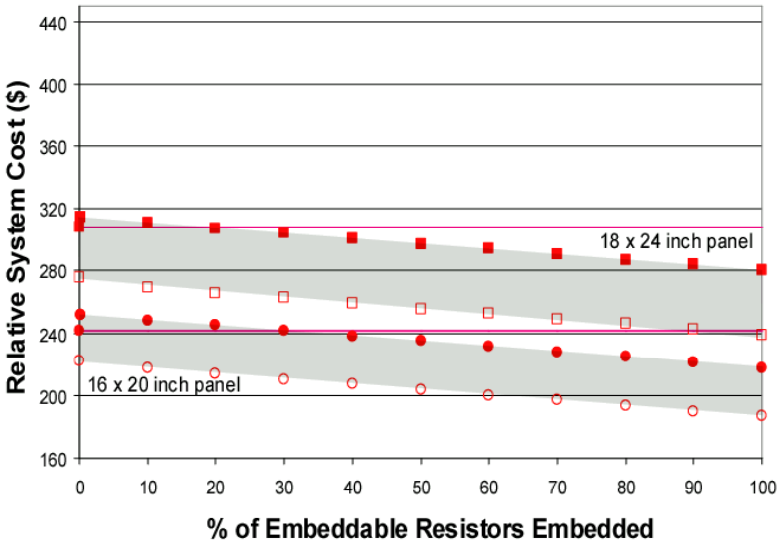


Figure 3-7: The economics of embedded resistors for the fiber channel card. The data points represent embedded passive solutions; the solid horizontal lines are relative system costs of conventional implementations.

Figure 3-8 shows the effect of integrating bypass capacitors for the fiber channel card. For this example there are only 242 embeddable capacitors on a 12 x 18 inch board (1.12 embeddable capacitors per square inch). As indicated in the hand-held and picocell examples, with such a low embeddable capacitor density it is not likely to be economical to embed the capacitors.

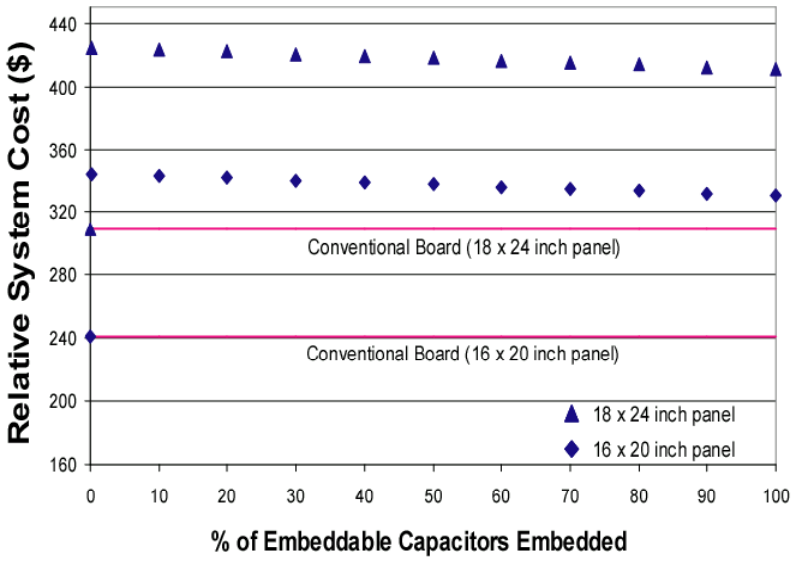


Figure 3-8: Capacitor embedding for the fiber channel card. Note, in this case there are no embeddable discrete non-bypass capacitors.

3.1.4 Generalization of Embedded Bypass Capacitor Results

The economics of embedded bypass capacitors can be generalized by observing the application-specific embeddable capacitor density necessary to breakeven on costs, i.e., by plotting the embeddable capacitor densities where the cost difference between the conventional and embedded passive implementations is zero (for the picocell board application this point is 6.9 embeddable bypass capacitors per square inch from Figure 34). Figure 3-9 shows the general result for the three applications considered in this chapter. The critical assumptions for this plot are: the board size and the number of layers required for routing is not allowed to change. The primary differentiator between the applications as far as this plot is concerned is the panelization efficiency (the total board area on the panel divided by the panel area). The dielectrics used to produce embedded capacitor layers are relatively expensive and would be purchased and used at the panel size, therefore, a low panelization efficiency indicates that the application is

wasting a lot of the expensive material, versus a larger panelization efficiency indicates less waste and therefore lower breakeven capacitor densities are possible.

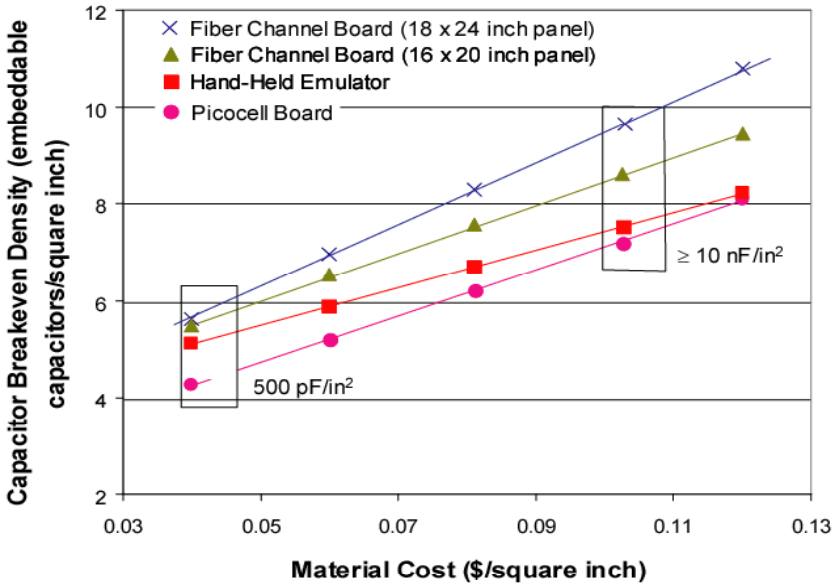


Figure 3-9: Bypass capacitor breakeven densities as a function of dielectric material replacement costs. Only single layer substitution is considered in this plot. The actual capacitor densities: Fiber Channel Board – 1.12 caps/in^2, Picocell Board – 2.76 caps/in^2, NEMI Hand Held Emulator – 23.44 caps/in^2.

3.2 Optimizing Embedded Passive Content

When passives are embedded into a PCB the designer would like to know what combination (type and quantity) of devices should be embedded to give the optimal cost (not every embeddable passive should necessarily be embedded). The model that has been discussed thus far (Chapter 2 and the examples in Section 3.1 of this chapter) utilizes the assumption that as long as a device is embeddable then it should be embedded, not taking into consideration that there may be a specific combination of embeddable devices that could produce a better cost benefit within the constraints of the quantity of embeddable devices present. For example each of the applications analyzed in this section demonstrate that embedding 100% of the embeddable resistors within the

PCB will be more economical than utilizing the conventional SMT method for resistors (using the additive technologies). However this analysis does not take into consideration that there may be a combination of different resistor types in the applications that may produce a smaller system cost than what is observed by embedding 100% of all the resistor types that are embeddable. Figure 3-10 illustrates the effects of embedding resistors on the board price function given by (13) for 2 different board sizes with the NEMI hand-held emulator characteristics. The change in board size demonstrates the

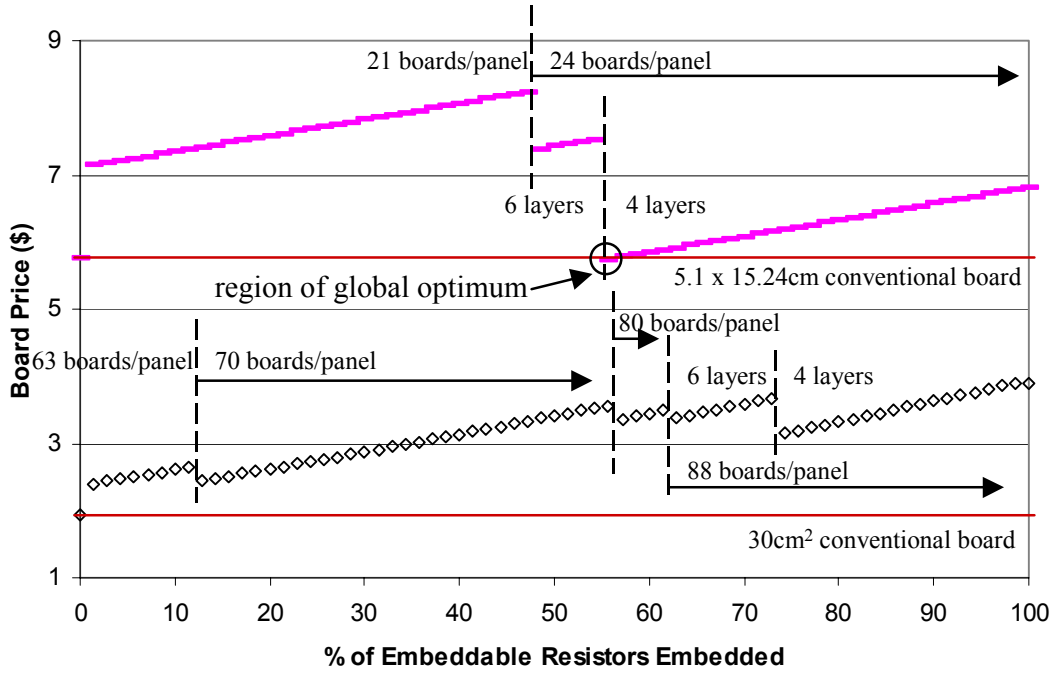


Figure 3-10: Effects of embedding embeddable resistors on the board price on NEMI hand-held emulator board. Note, minimization of the board price does not necessarily imply minimization of the system cost.

sensitivity of the embedded board price to the conventional board area. It also illustrates the region where the optimal board price is attainable for the 5.1 x 15.24 cm conventional board, but does not provide the combination of the resistor types that produces this result. For the 30 cm^2 conventional board the optimal board price solution is achieved by

maintaining the conventional surface mount technology (embedding zero resistors). Given the economic impact of the competing effects when embedded passives and the sensitivity of the system cost to the design variables it is imperative that some optimization technique be implemented using the model discussed in Chapter 2. To realize this potential benefit, the problem was simulated as an optimization problem that minimizes the system cost, (16). The optimization method used to solve for the optimal solution for embedding resistors and capacitors is discussed in Chapter 4.

CHAPTER 4 OPTIMIZATION OF EMBEDDED PASSIVE CONTENT IN A SYSTEM

Due to the large number of variables that are associated with the manufacturing of an electronic system, it is essential that an optimization model be implemented to capture the optimal number of embeddable devices that should be embedded to give the best cost value within the design constraints. The model discussed in Chapter 2 provides an insight into what is involve in the embedded passive process. Equations (1) through (23) show the discrete and continuous characteristics of the governing equations for the embedded passive process. These equations all contribute to total system cost, (16), for embedding passives in one form or another. Given the complex nature of the problem the evolutionary optimization technique called genetic algorithm (GA) is used to obtain the optimal solution.

This chapter details the implementation of a method built upon the analysis developed in Chapter 2 using Genetic Algorithms to obtain the optimal system cost solution for embedded resistors and capacitors. It also provides preliminary results from the Genetic Algorithms implemented model. Note it is not the objective of this dissertation to contribute in the field of optimization (or to even identify the best optimization approach to use); rather, the target here is to demonstrate that the embedded passive content of a system can be optimized, and to explore the resulting optimized solution in order to draw general conclusions.

4.1 Brief Overview of Genetic Algorithms (GAs)

Genetic algorithms (GAs) are search algorithms based on the mechanics of natural selection and natural genetics [32]. GAs models the idea of the survival of the

fittest and uses interbreeding between surviving populations as the basis of its search strategy. Each new population represents possible solutions to a specified problem. The GA keeps creating new populations from the old by ranking each member of the old population and interbreeding the fittest individuals to create the new populations, which are closer to the optimum solution to the given problem. Occasionally random new data is added to the process to keep the population from stagnating. This random new data is characterized as mutation. Each new population that is created by this process is considered a generation.

Figure 4-1 illustrates the structure of a single population genetic algorithm. There are 5 key components to this structure, namely, fitness function (operates within the evaluation of the function), selection, crossover (recombination), and mutation. The following discussion gives a brief summary of these components and the tasks associated with them.

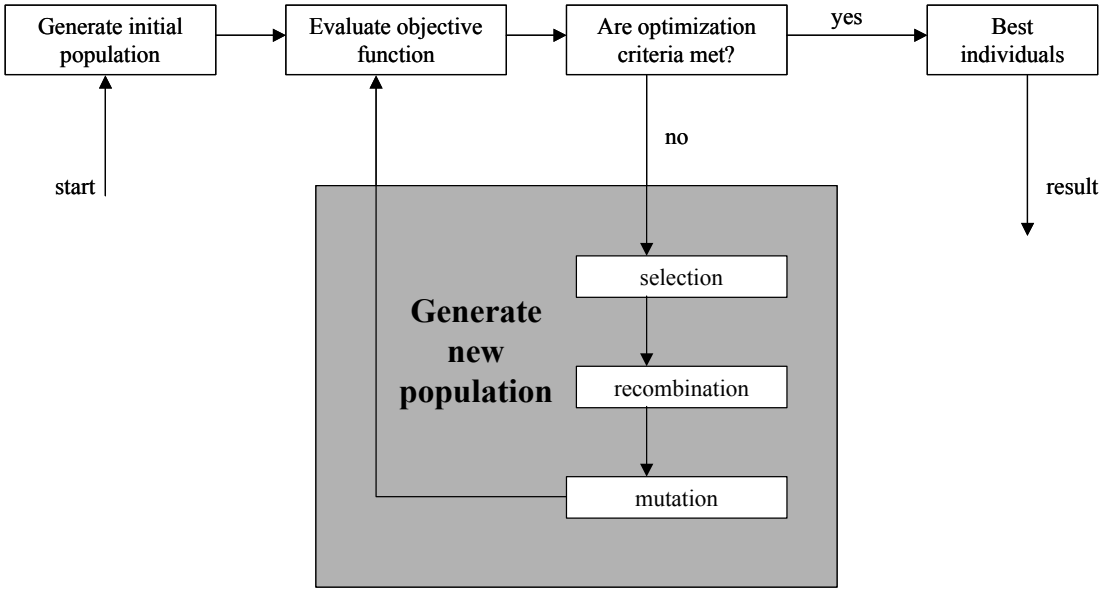


Figure 4-1: Structure of a single population genetic algorithm [33]

Fitness function as discussed previously is the measure used to rank the individuals of a population to determine which individual will survive for the next population generation. It is the measure of the quality of an individual. The fitness function is designed to give graded and continuous feedback about how well an individual performs.

The individuals that produce offspring are chosen in the selection component of the GA. This component comes directly after the fitness function has been evaluated. Each individual in the selection pool is given a reproduction probability depending on its objective value and the objective value of all other individuals in the selection pool. There are various different selection methods, including:

- Rank-based fitness assignment
- Roulette wheel selection
- Stochastic universal sampling
- Local selection
- Truncation selection
- Tournament selection

Choosing the appropriate method of selection for the GA application is critical since this is responsible for the speed of the evolution. In some cases it has also been responsible for premature convergence, which stalls the success of the GA.

Crossover is the method used by GAs for artificial mating. This method operates by picking out the individuals with high fitness values and explores the possibility that a combination of their characteristic (genes) may produce an even higher fitness value. Therefore individuals with high fitness values are given a high probability of mating.

Crossover is also a method of moving through the space of possible solutions based on the information gained from the existing solutions.

Mutation is regarded as the source of variation within the population and helps to keep the GA from stagnating. Variation increases an individual's chances of survival by making it more adaptable to its environment. Mutation represents innovation and is used as a search method in addition to crossover. In practice it is random adjustment in the individual's genetic structure (generally with a small probability).

4.1.1 The Difference Between GAs and Traditional Optimization Methods

The following list provides a few of the essential differences between GAs and other forms of optimization. A more detailed discussion of these differences can be found in Goldberg [32].

1. *Genetic algorithms use a coded form of the function values (parameter set), rather than with the actual values themselves*. For example, if we want to find the minimum of the function $f(x_1, x_2)=x_1^3+x_2^2+5$, the GA would not deal directly with x or $f(x_1, x_2)$ values, but with strings that encode these values. For this case, strings representing the binary x values would be used. This also gives GAs the ability to solve problems with a mixture of discrete and continuous variables.
2. *Genetic algorithms use a set, or population, of points to conduct a search, not just a single point in the problem space.* This gives GAs the power to search noisy spaces littered with local optimum points. Instead of relying on a single point to search through the space, the GAs looks at many different areas of the problem space at once, and uses all of this information to guide it, thus reducing the risk of getting stuck at local minima.

3. *GAs use only payoff information to guide them through the problem space*. Many search techniques need a variety of information to guide them. Hill climbing methods require derivatives, for example. The only information a GA needs is some measure of fitness about a point in the space (objective function value). Once the GA knows the current measure of fitness about a point, it can use this to continue searching for the optimum. This aspect makes GAs domain-independent
4. *GAs are probabilistic in nature, not deterministic.* This is a direct result of the randomization techniques used by GAs, making the search highly exploitative.
5. *GAs are inherently parallel.* This is one of the most powerful features of genetic algorithms. GAs, by their nature, are parallel, giving them the ability to deal with a large number of points (strings) simultaneously.

These differences of GAs over traditional optimization methods makes it a more advantageous methodology for optimizing embedded passives in printed circuit boards. The embedded passive system cost function, (16), is made up of a combination of discrete and continuous variables. For example $N_{up_{new}}$ and $N_{layers_{new}}$ are both discrete variables and A_{new} is a continuous variable. This discrete variable component of (16) hinders the hill climbing optimization methods capability of accurately modeling the function since these methods are dependent on the derivative of the function to search through the solution space. Also, for certain applications the solution space will contain multiple local minima making it even more difficult for the hill climbing method to find the global minimum. The use of a GA to minimize the system cost function will also produce faster solutions because of its inherent capabilities to evaluate the system costs for multiple types of resistors and capacitors simultaneously. A multi-population genetic

algorithm is used to search the solution space for embedded resistors and capacitors and find the optimal cost solution for specific system application.

A constrained nonlinear optimization method was initially applied to the embedded passive optimization problem but yielded unsatisfactory results. This was due to fact that the method assumes the function to be minimized and the constraints must both be continuous. Even when the embedded passive optimization problem is approximated as continuous (which is it not – you can not embedded a fraction of a resistor) the results only proved to be local minima and not the global minimum of (16), the embedded passives system cost function. These results prompted the abandonment of the constrained nonlinear method for the more robust multi-population genetic algorithm approach to solve the problem.

4.1.2 Multi-Population Genetic Algorithm (MPGA)

MPGAs are GAs that are equipped to handle many populations. In this case every subpopulation is allowed to evolve for a few generations in isolation similar to the single population genetic algorithm before one or more individuals are exchanged between the subpopulations by a process called migration. One of the major disadvantages of standard GAs is their inability to maintain diversity in the population. This lack of diversity can lead to a number of problems such as converging to a non-global optima or not being able to react to changes in the environment [39]. This gives MPGAs a significant edge over single population GAs which is its capability to model the evolution of species in a way that is more similar to nature. For this reason a MPGA is used to optimize the embedded passive process.

4.2 Implementation of a Multi-Population Genetic Algorithm

The MPGA used to optimize the embedded passive process was developed by Chipperfield and Fleming from the department of Automatic Control and System Engineering at Sheffield University, UK [34]. This MPGA was developed as a Genetic Algorithm Toolbox for use in MatLab[11]. The process of implementing the embedded passive model into MPGA is discussed in Appendix D.

4.2.1 Objective Function for Optimization of Embedded Passive Content

The objective function for optimizing the embedded passive content is given by the following equation;

$$Min\ J = Min_{x=L,\, y=M,\, z=N}\left(C_{discrete}(x, y, z) + P_{board}(x, y, z)\right) \tag{24}$$

where,

L = [0, Total number of embeddable resistors]

M = [0, Total number of embeddable nonbypass capacitors]

N = [0, Total number of embeddable bypass capacitors]

P_{board} and $C_{discrete}$ are defined by (13) and (15), from Chapter 2, respectively. For nonnegative control, the objective function is obtained by using the following constraints:

New wiring per layer pair: $W_{layer_{new}}(2b) > 0$

Number of new boards per panel: $N_{up_{new}} > 0$

Area of new board: $A_{new}(1) > 0$

Discrete resistor value: R > 0

[11] MatLab (MATrix LABoratory) is an interactive system for matrix-based computation designed for scientific and engineering use. It is useful for many forms of numeric computation and visualization. Besides dealing with explicit matrices in linear algebra, it can handle differential equations, polynomials, signal processing, and other applications. Results can be made available both numerically and as excellent graphics. The program is written in Fortran and is designed to be readily installed under any operating system which permits interactive execution of Fortran programs.

Discrete capacitor value: c > 0

Area of conventional board: A_{conv} > 0

Number of I/O on conventional board: $N_{IO_{conv}}$ > 0

Number of discrete passives: $N_{discrete}$ ≥ 0

4.2.2 NEMI Hand Held Application Example

The MPGA developed in [34] has been tailored to accommodate the NEMI handheld PCB described in Tables 3-1 and 3-2. The objective function used in this analysis is defined by (24). The number of decision variables, NVAR, is 5, one for each control input (5 different distinct passives – 2 distinct resistors and 3 distinct capacitors present in the system).

The parameters for the MPGA are defined in Table 4-1.

Table 4-1: Parameters for MPGA Example

Generation gap	0.8
Crossover rate	1
Mutation rate	1/NVAR
Maximum number of generations	700
Insertion rate	0.9
Number of subpopulations	8
Migration rate	0.8
Number of generations / migration	20
Number of individuals / subpopulation	20

4.3 Analysis of MPGA Results for the NEMI Hand-Held Emulator

This section provides results obtained from the implementation of the MPGA with the Chapter 2 model on the NEMI hand-held emulator application. Only the embedding of the 2 distinct embeddable resistor types has been addressed in this section in order to simplify the visualization of the results and allow a complete explanation of the design space to be performed in order to verify the optimization analysis result. The

analysis provided herein verifies the complexity and application specificity that is inherent in the embedded passive technology. The NEMI hand-held emulator considered in this section differs from the one in Table 3-1 by the number of embeddable resistors that are available in both categories of resistors and the assumed board size. In this analysis there are 350 embeddable resistors for each resistor category and the conventional board size set at 5.1 x 15.25 cm.

4.3.1 MPGA Optimization

The optimization results obtain from the MPGA is shown in Figure 4-2. In the NEMI emulator there are 5 distinct embedded passive types (bypass capacitor, 2 distinct singulated capacitors, and 2 distinct resistors) – see Table 3-1.

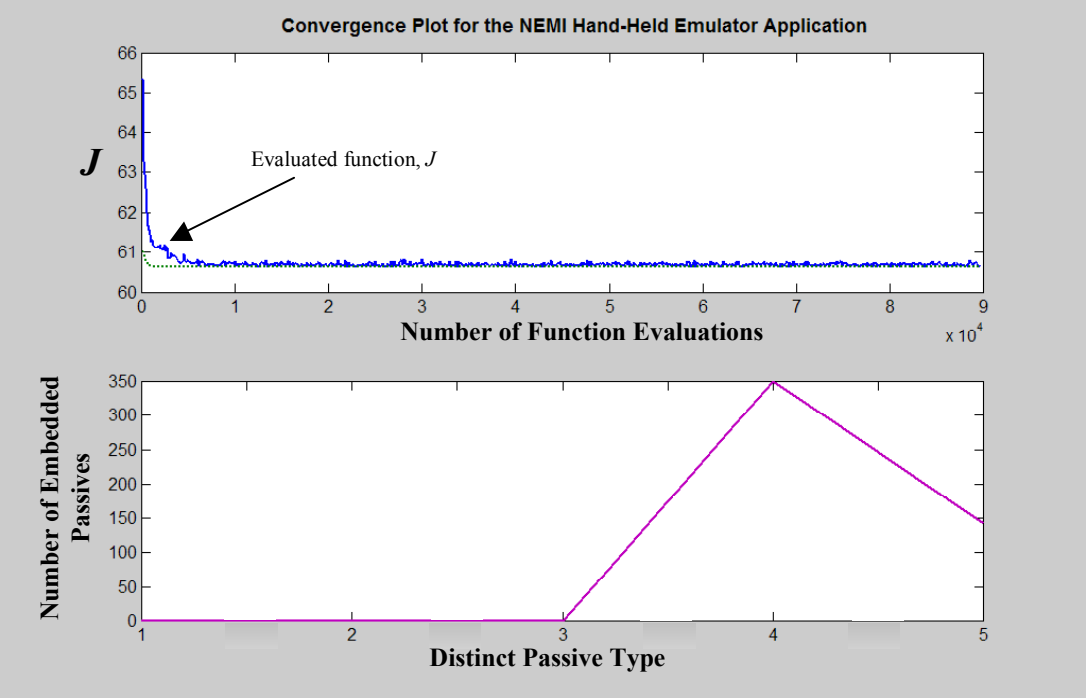


Figure 4-2: Convergence Plot for NEMI Hand-Held Application

The results shown in Figure 4-2 only takes into consideration the 2 distinct resistor types that are present in the NEMI hand-held emulator and are represented as

distinct passive type 4, 5 of which there are 350 of each. The difference in these resistor types are presented in Table 3-1 where the passive type 4 represents the resistors with values less than 100Ω and passive type 5 represents the resistors with values ranging from 100Ω to 1000Ω. The analysis presented in Figure 4-2 illustrates that the objective function, *J*, converges to approximately $60.60 and the number of embedded distinct passives of type 4 is 350 and type 5 is approximately 142 as shown in the bottom part of Figure 4-2. The exact number of passive types that are embedded in this example and the global minimum cost that are obtained from MatLab are: Optimal number of embedded passives = [350,142] and the global minimum cost is $60.63. Discussion and verification of these results is provided in the following section.

4.3.2 Verification of MPGA Results

A complete exploration of the design space using the model developed in Chapter 2 was used to verify the MPGA results. This was done by generating the surface plot of the total system cost function, (16), for all the possible combinations of embedding the 2 resistor types. A surface plot for the board price was also generated and is shown in Figure 4-3. Figures 4-4 and 4-5 both represent the total system cost for the NEMI handheld application when resistors are embedded. The resistor Type 1 and Type 2 shown in Figures 4-3 and 4-4 represent the resistors with values less than 100Ω and the resistors with values ranging from 100Ω to 1000Ω respectively and come from Table 3-1.

In order to understand the explanation of the features of the surface plots that follow in this section, some brief background on printed circuit board manufacturing is required. Printed circuit boards are fabricated by laminating together a set of “layer pairs”. A layer pair is a layer of dielectric with patterned conductors on both sides.

Conductor layers only occur in pairs in most printed circuit board constructions, i.e., you cannot have an odd number of conductor layers. The number of layer pairs needed depends, in part, on the amount of wiring resources required to route the application. Printed circuit boards are fabricated on large panels (e.g., 18 x 24 inches is one standard panel size). The maximum number of boards that can be laid out on a panel is called the number-up and depends on the size and aspect ratio of the individual boards. Many of the features of the surface plots that follow are a result of the changes in the number of required layer pairs and the number of boards that can be fabricated within a fixed panel size as resistors are embedded.

Figure 4-3 shows the effects of embedding resistors on the board price for the NEMI hand-held application. The numerical labels on the plot represent the regions of interest. Region 1 shows the effects of the resistor layer pair cost on the board price – when the first resistor is embedded the resistor layer pair cost increases significantly

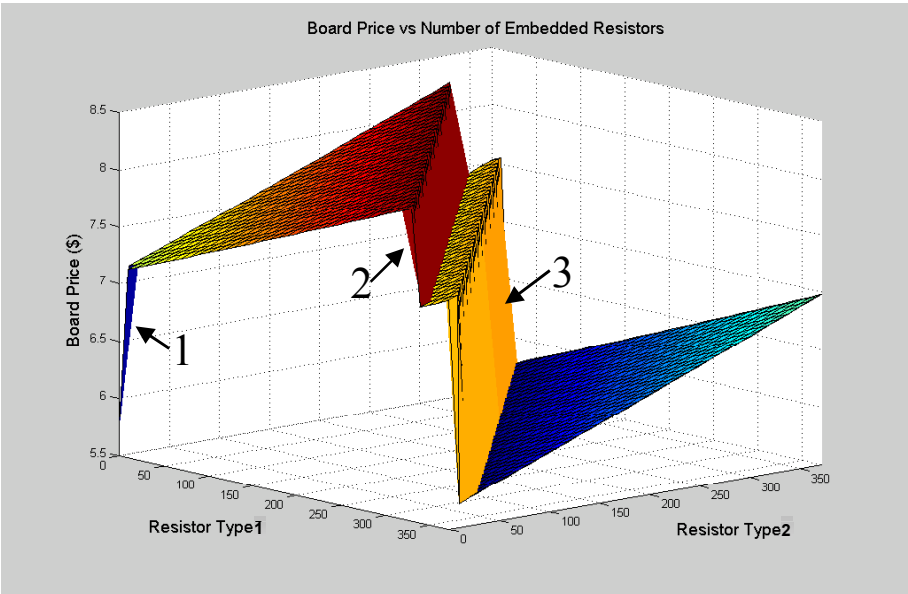


Figure 4-3: Surface plot showing the effects of embedding resistors on board price for the NEMI hand-held emulator

resulting in a jump in the board price. As resistors are embedded the board price increases until the number of boards on a panel (number-up) changes at region 2. At region 3 the board price is dropped even further by the decrease in the number of layer pairs required for this application. The number of layer pairs required decreases because the increase in wiring blocked occurs at a much smaller rate than the decrease in board area, therefore the minimum number of layers required for embedding resistors decreases. The regions in between the numerical labels show the linear relationship of embedding resistors on the board price. The global minimum in board price for this application is observed when all the resistors of Type 1 and 0 resistors of Type 2 are embedded.

Figure 4-4, shows the surface plot for the total system cost. The numerical labels 1 to 7 illustrate the regions on the surface where there is a significant change in the total system cost. The regions numbered 2, 3, 5, and 6 illustrate the effects of layer pair change on the system cost. At each of these regions the number of layer pairs has increased resulting in an increase in the total system cost. Region 1 shows the effect of the resistor

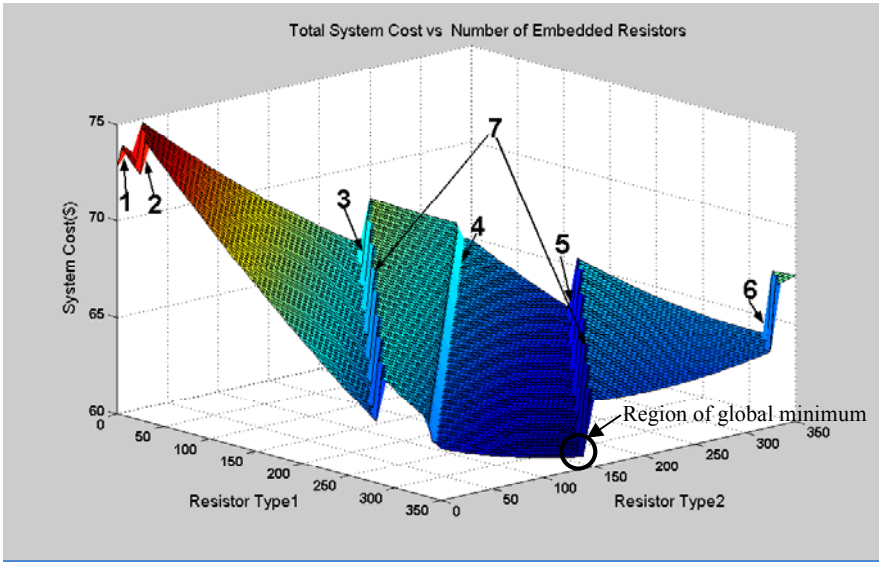


Figure 4-4: Surface plot of optimization results for system cost on the NEMI hand-held emulator

layer cost on the system cost and region 4 shows a drop in the system cost when the number of boards produced on the panel increases. Region 7 shows the effects of the resistor type on the system cost. In this analysis the resistor value of Type 1 resistor is less than that of Type 2, therefore it utilizes less area on the board and contributes less to the increase in the minimum number of layer pairs required to route the application. This effect is demonstrated by the step formation that is observed at the regions of layer pair change in the system. Figure 4-4 also shows the region where the global minimum is attainable. The system cost and the number of embedded resistors of each type that are observed at the region of global minimum is consistent with the solution obtained by the MPGA in Section 4.3.1.

Figure 4-5 shows the diagonal cross section of the surface plot shown in Figure 4 4. It is important to note that in this application although embedding all embeddable resistors is more economical than the conventional solution it does not provide the optimal cost for the system. The minimum feature size for the embedded resistors in the

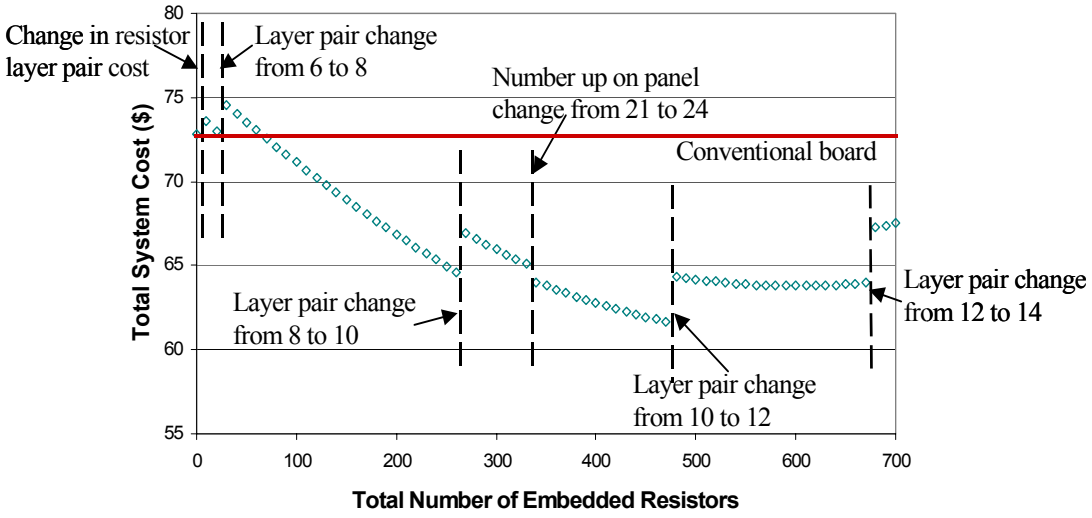


Figure 4-5: Cross section of the surface plot presented in Figure 4-4 for total system cost

analysis shown in Figures 4-2, 4-4, and 4-5 was set at 50 mils (.050 inches) as oppose to the 15 mils (.015 inches) shown in Table 3-2. This increase in the minimum feature size increases the rate at which the wiring block increases to a rate much faster than what is observed in Figure 4-3, therefore the minimum number of layers required for embedding resistors increases at regions 2, 3, 5, and 6 in Figure 4-5.

By restricting the analysis to 2 variables it is possible to visualize the effects of embedding devices on the system cost. In reality the system will have more than 2 variables, as is the case for the full NEMI application. In this case the system optimization is difficult to visualize. The MPGA utilized to optimize the model in Chapter 2 provides a quick and reliable solution to finding the mix of embeddable devices to embed to realize the best cost solution for embedded passive applications.

4.4 Summary

This chapter provided the basis for using GAs as the means for finding the optimal solution for embedding resistors and capacitors into a printed circuit board. It presented a simplified example to demonstrate the viability of the model. The chapter also included a verification of the optimizer result generated by considering all solutions for the simple case. Chapter 5 discusses the results of a real case study.

CHAPTER 5 SENDO GSM M550 CELL PHONE CASE STUDY

In order to demonstrate the validity and commercial benefits of the embedded passive cost model developed in this research the model was applied to an existing hand held device, a SENDO M550 dual-band GSM folder-phone shown in Figure 5-1. This chapter provides an analysis of the system cost for a SENDO M550 GSM cell phone main board.

Figure 5-1: SENDO M550 (courtesy Portelligent)

5.1 Product Description

The SENDO M550 is a dual band GSM phone with a clamshell design and a WAP 1.2.1 color browser and class 8 GPRS. The phone features an internal CSTN 4,096 color display with a 128 X 128 pixel resolution. The outer LCD is a reverse video, monochrome display with a 96 x 64 pixel resolution. The phone utilizes Tegic T9® text

input as well as SMS templates to allow for faster text messaging. SENDO has included a battery pack that allows for up to three hours of continuous play [40].

This phone is made up of 17 major components listed below [40]:

1) Display Bezel	7) RF Shields	13) Inside Display
2) Main Board	8) Hinge Flex	14) Main Display
3) Battery	9) Buzzer/Ringer	15) Rear Enclosure
4) Display Board	10) Earpiece	16) Rear Cover
5) Display Enclosure	11) Keyboard Bezel	17) Hinge Spring
6) Outside Cover	12) Keypad	

The component of interest for this study is the main board shown in Figure 5-2.

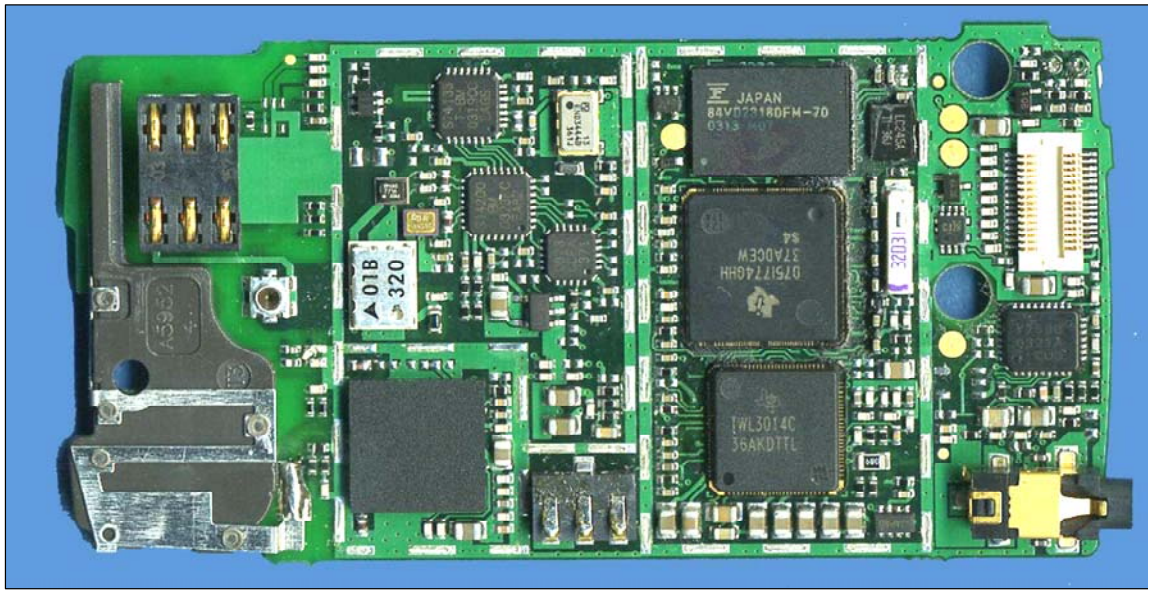


Figure 5-2: Main board for SENDO M550 GSM cell phone showing the majority of the electronics in the product (courtesy Portelligent)

The breakdown of the relevant passive components and their associated characteristics and board design parameters are listed in Table 5-1.

Table 5-1: SENDO M550 GSM/GPRS phone main board characteristics

	centimeters	inches			
Board Width	3.88	1.53			
Board Length	7.58	2.98			
Number of nets	326				
Number of holes	1303				
Assembly cost ($/discrete)	0.005				
Part Type	**Cost per part ($)**	**Quantity**			
Resistors	0.001	55			
Capacitors	0.005	149			
Resistor breakdown	**Length (mils)**	**Width (mils)**		**Quantity**	
100 ohms	40	20		7	
500 ohms	40	20		24	
5000 ohms	40	20		7	
50000 ohms	40	20		14	
500000 ohms	80	50		2	
1000000 ohms	80	50		1	not embeddable
			Total	**55**	
Total number of embeddable resistors				**54**	
Capacitor breakdown	**Length (mils)**	**Width (mils)**		**Quantity**	
bypass 100 pF	40	20		64	
bypass 1 nF	40	20		24	
bypass 15 nF	40	20		13	
bypass 30 nF	60	30		14	
bypass 100 nF	60	30		19	
non-bypass 250 nF	80	50		1	
non-bypass 1 microF	80	50		8	
non-bypass 2 microF	120	60		1	
non-bypass 9 microF	130	100		1	
non-bypass 10 microF	138	110		4	not embeddable
			Total	**149**	
Total number of embeddable bypass capacitors				**134**	
Total number of embeddable non bypass capacitors				**11**	
Total number of embeddable capacitors				**145**	

The SENDO M550 main board was analyzed using both the simple model discussed in Section 2.1.1 and the new model developed in this research. Figure 5-3 shows the process flow for the existing simple model consisting of the following three steps: 1) reduce the system cost by the purchase price and conversion costs associated with the replaced discrete passives, 2) reduce the board size by the sum of the layout areas associated with the replaced discrete passives and determine the new number of boards on the panel, and 3) determine the new board cost based on a higher per unit area

cost for the embedded passive panel fabrication and the new number-up computed in step 2. The results of these three steps determine the new system cost.

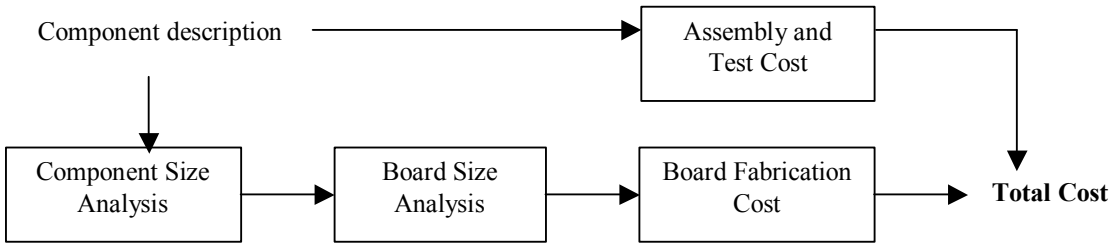


Figure 5-3: Existing Simple Model

Figure 2-1 and Section 2.1.2 in Chapter 2 illustrates and describes the process flow for the new model developed in this research, which has an additional five process steps in addition to the four present in the simple model.

5.2 Results and Discussion

This section discusses the results obtained from the simple and the new model for performing economic analysis of embedded passives for the SENDO mobile phone main board. The Portelligent information provided an actual board manufacturing cost, which was used to calibrate both the simple and new model. This calibration was done by equating the board manufacturing cost in the models when no passive devices are embedded to that of Portelligent's board manufacturing cost. This board manufacturing cost was used as a benchmark throughout the modeling process. Table 5-2 shows the system cost for embedding the embeddable passive components on a SENDO M550 GSM phone main board when using the existing system cost model and the new system cost model developed within this research.

The results obtained from each model are significantly different when applied to the same type and quantity of embeddable passives. In the simple model case it is observed that by embedding all the embeddable passive components it is possible to get a

Table 5-2: SENDO M550 GSM/GPRS main board system cost for varying combinations of embedded passive components predicted by the existing simple model and the new model (board shrinkage allowed).

	Bypass Cap	Resistor ≤ 5 kΩ	5 kΩ < Resistor ≤ 50 kΩ	50 kΩ < Resistor ≤ 500 kΩ	System cost ($)	18 x 24 inch panel
Simple Model	134	38	14	2	31.90	No. of Layers = 6 No. of boards/panel = 70
	134	38	14	0	31.08	**Best Cost Solution** No. of Layers = 6 No. of boards/panel = 70
	0	0	0	0	34.43	No. of Layers = 6 No. of boards/panel = 65
New Model	134	38	14	2	35.99	No. of Layers = 10 No. of boards/panel = 70
	134	38	6	0	32.37	**Best Cost Solution** No. of Layers = 6 No. of boards/panel = 70
	0	0	0	0	34.43	No. of Layers = 6 No. of boards/panel = 65

significantly lower system cost than by not embedding any of the embeddable passives. This observation is reversed when looking at the system cost obtained from the new model. This disparity is primarily due to the routing analysis and layer pair calculation performed within the new model, which is not accommodated within the existing simple model. In the existing simple model the number of layers utilized remains the same as that used in the conventional passive board manufacture regardless of the number of passives embedded. If a decision had been made based on the simple model then all of the embeddable passive would be embedded and the true system cost for the SENDO M550 GSM main board would in fact be greater than the system cost when no embeddable passives are embedded, $35.99 as oppose to $34.43 respectively. This simple model analysis is unrealistic since it does not take into consideration the wiring capacity of the board as passives are embedded especially when board shrinkage is allowed.

The best cost solution for the SENDO M550 GSM phone main board was also analyzed for both models by running each model within an optimization environment. In the simple model the best cost solution is realized when there are 134 bypass capacitors,

38 resistors with values ≤ 5 kΩ and 14 resistors with values ≤ 50 kΩ embedded. This combination of embedded passive components provides a system cost of approximately $31.08. In the new model the best cost solution is realized when there are 134 bypass capacitors, 38 resistors with values ≤ 5 kΩ and 6 resistors with values ≤ 50 kΩ embedded. This combination of embedded passives provides a system cost of approximately $32.37. Note only 6 resistors with values ≤ 50 kΩ are embedded in the new model since any increase beyond 6 resistors would require an additional layer pair thus increasing the system cost. The increase in system cost for the new model is due to the profit margin/throughput analysis performed in the new model as well as the rework analysis and the layer pair calculation.

The best cost solution for the simple cost model is realized when 134 bypass capacitors, 38 resistors ≤ 5 kΩ and 14 resistors ≤ 50 kΩ and the best cost solution for the new cost model is realized when there are 134 bypass capacitors, 38 resistors ≤ 5 kΩ and 6 resistors ≤ 50 kΩ. Figures 5-4 to 5-9 shows the surface plot for the best cost solution for both the simple embedded passive cost model and the new embedded passive cost model.

The effects of embedding resistors ≤ 5 kΩ and resistors ≤ 50 kΩ for the new model and the simple model is shown in Figure 5-4 and Figure 5-5 respectively. Figure 5-4 and Figure 5-5 demonstrate significant differences in utilizing the new model and the existing model to perform economic analysis on the embedded passive technology. Figure 5-4 shows the effects of the routing analysis on the system cost when the layer count changes and limits the embedding of resistors ≤ 50 kΩ to 6 for the best cost solution. Due to the absence of this routing analysis in Figure 5-5 there are no changes in

the layer count and the best cost solution is observed when all 14 of the resistors ≤ 50 kΩ are embedded.

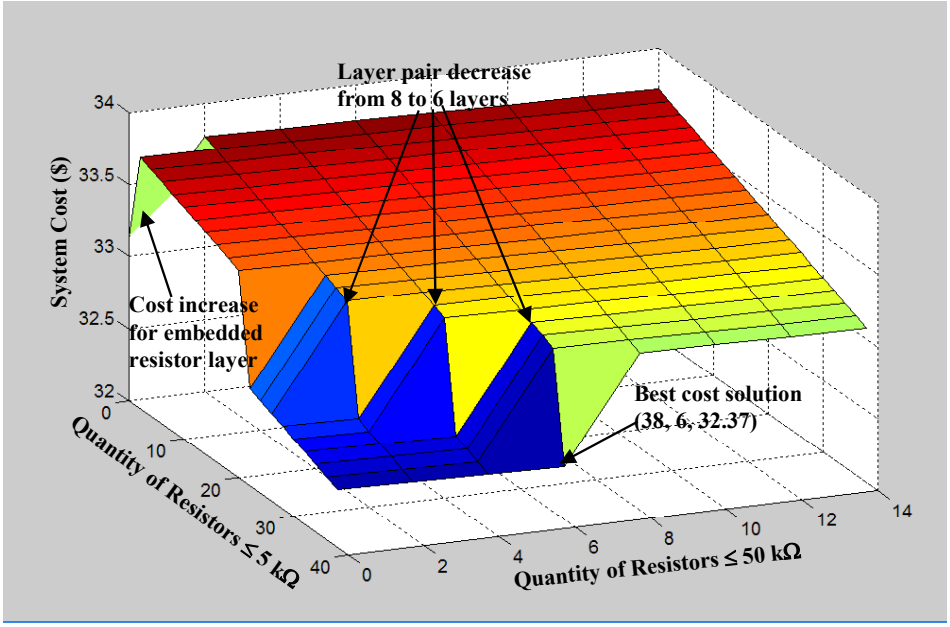


Figure 5-4: Surface plot showing system cost as a function of embedding resistors ≤ 5 kΩ and resistors ≤ 50 kΩ for the best cost solution within the new model

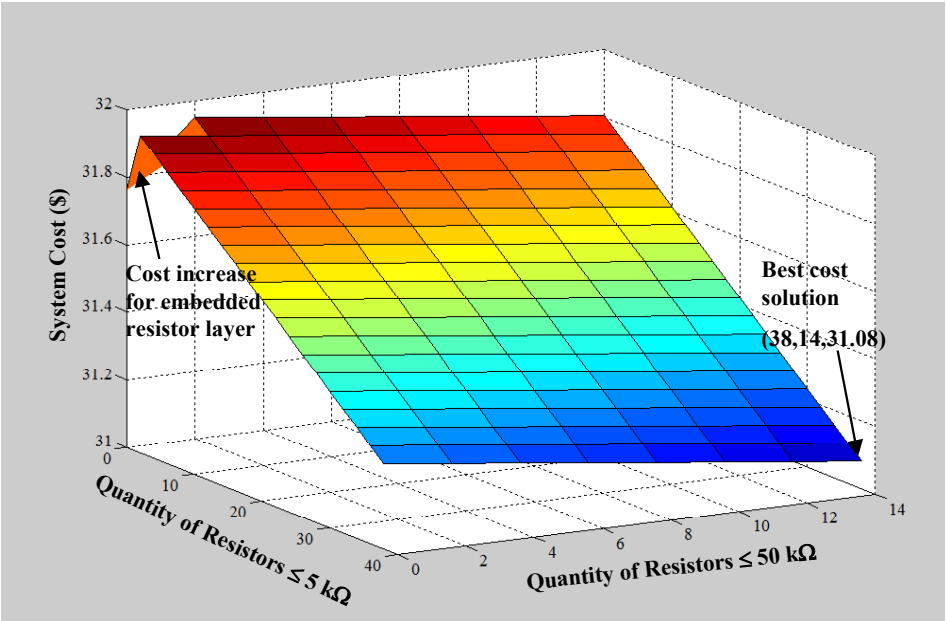


Figure 5-5: Surface plot showing system cost as a function of embedding resistors ≤ 5 kΩ and resistors ≤ 50 kΩ for the best cost solution within the simple model

Figure 5-6 and Figure 5-7 show the effects of embedding resistors ≤ 5 kΩ and bypass capacitors on the system cost where Figure 5-6 represents the new model and Figure 5-7 represents the existing simple model. Although these figures demonstrate significantly different in the surface analysis they both illustrate that the best cost solution

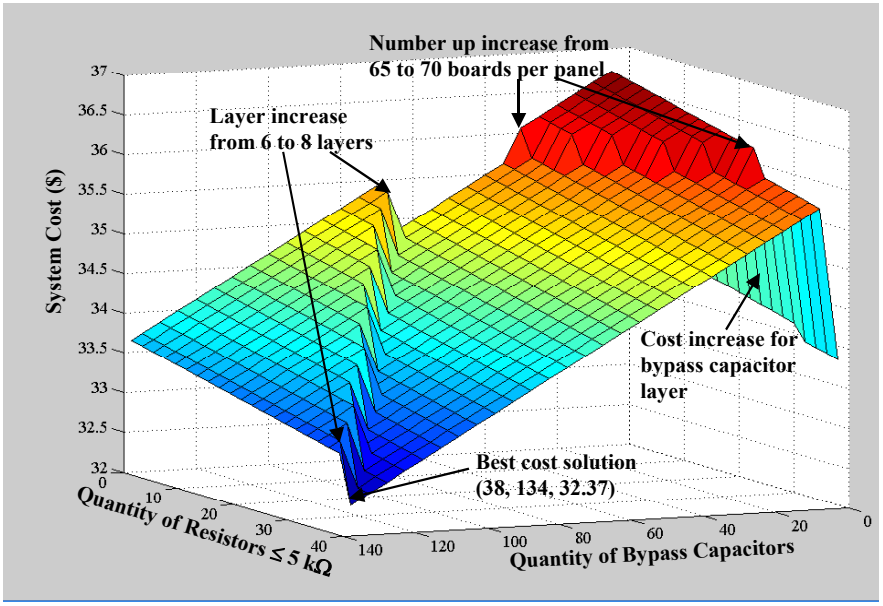


Figure 5-6: Surface plot showing system cost as a function of embedding resistors ≤ 5 kΩ and bypass capacitors for the best cost solution within the new model

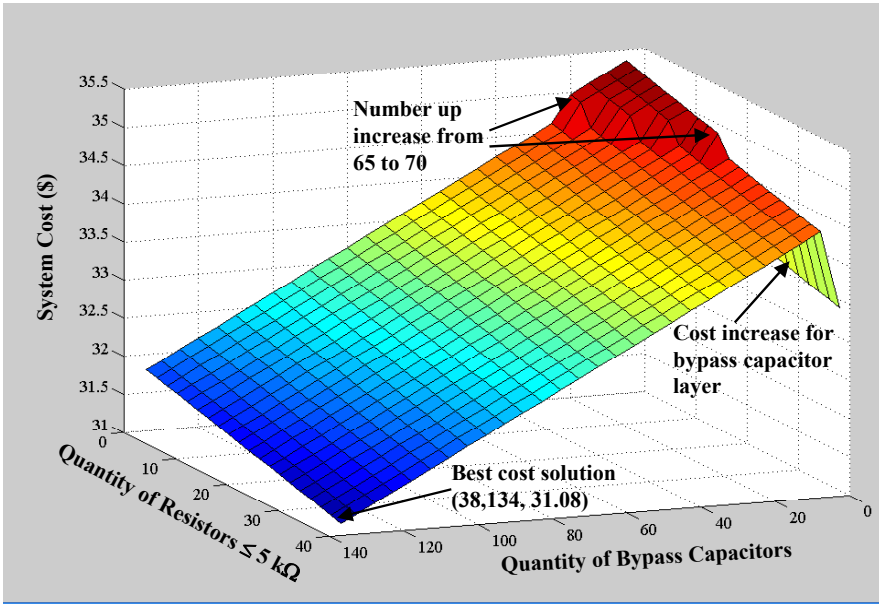


Figure 5-7 Surface plot showing system cost as a function of embedding resistors ≤ 5 kΩ and bypass capacitors for the best cost solution within the simple model

is achieved by embedding all the resistors ≤ 5 kΩ (38 resistors) and by embedding all bypass capacitors (134 bypass capacitors).

Figure 5-8 and Figure 5-9 demonstrate the effects of embedding resistors ≤ 50 kΩ and bypass capacitors on the system cost. In this case Figure 5-8 represent the new model

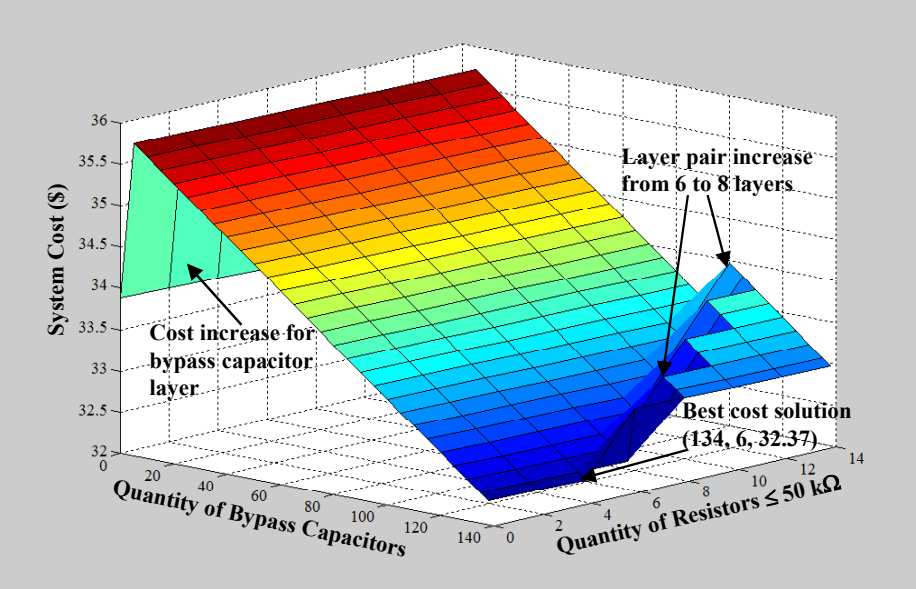


Figure 5-8: Surface plot showing system cost as a function of embedding resistors ≤ 50 kΩ and bypass capacitors for the best cost solution within the new model

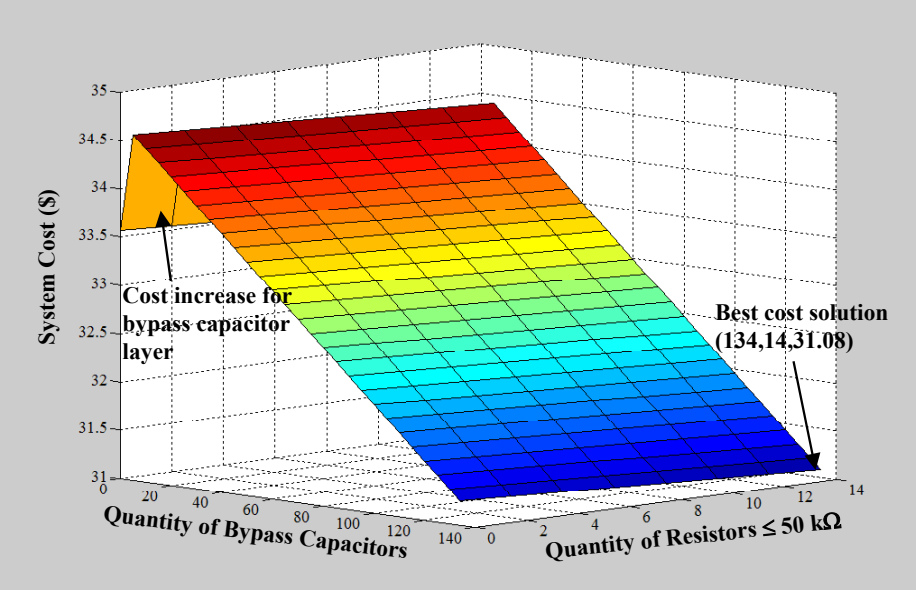


Figure 5-9: Surface plot showing system cost as a function of embedding resistors ≤ 50 kΩ and bypass capacitors for the best cost solution within the simple model

and Figure 5-9 represent the simple model. Like in Figure 5-4 the effects of the routing analysis and layer pair calculation limits the number of embedded resistors ≤ 50 kΩ to six layers in order to realize the best cost solution. This is not the case in from the simple model which dictates that all 14 resistors ≤ 50 kΩ and all bypass capacitors should be embedded to obtain the best cost solution.

Figure 5-10 shows the convergence plot for the SENDO M550 GSM cell phone within new model (*J* represents the objective function and is defined in (24)).

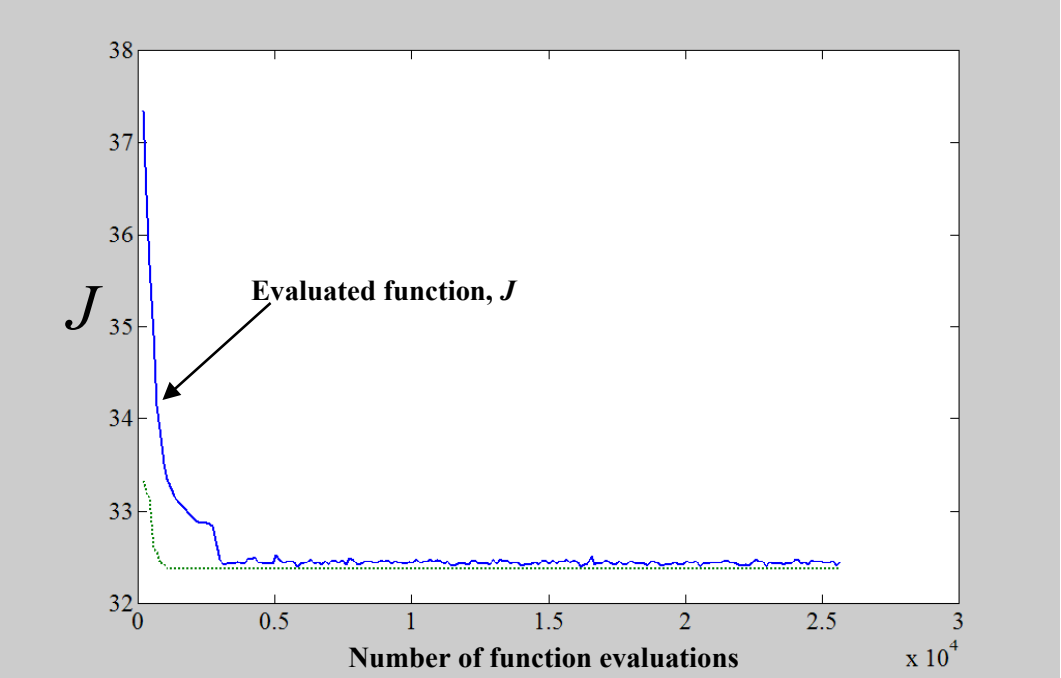


Figure 5-11: Convergence plot for the SENDO M550 GSM cell phone application

5.3 Summary

This chapter provided the results from both the existing approach to performing embedded passive economic analysis and the new approach developed within this research on a SENDO M550 cell phone. The results demonstrate the potential misleading conclusions (and the risk of poor design decisions) that can be drawn when using the simple model in some cases. The new model developed also shows the economic saving

that is possible by embedding the right combination of embeddable devices thus making available a much needed embedded passive economic analysis package to the decision makers within the embedded passive industry.

CHAPTER 6 ANALYZING SYSTEM SIZE/COST TRADEOFF

The solution from the analysis performed in Chapters 3-5 only considered either maintaining a constant board area (board area remains unchanged as parts are embedded) or reducing the board area by the part footprint areas as parts are embedded (preserving the board's original aspect ratio). This chapter more closely examines the effect of board size on the optimum solution (minimum cost solution) and assesses whether better system solutions can be found by varying or constraining the size of the board in different ways. Besides the original board area treatments mentioned above, two additional approaches were formulated to analyze the effects of board size on the system cost. The first approach was to select a range of fixed board sizes and determine the optimal embedded content for each size, then check to see if the selected fixed size/content is a physically possible solution. The second approach was to select a range of fixed board sizes and determine what content has to be embedded to allow the selected fixed board size to happen.

The size/cost analyses in this chapter are carried out for two specific applications, the SENDO GSM cell phone (described in Chapter 5, Table 5-1) and the NEMI Hand Held emulator (described in Chapter 3, Table 3-1). The two alternative approaches to determining/constraining board area and content shed considerable additional light on the assumptions in the original optimal solution and allows the determination of the circumstances under which the solution approach taken in Chapter 4 represents the optimal solution.

6.1 Determining Optimal Embedded Content for Selected Fixed Board Sizes

Determining the optimal embedded content for fixed board sizes was done by varying the size of the SENDO and the NEMI Hand-Held printed circuit boards by small increments. Each new board size was then subjected to the MPGA process discussed in Chapter 4 to determine the optimal embedded content, i.e., the embedded passive content that minimizes the system cost for the selected fixed board size. Note, the components that must be accommodated by the boards are a constant, i.e., they do not vary with the board size. Also, the passive components that are candidates for embedding (i.e., embeddable passive content) is a constant that does not vary with board size. An analysis was then performed to determine the conditions under which each result could be valid, i.e., to determine whether the selected board sizes and their optimized embedded content are physically possible to obtain.

Figure 6-1 shows the effects of board area on system cost for the SENDO GSM cell phone application. In Figure 6-1 each data point was generated by selecting a fixed board area (the fixed areas range from 2 in^2 to the conventional board area of 4.56 in^2) and running the optimization process in Chapter 4 with board shrinkage not allowed, to determine the content and system cost. The "Allow board shrinkage solution" in Figure 6-1 represents the Chapter 4 solution that shrinks the conventional board as embeddable passives are embedded. The decrease in system cost for the fixed board size solutions is primarily governed by the changes in the number of boards that can be produced per panel area (number-up). In cases where the number of boards produced per panel is constant, the system cost remained constant (even when the board size was decreased).

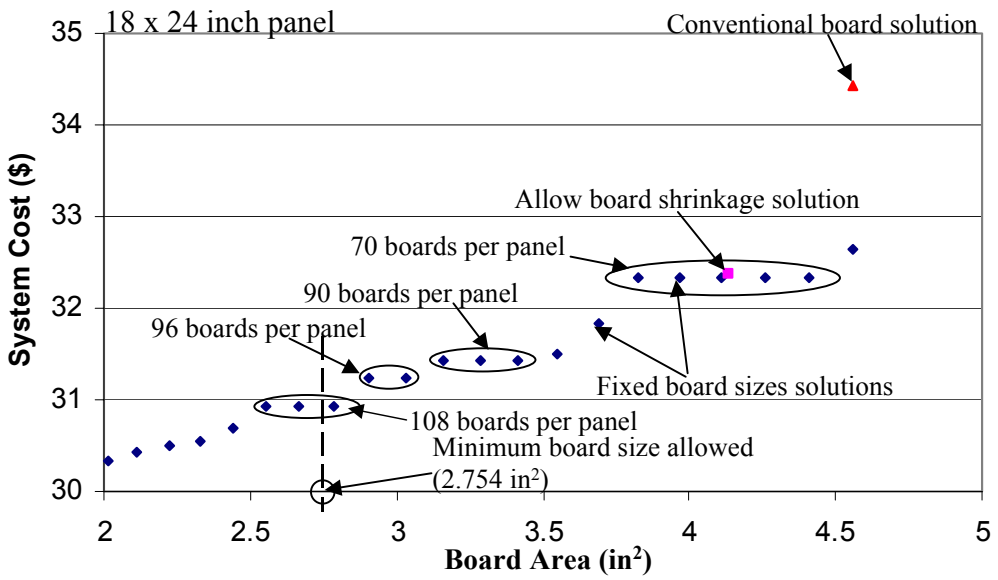


Figure 6-1: Effects of fixed board sizes on system cost for SENDO GSM cell phone application, where the optimized embedded content was determined for each fixed board size.

The embedded content also remains the same in all cases (134 bypass capacitors, 38 resistor of resistive value less than 5 kΩ and 14 resistors of resistive value between 5 kΩ and 50 kΩ)[12] except board areas 2.12 in^2 and 2.01 in^2 where the number of resistors with resistive values between 5 kΩ and 50 kΩ are 13 and 12 respectively.

The system cost for the case where boards shrink as parts are embedded (the Chapter 4 optimum) is greater than the system cost for the fixed board sizes with the same number of boards produced per panel (70 boards per panel range). This is due to the fact that the embedded passive content for the allow board shrinkage solution has only 6 resistors of resistive value between 5 kΩ and 50 kΩ embedded as oppose to 14 resistors in the fixed board size solution. The assembly, rework, procurement and AOI cost associated with the 8 resistors that are not embedded in the "Allow board shrinkage solution" increases the cost by half a cent ($0.05).

The absolute minimum physical size constraint for the SENDO application with every embeddable part embedded is 2.754 in^2, which is the total assembly spacing and assembly area required to accommodate all the non-embedded embeddable devices on the surface of the SENDO application (assuming they tile together perfectly, i.e., no empty space). The embedded passive content at 2.754 in^2 is 134 bypass capacitors, 38 resistors of resistive value less than 5 kΩ and 14 resistors of resistive value between 5 kΩ and 50 kΩ. This means that the solutions in Figure 6-1 below 2.754 in^2 are never physically possible under any conditions.

We will now analyze in detail the solutions for the fixed board sizes that produce 70 boards per panel and compared to the "Allow board shrinkage solution". The analysis done in this section involves the following steps:

1. Calculating the conventional board ratio (CR), which is the ratio of the conventional board area to the sum of the assembly footprints of <u>all</u> the parts. Where a part's assembly footprint is its physical area plus the space around it required for its assembly (assembly spacing). CR is the inverse of the "packaging density". This ratio was used to determine the minimum board size that is allowable for a given fix board area solution that would preserve the conventional board surface mount passive component placement.
2. Calculating the allow board shrinkage ratio (SR), which is the ratio of the "Allow board shrinkage solution" area to the sum of the footprints of all the parts that are not embedded. SR is the inverse of the "packaging density" for the "Allow board

[12] Note, the embedded content is not the same as the optimum Chapter 4 solution which has only 6 resistors of resistive value between 5 kΩ and 50 kΩ embedded as oppose to 14 resistors in the fixed board size solution.

shrinkage solution" area. This ratio was used to determine the maximum board size that is allowed for a given fix board area solution that would preserve the allow board shrinkage surface mount passive component placement.

3. The embedded content needed to obtain the minimum and maximum board size allowed was determined and the system cost for that particular embedded content was plotted. CR and SR determine the minimum allowable and maximum likely board sizes respectively. Note, not all the fixed board areas in Figure 6-1 will fall within the minimum allowable and maximum likely board size (this will be expanded upon later in this section).

The following are the formulas used to determine the maximum likely and minimum allowable board sizes:

$$CR = \frac{CB_A}{AA_C}, \text{ the conventional board ratio} \quad (25)$$

where CB_A is the conventional board area and AA_C is the sum of the assembly footprints for all parts for the conventional board (nothing embedded);

$$SR = \frac{SB_A}{AA_{SB}}, \text{ allowed board shrinkage ratio} \quad (26)$$

where SB_A is the "Allow board shrinkage solution" board area and AA_{SB} is the sum of the assembly footprints for all non-embedded parts for the "Allow board shrinkage solution".

The minimum allowable board area (MIN_{BA}) and maximum likely board area (MAX_{BA}) are determined from,

$$\mathrm{MIN}_{\mathrm{BA}} = \mathrm{MIN}\left[\mathrm{CR} \times \mathrm{AA}_{\mathrm{SB}}, \mathrm{SR} \times \mathrm{AA}_{\mathrm{SB}}\right]$$
$$\mathrm{MAX}_{\mathrm{BA}} = \mathrm{MAX}\left[\mathrm{CR} \times \mathrm{AA}_{\mathrm{SB}}, \mathrm{SR} \times \mathrm{AA}_{\mathrm{SB}}\right] \quad (27)$$

For the SENDO application, the ratio of conventional board area to total surface assembly area of conventional board (CR) is 1.40 and the ratio of allow board shrinkage solution board area and total surface assembly area of allow board shrinkage solution (SR) is 1.49. If perfect placement of all non-embedded parts was possible than the ratio of the board area and the total assembly area would be 1. The ratio for the embedded case is greater than that of the conventional case due to the absence of small (relative to other non-embedded components, see Table 5-1) embedded passives. This increase in ratio for the embedded case can be better understood using the schematic presented in Figure 6-2. By embedding the smaller embeddable devices the packaging density for the system decreases because the placement can't change very much when just small parts are removed, which results in an increase in the allow board shrinkage ratio (SR). Note it is not the focus of this research to optimize layout placement of surface mount devices as passives are embedded. If it is assumed that the relative placement of the surface mount

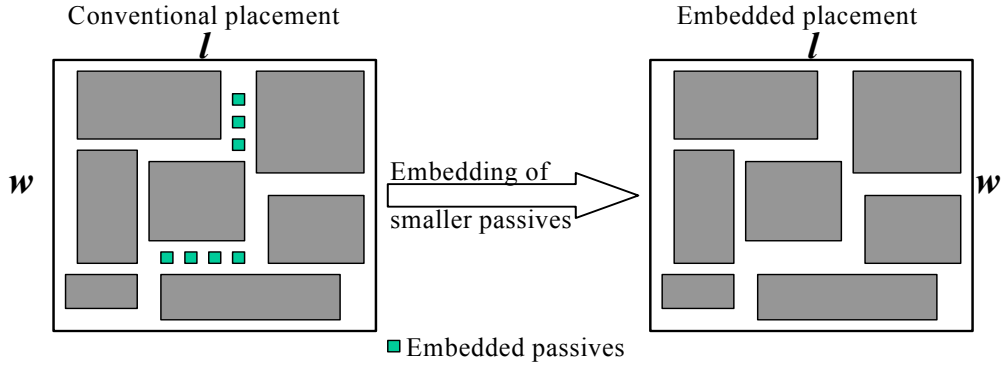


Figure 6-2: Effects of embedding smaller devices on packaging density (embedding the embedded passives on the left may cause no change in the board size because of placement constraints driven by the larger parts).

devices on the conventional board is constrained by a performance specification and should be kept constant, then the ratios, CR and SR, would be kept constant to maintain the same relative placement for the printed circuit board application (i.e., the relative locations of parts may be important to the performance and/or functionality of the system). These ratios were used to determine the minimum allowable and maximum likely allowable board area for a particular fix board size. These maximum and minimum board areas were found by multiplying each ratio, CR and SR, by the total surface assembly area required for the "Allow board shrinkage solution", (27).

The system cost at the minimum and maximum board size was determined by varying the embedded passive content for the system and allowing the fixed board size to vary. Figure 6-3 is the analysis corresponding to one of the points from Figure 6-1. Figure 6-3 shows an analysis of the fixed board size of 4.26 in^2 on the system cost for the SENDO application and the possible ranges of board sizes that are attainable. In Figure 6-3 it is observed that the fixed board area of 4.26 in^2 and the allow board shrinkage solution area of 4.13 in^2 are both greater than the maximum board area of 4.10 in^2. This is due to the fact that the placement of passive devices (utilization of surface area) is not optimized for this particular case. It is also observed that the system cost at both the minimum and maximum board areas are much more than that of the "Allow board shrinkage solution" and the fixed board area solution.

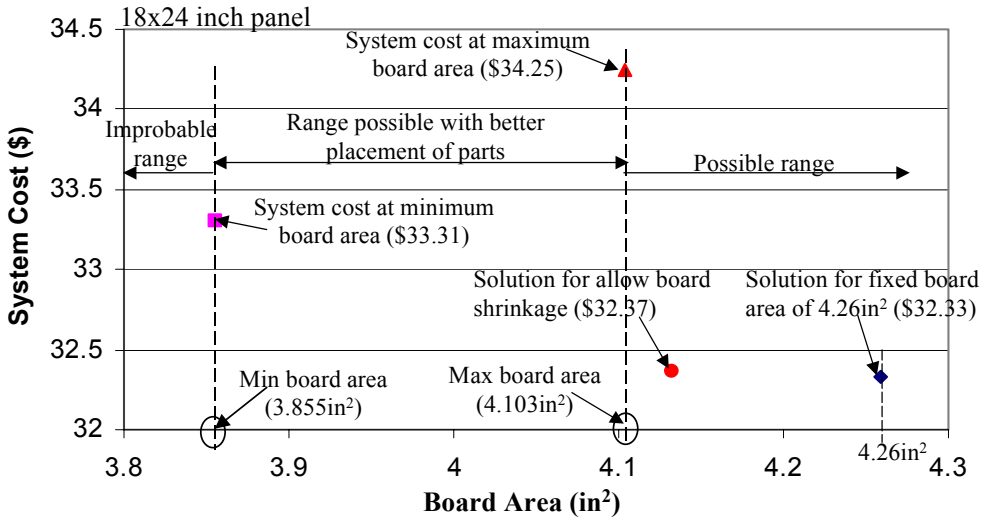


Figure 6-3: Effects of board size 4.26 inch^2 on system cost for SENDO application (70 boards / panel) (AA_{SB} = 2.76 in^2)

This increase in the system cost is a direct result of moving away from the optimal embedded content to obtain these board areas. The range between the minimum and maximum board areas is considered possible with "better" placement (i.e., better placement than the "Allow board shrinkage solution") of all components, and the board areas below the minimum board area are considered improbably since they would require better placement than the conventional system.

Similar to Figure 6-3, Figures 6-4 through 6-6 show the effect that the fixed board areas that produce 70 boards per panel have on the system cost and which of these areas are physically possible. In Figure 6-4 it is observed that the fixed board area of 4.11 in^2 has the same general characteristics as the fix board area of 4.26 in^2 shown in Figure 6-3.

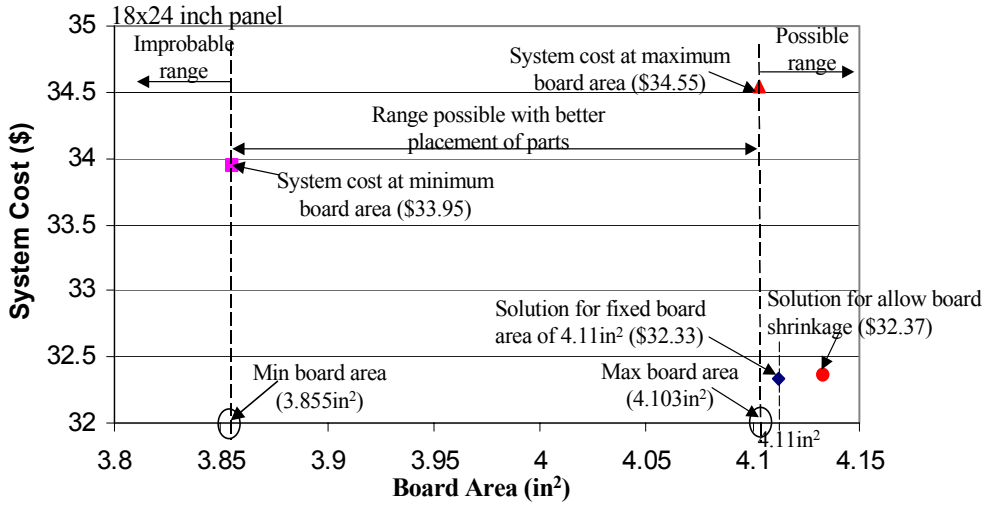


Figure 6-4: Effects of board size 4.11 inch^2 on system cost for SENDO application (70 boards/ panel) (AA_{SB} = 2.76 in^2)

The differences are that the fixed board area of 4.11 in^2 is much closer to the maximum board area and the system cost at the minimum and maximum board area are slightly greater in Figure 6-4. In Figure 6-5 the fixed board area of 3.97 in^2 falls between the minimum and maximum board area. This means that better placement of all parts is required if this board area is going to be valid. It is also not possible to obtain the maximum board area in this case since for the GSM SENDO main board the total surface area required to have all parts surface mounted is 3.20 in^2 which is less than the maximum board area of 4.10 in^2, therefore there is no system cost at the maximum board area.

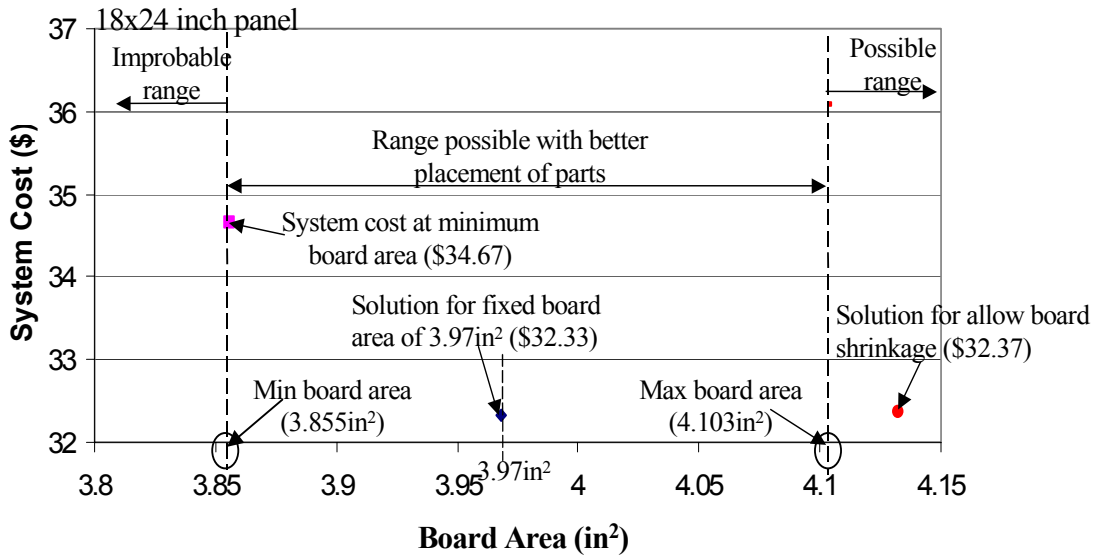


Figure 6-5: Effects of board size 3.97 inch^2 on system cost for SENDO application (70 boards/ panel) (AA_{SB} = 2.76 in^2)

The system cost at the minimum board area is observed to be higher than that found in Figures 6-3 and 6-4. In Figure 6-6 it is shown that the fixed board area of 3.83 in^2 falls into the improbable range of board areas. It also shows that when the board area of 3.83 in^2 was allowed to vary by varying the embedded content the minimum board area was not attainable.

The ratio analysis was conducted for all the SENDO fixed board areas presented in Figure 6-1. This ratio analysis is depicted in Figure 6-7 where the conventional board ratio (CR) and the allow board shrinkage ratio (SR) are shown. This analysis shows that only a few of the board areas from Figure 6-1 actually fall within the possible range of board area that can be manufactured.

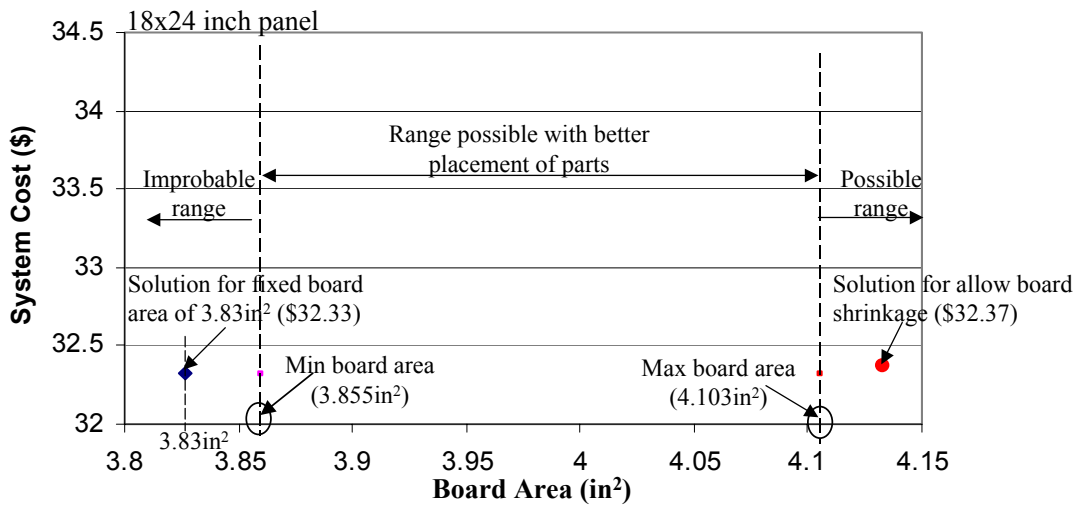


Figure 6-6: Effects of board size 3.83 inch^2 on system cost for SENDO application (70 boards/ panel) (AA_{SB} = 2.76 in^2)

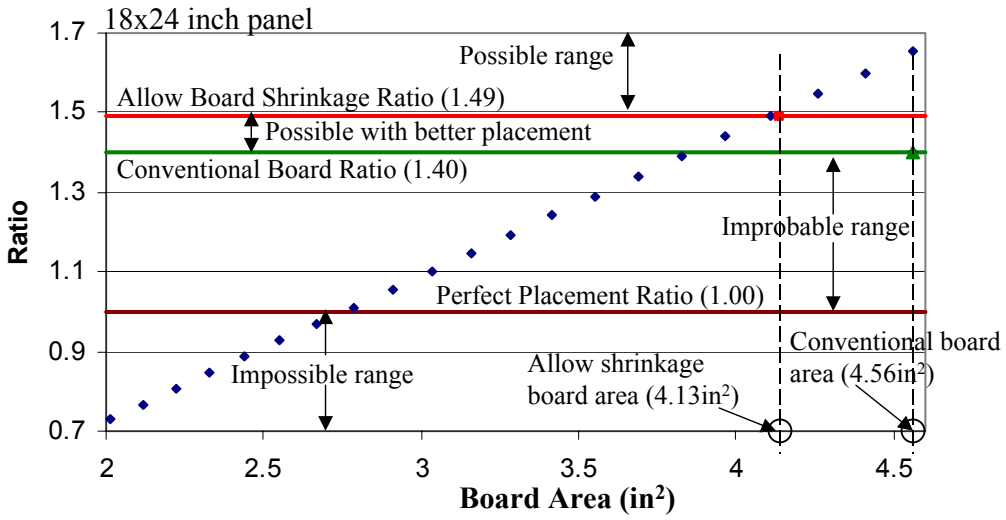
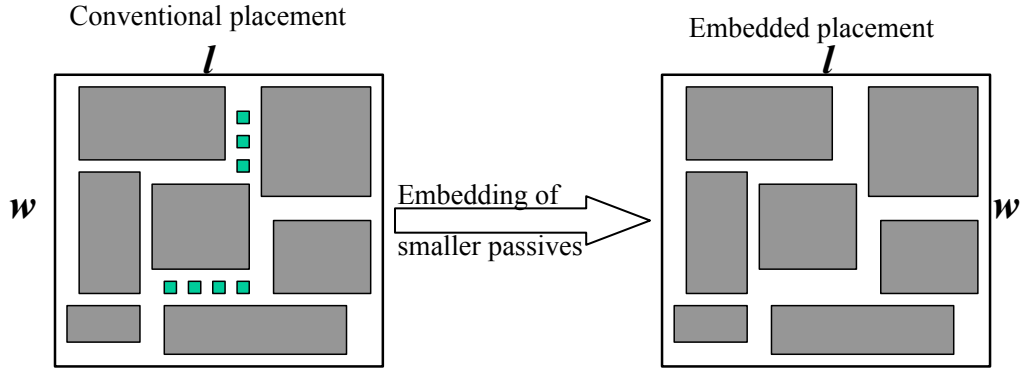


Figure 6-7: Ratio analysis for fix board areas for the SENDO GSM cell phone application

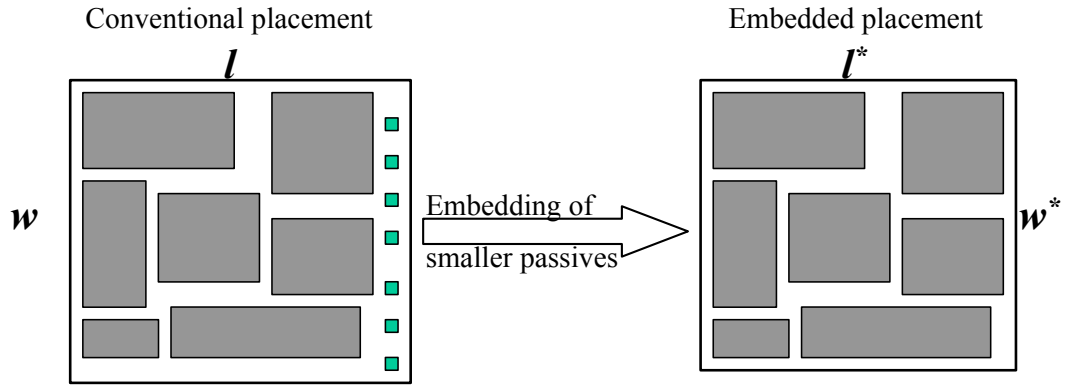
Figure 6-8 provides an example of how a placement ratio that is less than that of the conventional system can be obtained. For the most part, the embeddable passive devices are much smaller than the non-embeddable devices and the possibility of getting a smaller placement ratio is dependent on the placement of embeddable passive devices

on the surface of the original board. Figure 6-8b demonstrates one of the cases in which it may be possible to obtain a smaller ratio than that of the conventional system.



In this case the ratio for the conventional placement is smaller than that of the embedded placement since more of the assembly area is utilized in the conventional case and the board area remains the same.

Figure 6-8a: Possibility of getting a ratio that is greater than the conventional ratio



$l^*=l$ – *(length of embedded passive + assembly spacing)*
$w^*=w$-*(width of embedded passive + assembly spacing)*

In this case it is possible that the ratio for embedded placement is smaller than that of the conventional placement since the board area in the embedded case is reduced by embedding the smaller passives devices.

Figure 6-8b: Possibility of getting a ratio that is less than that of the convention ratio

Figure 6-9 is a duplicate of Figure 6-1 illustrating the board areas that are impossible based on the ratio analysis described above. The improbable solutions, possible with better placement solutions, and the possible solutions are also highlighted.

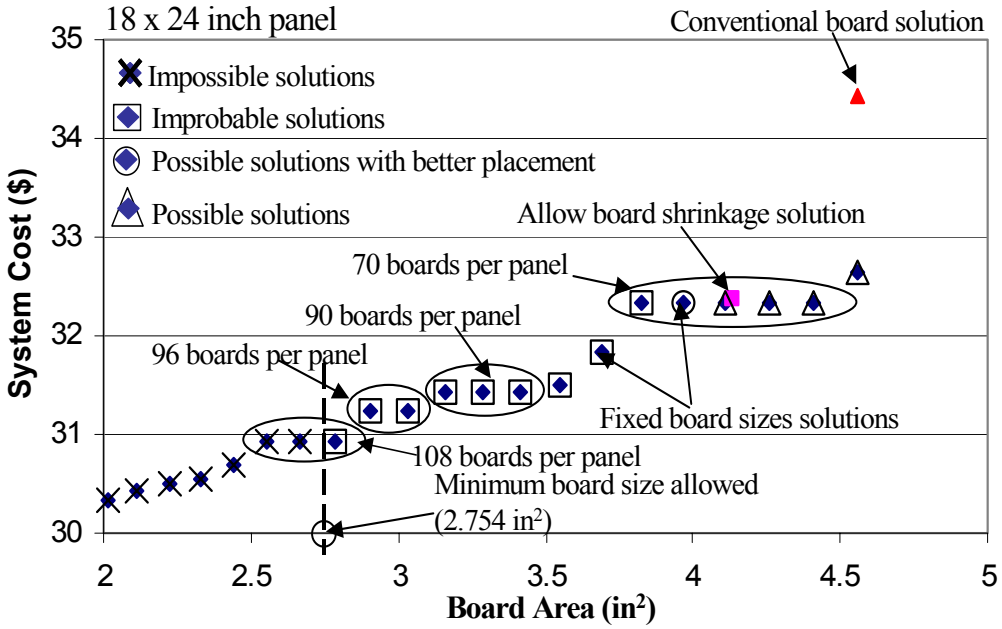


Figure 6-9: Possible and impossible board areas for the SENDO GSM application main board

The NEMI Hand-Held product sector emulator was analyzed using the same method as the SENDO GSM cell phone main board. Figure 6-10 shows the effects of board size on system cost for the NEMI Hand-Held product sector. In Figure 6-10 it is shown that the number of layers varies making the board area versus cost relationship for the NEMI Hand-Held board much more dynamic than the SENDO board (the number of layers never varied for the SENDO board). All the points that are not labeled as 8 layers in Figure 6-10 are 6 layers[13]. Figure 6-10 shows that as the layer count increases, the system cost increases; and as the number of boards produced per panel increases the system cost decreases. This variation in layer count is primarily due to the large number of embeddable resistors that are present in this system. It was observed that when the number of layers increased the embedded content also varied. With the increase in

[13] The layer count changes based on the amount of wiring needed to interconnect the parts. The amount of wiring available is a function of the area of board, the layer count, and the board area blocked by embedded passives. See Section 2.1.2 for an explanation of the model used to determine the layer count.

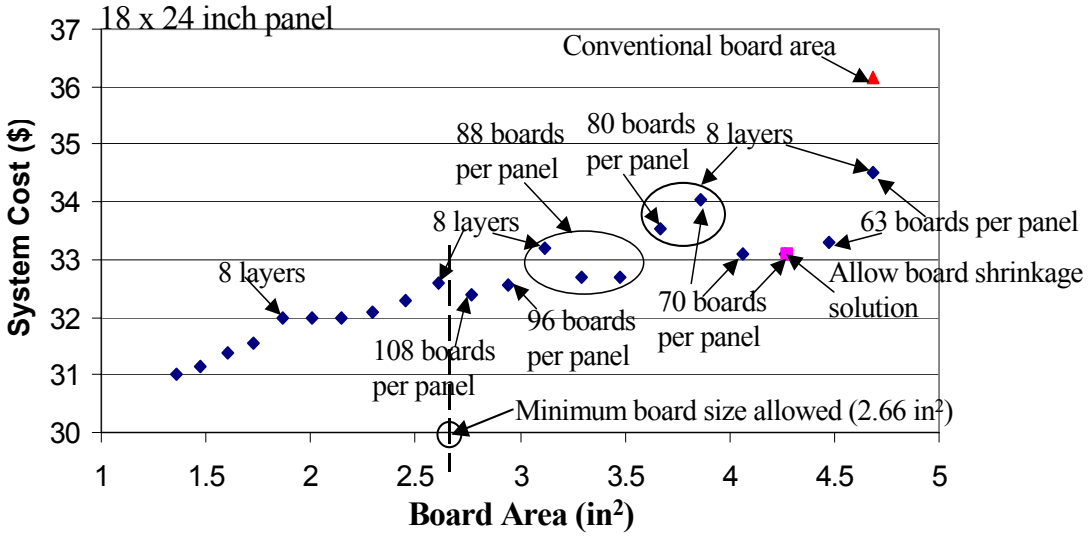


Figure 6-10: Effects of board size on system cost for the NEMI Hand-Held product sector optimized embedded content determined for each fixed board size.

number of layers available there is an increase in the space available for routing embedded resistors and non-bypass capacitors. This variation in embedded content did not occur in the SENDO GSM application, which only showed a variation in the embedded content for the "Allow board shrinkage solution" area and the board areas of 2.01 in^2 and 2.12 in^2.

Figures 6-11 through 6-14 show the effect of various fixed board sizes on system cost for the NEMI Hand-Held product sector emulator. Similar to the analysis done in the SENDO application, this analysis examines the feasibility of the board sizes that are shown in Figure 6-10. Figure 6-11 shows the effect of the board area 4.47 in^2 on the system cost for the NEMI Hand-Held application. In Figure 6-11 it is shown that the fix board area of 4.47 in^2 falls within the possible range of board sizes for this system and it is slightly higher in cost than the "Allow board shrinkage solution". It is also shown that the "Allow board shrinkage solution" board area is the same as the maximum board area.

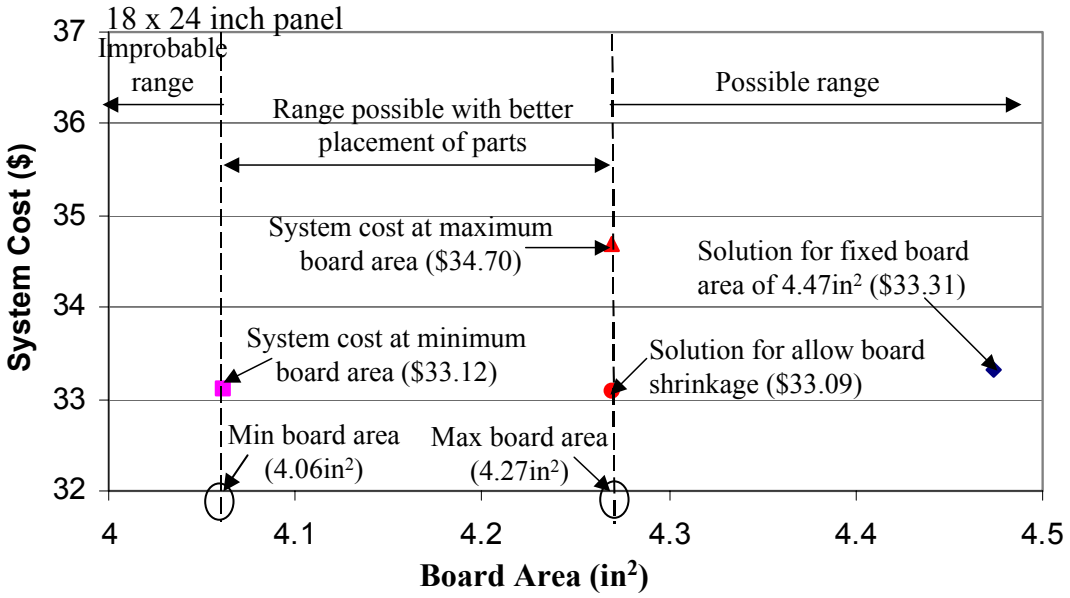


Figure 6-11: Effects of board size 4.47 in^2 on system cost for NEMI Hand-Held application (63 boards /panel) (AA_{SB} = 2.79 in^2)

Figure 6-12 shows the effect of the fixed board size 4.26 in^2 on the system cost for the NEMI application. In Figure 6-12 it is shown that the fixed board area of 4.26 in^2 solution falls between the minimum and maximum board area, which is the region that is possible with better placement of surface mount devices. It is also shows that the system cost for allow board shrinkage solution and the fix board area solution cost is the same ($33.09). This is due to the fact that both areas have the same embedded. For this fixed board size and embedded content solution it is not possible to attain the maximum board area therefore there is no system cost at maximum board area.

Figure 6-13 shows the effect of board size 4.06 in^2 on system cost for the NEMI Hand-Held Emulator application. In Figure 6-13 the fixed board area is the same as the minimum board area, which means that with better placement it is possible to find a solution that will maintain the placement layout of the conventional system. Similarly to the fixed board area of 4.26 in^2 it is not possible to attain the maximum board area for the

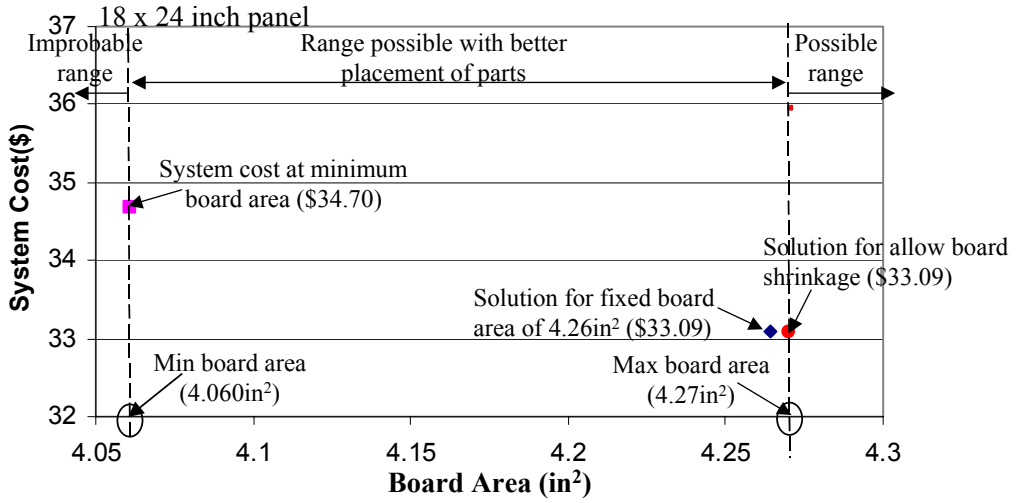


Figure 6-12: Effects of board size 4.26 in^2 on system cost for NEMI Hand-Held application (70 boards/ panel) (AA_{SB} = 3.04 in^2)

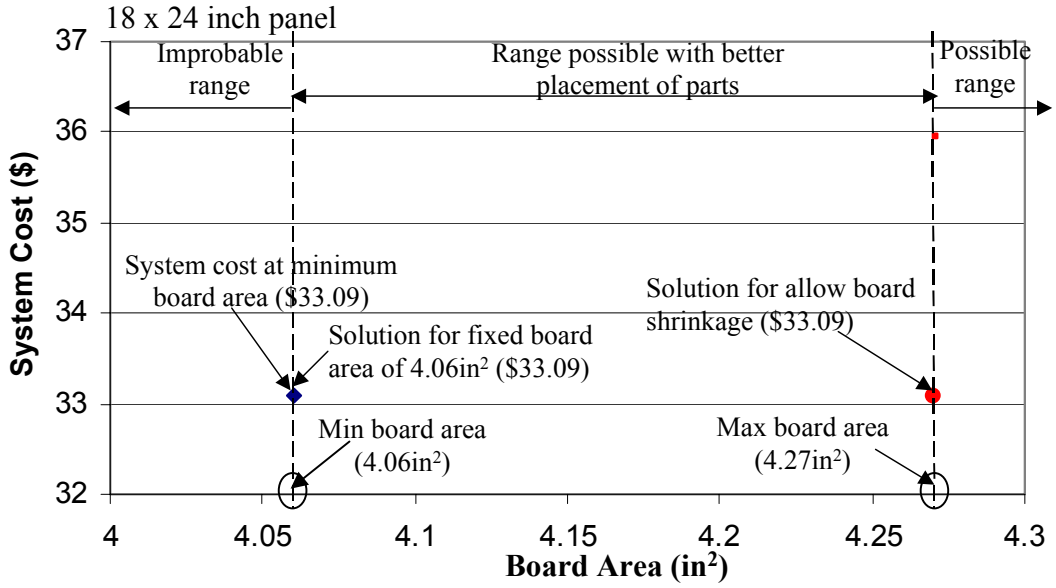


Figure 6-13: Effects of board size 4.06 in^2 on system cost for NEMI Hand-Held application (70 boards/ panel) (AA_{SB} = 3.04 in^2)

fixed board size of 4.06 in^2.

A ratio analysis was done for the NEMI Hand-Held product sector application using the fixed board areas that where analyzed in Figure 6-10. The results of this analysis can be seen in Figure 6-14. In Figure 6-14 it is shown that only a few board areas smaller than the "Allow board shrinkage solution" area are within the possible range with

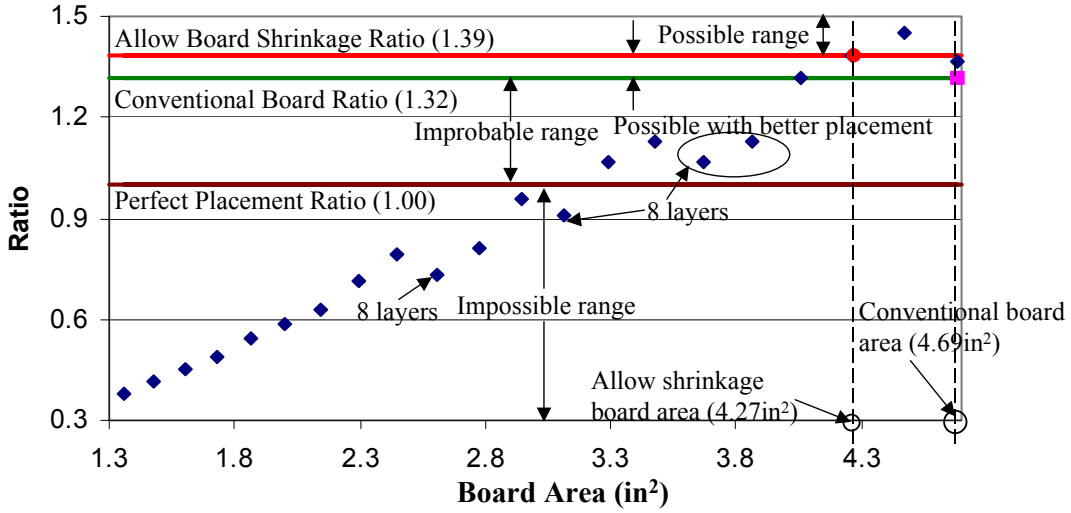


Figure 6-14: Ratio analysis for fix board areas for the NEMI Hand-Held product sector emulator

better placement (4.06 in^2 to 4.27 in^2). In this Figure all the board areas that are not labeled as having 8 layers have 6 layers. It also shows that the ratios are sensitive to the number of layers in the system. When the number of layers required to route the system increases the ratio decreases. Figure 6-15 shows the possible and impossible board areas for the NEMI Hand-Held application. The ratios that fall within the impossible range from Figure 6-14 are used to determine the areas highlighted as impossible in Figure 6-15. In Figure 6-15 it is observed that the impossible areas begin above the minimum board size allowed. This Figure also highlights the improbable solutions, the solution with better placement and the possible solutions for this analysis. It is shown that the possible solution begins on the "Allow board shrinkage solution".

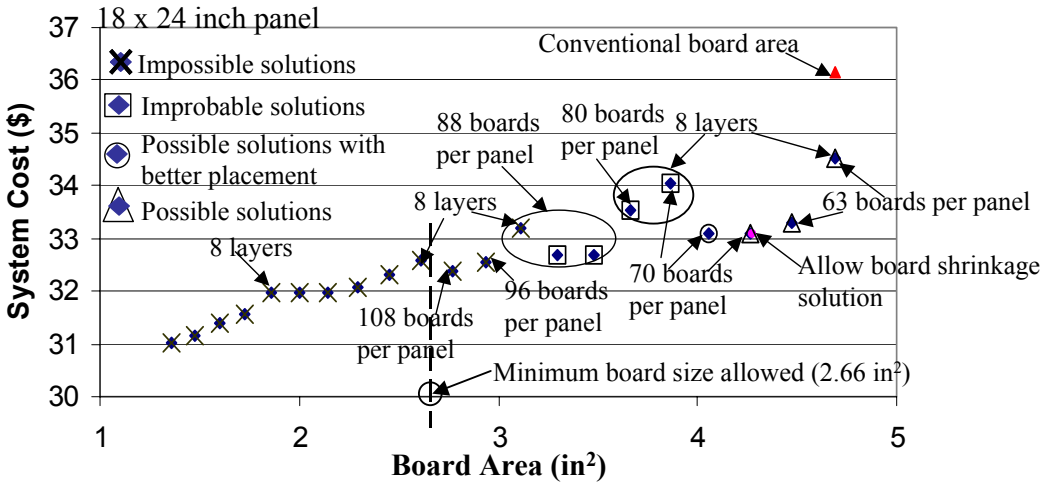


Figure 6-15: Possible and impossible areas for the NEMI Hand-Held product emulator

6.2 General Insights Gained

The analysis performed in this chapter has provided significant insight into the size limitations of applications using embedded passive technology. Relevant measures that can be used to describe the regions of applicability of the design optimization are the ratios illustrated in Figure 6-7 and Figure 6-14 and represented by (25) and (26). Four ratio regions were identified: the impossible region, the improbable region, the region possible with better placement, and the possible region.

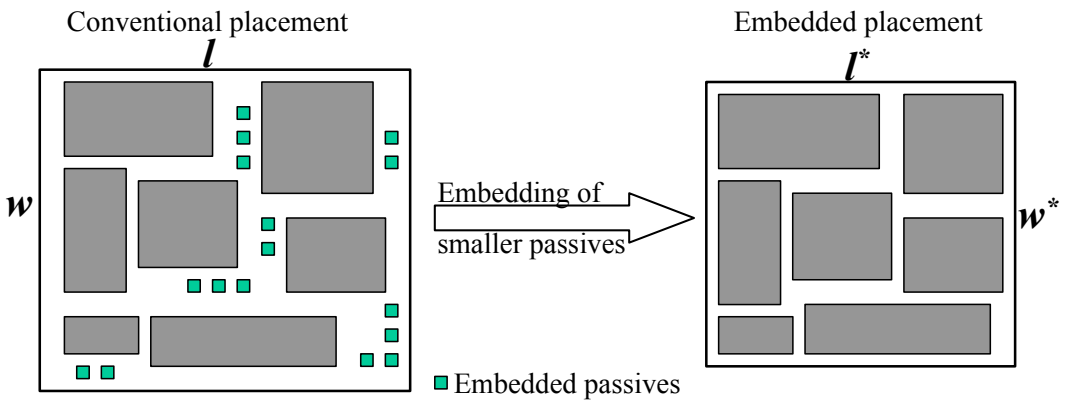
In this analysis it has been shown that the "Allow board shrinkage solution" (the "optimum" solution methodology developed in Chapter 4) represents the minimum system cost within the region possible with better placement and the possible region. If systems have placement ratios that fall within the improbable region then, it is possible to obtain system costs that are less than that of the "Allow board shrinkage solution", however given that the passives that are embedded are much smaller than the non-embeddable parts, better placement solutions (smaller placement ratio) is considered

improbable. Smaller placement ratios (ratios within the improbable region) can only be attained if the layout specification for the conventional system is ignored and the placement of non-embeddable parts are optimized to render a greater packaging density than that of the conventional system – performance and functionality constraints may not allow this.

The analysis has also shown that the system size limitation when embedded passives are used is not only dependent on the quantity, type, and electrical properties (capacitance and resistance) of the embeddable components but is, in fact, more dependent on layout specifications and the placement of the non-embeddable parts. From the analysis performed in this chapter it is evident that the optimum system cost solution presented in Chapters 4 and 5 does not generally result in the minimum possible size for the system. This analysis shows that it is possible to attain smaller board areas for a printed circuit board application if the possibility of better placement of surface mount devices is considered. It also shows that when the layer count increases, the packaging density increases thus providing a better (smaller) placement ratio for the system since more passives can be embedded on a smaller board area, however this better placement ratio comes at a higher system cost due to the layer addition. This analysis shows that even though the optimum solution from Chapter 4 does in fact provide the minimum system cost (under the placement constraints summarized in the preceding paragraph) it does not provide the minimum size. This is due to the fact that the optimization of the layout of parts on the surface of the system is not considered within the methodology described in this dissertation.

6.3 Application-specific insights gained

It was also observed in this analysis that the ratio of the fix board area for the NEMI Hand-Held (Figure 6-14) is not linear with respect to the board area as was observed in Figure 6-7 for the SENDO application. This is due to the fact that the SENDO system does not have enough embeddable resistors (even if they are all embedded) to ever demand an additional layer pair for routing. The Chapter 4 optimization work produces a better solution in the case of the NEMI Hand-Held product sector emulator than in the case of the SENDO GSM cell phone application. This is evident when comparing the "Allow board shrinkage solution" for both cases. In the SENDO case the "Allow board shrinkage solution" area is greater than the maximum board area (27), whereas in the case of the NEMI Hand-Held application the "Allow board shrinkage solution" area is the same as that of the maximum board area. The reason for this is that the NEMI Hand-Held application has more embeddable passive components than the SENDO application (more generally, the NEMI Hand-Held application has a higher embeddable resistor density). Because there are more embeddable parts to embed (per unit area), it is possible to clear out a bigger fraction of the surface area of the board size. This, in effect, results in better placement of parts for the "Allow board shrinkage solution" in the NEMI case. Figure 6-16 demonstrates the effective better placement that is attainable by embedding passives. In the conventional placement it is observed that the non-embeddable parts are spaced out much further from each other due to the placement of the embeddable passives on the surface. In the embedded placement case, all the embeddable passives are embedded and the non-embeddable components are placed much closer to each other allowing the board size to



l^*=l – (length of embedded passive + assembly spacing)
w^*=w-(width of embedded passive + assembly spacing)

Figure 6-16: Effective better placement by embedding passives

shrink making better use of the available space, which results in a higher packaging density than that observed in the conventional placement. This results in smaller placement ratio for the embedded case. Stated more generally, the higher the embeddable passive density (embeddable passives per unit area), the greater the probability that embedding those passives will improve the placement, i.e., maintain a ratio within the region possible with better placement or decrease the ratio to the improbable region.

CHAPTER 7 SUMMARY AND CONCLUSIONS

This chapter summarizes the work that has been conducted in this research effort. It then lists the significant research contributions of this work and presents the direction and opportunities for future work to improve on the modeling of embedded passive technology. The chapter ends with some concluding remarks on the new model developed in this research and its applicability within the embedded passive printed circuit board industry.

7.1 Summary

This research developed a new and more comprehensive approach to modeling the economic impact of embedding resistors and capacitors in printed circuit boards than the existing models that are presently utilized by industry. To this end a model has been developed that captures the size and cost effects of embedding passives in printed circuit boards (Chapter 2). The results of applying this model to several example boards have been discussed in Chapter 3, which demonstrates key tradeoffs and competing effects that are inherent in the embedded passive process. These results also show that the economics of the embedded passive technology is application specific. The Chapter 2 model has also been implemented as a Java Applet, which is available on the web and has been used by the members of the Advanced Embedded Passives Technology Consortium to perform size/cost analysis on various system applications and by the NEMI Passive Components committee in preparation of the NEMI technology roadmaps, [35]. Chapter 4 demonstrates the use of the model for finding the optimal (lowest cost) solution for embedding resistors and capacitors in a system. The optimization analysis has been demonstrated on a simple case that involves embedding 2 distinct types of embeddable

resistors. Chapter 5 demonstrates the use of the new model developed in this research on a SENDO M550 GSM mobile phone main board and compares the results with that of the existing simple models, thus illustrating the areas and conditions in which the two modeling approaches diverge. Chapter 6 studies the effects of board size on system cost.

7.2 Contributions of this Work

This work has performed a detail assessment of embedded passives in printed circuit boards by developing a robust size/cost model and using it to perform size/cost tradeoff analyses that are inherent within the embedded passive technology. This research has developed the most complete embedded passive size/cost model in the world to date accommodating the analysis of mixed real systems, manufacturing yields and data uncertainties. This work has introduced a new method for relative routing analysis/layer pair calculation and performs profit margin calculations via throughput analysis. It has demonstrated that it is possible to optimize embedded passive content for application-specific printed circuit board applications. The analysis performed in this research provides the limits of miniaturization that is attainable during the embedded passive process for printed circuit boards by identifying the role that layout constraints play in obtaining minimum cost solutions.

7.3 Discussion of Modeling Work and Modeling Contributions

The embedded passive system size/cost model developed in this research utilizes a top-down parametric cost estimating approach. The model developed involves the following steps:

1. Break the system into its elements, including component sizing, board sizing, wiring specification and layer calculation.

2. Estimate the labor, capital, and resource requirements imposed for each element in the system.
3. Construction of the subsystem costs from the requirements imposed on each subsystem. The system models are used to assist in cost estimating, and they include models of the manufacturing process: assembly, test, rework, throughput, and board sizing.
4. The system costs are determined by aggregating the subsystem costs.

This is a predictive modeling process, using physical models to predict the characteristics of the cost incurring activities in the system (sometimes this type of model is referred to as a "technical cost model" [37]).

The global contributions enabled by the new model are discussed in Section 7.3. This section summarizes the specific modeling contributions. The embedded passive cost model developed takes into consideration a number of critical modeling effects that previous models have not accounted for. These modeling effects include:

- The new model accounts for the yield of both discrete passive components and the variation in board yield due to embedding passives. These yields significantly affect the cost of the system by directly impacting the embedded passive layer pair cost and the assembly and rework cost associated with the conventional passive technology.
- The new model accounts for the effects of routing (wiring) on the number of layer pairs required when embedding resistors and capacitors. An increase or decrease in the number of layer pairs directly increases or decreases the embedded passive system cost.

- The new model accounts for the potential decreases in throughput for embedded passive board fabrication. A decreased throughput (when fabricating boards with embedded passives) will require the embedded passive board manufacturer to increase the embedded passive board profit margin in order to obtain the same profit (per unit time) experienced when manufacturing conventional boards. This increase in profit margin directly increases the price of the embedded passive system.
- The new model accommodates real mixed systems (multiple embedding technologies used in the same board, and resistors and capacitors embedded at the same time).
- The new model accounts for the potentially significant uncertainties present in some of the input data. It is impossible to obtain a complete dataset where every property is known exactly. Therefore, both inputs and solutions must take the form of probability distributions.

This new model has been used within an optimization environment that enables the optimum mix of resistors and capacitor values to be determined for specific electronic system applications. The model has been exercised and validated using a series of example systems provided by members of the NIST Advanced Embedded Passives Consortium (specifically Nortel), Boeing, and StorageTek. The basic operation of the optimization process has also been validated via comparison with searches of the entire design space for various printed circuit board applications.

The additional effects included within the new model have been analyzed to determine when and how they impact the cost/size tradeoff by comparing the existing

simple model and the new model. This was done by implementing both embedded passives modeling approaches and testing them on a SENDO M550 GSM mobile phone main board. This model comparison included the detail optimization analysis of a real system with multiple distinct types of embeddable devices.

7.3 Discussion of Global Contributions

This section summarizes the conclusions and contributions associated with using the new model. Today, designers who are considering including embedded passives in their boards use the simplified modeling approach discussed in Section 2.1.1 that consists of the following three steps: 1) reduce the system cost by the purchase price and conversion costs associated with the replaced discrete passives, 2) reduce the board size by the sum of the layout areas associated with the replaced discrete passives and determine the new number of boards on the panel, and 3) determine the new board cost based on a higher per unit area cost for the embedded passive panel fabrication and the new number-up computed in step 2. This simplified modeling approach is being used in decision making today and potentially impacts millions of dollars worth of product containing embedded passives. Figure 7-1 illustrates that by 2010 embedded passives will account for approximately 10 percent of the market share of passive components (or $2.6 billion). Therefore it is becoming critical that accurate and well understood decision support models be used in determining the embedded passive content in systems and in analyzing the system size and cost impacts for embedded passive technology. The existing approaches for embedded passives assessment omit many potentially significant effects that have been included within the new model developed herein. To enable more effective embedded passive decision making, three primary contributions from this work

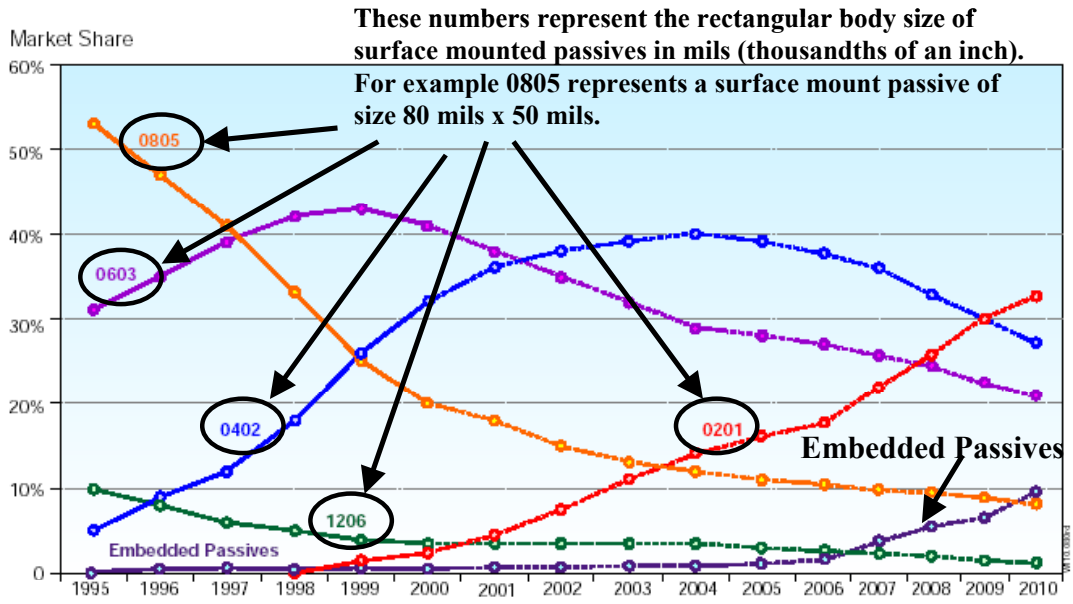


Figure 7-1: Estimated growth rate of embedded passives compared with other packaging technologies [10]

have been identified – they are discussed below.

7.3.1 Contribution #1: General Result for the Economics of Embedding Bypass Capacitors

The new model has been used to generalized bypass capacitor results by modeling the effects of bypass capacitor material properties (cost and capacitance) on bypass capacitor breakeven density to determine the density of capacitors at which it becomes cost effective to use embedded capacitors for a specific application. Section 3.1.4 and Figure 3-9 provides an analysis of generalized bypass capacitor results for specific board applications. The results (for a range of different applications) indicate that for dielectric systems with ~10 nF/in^2 the application must have 7-10 embeddable bypass capacitors per square inch or more for it to be cost effective to replace discrete bypass capacitors with embedded bypass capacitors. Within the range of required capacitor densities, as the panelization efficiency (panel area occupied by boards divided by the overall panel

area) decreases, a higher embeddable bypass capacitor density is needed to breakeven. This is primarily due to the reduction in dielectric wastage, higher panelization efficiency, less wasted expensive dielectric material.

7.3.2 Contribution #2: Determining and Demonstrating the Advantages of Optimizing Embedded Passive Content

The current approach to determining embedding passive content (i.e., simple rules of thumb) do not always result in optimal decisions, i.e., minimization of system cost. For example, one of these simple rules is to embed every discrete resistor that is embeddable from the conventional printed circuit board. The SENDO M550 GSM cell phone case study presented in Chapter 5 Table 5-2 shows that by embedding all embeddable passive devices within the simple model the board manufacture cost is not optimal. In the new model it is observed that both embedding all embeddable passives and not embedding any embeddable passive does not provide the optimal manufacture cost for the system. The optimal manufacture cost for the SENDO GSM application demonstrates a saving of $2.06 for each board manufactured ($34.43 - $32.37). Saving $2 in the manufacture cost for a cell phone main board would result in a very significant increased profit and/or increased market share.

It is also important to note that if the simple existing modeling approach (without inclusion of the additional effects considered in this dissertation) was used to consider the optimal embedding passives in the example above, a different conclusion would be reached. Using the existing model, the optimal solution occurs when all the resistors $\leq$50 k$\Omega$are embedded (14 resistors as opposed to only 6 resistors in the new model). When the new model is used to analyze the optimal embedded content realized by the existing

model we see an increase of $0.70 above the optimal solution realized in the simple model - a much different answer that would lead to a different embedding decision.

Detailed size/cost tradeoff analyses show that the system size limitation when embedded passives are used is not only dependent on the quantity, type, and electrical properties (capacitance and resistance) of the embeddable components, but is, in fact, more dependent on layout specifications and the placement of the non-embeddable parts.

7.3.3 Contribution #3: Determining the Applicability and Limitations of the Existing Modeling Approaches

The new model develop in this research increases the accuracy and robustness of analyzing the cost of embedding resistors and capacitors into a printed circuit board thus saving the printed circuit board industry and the system integrators considerable money when applying embedded passive technology. The new model also demonstrates the relationship between the throughput and profit margin, which is critical information for the board manufacturer when considering the embedded passive technology. This throughput and profit margin relationship is discussed in detail in Section 2.1.3. In Section 5.2 the economic analysis from the new model and the existing model for the SENDO M550 GSM phone main board are compared and discussed. This example application clear demonstrated that critical information was missing in the existing model, e.g., the surface plot from Figure 5-4 shows the effects of layer pair decrease/increase and at what combination and quantity of embeddable resistors embedded the layer pair decreases/increases, this information is not present in Figure 5-5 due to the absence of routing analysis in the existing model. This case demonstrates that the existing model produces an erroneous answer since it identifies that the optimal

solution lies in an area where the new model has detected an increase in the number of layer pairs required. In this case, this increase in layer pair count results in an increase of system cost at the optimal solution in the existing model by $0.70. The SENDO board analysis demonstrates that the optimal solution obtained using the existing model can be misleading and therefore lead to poor design decisions.

7.4 Future Work

Embedding passives in printed circuit boards is a growing market opportunity that is expected to keep evolving over the next few years. Therefore more analysis is needed in order to fully understand the market potential of the technology. In this regard performance and size optimization of printed circuit boards with embedded passive should be considered in future studies.

7.4.1 Switching noise analysis

The primary function of bypass capacitors is to manage switching noise that is inherent in printed circuit boards. However, the connection inductance of surface mounted bypass capacitors limits their effectiveness in managing switching noise. This results in a need for more bypass capacitors to realize a certain level of switching noise control. In the case of embedded bypass capacitors the connection inductance is minimized through the elimination of individual bypass capacitor terminals, therefore less bypass capacitance is required to obtain the same level of switching noise management in the printed circuit board. This would result in waste reduction of expensive bypass capacitor material which transmits to cost savings in the embedded passive board manufacture. As of this time, no analysis has been done to determine when the acceptable switching noise level is achieved when embedding bypass capacitors.

7.4.2 Optimization of resistive material selection

The analysis done so far has utilized a fixed material resistivity for embedding resistors. In reality there are various resistive materials available each having an associated cost, resistivity and performance characteristics. Based on the application of the printed circuit board it would be possible to optimize the selection of resistive material.

7.4.3 Trim/no trim decisions and reworks consideration

In the research conducted all the embedded resistors are trimmed. This analysis does not take into consideration the high cost of the laser trimming equipment. It is also did not take into consideration the possibility of reworking defective embedded resistors prior to the board fabrication process. An assessment of the resistor trim and rework processes and its economic consideration along with a trim and rework model can be found in [25]. The model discussed in [25] could be merged with the model developed in this research to provide a much clearer picture of the economics of an embedded passive application to the decision makers.

7.4.4 Conversion of double-sided printed circuit board to single-sided printed circuit board

The analysis performed in this research has not accounted for the embedding of passives in double-sided printed circuit board (parts mounted on both sides) that may lead to the ability to convert these boards to single-sided printed circuit boards (parts only mounted on one side). The embedding of passive devices frees up valuable real estate on the surface of printed circuit board. By embedding passives devices it is possible to free up enough space on a double-sided printed circuit board to accommodate all the

remaining non-embeddable devices on a single-sided printed circuit board, thus eliminating the manufacturing cost associated with double-sided printed circuit board assembly. This analysis would enhance the capabilities of performing embedded passive economic analysis.

7.4.5 Determining the best optimization method

The optimizing of embedded content was accomplished via the use of a genetic algorithm optimization method. It was not within the scope of the dissertation to determine the "best" optimization method to use. Different optimization methods should be explored in the future to determine whether there is a better suited optimization method for the optimizing of embedded content for an electronic system.

Appendix A – Publications Associated with this Dissertation

B. Etienne and P. A. Sandborn, “Application-Specific Economic Analysis of Integral Passives,” in *Proceedings of the IMAPS Advanced Packaging Materials Processes, Properties and Interfaces Symposium*, Braselton GA, March 2001, pp. 399-404.

P. A. Sandborn, B. Etienne, and G. Subramanian, “Application-Specific Economic Analysis of Integral Passives,” *IEEE Trans. on Electronics Packaging Manufacturing,* Vol. 24, No. 3, pp. 203-213, July 2001.

P. Sandborn, B. Etienne and D. Becker, "Analysis of the Cost of Embedded Passives in Printed Circuit Boards," in *Proceedings of the IPC Annual Meeting*, Orlando, FL, October 2001.

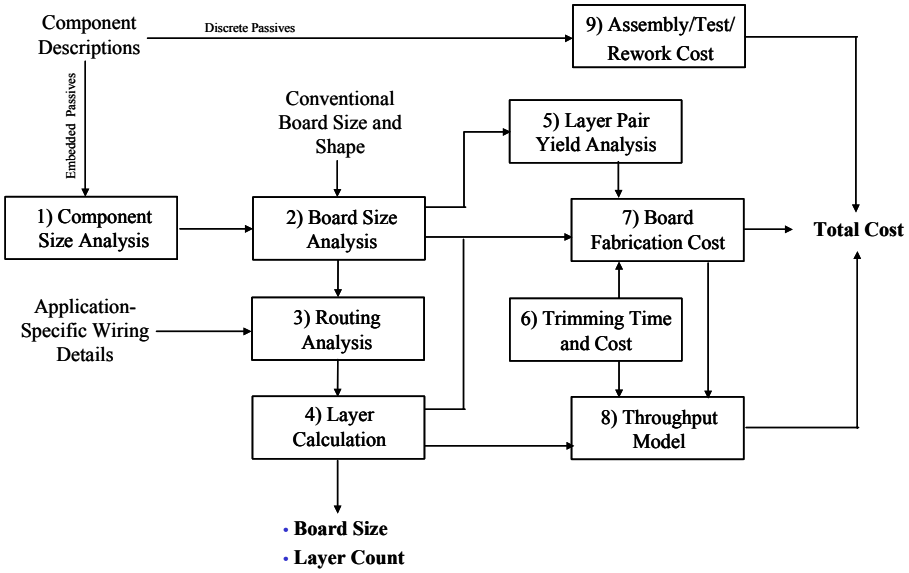
P. Sandborn, B. Etienne, J. W. Herrmann, and M. M. Chincholkar, "Cost and Production Analysis for Substrates with Embedded Passives," *Circuit World*, Vol. 30, No. 1, pp. 2530, 2003.

Appendix B – Embedded/Integrated Passives Cost Analysis Software

This software was developed jointly by the NIST Advanced Embedded Passives Consortium and the CALCE Electronic Products and Systems Consortium at the University of Maryland and is supported by the Electronic Systems Cost Modeling Laboratory (ESCML).

This model delivers an application-specific economic analysis of the conversion of discrete passive components (resistors and capacitors) to integral passives that are embedded within a printed circuit board and to integrated passives (IPDs). The model performs three basic analyses:

1) Board size analysis is used to determine board sizes, layer counts, and the number of boards that can be fabricated on a panel;
2) Panel fabrication cost modeling including a cost of ownership model is used to determine the impact of throughput changes associated with fabricating integral passive panels; and
3) Assembly modeling is used to determine the cost of assembling all discrete



components, and their associated inspection and rework.

Details of the model formulations and examples produced using the model can be found in [5], [36].

The following are the model features:

- Supports resistor, capacitor, and mixed resistor and capacitor embedding
- Board fabrication throughput treated via profit margins
- Bypass and non-bypass capacitors supported
- Board re-sizing (option to fix or float)
- Routing estimation (board layer requirements)
- Board panelization (homogeneous layout only)
- Discrete passive yields
- Discrete passive assembly costs and yields
- Discrete passive assembly rework
- Supports full Monte Carlo uncertainty analysis
- Supports local file system Save and Load
- Includes plotting and printing
- Includes help page defining all input fields

The following figures illustrate the software model interface and a few of its capabilities.

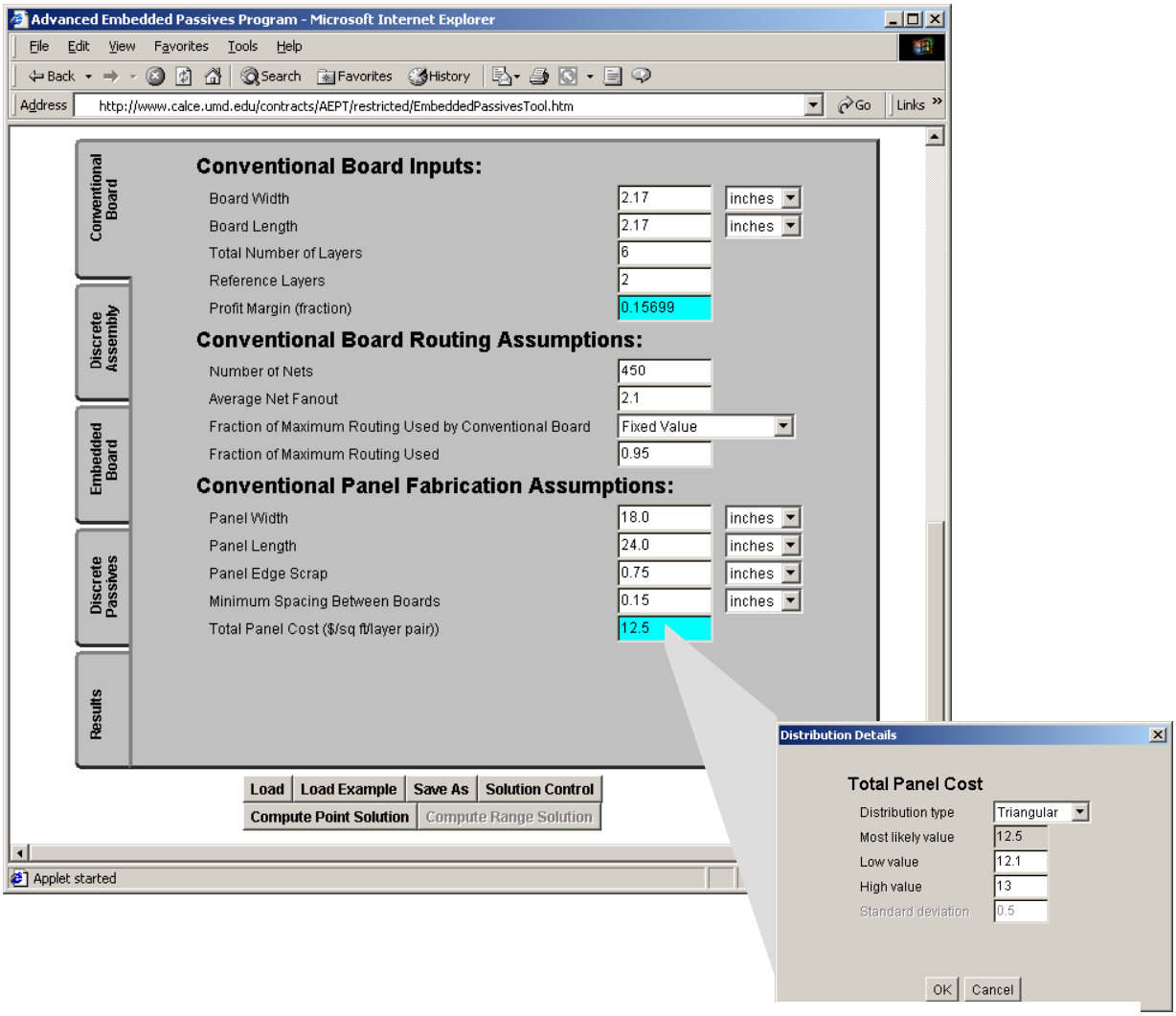


Figure B-1: Software conventional board input interface showing the capabilities of assigning probability distributions to input values.

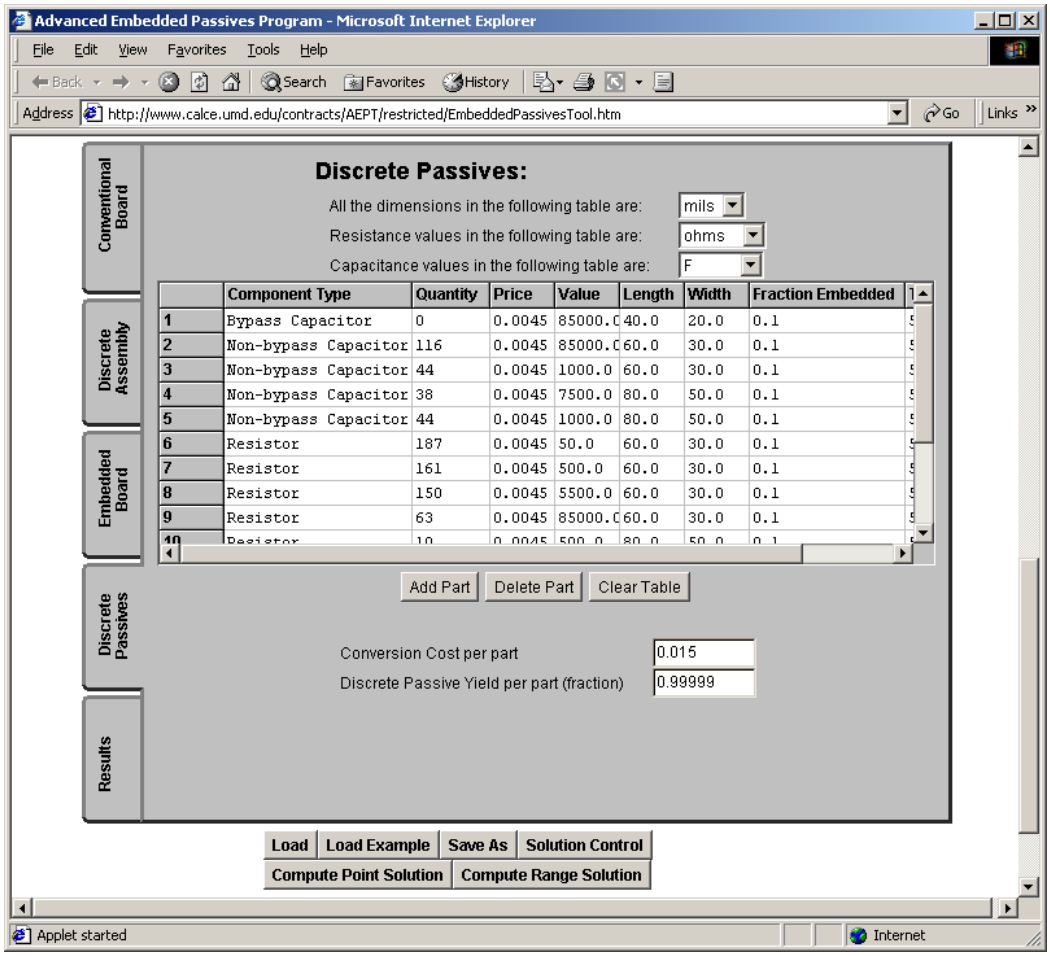


Figure B-2: Software Discrete Passives interface. The assignment of the characteristics for each distinct passive type is inserted for analysis.

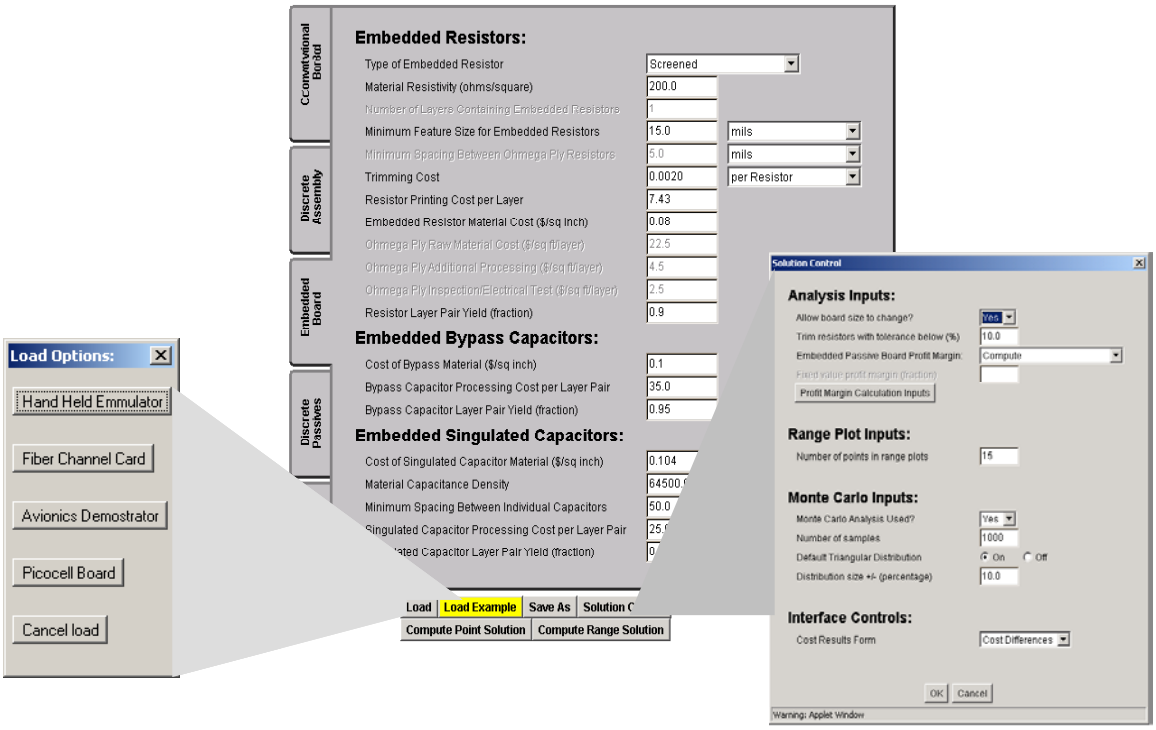


Figure B-3: Embedded passive board input interface illustrating the capabilities of loading examples and controlling the solution.

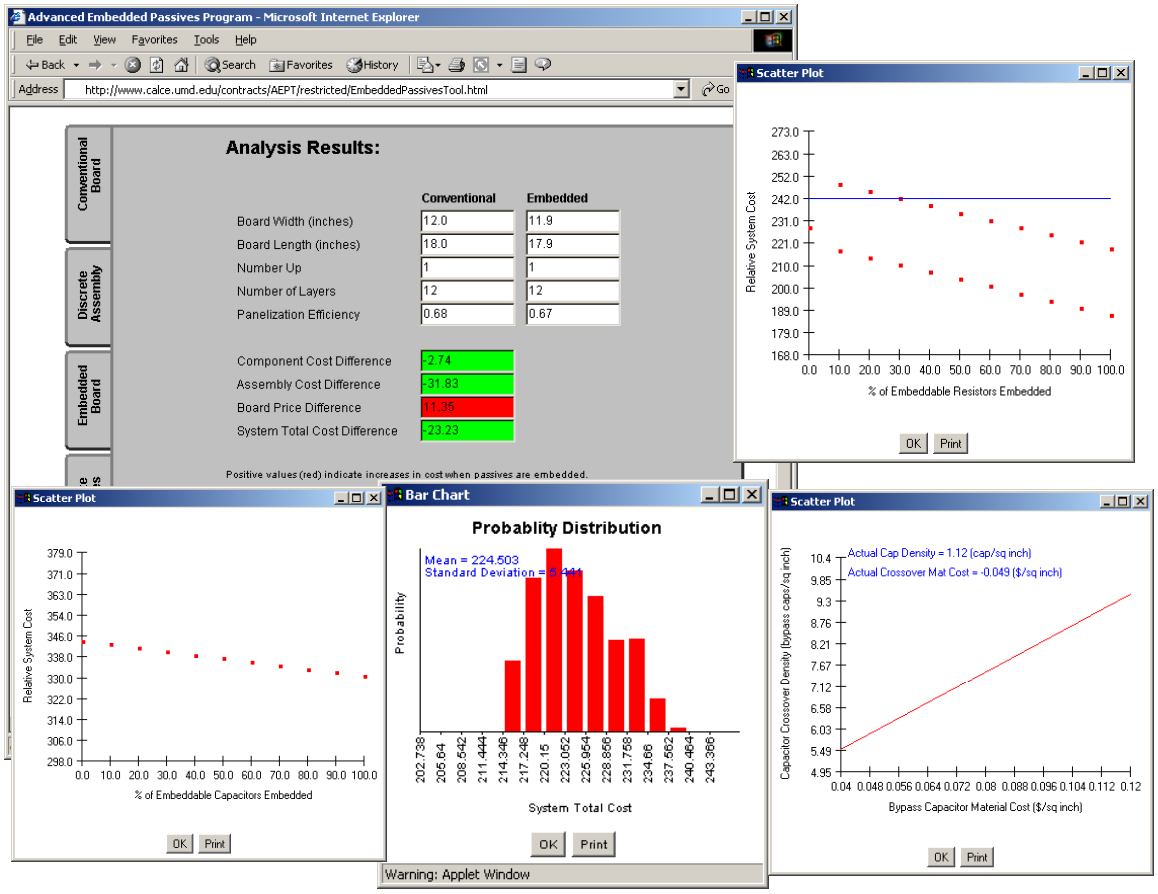


Figure B-4: Software Analysis Results interface illustrating the various types of results and results analysis that are attainable

Appendix C – Input and Output Variables for the Panel Trimming Model

			Inputs
Customer Inputs	Board Width (inches)	w =	2.165
	Board Length (inches)	l =	2.165
	Panel Width (inches)	W =	18
	Panel Length (inches)	L =	24
	Total # Resistors per Board	r =	174
	Incremental Resistor Count	$(r)_i$ =	100
	Average Resistor Value (Ω)	R =	7560
	Average Pad Size (Φ in)	A_P =	0.05
	Average Pad Alignment Error (in)	e_P =	0.0001
	Estimated Distance per Table Home (in)	Dth=	30.00
	Estimated Distance per Board Hop (in)	Dbh=	0.32

Equipment Capability	Galvo Field (inches)	f =	4
	Probe Type (0 = Probe Card, 1 = Flying Probe)	P_t =	0
	Max # Probes per Card	p =	14
	Average Probe Size (Φ in)	a_p =	0.01
	Average Probe Alignment Error	e_p =	0.005
	Forcer Acceleration (g)	d^2s/dt^2 =	0.5
	Accel Increment (g)	$(d^2s/dt^2)_i$ =	0.00
	Forcer Max Velocity (in/s)	ds/dt =	10.00
	Vel Increment (in/s)	$(ds/dt)_i$ =	0.00
	Flying Probe Acceleration (g)	$\delta^2s/\delta t^2$ =	1.5
	Flying Probe Max Velocity (in/s)	$\delta s/\delta t$ =	40
	Time per Vision Alignment (s)	T_V =	0.30
	Align Increment (s)	$(T_V)_i$ =	0.00
	Time per Probe Lift (s)	T_L =	0.1250
	Laser Rep Rate (s^{-1})	QR =	5000
	Laser Bite Size (μin)	BS =	200
	Max Trim Cut Length (in)	C_L =	0.030

Equipment Performance			
	Probes per Contact (Kelvin = 2)	K =	1
	# Probe Downs before Vision Alignment	P_v =	1
	# Probe Downs per Table Step	Np =	1
	Acceleration Time Per Table Home	ath =	0.100
	Acceleration Time Per Board Hop=	abh =	0.0008
	Max Velocity Time Per Table Home =	Vth =	2.900
	Max Velocity Time Per Board Hop =	Vbh =	0.000
	Time To Max Velocity =	Tmv=	0.050
	Acceleration Time per Table Step (s)	t_{at} =	0.093
	Constant Velocity Time per Table Step (s)	t_{vt} =	0.000
	Time per Table Step (s)	T_S =	0.093
	Time per Probe Card Step (s)	T_{pc} =	0.60
	Time to Max Flying Probe Velocity =	t_{fpmv} =	0.067
	Acceleration Time per Flying Probe Step (s)	t_{afp} =	0.033
	Constant Velocity Time per Flying Probe Step (s)	t_{vfp} =	0.000
	Flying Probe Time per Table Step (s)	T_{fp} =	49.3
	Galvo Time per Resistor Trim (s)	t =	0.036
	Time per Table Home (s)	T_H =	3.0
	Time per Board Hop (s)	T_B =	0.0008

Panel Processing			
	Board Density (per Panel)	ρ_B =	70
	Galvo Views (per Board)	ρ_V =	1
	Total # Resistors per Panel	R =	12180
	Resistor Density (in^{-2})	ρ_r =	37.12
	Resistors per Probe Step	ρ_R =	7
	Total # Probe Card Steps per Board	S_{Bpc} =	25
	Total # Flying Probe Steps per Panel	S_{Bfp} =	12180
	Total # Table Steps per Board	S_B =	25
	Total # Table Steps per Panel	S_P =	1680
	Average Table Step (in)	s_t =	0.43
	Average Flying Probe Step (in)	s_{fp} =	0.16
	Total # Vision Alignments per Panel	v_P =	1685
Output	**Total Time per Panel (minutes)**	**Σ T =**	**25.77**

Utilization

		Time (sec)
Step and Repeat Acceleration	t_{SRa} =	156.5911
Step and Repeat Velocity	t_{SRv} =	5.80
Step & Repeat Total	t_{SR} =	162.39
Probe Movement	t_{PL} =	858.75
Pattern Recognition	t_{PR} =	84.25
Galvo Movement	t_G =	434.74
Resistor Trim	t_{RT} =	6.264
Total (min)	Σ T =	25.77

		%Utilization
Step and Repeat Acceleration	t_{SRa} =	0.1012623
Step and Repeat Velocity	t_{SRv} =	0.0037507
Step and Repeat Total	t_{SR} =	0.105
Probe Movement	t_{PL} =	0.555
Pattern Recognition	t_{PR} =	0.054
Galvo Movement	t_G =	0.281
Resistor Trim	t_{RT} =	0.004
Total	**Σ U =**	**1.000**

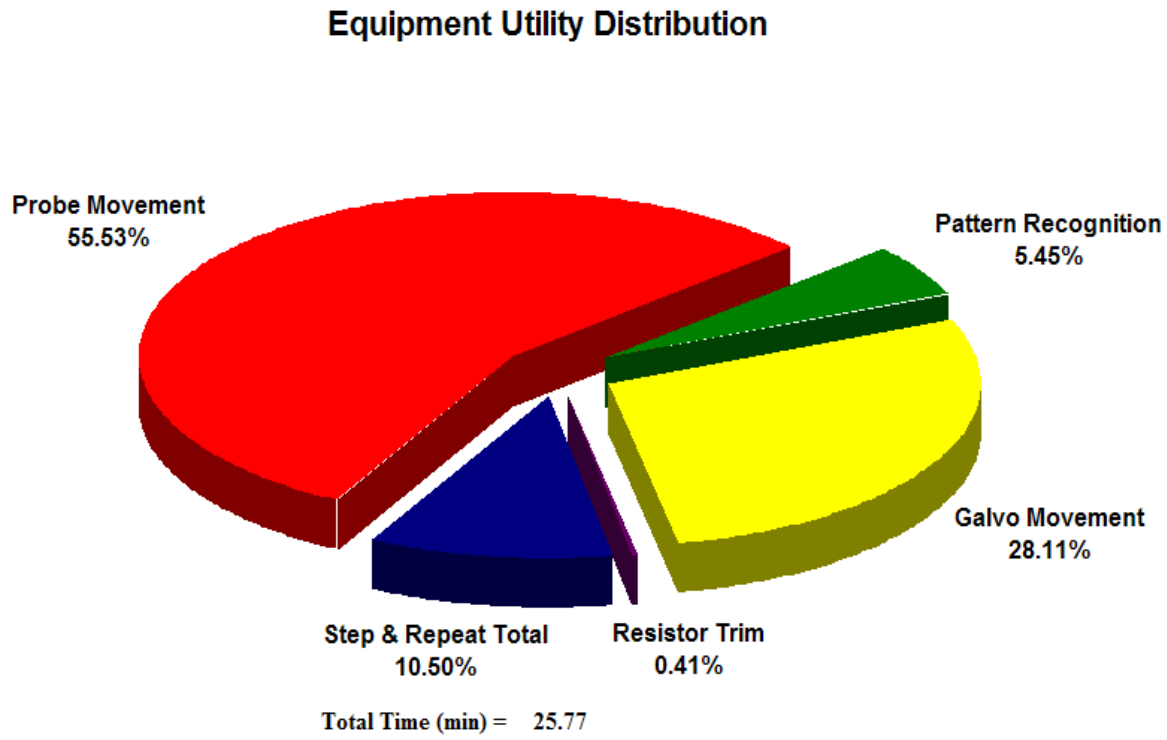


Figure C-1: Laser trimming equipment utility distribution

The equipment utility distribution pie chart shown in Figure C-1 was generated by utilizing the panel trimming model discussed in [38] and the inputs provided in this appendix. This pie chart illustrates the percentage of time allocated to the five major activities performed by the laser trimming machine for the trimming of embedded resistors. From this illustration it is shown that the actual trimming activity of an embedded resistor gets the smallest fraction of time.

Appendix D – Implementation of Multi-Population Genetic Algorithm

The first step to implementing the MPGA is to define the objective function and its constraints. Picking the initial guess value, which can be any value within the initial population, follows this step. The number of control steps (*N*) is determined for the specified problem. This is usually the total number of decision variables (NVAR) within the option space of the problem. The decision variables are bounded within the population range, limiting the maximum control input, at any time-step, to the maximum population size (MPS). Each decision variable is then described by using the MatLab matrix replication function, *rep*, with each descriptor being assigned to a description matrix called *FieldD*. The description matrix is constructed in MatLab using the following commands:

NVAR = *N*;

RANGE = [0; MPS];

FieldD = *rep*(*RANGE*,[1,NVAR]);

The parameters to be defined for executing the MPGA are given below;

Generation gap (GGAP)

Crossover rate (XOVR)

Mutation rate (MUTR)

Maximum number of generations (MAXGEN)

Insertion rate (INSR)

Number of subpopulations (SUBPOP)

Migration rate (MIGR)

Number of generations / migration (MIGGEN)

Number of individuals / subpopulation (NIND)

Where GGAP specifies the fraction of the population to be reproduced, INSR specifies the number of individuals that will be reinserted into the population after each generation and MIGR specifies the rate of migration between subpopulations. Each subpopulation will contain a specified number of individuals, NIND.

The initial population is obtained by using the Genetic Algorithm Toolbox function, *crtrp*, which creates real-valued initial population when the generation counter, *gen*, is set to zero:

Chrom = *crtrp*(SUBPOP*NIND,*FieldD*);

g*en* = 0;

This consists of SUBPOP × NIND individuals with individual decision variables chosen uniformly at random in the range specified by *FieldD*. The *Chrom* matrix contains all of the subpopulations and the objective function values for all the individuals in all the subpopulations. Using the MatLab *feval* command the objective function is evaluated with all the remaining parameters as its input arguments. The objective function is then passed through the generation loop where the fitness value is evaluated and the process of selection; crossover, mutation, migration, and reinsertion are computed. When this is completed the generation counter is incremented and the generation loop is revisited. This process continues until the generation counter reaches the set maximum number of generations assigned to the problem, MAXGEN. At that point the program is terminated yielding the optimization results.

GLOSSARY

Active Part Additive	A part that provides amplification or power gain.
Additive	In the context of this dissertation additive refers to adding material onto the inner layer of a substrate to form an embedded resistor of specified value.
Bypass capacitor	A capacitor that releases a stored electrical charge to the power distribution system whenever a transient voltage spike occurs. Bypass capacitors provide a low impedance supply, thereby minimizing the noise generated by switching outputs of a system.
Conversion Cost	The handling, storage and assembly costs associated with a discrete component.
Cycle Time	The time that elapses from the beginning to the end of a process or subprocess.
Discrete Passive	A single passive element in a leaded or surface mount package.
Embedded Passive	A passive device that is buried in the substrate material. Also referred to as an integral passive.
Fanout	A measure of the ability of a logic gate, implemented electronically, to drive further logic gates. In the context of this dissertation, fanout is one less than the number of pins connected together by a net
Integrated Passive	Multiple passive elements of more that one function

	and possibly a few active elements within a common package.
Interdeparture Time	Time elapse between completed products.
IO	Number of pins connectors that are present in the surface mount devices.
Layer Pair	A layer of dielectric with patterned conductors on both sides.
Monte Carlo	A means of statistical evaluation of mathematical functions using random samples.
NEMI	National Electronic Manufacturing Initiative
Net	Electrical connection between a group of two or more component pins.
Non-Negative Control	A constraint put in place in order to prevent the objective cost function from having negative values when subjected to the optimization environment.
Number-up	The number of boards produced on a panel.
Panel	A flat, rectangular piece of laminated resin on which printed circuit boards are formed.
Passive Component	Electrical components that do not provide amplification or gain, e.g., resistors, capacitors, and inductors.
Profit Margin	Earnings express as a percentage of revenue, i.e., the percentage of sales the company has left over as profit after paying all expenses.

Routing	Conductor paths for connecting all electronic components in a printed circuit board.
Subtractive	In the context of this dissertation subtractive refers to the etching out of resistive material from a dedicated layer pair to form individual resistors.
Surface Mount	A circuit board packaging technique in which the leads (pins) on the chip and components are soldered on top of the board, not through it.
Trimming	The value adjustment of embedded resistors by performing specific cuts within the resistive material to scale up the resistor to the desired resistive value.
Via	A vertical connection in a printed circuit board that is filled or plated with a conductor that touches (and connects) the conductor patterns on both sides of the printed circuit board.

REFERENCES

[1] Whitaker, J., *The Electronics Handbook*, CRC Press, Inc., Boca Raton, FL, 1996, pp.105.

[2] Marcanti, L. and Dougherty, J., "Embedded Passives: Promising Improved Performance," *Circuits Assembly*, July 2001, pp. 28-39.

[3] Electronic Industry Market Research and Knowledge Networks, "Passive Components - Private Companies Report," April 2001.

[4] Frost & Sullivan, Research Publication: 5261-25 - World Discrete Resistor Market by End-User Industry, December 1998. Also see: http://www.frost.com/verity/press/electronics_semiconductors/pr526125.htm.

[5] Sandborn, P, Etienne, B. and Subramanian, G., "Application-specific economic analysis of integral passives," *IEEE Trans. on Electronics Packaging Manufacturing,* Vol. 24, No. 3, July 2001, pp. 203-213.

[6] *Prismark Partners, LLC.*, 2001 company presentation provided by Tracey Finnerty, email: tracey@prismark.com.

[7] Lasky, R., "Growth continues for passive components," *Electronic Packaging & Production*, Vol. 38, No. 3, March 1998, pp. 77-78.

[8] Tummala, R., White, G., Sundaram, V. and Bhattacharyam, S., "SOP: The Microelectronics for the 21st Century with Integral Passive Integration," *Advancing Microelectronics*, IMAPS

[9] J. Rector, "Economic and technical viability of integral passives," in *Proc. Electronic Components and Technology Conference*, Seattle, WA, May 1998, pp. 218-224.

[10] *Prismark Partners, LLC.*, "Pushing the Shrinking Envelope: A Status Report on Embedded Passives in PCBs," December 2000.

[11] McGregor, D., "Standards Development Efforts for Embedded Passive Materials," *IPC Annual Meeting*, October 2001.

[12] B. Kim, "Embedded Passive Components," Arizona State University Department of Electrical Engineering

[13] Fjeldsted, K., and Chase, S., "Embedded passives: Laser trimmed resistors," *CircuiTree*, March 2002.

[14] Hickman, J., "Embedded Passive Components – Are We Ready?," *Huntsman Optronics Global News*, 2003.

[15] Rector, J., Dougherty, J. and Brown, V., "Integrated and Integral Passive Components: A Technology Roadmap," in *Proc. 47th Electronics Components and Technology Conference (ECTC)*, 1997, pp. 713-723.

[16] NEMI, "National Electronics Manufacturing Technology Road Maps," December 1996, Herndon VA.

[17] D. Brown, "The economics of integrated passive component technologies - An Ongoing Exploration of a Life Cycle Cost Analysis," *Advancing Microelectronics*, Vol. 25, No. 3, 1998, pp. 55-58.

[18] "Passive components technology roadmap," National Electronics Manufacturing Technology Roadmaps, NEMI, Inc., 1998.

[19] "Ohmega-Ply® cost analysis," a white paper available from Ohmega Technologies, Inc., Culver City, CA, www.ohmega.com.

[20] M. Realff and C. Power, "Technical cost modeling for decisions in integrated vs.

surface mount passives," in *Proc. IMAPS 3rd Advanced Technology Workshop on Integrated Passives Technology*, Denver, CO, April 1998.

[21] C. Power, M. Realff, and S. Battacharya, "A decision tool for design of manufacturing systems for integrated passive substrates," in *Proc. IMAPS 4th Advanced Technology Workshop on Integrated Passives Technology*, Denver, CO, April 1999.

[22] M. Scheffler, G. Tröster, J. L. Contreras, J. Hartung, and M. Menard, "Assessing the cost-effectiveness of integrated passives," *Microelectronics International*, Vol. 17, No. 3, 2000, pp. 11-15.

[23] D. J. Hayes, D. B. Wallace and W. R. Cox, "MicroJet printing of solder and polymers for multi-chip modules and chip-scale packages," in *Proc. IMAPS International Conference on High Density Packaging and MCMs*, Denver, CO, April 1999, pp. 242-247.

[24] G. Min, "Developments of polyimide-based capacitors and resistors for integral passives," in *Proc. IPC Printed Circuits Expo.*, San Jose, CA, 2000.

[25] P. Sandborn, "An Assessment of Embedded Resistor Trimming and Rework," to be published *IEEE Trans. on Electronics Packaging Manufacturing*.

[26] P. Sandborn and P. Spletter, "A Comparison of Routing Estimation Methods for Microelectronic Modules," *Microelectronics International*, December 1999, pp. 36-41.

[27] P. A. Sandborn, J. W. Lott, and C. F. Murphy, "Material-centric process flow modeling of PWB fabrication and waste disposal," in *Proc. IPC Printed Circuits Expo.*, San Jose, CA, 1997, pp. S10-4-4-S10-4-12.

[28] C. Habiger, *An Investigation into the Cost-Effectiveness of Multi-Chip Modules for Massively Parallel Computing Applications*, Hartung-Gorre Verlag Konstanz, 1995.

[29] D. Dance, T. DiFloria, and D. W. Jimenez, "Modeling the cost of ownership of assembly and inspection," *IEEE Transactions on Components, Packaging, and Manufacturing Technology – Part C*, Vol. 19, No. 1, pp. 57-60, January 1996.

[30] "Passive components technology roadmap," National Electronics Manufacturing Technology Roadmaps, NEMI, Inc., 2000.

[31] T. Takken and D. Tuckerman, "Integral decoupling capacitance reduces Multichip module ground bounce," *Proc. IEEE Multi-chip Module Conference*, Santa Cruz, CA, 1993, pp. 79-84.

[32] D. E. Goldberg, *Genetic Algorithms in Search, Optimization, and Machine Learning*, Addison Wesley Publishing Company, October 1989.

[33] J. Kingdon, *Intelligent Systems and Financial Forecasting*, Springer-Verlag New York, , January 1997.

[34] A. Chipperfield and P. Fleming, "Genetic Algorithm Toolbox for Use in MatLab: User Guide," University of Sheffield Department of Automatic Control and System Engineering

[35] J. P. Dougherty, J. Galvagni, L. Marcanti, R. Sheffield, P. Sandborn, and R. Ulrich, "The NEMI Roadmap: Integrated Passives Technology and Economics," *Proceedings of the Capacitor and Resistor Technology Symposium (CARTS)*, Scottsdale, AZ, April 2003.

[36] P. Sandborn, "The Economics of Embedded Passives," in Integrated Passive

Component Technology, R. Ulrich and L. Schaper editors, IEEE Press, 2003.

[37] M. Chincholkar, "Design for Production: Using Manufacturing Cycle Time Information to Improve Product Development," *Ph.D. Thesis*, University of Maryland College Park, 2002.

[38] K. Fjeldsted and S. L. Chase, "Trimming embedded passives: cost of ownership," *CircuiTree,* September 2002.

[39] Marco Tomassini, L.Vanneschi, Francisco Fernandez, and Germain Galeano, "A Study of Diversity in Multipopulation Genetic Programming," 6th International Conference on Evolutionary Computation EA'03", Proceedings, Lecture Notes in Computer Science, Springer Verlag.

[40] Portelligent, SENDO M550 GSM/GPRS Handset, Report # 118.1-031114-1c, www.teardown.com