ABSTRACT

Title of dissertation: QUALIFICATION OF METALLIZED OPTICAL FIBER CONNECTIONS FOR CHIP-LEVEL MEMS PACKAGING

Michael Andrew Deeds, Doctor of Philosophy, 2004

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A MEMS-based Safety and Arming (S&A) device is being developed for the next generation of Navy torpedoes. The MEMS-based S&A consists of a high aspect ratio MEMS chip fabricated by deep reactive ion etching (DRIE) of silicon on insulator substrates (SOI). The micro-machined structures, which include environmental sensors, actuators, and optical components, are susceptible to stiction related failures. A robust package is essential to transform the fragile MEMS S&A device into a rugged package capable of reliably functioning throughout the military stockpile to target sequence. To adequately protect the MEMS device from deleterious effects of the external environment, the package must be housed in a hermetic, organic-free package.

This dissertation presents the design of, analyzes, and qualifies a die-level fluxless packaging concept. The die-level package consists of a metallized seal ring patterned around the perimeter of the chip, including the fiber groove, sidewalls, and base. The fiber grooves provide a fiber optic interconnect between the microstructure area and the

macro-environment. A cap chip, with a matching seal ring, completes the clamshell package. Solder is deposited onto the seal ring and in the grooves at the wafer-level on the device and cap chips. A fluxless, and hence organic-free, soldering process joins and seals the fiber-chip assembly on the chip-level.

The conditions that govern fluxless soldering are addressed and tailored for success in the developed design. Surface energy models are used to understand the fluxless soldering conditions and to study the geometric stability of fluid solder joints at the fiber to chip interface. Several techniques for fabrication of the chips and assembly of the packages are investigated.

The effects of leak rate of the package seal on the internal package environment are discussed in detail to establish an acceptable leak rate of small volume MEMS packages. The calculations are then furthered to determine the acceptable leak path dimensions to ensure moisture does reach unacceptable levels during the package life.

The presented work represents the first reported organic-free (fluxless) die-level package seal with optical fibers that cross the seal boundary.

Qualification of Metallized Optical Fiber Connections for Chip-Level MEMS Packaging

By

Michael Andrew Deeds

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Dedication

For my daughter Alison Hope Deeds who became my true inspiration through her bravery and strength.

Acknowledgements

This is the fun part. There are so many people to thank for their support throughout my personal life, work, and school. I'd like to start with my advisor, Dr. Peter Sandborn. Your patience and timely persistence was key to the realization of this quest.

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Which brings me to my family. My heart goes out to Alison, who has taught me more in her 5 years than I was able to learn in the thirty years leading up to her birth. My son, Drew, who at the age of 1 is already preparing himself to help his old man fix up his fleet of cars. I must graciously thank my wife, Chrissy, for her patience through several of my all night modeling and writing binges. The mornings after those nightsmust have been entertaining as I took things out to the trash that never belonged there and then asked what she did with them. I want to extend my most humble gratitude to my parents, who have always believed in me and are the primary reason I pursued a doctorate degree in the first place. Ma, thanks for impressing upon me the value of a good education and for just being you, an accomplished woman and even better mother. Dad, they don't make them any better than you. Thanks for being a great parent, role model, and friend. Which brings me to my brothers and sisters (this could take some time, for I have 6 of them). Suzi, I thank you for rushing to my aide in my weakest moment. Somehow, I knew you would. You not only helped Ali through her treatment, but also helped me to help her. Angela, you to helped me to stand tall when I could barely stand at all. Don, so many years of good memories and another awesome role model. Jack, you have always been there for me with well thought out and helpful guidance. Lou, I still miss our football games at Granddad's house. Nancy, thanks for being my pal for all these years. Pat and Packy, thanks for a great friendship that has only grown stronger after 33 years. And perhaps most importantly, I want to thank the doctors, nurses, and technicians at Children's National Medical Center and National Institute of Health. There is no greater responsibility than saving a child's life. Dr. Seibel, I thank you for saving my little girl.

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CHAPTER 1:   INTRODUCTION

Microelectromechanical systems (MEMS) technology was first introduced in the 1960s in the form of pressure sensors. The MEMS structures in the pressure sensors, etched diaphragms with embedded resistors, are based on small deflections without friction or stiction related issues. Packaging of these sensors was able to readily leverage common integrated circuit (IC) packaging techniques, including passivation. In the 1980s, MEMS accelerometers entered the commercial market. The MEMS accelerometers did not need to directly interface with the surrounding environment. Packaging techniques for the accelerometers leveraged established IC packaging techniques, resulting in a more readily adaptable commercial product.

By the 1990s, MEMS research had expanded into more complex devices such as accelerometers, relays, optical devices, motors, pumps, and valves. The potential applications of MEMS also grew, spanning military, telecommunication, automotive, biological, hydrodynamic, and aerodynamic fields [1].   The expansion of MEMS into these fields arose from material improvements and processing advances. The new applications acted to further the advancement of MEMS technology.

Surface micro-machining and deep reactive ion etching (DRIE) expanded the potential for MEMS far beyond the bulk etched pressure sensors of the 1960s [2]. These processes provide precise control of mechanical structure geometry. As a result, complex systems can now be fabricated with or without assembly. However, the new devices posed new issues. Micron-sized contaminants rendered devices useless. Stiction, a

phenomenon where the surface micromachined device becomes bonded to the substrate, became a common source of device failure, both during processing and in-field use. Understanding material properties, friction, and wear at the micro-scale became important. In addition, the effect of humidity and the forces associated with fluid surface tension became critical to device performance. The role of the package grew to not only protect the device from the external environment but also to interface with the environment. The package could also enhance the device performance through control of the internal environment. It became clear that, although IC packaging techniques could still be leveraged, new packaging techniques needed to be developed [3].

1.1 MEMS packaging

MEMS packaging can build upon IC packaging, but significant differences in the package requirements necessitate new designs, processes, and evaluation techniques [4]. Perhaps the most striking characteristic of many MEMS devices is that they are required to react to and influence the external environment while at the same time be protected from it. In addition, the mechanical interaction between multiple MEMS structures and the fact that moving structures exist inside the package require that additional issues, such as stiction, be addressed. Passivation techniques, which have greatly enhanced the reliability of IC packaging, are not directly applicable to MEMS devices due to the relatively large-scale motion of their components. Finally, the introduction of new

materials and processes on the chip introduces new failure modes and requires unique reliability assessment techniques.

Shouldering the burden of several often conflicting requirements, the package cost of MEMS is estimated to be somewhere from 60% to 95% of the final product [1, 5]. Two of the most successful commercial MEMS products, Analog Devices' accelerometers (e.g., ADXL models) and Texas Instruments' Digital Mirror Device™, are both packaged hermetically [6, 7]. The prominence of hermetic packaging in MEMS arises for several reasons:

- Difficulty in passivating moving structures (corrosion failures)
- Effect of moisture on moving structures (stiction and friction)
- Effect of moisture on reflecting surfaces
- Control of out-gassing materials in the package (stiction, friction, mirror haze).

Despite the advances made by Analog Devices and Texas Instruments, relatively few MEMS devices have reached the commercial market. This is due largely to the unique requirements placed on the packaging by each unique device and its intended application. Several aspects of packaging, such as protection from contaminants and moisture control, are common to most MEMS devices. However, the manner in which the MEMS interface with the external environment significantly affects the package architecture. As a result, most MEMS devices will require application-specific packaging designs. The industry could, however, benefit from a common toolbox of technologies and processes to successfully package devices.

To produce a reliable, cost effective system, packaging must be considered early in the design cycle. The device drives the functional requirements of the package. A device that is not designed for packaging can put enormous and unnecessary demands on the package (functional, performance, and economic).

1.2 MOEMS Packaging

Microoptoelectromechanical systems (MOEMS), which are MEMS integrated with photonics, share the traditional challenges of MEMS with the additional issues of optical interconnects and of optical surface contamination. The challenges posed by optical interconnects pales in comparison to the potential payoff. Traditionally, switching in the telecommunication industry is performed electrically, even in optical networks. MOEMS offers significant savings in power, cost, and volume. More importantly, it eliminates bottlenecks at the electrical switch or router and allows wavelength division multiplexing (WDM) to reach its full performance potential.

Facilitating all optical networks, MOEMS is expected to have a huge impact on the telecommunications market [8, 9]. The optical component market, in general, is projected to grow anywhere from 35% to 50% per year for the next several years [5, 10]. MOEMS is well positioned to impact the existing market as well as the expanding market. Most MOEMS applications place additional emphasis on hermetic packaging due to potential contamination of the optical surfaces [11]. The proliferation of hermetic optical packaging needs has resulted in a library of standard packages and numerous

sources for custom package fabrication [12]. AXSUN Technologies uses a metal butterfly package to protect their MOEMS device, Acutune Detector Module, Figure 1-1 [13].

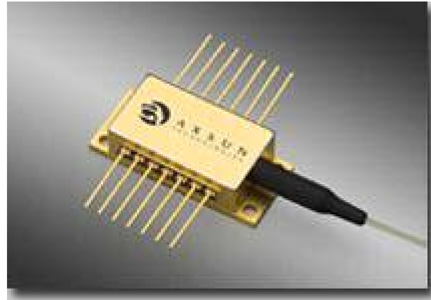


Figure 1-1: AXSUN Technologies Acutune Detector Module

1.3 The United States Navy's MEMS safety and arming (S&A) device

A MOEMS-based safety and arming system (S&A) for use in underwater weapons has been developed by the Indian Head Division, Naval Surface Warfare Center [4, 14, 15]. MEMS are the enabling technology for the next generation of lightweight torpedoes. Reducing volume by an order of magnitude, MEMS technology provides a means to reduce the diameter of torpedoes to one third to one half of previous systems. In addition, the expanding infrastructure of MEMS fabrication facilities is a stark contrast to the dwindling conventional mechanical S&A component-manufacturing infrastructure.

The purpose of the S&A system is to arm and detonate the weapon when appropriate and to prevent inadvertent weapon detonation. Reliability of the S&A is critical to the survivability of Naval assets, including the ship and its crew.

The S&A is composed of environmental sensors and actuators that control two fiber optic switches with mechanical locks. All structures are fabricated using the Bosch DRIE process [2] and are selectively released to eliminate micro-assembly. Silicon on insulator (SOI) wafers are utilized to provide an accurate etch stop and to provide an accurate gap between the MEMS structures and the underlying substrate. The S&A has been demonstrated in 100 μm and 125 μm device layer thickness. Once specified environmental operation criteria are met, the S&A arms by removing locks and pushing opposing optical fibers in and out of direct alignment with each other using v-beam electrothermal actuators [16, 17]. The switch is configured so that the fibers are initially offset in the out-of-line (off) position and are then actuated to the in-line (on) position.

The S&A chip has to be able to operate in a variety of environments, including temperature, humidity, shock, and vibration. The device must have a shelf life of 20 years. Although the S&A device is only required to function (arm) once, both its safety and arming functions are critical. The S&A must be highly reliable throughout its life to ensure weapon safety and function. To meet the above requirements, the package must be hermetically sealed (this requirement is discussed in more detail in Section 1.5). The baseline packaging approach for the Navy S&A is to adapt conventional hermetic packaging techniques from the high reliability IC and telecommunication applications. In this approach, the S&A chip is enclosed in a hermetic housing, such as Kovar®, a specialty nickel cobalt alloy with a thermal coefficient of expansion close to silicon. The package is hermetically sealed at each interconnect, including electrical and optical

interfaces. The final hermetic seal is formed by sealing a Kovar® lid to the package. The sequence used to package the S&A is shown in Figure 1-2.

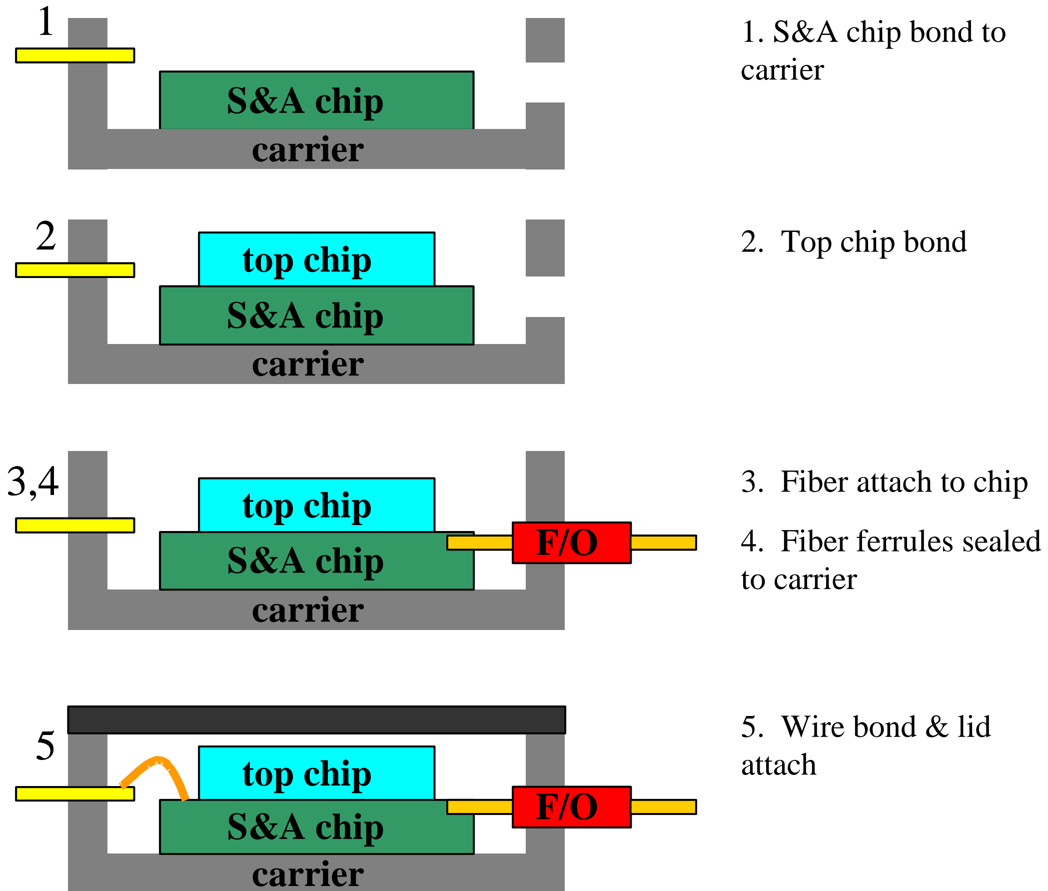


Figure 1-2: Baseline MEMS S&A packaging sequence (F/O denotes optical fiber)

Notice that several packaging steps are performed before the exposed MEMS structures are protected. The S&A chip in its package is shown in Figure 1-3.

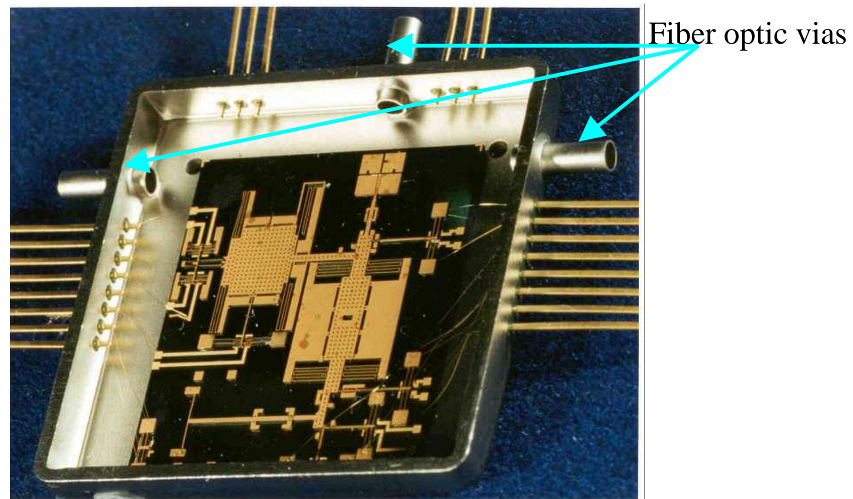


Figure 1-3: MEMS S&A chip in Kovar® package

1.4 Motivation for improved MEMS packaging

This section provides the motivation for this dissertation and the resulting benefits of this research. The role of packaging in the integrated circuit (IC) industry has transformed the IC market. Low-cost, reliable packaging was the final hurdle for the boom in the IC industry. Likewise, packaging is likely to have a similar effect on the commercialization of the MEMS technology. As the IC industry continues to benefit from the extensive research in IC package reliability, MEMS packaging must leverage the lessons that have been learned. However, MEMS, unique in its nature, will require unique solutions and evaluation techniques. Most successfully commercialized MEMS share two important commonalities:

- They are hermetic
- The hermetic seal is formed between 2 chips

The goal of this research is to provide a sealed package with optical fibers crossing the seal boundary using only batch fabrication techniques to form the package. This elimination of the Kovar® package is to be done without compromising hermeticity. However, a hermetic seal between two chips with a fiber crossing the hermetic boundary has yet to be demonstrated. This dissertation provides the foundation to realize a package in which the microstructure area is hermetically sealed between two chips with provisions for fibers to cross the boundary. This section details the benefits of realizing this package.

1.4.1 Increase packaged MEMS die yield

For the economy of batch fabrication to be realized for complex MEMS, high yields are required at each yield-critical phase of production. Significant yield issues may arise during fabrication, structure release, dicing, and packaging. Although 100% yield is not expected, even a 90% yield at each of these four critical steps would reduce final packaged yield to a meager 66%.

Low yields in the front-end processing are more acceptable than in the back-end processing because less has been invested in the product at the beginning of the process (this statement assumes that test and/or inspection can identify and scrap defective products during the fabrication process). Estimates for the packaging cost of a finished MEMS product may be anywhere from 60% to 95% of the overall cost [5]. A loss during the packaging process is therefore much more costly than at any other stage of development. The loss at the packaging phase can arise from two general sources:

- Before packaging, the unprotected device is exposed to a harmful environment (e.g., errant dust particles, rough handling, etc.)
- The environmental conditions associated with the packaging process induce a failure

Therefore, the packaging techniques need to be developed to protect the MEMS as early as possible in the packaging process. In addition, benign packaging environments are desirable to limit induced failures.

High reliability applications often use a ceramic or specialty metal package to house and hermetically seal the critical components. These carrier-level packages do not provide protection of the microstructure area until the final packaging step. Alternatively, some high reliability hermetic applications, such as Analog Devices' hermetic accelerometers, have been able to eliminate the carrier and seal the microstructure between two chips. Using its wafer-level sealing process, Analog Devices was the first to mass-produce MEMS accelerometers in 1993 with their ADXL50 model, which was the first commercial surface micromachined device [18, 19]. This chip seal approach provides protection of the fragile MEMS structures early in packaging process, thus exposing the structures to less handling and contaminants. A chip-level seal enables performing several packaging steps, such as die attach and wire bonding, after the MEMS is already protected.

1.4.2 Design flexibility

Both MEMS and optical devices are sensitive to humidity, out-gassing, and corrosion. The humidity in the package alters the friction between movable MEMS devices and can cause a phenomenon known as stiction. Stiction occurs when the once suspended MEMS structure makes contact with the substrate and the forces from MEMS actuators are insufficient to overcome the surface forces, most typically van der Waals forces. In more severe cases, external, macro-forces break the MEMS structure before the stiction can be alleviated. The fiber optic reflectors and fiber ends are also degraded by humidity. Out-gassing of organic material can also cause both stiction and fiber optic surface contamination. These concerns combine to greatly limit the viable material choices available to the packaging engineer. In addition, the use of out-gassing species requires compatibility studies between the selected bond materials and the MOEMS structures. A change in the assembly process or change in organic material selection will thus require additional compatibility testing. The addition of compatibility concerns expands the matrix of tests performed during test and evaluation. Another compounding factor is that compatibility concerns further burdens the interpretation of accelerated aging tests of the MEMS devices, which are performed in the absence of acceleration factors that are specific to MEMS failure mechanisms, further compounding risk.

Generally, it is prudent to minimize the variety of materials in the package to reduce the amount of testing required and to reduce the risk of field failures. Performing a chip-level hermetic seal accomplishes this. The hermetic portion of the package is as

small as possible, reducing, in most cases, the variety and quantity of materials involved. This allows for more freedom in the selection of packaging materials in the latter packaging steps. For example, out-gassing concerns from the die attach material are not relevant to a package sealed at the chip-level.

1.4.3 Increase package life cycle

Little field data exists on the life of MEMS. Acceleration factors for accelerated aging tests that hope to accelerate MEMS-specific failure mechanisms are educated guesses, if they exist at all. The understanding of the failure modes specific to MEMS is in its infancy. An extensive environmental conditioning program can add great confidence with regards to the robustness of the MEMS/MOEMS package, but cannot accurately predict the package life. If the life of the product falls short of the design goal, the life may be extended by periodic maintenance, such as inert gas back-fill, typical for most long-term storage military systems.

The chip-level packaging approach should increase the life of the MEMS package. The protection early in the packaging phase reduces the defects introduced into the system. Defects often are undetected in the screening phase (especially in the case of MEMS because there is little knowledge about how to design an effective screen), but reveal themselves years later after repeated environmental exposure. Reducing the variety of materials in the MOEMS portion of the package also decreases the risk of future failures. And finally, the increased design flexibility allows the package designer

to choose packaging material based on its mechanical and thermal properties without the additional constraints of chemical compatibility.

1.4.4 Cost

All of the reasons cited above have an impact on cost. Increasing die yields reduces the number of rejected die and also packaged devices. Greater design flexibility allows an additional emphasis on cost reduction through material and process selection. Another factor reducing cost is the reduction of testing requirements that shortens the design cycle providing shorter time to market at a lower unit cost. Increasing package life impacts system maintenance and inventory and reduces system sustainment costs.

Consider, for example, the carrier package. Specialty metals, typically Kovar®, are used to provide a close coefficient of thermal expansion match at the die mount between the silicon chip and the package. Glass seals in the walls of the package provide the electrical isolation and the hermetic feed through for the electrical interconnects. Kovar® is an expensive metal that is difficult to machine, typically handled by specialty machine shops. The glass electrical interconnect seal is also a specialty process. The result, for custom applications, is a carrier that can cost upwards of $100. Contrast that to a chip, which can serve as a hermetic lid for pennies.

1.5 Package requirements

To meet the requirements presented in Section 1.3, the package must be hermetically sealed and free of organics [20]. Although the Naval requirements were the driver for the selection of an organic-free hermetic package, other MEMS applications, such as telecommunications, share similar issues that result in the same package definition.

The two key factors driving hermetic enclosure requirement for the MEMS structures are the following:

1) Moisture content in the package affects the performance of the MEMS device and can lead to catastrophic stiction failures.
2) Optical components (mirrors, lenses, etc.) are also sensitive to moisture.

The actual usage temperature of MEMS (and in particular the Navy S&A device shown in Figure 1-3) will vary over a wide range, making the usage relative humidity difficult to control. The storage temperatures will vary over an even greater range. This is significant in that it is imperative not to form condensation in or around the MEMS. Recall that MEMS devices are prone to stiction related failures; that is, capillary forces from moisture in the package draw the suspended structures to the substrate and the van der Waals forces keep them there. Even a small amount of moisture in the package during packaging or ingress during storage can result in condensate formation (Table

1-1). The values calculated in Table 1-1 are derived from the thermodynamic steam tables assuming a constant pressure control volume.

Table 1-1: Temperature and humidity conditions necessary to form condensation before freezing

Process	Temperature	Relative humidity (0 °C dew point)
Typical room (air used in packaging)	22 °C	22%
Packaging	125 °C	0.25%
Storage	60 °C	3%

Another factor in the reliability of MEMS is organic out-gassing. Out-gassed species pollute the internal environment and contaminate the optical surfaces and MEMS structures. A hermetic package can prevent ingress of organics from outside the package. However, a hermetic package also traps out-gassed materials inside the package. Therefore, a packaging design and process that yields a hermetic package with minimal internal volatile material is sought. Elimination of organics precludes the use of adhesives and solder fluxes within the sealed portion of the package. In addition, the package seals must maintain their integrity throughout the life of the MEMS.

1.6 Other relevant efforts and background literature

Due to large potential economic payoff of fielded MEMS devices, the details of the package design and processing tend to be guarded as trade secrets and as a result slowed

the progress of the industry [21]. More specifically, details of optical component packaging are not widely shared. Even less is published on MOEMS optical interconnects. Knowledge about optical interconnection methods is a highly guarded trade secret, even regarding the traditional fiber-to-carrier seal. Due to the fact that MOEMS is still in its infancy, this section also includes a brief description of relevant MOEMS work currently being performed.

1.6.1 Fiber optic packaging

The vast majority of fiber optic components are hermetically packaged [22]. This holds true even if MOEMS are not inside the package. Although there has been a significant effort to launch non-hermetic packages, most of the telecommunication industry uses hermetic components. The Telcordia standard, GR-468-CORE [23], imposed on all components in the telecommunication industry is, in general, stricter than military standards. The lower-end market, for example light emitting diodes, utilizes both hermetic and non-hermetic packages. The packaging of micro-optical components is key to the proliferation of commercial MOEMS [24].

It is the very fact that so little is published on packaging techniques for fiber optic components that fuels the fiercely competitive nature of the networking market at infrastructure companies such as Agere and Cisco, and contributes to the close guarding of intellectual property.

Agilent recently introduced a non-hermetic package for an optical transceiver that satisfies the Bellcore standard [25]. An encapsulation technique with silicone was used to achieve the hermetic-equivalent reliability. Strict attention to details in the design of the device and package are necessary to implement an approach such as this that uses passivation and encapsulation. In addition, the life of the non-hermetic package has yet to be demonstrated in field use.

1.6.2 Metallized fiber

In Section 2.1, it will be established that most fiber optic packages are hermetic. A key component to make these packages hermetic is metallized fiber. The metal is hermetically sealed to the fiber and provides a surface for solder to wet and form a hermetic seal. To make metallized fiber, the jacket is stripped off the end of the fiber over a specified length, usually on the order of a few millimeters. The exposed cladding is then coated with a nickel adhesion layer to facilitate soldering. This process is considered mature and metallized fiber can be readily ordered to customer specifications [22]. The metallization scheme can be specified by the end user, but usually consists of a gold plating over nickel. The gold prevents oxidation of the nickel and the nickel serves as the wetable surface for solder during packaging.

The fiber metallization facilitates attachment of the fiber to both the chip and the carrier. For the chip attachment, the fiber is typically soldered or welded to a metallized portion of the chip. Often a welding tab is placed on the fiber to facilitate the attachment

to the chip. The soldering and welding techniques avoid the use of organics and provide a robust, precise alignment between the fiber and the chip. For the attachment to the carrier, the metallized fiber is often first soldered to a Kovar® ferrule and the ferrule is the soldered to the package. The ferrule serves two purposes. First and foremost, the ferrule reduces the gap between the fiber and the hole in the wall of the package. The hole in the package is made much larger than the fiber to accommodate the welding tab for the chip attachment. The large clearance between the fiber and the conduit requires use of more solder and results in a weaker bond than a thinner solder joint. The second reason for a ferrule is to provide a robust feature for the automated grippers used in the assembly of the fiber to the chip and carrier. The ferrule does increase the cost of the fiber significantly and the complexity results in another potential leak path and thus increases likelihood for hermetic seal failures. Designs that eliminate the use of a ferrule benefit from reduced cost, reduced complexity, and should result in greater reliability. The key is to eliminate the ferrule while still maintaining the needed positional accuracy between the fiber and the chip.

1.6.3 MEMS packaging

MEMS packaging continues to be an active area of research [26]. Presently, packaging platforms are tailored to the application as well as the processing techniques and the microstructure materials selected to fulfill the application specific requirements. The MEMS industry is unlikely to achieve the level of standardization achieved by the IC

industry due to the fact that the MEMS must often interact with the environment and typically must maintain a certain degree of motion [27]. However, processes and techniques for one application can be applied or adapted to another. There is a strong need in the industry for standard packaging tools that are applicable across numerous applications [28]. Aside from pressure sensors, which only consist of the deflection of a silicon diaphragm, most commercial MEMS devices are hermetically sealed [29]. Accelerometers, rate sensors, and optical mirrors are typically hermetic. The hermeticity allows for control of the internal package environment, including humidity, pressure, and out-gassing. The hermetic package is not just critical to the long-term reliability of the package, but also impacts the performance of the device. From a reliability perspective, the hermetic seal protects the MEMS device from stiction related failures. In addition, it reduces the likelihood of corrosion related failures. From a performance perspective, the hermetic seal allows precise control over the internal environment. Moisture levels and pressure in the package can be selected to optimize the MEMS device performance. Various techniques are being explored to form the hermetic seal. Most of these techniques are being applied at the wafer-level to reduce final product cost, enhance product reliability, and reduce yield losses. Anodic bonding uses glass to make the hermetic seal and thus avoid stresses due to large coefficient of thermal expansion mismatch [30, 31, 32]. Silicon fusion bonding is advantageous in that two silicon wafers can be directly bonded together without any other material, but requires high bonding temperatures [33]. Solder remains an attractive choice since the seal can be performed at lower temperatures [34, 35, 36]. Finally, 0-level packaging approaches are being

investigated where micro-caps over the MEMS structures can be formed during the micro-machining process [37, 38].

Die attach of MEMS structures requires special consideration. A comprehensive study was performed jointly between NSWC and the University of Maryland's CALCE center to evaluate materials for die attach and chip-to-chip attach [39,40]. Indium samples were fabricated using the sequence outlined in Section 2.6. In this study a coefficient of thermal expansion (CTE) mismatch was introduced by bonding a silicon die to a ceramic die. Reflow of the indium samples was performed in a fixture at an extremely low value of absolute pressure. Test structures were inspected for delamination using scanning acoustic microscopy (SAM) and then put through a battery of environmental testing, including accelerated aging, thermal cycling, and shock. After completion of environmental testing, samples were again inspected for delamination and then die sheared. The indium solder did not see delamination growth due to environmentally induced stresses, Table 1-2. In addition, the indium samples were stronger in die shear than the organic based materials.

Table 1-2: Environmental study results of indium die attach material

Environmental Conditioning	Range of initial delamination (%)	Delamination growth (%)	Range of die shear (MPa)	Average die shear (MPa)
None	2 - 30	0	4.5 – 6.3	5.2
100 days 85% RH at 85°C	9 - 48	0	7.0 – 8.4	7.7
Thermal cycling: 28 cycles -54°C to 71°C	0 - 0	0	5.5 – 7.4	6.4
Shock: 250 gs, 4.5 ms	10 -38	0	4.6-13.8	7.9

1.6.4 MOEMS packaging

As a subset of MEMS packaging, MOEMS are also primarily hermetic. The reliability of the packaged device and the repeatability of the packaging process are the major hurdles to commercialization of MOEMS [41, 42, 43]. Hermetic packages with accommodations for optical fibers are commercially available [12]. Other packages, such as Texas Instruments' successfully commercialized MOEMS based overhead projector, use specialized hermetic packaging techniques. Still others, such as Agere's 64x64 3D MEMS optical switch, have developed non-hermetic solutions [44]. Optical interconnects for MOEMS have historically consisted of a hermetic interconnect where the fiber passes through a wall. However, wave-guides and windows are feasible alternatives to the fiber optic interconnect.

Current efforts in MEM/MOEMS packaging at the universities are not focused on optical interconnection. The Center for Advanced Manufacturing and Packaging of Microwave, Optical, and Digital Electronics (CAMPmode) at the University of Colorado at Boulder is a National Science Foundation (NSF) funded organization with a strong focus on MOEMS packaging [45,46]. However, most of CAMPmode published MOEMS packaging work is focused on lens alignment. The Defense Advanced Research Projects Agency (DARPA) has established the University Opto Centers program that focuses on the integration of photonics, electronics and MEMS [47]. Although many of these DARPA funded projects utilize waveguide interconnects, none appear to address interconnects with fibers at this time.

1.6.5 Fluxless soldering

Fluxless soldering continues to be an active research field, as it has been for the last 20 years. Environmental concerns are driving the industry away from the standard lead-based solders as well as the conventional rosin-based fluxes. The role of the flux is to effectively clean the oxides from both the solder and the surfaces to be wetted. Metal oxides typically have a very high melting point and inhibit the chemical bond between the solder and the wetting surface [48]. The flux is critical to forming a reliable solder joint, however, residue from the flux is the primary source of corrosion and out-gassing related failures in microelectronics [49]. The rosin-based fluxes can be difficult to remove and trap corrosive flux activators. In a conventional soldering process, the rosin-based flux is cleaned with a chlorofluorocarbon (CFC), which was banned by the Clean Air Act of 1995. As a result, no-clean and water-based fluxes were developed to replace the CFC-based cleaners [50]. These alternatives fluxes fail to clean the oxides as effectively as the rosin-based fluxes. As a result, soldering processes with non-rosin based fluxes often require control over the oxygen content in the environment during reflow [51]. In addition, the no-clean fluxes leave behind an unsightly residue. Conceptually, the no-clean fluxes do not require post solder reflow cleaning, but are typically cleaned for aesthetics as well as out-gassing concerns. The cleaners used to remove the no-clean and water-based cleaned fluxes still suffer from environmental concerns and do not clean the flux residue as effectively as the CFC cleaners. As a result, soldering for high reliability applications, such as space applications, is performed

without the aid of fluxes [52, 53]. Some systems, such as MEMS, are adversely affected by liquids due to stiction related issues and are difficult to clean due to small clearances between structures. This has further driven the need for fluxless soldering processes.

Fluxless soldering processes fall into two major categories:

- Passivation of the metallization surface and solder
- Atmospheric control of the oxygen content

Passivation of the metallized surface prevents oxidation of the solder. The passivation layer is dissolved into the solder joint during reflow. A fluxless soldering process using a vacuum deposition of gold onto indium was demonstrated for a variety of solder systems [54, 55, 56, 57, 58, 59]. In these processes, the indium in the pure indium or binary lead/indium, silver/indium, or tin/indium binary solder systems react with the gold to form a gold indium intermetallic that passivates the solder, thus preventing oxidation formation.

In an atmosphere-controlled soldering process, the atmosphere either protects the solder and wetting surfaces from further oxidation or reduces the existing oxides from these surfaces. Nitrogen and vacuum are used to prevent further oxidation during the reflow process [60, 61, 62]. Lee found that the atmosphere must be below 180 ppm for reliable wetting of indium solder to a nickel surface [63]. Dong found that a tin-indium solder would not spread on nickel in an inert environment unless the oxygen concentration was on the order of 10 ppm [64, 65]. Dong reports the reduction rate of the indium oxide, but fails to cite the thermodynamic conditions at which the reduction took place. The use of hydrogen to reduce oxides from the metal surfaces was demonstrated

to be feasible by Kuhmann [66] at temperatures well above the reflow temperature of the solder. Based on a thermodynamic analysis, Kuhmann later refuted the work of several others that claimed to be using hydrogen to reduce oxides at reflow temperatures [67]. Alternatively, formic acid vapor can also be used to reduce metal oxides in the soldering process [68].

1.6.6 Solder energy modeling

Modeling the solder shape, energy, and forces provides a deeper understanding of the solder process and can result in a valuable design tool. Empirical data can be used to obtain necessary data, but the complexity of the soldering process and the difficulty in controlling all of the factors that govern it make it difficult to obtain a firm understanding of the effects of the design parameters. A model need not necessarily be absolutely accurate to provide an understanding of the trends that govern the final shape of the solder joint. Rather the model should provide the designer a qualitative tool to predict the solidified solder geometry and the energy state of the solder in the fluid state. The final shape and energy state of a fluid and the resultant forces between the fluid and the boundary surfaces can be solved in a closed form for the simplest of cases using the Laplace Equation of Capillarity [69]. For more complex scenarios, several numerical techniques can be used to resolve the shape and energy of the fluid [70]. The energy state and geometry of a fluid, such as solder during reflow, can be modeled using Surface Evolver [71]. Surface Evolver is software developed at Susquehanna University by

Kenneth Brakke to study the surfaces shaped by surface tension and other energies, such as gravitational potential energy. It evolves a user-defined shape to a minimal energy state constrained by user-applied boundary conditions. Energy modeling of the solder can be used to predict final joint shape and reliability. Yeung used an energy model to predict the final joint shape to guide design of flip-chip and wafer-level packaging [72, 73]. The restoring force between two misaligned chips was studied at the Center for Advanced Manufacturing and Packaging at the University of Colorado under a DARPA contract [74]. The modeling was later extended to determine equilibrium shape and the final position of a MEMS structure that was actuated by the wetting forces of the molten solder [75]. These self-assembly techniques were verified experimentally [76, 77]. The stresses calculated in the Surface Evolver model of the molten solder, can be coupled into a finite element model for stress analysis of the resulting solder joint [78].

1.7 Scope and objective of present effort

A potentially hermetic package between two chips with a fiber crossing the hermetic boundary has yet to be demonstrated. The work in this dissertation lays the foundation for a chip-level fiber-based optical interconnect. The broad objective of this research is to demonstrate a fiber optic connection into a hermetic chip-level MEMS package supported by the development of an experimental database of soldering test structures combined with energy modeling.

The optical interconnect treated in this dissertation is formed by reflowing solder to seal between the two chips and at the fiber-to-chip interfaces, including the fiber groove. The chips are batch fabricated using MEMS compatible fabrication techniques. The steps added to the process to make the structures for the hermetic seal are all performed at the wafer-level using batch fabrication techniques. The undermetallization is sputtered onto the top mesas of the chips and into the grooves. The solder is evaporated on the top mesas of the chips and into the grooves. The solder and undermetallization designs are modeled using an energy minimization software tool, Surface Evolver, to provide guidance on the joint design. The assembly of the chip and fiber uses an inert environment, or preferably a reducing environment to provide more consistent post-reflow solder joint shape and consistency.

Several steps had to be completed to realize the chip-level optical interconnect package. These steps encompass fabrication, design, modeling, soldering, and assembly techniques. Each of these key steps required advancement in the state of the art or an improved fundamental understanding to result in a consistent, producible package.

1. Design and process development for fabricating the sealing die interface: First a design and processing approach was conceived and refined to seal a fiber between two chips (Sections 2.1 and 2.6). The selected design approach for this dissertation requires a hermetic seal of a round fiber in a faceted groove. In addition, a contiguous metallization ring is needed on the top mesa, on the fiber groove sidewalls, and on the bottom of the fiber grooves. Process techniques were tailored to meet these requirements. In addition, the sealing of the round

fiber in a faceted groove required additional solder volume near these interconnects. Masks had to be appropriately designed to define the wetable areas of the chip and to provide sufficient solder to fill the void geometry. The deposition techniques and the practical limits necessary to form solder pads significantly larger than the undermetallization pads were developed and evaluated.

2. Solder system design: The second major task that was addressed is the design of the solder system, Section 2.4. The metallization of the fibers and chips must be selected to ensure good adhesion, wetting, and compatibility with the solder. The thickness of each layer also plays an important role from both a thermodynamic and metallurgical perspective, which ultimately affects the success of any soldering technique. Proper selection of material and the material thickness of adhesion layer, wetting layer, passivation layer, and the solder layer are interdependent and dictate the success of a fluxless soldering process, joint strength, and joint reliability.
3. Fluxless soldering process: The third major task was to assess the viability of fluxless soldering and then apply the fluxless soldering process. The fluxless soldering process, although very dependent on the solder system, can be thought of being comprised of both the cleaning and assembly of the chips. A thermodynamic model that ideally governs the reactions of the metal oxides was applied and tailored to the reduction of oxides considered in this dissertation, Section 2.7. The understanding of thermodynamics behind the soldering process

was used to interpret the reflow results and then adapt the cleaning and assembly processes to realize the fluxless soldering process. An assembly process was designed to minimize solder oxidation, Section 2.9. The assembly process encompasses a series of steps and characteristics, including the handling of the die after cleaning, the method to apply the heat for reflow, the amount of heat to apply, the heat rate, and the gaseous reflow environment.

4. Joint stability modeling: Modeling is used as a design tool to predict the final energy, and thus the stability, of the reflowed solder joint, Section 3.3. In addition, the model provides a deeper understanding of the interaction between the wetting forces and the surface tension forces.
5. Experimental valdation: The final major task was to evaluate the reflowed solder coupons, Section 3.1 and 3.2. A scanning electron microscope (SEM) equipped with an energy dispersive x-ray (EDX) was used to evaluate the quality of un-sectioned and cross-sectioned solder joints. The EDX was particularly useful in identifying grain structures in post reflow solder joints. Destructive tests, such as die shear, were used as a quantitative evaluation of the quality of the solder.

The primary contribution of this dissertation is a method to hermetically seal a metallized optical fiber between two chips without the use of a flux. To date, no such package has been reported, with or without the use of fluxes. In addition to this umbrella contribution, several smaller contributions were also realized. First, a method to deposit a contiguous metal layer onto all the surfaces of a MEMS fabricated groove was

demonstrated. Second, a Surface Evolver model was generated to predict the flow of solder on a surface with a variable wetting angle. Third, the behavior of high aspect ratio indium solder during reflow, especially with regards to fluxless soldering, was examined. Fourth, a Surface Evolver model was generated to predict the stability of a solder joint between a round fiber and a faceted groove. Finally, conditions for fluxless soldering with indium were defined.

In Chapter 2, the design of test structures and the methods to fabricate these structures is presented. In addition, the parameters that govern the fluxless soldering process are examined. In Chapter 3, the energy modeling and the experimental results of the test structures is presented and discussed. In Chapter 4, the robustness of the package is evaluated through fiber pull, die shear, and highly accelerated life testing.

CHAPTER 2: INTERCONNECT DESIGN AND FABRICATION

In this chapter, the approach used to form a chip-level hermetic MOEMS package in which the fiber crosses the hermetic boundary is presented in detail [79]. The design concept is presented and associated issues are discussed. The batch fabrication processes used to make the chips, common to most MEMS foundries, are discussed and evaluated. The coverage of the sidewalls of the high aspect ratio trenches, one of the key features that must be realized for the producibility of the presented design, is evaluated for different processing techniques. The rationale of the solder system selection and parameter variations studied in this dissertation are discussed. The solder system is a critical step in the design of any solder joint due to formation of brittle intermetallics and failures along grain boundaries. For fluxless soldering applications, especially those that utilize capillary forces to drive the solder flow, the selection of the solder system requires further emphasis such that oxidation formation is limited and intermetallic formation does not impede the flow of the solder during wetting. To further address the fluxless soldering and oxidation, a thermodynamic model that governs the reactions of the metal oxides was applied and tailored to the reduction of oxides considered in this dissertation. After demonstrating that a vacuum and inert reflow environments are insufficient for fluxless soldering of the candidate solders, the use of a hydrogen reducing gas is discussed with a focus on the thermodynamic conditions to reduce the oxygen in the atmosphere to the point where the conditions are favorable to the reduction of the metal oxide. Having noted that the reduction of the oxide without use of flux is not trivial,

methods to remove the native oxide from the solder are presented. To further develop appropriate handling techniques, the reoxidation rate of the metal oxide as a function of temperature is introduced.

2.1 Device and cap chip design

In the studied approach, the fiber is to be sealed between two chips. The device chip is from a silicon on insulator (SOI) wafer with a 300µm handle wafer and a 100 µm device wafer. SOI wafers are commonly used in DRIE applications. A SOI wafers used in this dissertation consist of a 2 µm oxide sacrificial layer sandwiched between two silicon wafers, 300 µm and 100 µm thick in this case [80]. The 300µm layer serves as the handle wafer, providing compatibility with the fabrication equipment as well as rigidity during processing and in use. The 100 µm layer is the active or device layer. The device layer is machined to create the MEMS structures, such as the optical mirror. The sacrificial layer can be etched to selectively release structures and thus allow movement of the micromachined structures. A 100 µm device layer was selected to meet the requirements of the Navy MEMS S&A (Appendix A) and is considered fixed for the present effort. The thickness of the active layer is similar to other optical devices and the present technique may be extended to those applications.

The multimode fiber used in the present effort will have an approximately 125 µm outer diameter. Hence the fiber will protrude from the groove. The cap chip, made from silicon, was micromachined to account for this protrusion.

The channel dimensions in the DRIE die (Figure 2-1) must be optimized to meet two primary goals. The first goal is to house and provide passive alignment between the fiber and the MEMS structures. The second is to allow for the formation of a hermetic seal without the use of any fluxes. The use of flux with MEMS is undesirable from two standpoints 1) the surface tension of the flux is likely to cause stiction, and 2) residual matter from the flux is difficult to remove from or between the MEMS structures.

The passive alignment structures have been used in the S&A since 1997 and are not within the scope of this research [16]. Provisions were made for the passive alignment structures to ensure complete process compatibility. These designs were directly imported into a layout created strictly for the present effort. To maximize die yield in the fabrication process, entire S&A chips were not fabricated. However, the test structures were fabricated using essentially the same processing techniques used to make the entire S&A to ensure future process compatibility.

To facilitate the seal between the chips and between the fiber and chips, metal was patterned in a ring around the perimeter of the chips and in the DRIE grooves, respectively. There are three key elements to achieve a hermetic seal at these interfaces:

- Perimeter seal
- Metallization and solder deposition into the DRIE channel
- Reflow of solder in grooves

The perimeter seal is the most straightforward facet of the hermetic seal formation. The challenge in the perimeter seal lies in the criteria to form the seal without the use of fluxes. The impact of the decision to forgo the use of fluxes is discussed in detail in

Section 2.7. The process windows developed here represent the simplest case and does not address the need for the solder to move during reflow to fill voids. Rather, it provides a starting point for the conditions for fluxless soldering to be viable. The fluxless soldering process was demonstrated through a series of tests. First, bare indium wire was used to determine the process variables that govern the fluxless soldering process. Next, metallized chips with evaporated solder were bonded together and die sheared to assess the integrity of the bond in the process windows determined in the bare indium wire experiments.

In the second step the processing techniques had to be tuned to ensure a complete coating of the metallization onto the sidewall of the DRIE groove in the device layer. The metallization has to cover the cap chip grooves as well, but this is not as challenging as the deeper trenched device chip. Complete coverage of the etched grooves with metal is the key to providing a wetable surface for the solder. Without complete metallization, the solder fails to wet the silicon and thus a hermetic seal is not obtained. In addition to depositing the metal in the fiber groove, the metal also has to overlap the perimeter seal ring to complete the continuous seal around the entire chip. After formation of the metallization ring around the chip, solder is deposited over the metallization to facilitate the formation of the hermetic seal. The solder could be applied via a preform, but batch fabrication techniques are preferred. Once a complete metallized groove is formed, solder will be deposited into the grooves and around the perimeter. The deposition technique for the solder is most likely shadow masked sputtering, as is discussed in more detail in

Section 2.6. The third step, discussed in Section 2.9, is to perform a complete reflow of the perimeter seal and optical interconnect.

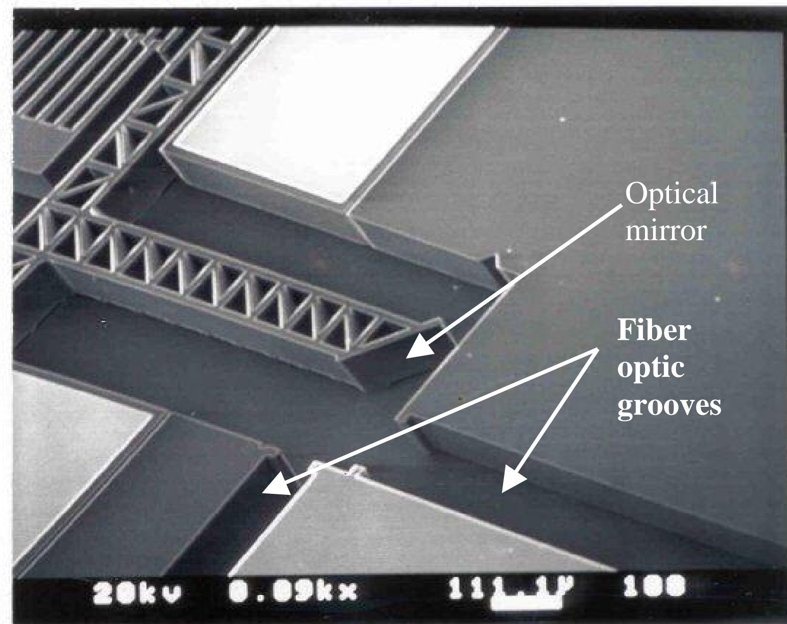


Figure 2-1: DRIE optical channels

The chip designs, device and cap, layouts were generated in AutoCAD and then transferred to L-edit (Tanner EDA) for mask production. The mask designs were sent to Cronos (JDS Uniphase) and John Hopkins University's Applied Physics Lab (JHU/APL) for review and fabrication. After a full review, CRONOS performed the DRIE portion of the fabrication and JHU/APL performed the metallization, indium deposition, and dicing.

2.2 Fiber

The two critical elements in the fiber design are metallization and outside diameter. The fibers used in this research are Dow Corning's SMF-28-50 multimode fiber. SMF-28 fiber is the most widely used fiber today and serves as the primary fiber in today's Internet infrastructure. The fibers have a 125 µm outside diameter before metallization. The fibers were metal coated with chrome, nickel, and gold. The chrome serves as the adhesion layer, the nickel is the wetting metal, and the gold prevents oxidation of the nickel. The selection of the undermetallization is discussed in more detail in the section on soldering (Section 2.4.3). Resonetics was selected to metallize the fiber based on their proprietary process of selectively coating portions of the fiber with metal.

2.3 Optical fiber interface

In Section 1.4, it was established that the optical via must be designed for hermeticity. Although the hermetic seal may be obtained at the carrier-level, a strong argument was made to perform this seal on the chip-level. This is accomplished by bonding a cap chip to the device chip, complete with the MOEMS structures. This approach is similar to that used to package MEMS accelerometers. However, the addition of the fiber optic interconnect increases the difficulty in creating this hermetic seal. A hermetic seal at the chip-level requires three species of hermetic seals:

- Device chip to cap chip

- Device chip to fiber to cap chip
- Device chip to electrical via to cap chip

The first two items in the above list are the focus of this research. The electrical via, although not trivial, is already being performed commercially and is compatible with the top chip processing.

The alignment and seal channels can be readily formed with deep reactive ion etching (DRIE) or potassium hydroxide (KOH). Diagrams of both fabrication techniques are shown in Figure 2-2 and Figure 2-3.

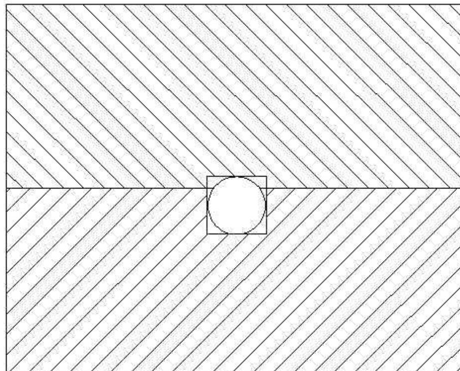


Figure 2-2: DRIE cap chip

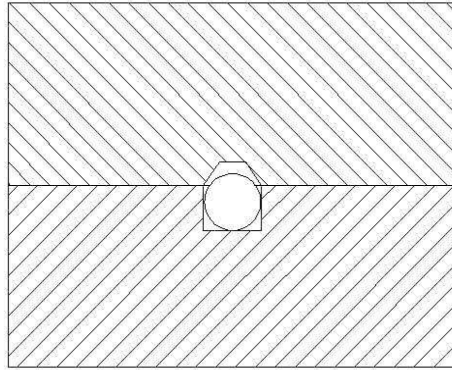


Figure 2-3: KOH etched cap chip

Note that the DRIE results in nearly vertical walls and that the KOH etches along the <111> plane of silicon, which yields a 54° slope in commonly available <100> silicon. In both cases, a round fiber must be sealed in a faceted surface with four to six faces. Since the S&A chip uses DRIE and thus a rectangular channel, the top chip was also machined using DRIE to mirror the processing on the device chip and to avoid introducing additional fabrication processes, which also can introduce new issues. Figure 2-4 shows a more detailed view of the DRIE optical interconnects, before reflow.

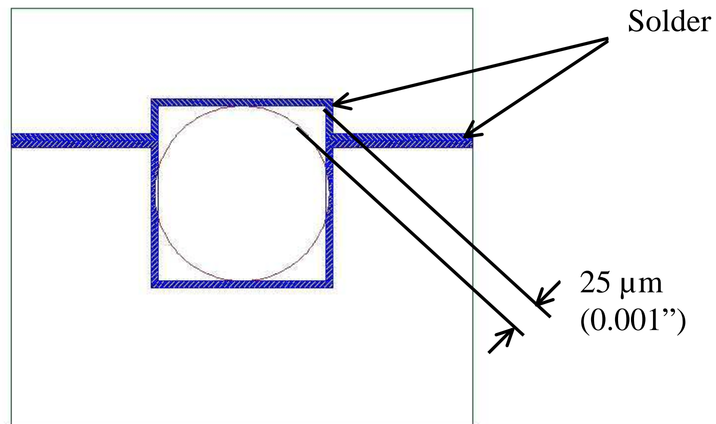


Figure 2-4: DRIE optical interconnect geometry

The key to this effort will be to design the solder joint such that the surface tension in the solder during reflow pulls the solder up to fill the voids around the fiber. Several parameters affect the ability of the solder to close the voids in the optical interconnect, including solder design, deposition process, and reflow parameters.

The solder geometry, undermetallization geometry, and the reflow environment play key roles in allowing the surface tension forces to act on the solder to close the voids. This aspect of the research is presented Section 2.4.

The process to metallize the two chips and to deposit the solder will have a significant effect on the ability to reliably obtain a hermetic seal. A controlled process is desirable for repeatability, and thus reliability. Therefore, hand soldering is not a desirable option. In the present S&A design, the device chip and the cap chip are bonded together by indium solder that is evaporated in place. The evaporation process is strongly dependent on line-of-sight. DRIE structures, with vertical walls, would receive little if any coating of the metal. Sputtering, however, yields better step coverage [2]. In

addition, the sputtering process yields more accurate thickness, more consistent material properties, and better adhesion [2]. The wafer is shadow masked to pattern the metallization only in desired locations.

2.4 Solder system design

In this section, the interdependency of the selection of the undermetallization, solder, and substrates are discussed. The solder system is comprised of the undermetallization material, the solder material, the thickness of the metal layers, and the flux, if applicable. The selection of the materials and the thickness of the solder system are dictated by the substrate materials involved, the processing limitations, and the application requirements. For this dissertation, the solder system joins two silicon chips, so stresses due to thermal expansion are not critical nor is small movement of the joint during loading. However, uninhibited flow of the solder is critical for the solder to flow to fill voids between the fiber and the channel.

2.4.1 Solder selection

A large variety of solders are used to make hermetic seals. Indium solder was selected due to its low processing temperature, hermeticity, mechanical material properties, bond reliability [39], and its amenability to the fluxless soldering process. Indium, a pure alloy solder, is a eutectic solder in that it transitions from solid to liquid at

one temperature. The lower melting point (indium reflows at 157°C) reduces the point at which the stress begins due to the coefficient of thermal expansion mismatch. Indium has a low modulus of elasticity resulting in a compliant solder joint. The low yield strength of indium can result in plastic deformation of the solder joint. For applications without stringent alignment requirements, the plasticity of indium can effectively mitigate stresses from external influence like thermal and mechanical shock. With regards to fluxless soldering, indium self passivates with an oxide layer on the order of 80 Å at room temperature. Indium oxide is readily removed with a plasma clean or acid dip. Indium can be compatible with gold if designed properly as discussed in Section 2.4.3. The intermetallics formed between indium and gold are relatively soft, as opposed to the brittle intermetallics formed between tin and gold. Gold is the ideal metal for use in fluxless soldering since it does not form oxides at or above room temperature and can protect other metals from oxidation.

2.4.2 Solder deposition

Solder can be applied to a wafer or a chip through a wide variety of methods, including dispensing, electroplating, evaporation, sputtering, and preforms. Dispensing and electroplating are wet processes that can adversely affect the MEMS device by introducing contaminants into the microstructure area and also by bringing large stiction producing capillary forces into action. The preforms and hand soldering introduce potential mechanical hazards to the unprotected device and are cumbersome and less

repeatable than deposited solder. Evaporation and sputtering are both batch fabrication techniques that are performed dry. Sputtering is a higher energy process and can be used to coat sidewalls. The evaporation process is very directional and will not coat sidewalls. Virtually any solder can be sputtered using a target of the appropriate alloy. It is difficult to control solder alloy composition with evaporation. However, evaporation of pure solder, such as indium, is a fairly standard process. For the present study, an evaporative or sputtering process was deemed suitable. Evaporation was chosen simply because of availability of an indium evaporator.

2.4.3 Undermetallization

The undermetallization must be compatible with the solder. Brittle intermetallics formed between the solder and the undermetallization during and after reflow is one of the most common failure sources for solder joints. Unlike tin, indium does not form a brittle intermetallic with gold. Therefore, indium solder systems can take advantage of gold nobility without suffering from brittle failures. Gold will not, however, adhere well to the substrate. Gold readily adheres to a seed layer of metal, such as chromium (Cr) or titanium-tungsten (TiW). Indium has a strong affinity for gold and will typically consume all the gold during the reflow process. Therefore, the metal under the gold serves as the adhesion layer to the substrate and as the wetting layer for the indium solder. Cr and TiW are rated as difficult to solder [81]. However, these metals can be wetted by solder if passivated in the deposition process. Another important concern is

the compatibility of metals with each other. Indium, which ultimately comes into direct contact with the undermetallization, is compatible with both Cr and TiW. The gold can be in direct contact with the undermetallization alloys without formation of intermetallics. An additional metal, such as nickel or platinum, can be placed between the adhesion layer and the gold for improved wetability if desired. In this dissertation, an additional metal layer was not used to reduce process flow cost.

The thickness of the gold layer and the ratio of gold to the indium are two important parameters in the design of the solder joint. The gold layer must be thick enough to prevent diffusion of oxides through the gold and from “pin hole” leaks in the gold layer allowing the underlying metal to oxidize. Solder systems that use gold to passivate the underlying metals often use 1000 Å or 5000 Å thick layer of gold. However, the gold layer can be too thick. Gold rich solder joints can form brittle intermetallics. In addition, the precipitation of the intermetallics at the now broad reflow range leads to inconsistent solder reflow and final joint geometry. Harsh et al. found that the gold content had to be below 3% by weight for the solder to flow freely and result in a predictable final shape [82].

Several solder systems are investigated in the present study. The followings metallization schemes are explored in this dissertation:

- TiW/Au/In: 400 Å of TiW, 5000 Å of Au, and 15-25 μm of In
- Cr/Au/In: 200 Å Cr, 1000 Å of Au, 15-25 μm of In
- Cr/Au/In: 200 Å Cr, 5000 Å of Au, 15-25 μm of In
- TiW/Au/In/Au: 400 Å of TiW, 5000 Å of Au, and 15-25 μm of In, 1000 Å of Au

• Cr/Au/In/Au: 200 Å Cr, 1000 Å of Au, 15-25 µm In, 1000 Å of Au

The performance of the different metallization schemes is discussed in detail in Chapter 3.

The amount of gold that is dissolved in the solder can be controlled through design and process control. By minimizing the amount of time the solder is held at an elevated temperature, the reaction rate between the gold and the indium can be slowed. However, the thin layer of gold used in the present effort, ranging from 0.1 to 0.5 µm, is completely consumed during the reflow. Even at the reflow temperature for indium (160°C), 0.5 µm of gold is consumed within a second, Figure 2-5 [83]. Therefore, in design of the solder joint, it must be assumed that all the gold is dissolved into the joint during reflow and must be accounted for to maintain the gold content at less than 3% by weight.

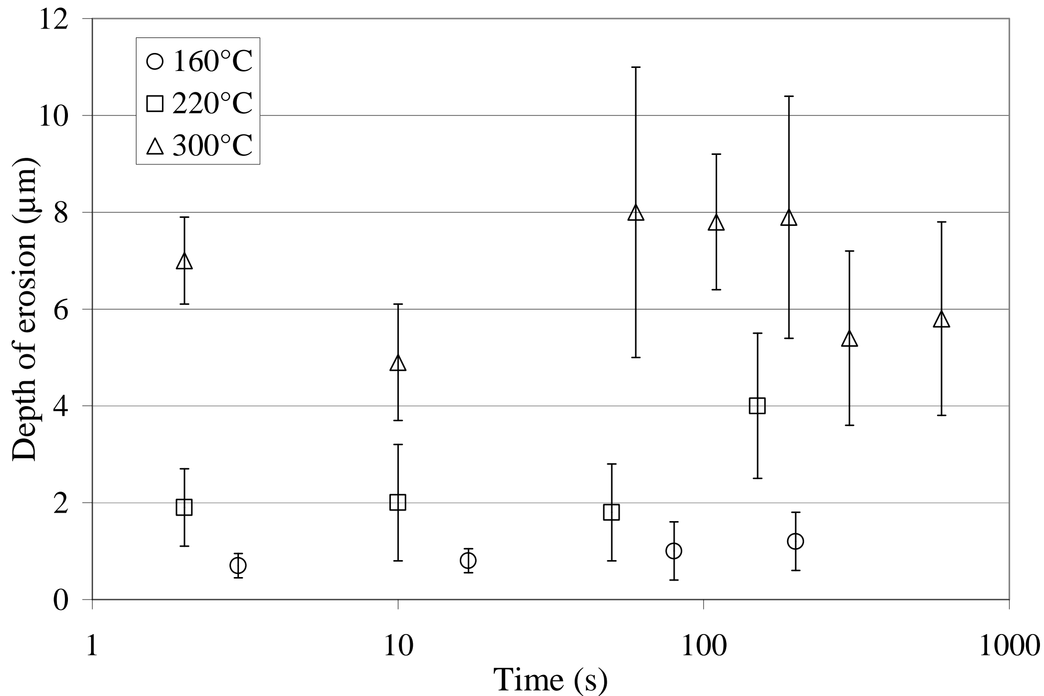


Figure 2-5: Gold dissolution in indium

2.5 Test structure fabrication runs

Solder test coupons were designed to validate the concept of using surface tension forces to fill voids. Several runs were performed without the DRIE step to address processing concerns, to address the limits of the solder deposition technique, and to provide hardware for assessing the viability of using a fluxless soldering process to reflow high aspect ratio planar indium structures. The mask layout used to make these test structures is shown in Figure 2-6.

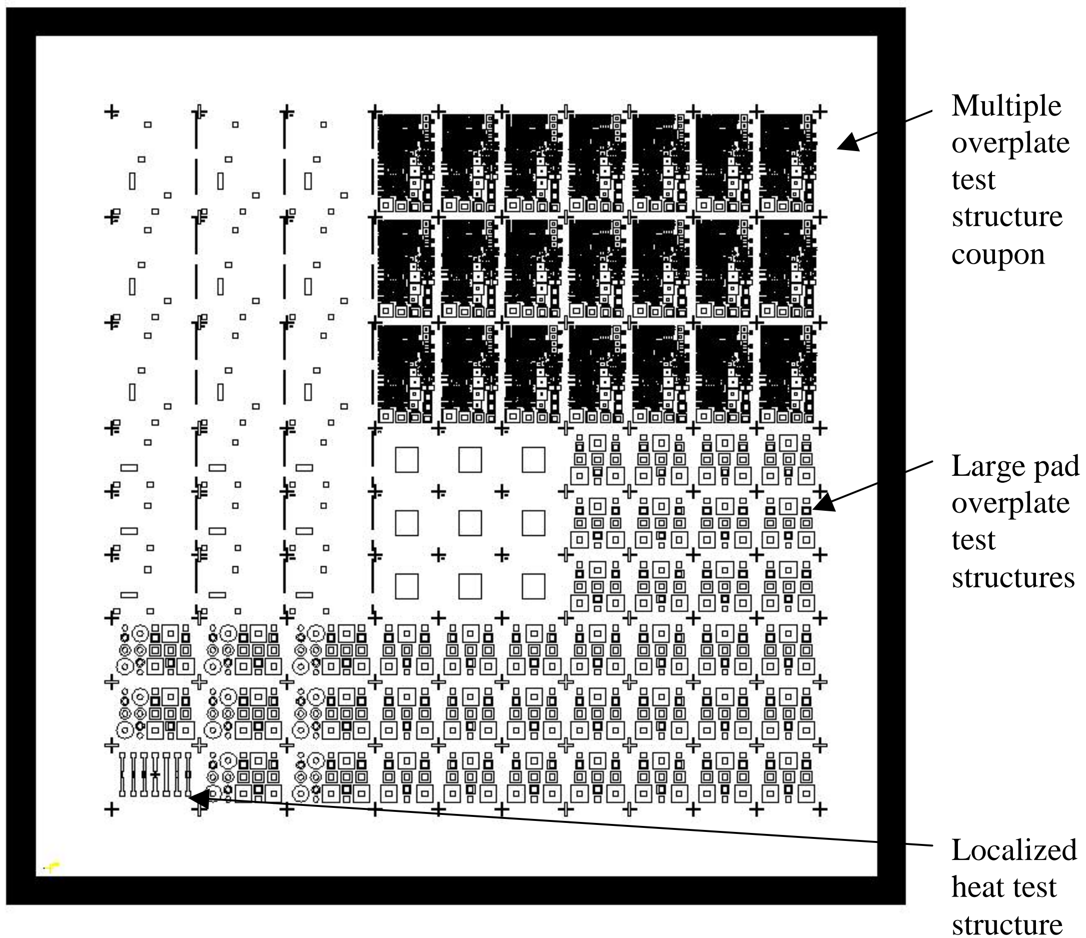


Figure 2-6: Mask layout for solder overplate test structures

Indium solder pads were designed to be, in some cases, larger than the undermetallization pad, Figure 2-7.

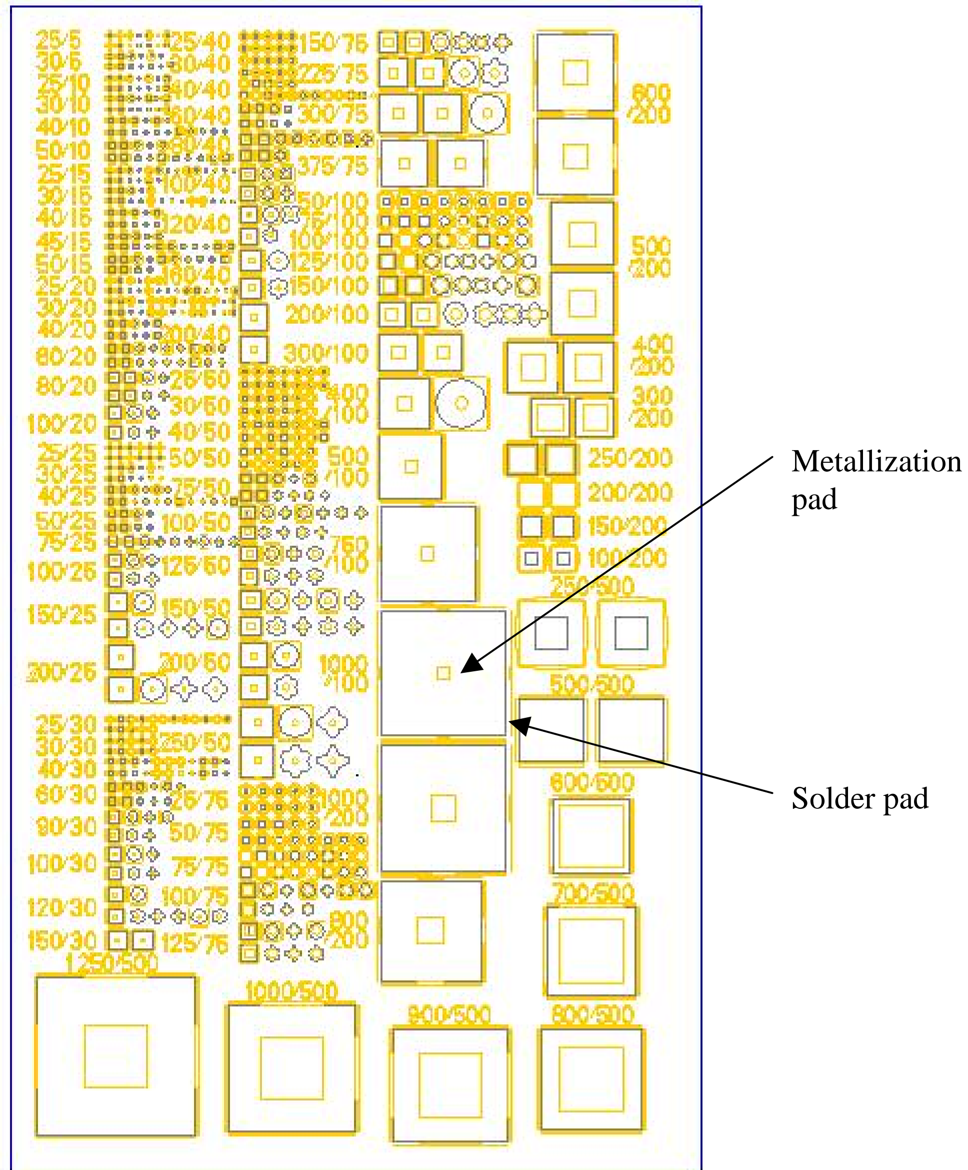


Figure 2-7: Multiple overplate test structure coupons

Labels are placed next to or on top of each family of designs. The first number in the label is the solder in-plane dimension in microns and the second number is the metallization pad in-plane dimension in microns. An example of fabricated structures on the multiple overplate chip is shown in Figure 2-8.

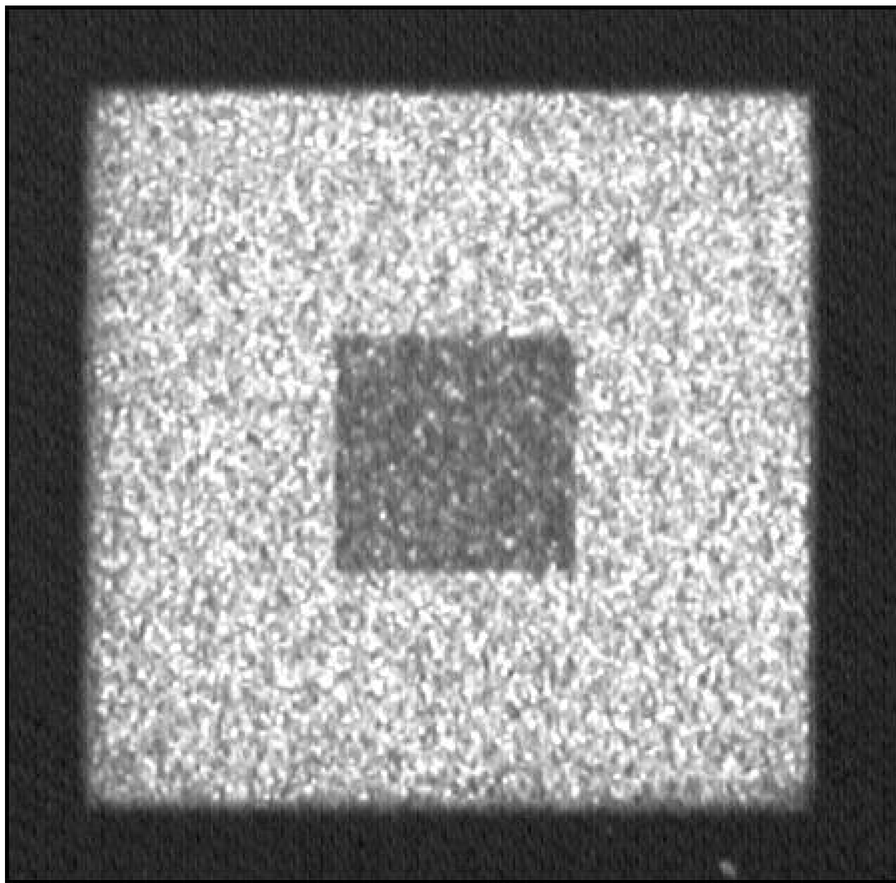


Figure 2-8: Fabricated structures on a multiple overplate chip

Structures were designed to explore the effects of the metallization pad size, solder pad size, and overplate ratios, Figure 2-9.

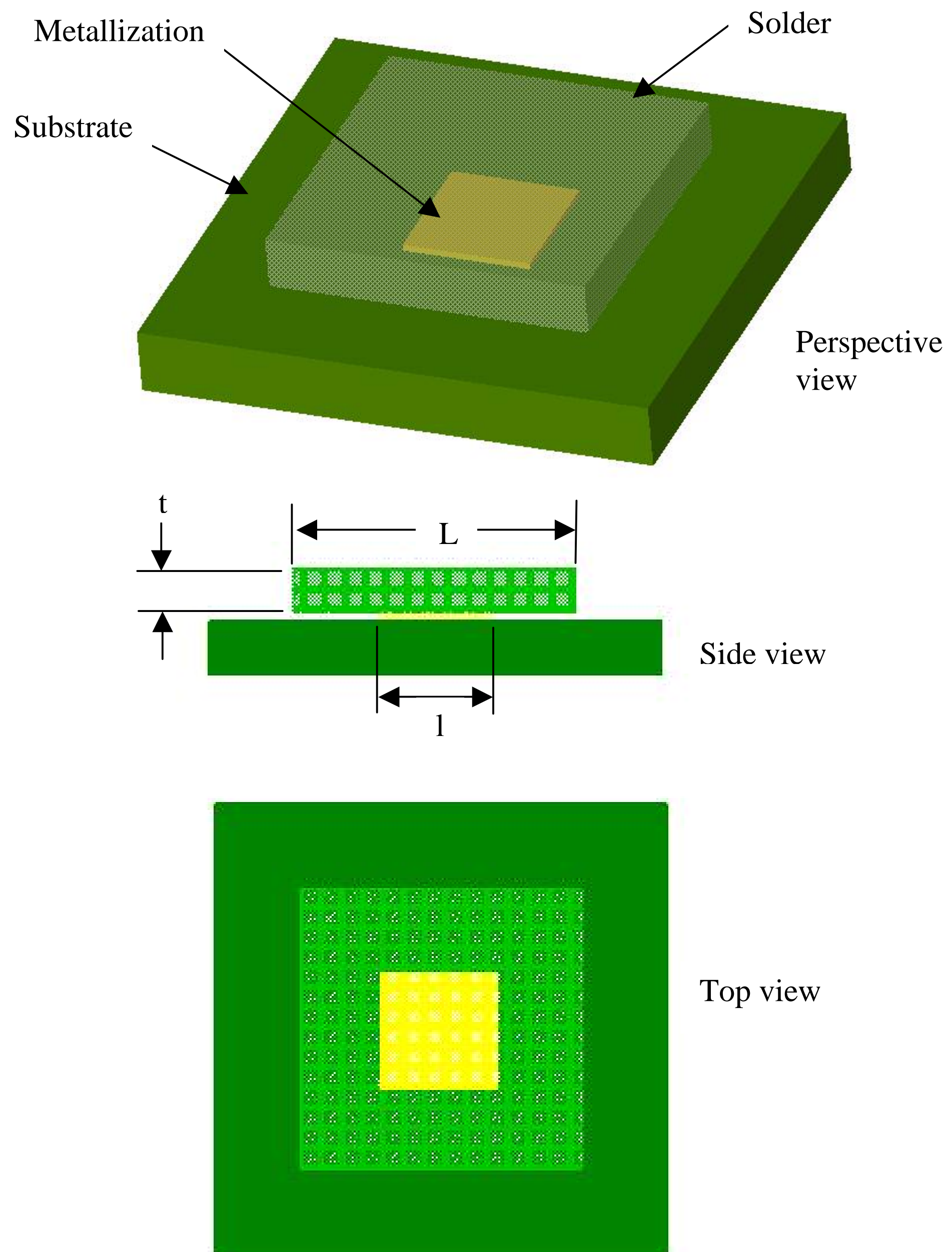


Figure 2-9: Overplate test structures

Where the metallization pad has in-plane dimensions, l, and the solder has in-plane dimensions, L, and thickness, t. The overplate ratio is defined as the ratio of the solder overplate length and the solder thickness.

$$\text{overplate ratio}=\frac{(L\text{-}l)}{2t} \tag{2.1}$$

Another useful parameter in comparing solder joint is the volume ratio. The volume ratio is defined as the ratio of the actual solder volume and the hemispherical volume of solder that is prescribed on the metallization pad (i.e., with a 90° wetting angle and without the presence of body forces).

$$\text{volume ratio} = \frac{L^2 t}{\frac{2}{3}\pi r^3} \tag{2.2}$$

The tests structures focused primarily on square pads, but also included round and other geometries. For the case of round pads, L and l represent the diameters. The test structures were designed to determine the maximum overplate length of the indium solder beyond the gold. In addition, structures were designed to span a large range of gold content in the joint. The solder test coupons were designed to test both the limits of the processing and of the proposed assembly technique. Yield losses were encountered in the fabrication process. Solder pads less than 30 µm were not achieved. However, 40µm solder pads could be reliably fabricated. Large overplate structures, with as much as 1000 µm indium pads on 300 µm gold pads, were created without solder loss. Earlier runs suffered from tearing of the solder as the mask was lifted off, at times only leaving solder over the metallized areas. The reflow of these and related structures is discussed in Chapter 3.

Particular attention was paid to the deposition of the indium. The evaporator was initially configured with a boat to hold the solder. Electrical current passes through the solder to resistively heat the solder. If a solder thickness greater than 5 μm is desired, the vacuum on the deposition chamber is broken and reestablished during the deposition process to add solder due to volume limitations in the indium boat. The boat also has a non-linear deposition rate, since the resistance of the solder increases as the volume of solder in the boat decreases. Breaking vacuum is of particular concern since it provides an opportunity for oxidation to form on the solder. The evaporator was reconfigured to use a crucible for holding the solder. The solder in this case is heated by the thermal conduction from the resistively heated crucible. The crucible holds enough solder so that 15 μm of solder can be deposited without breaking vacuum. However, the inside of the chamber heated up significantly. If more than 2 μm of solder was deposited at one time, the solder on the board would reflow or partially reflow during the deposition process in the chamber. Thus, thick depositions required that the process be shut off after 2μm and allowed to cool for several hours. The process time went from hours to days. In addition, the liftoff of the solder mask was much more difficult than for the boat deposition technique. Much of the gold and indium structures failed to survive the liftoff process. Wafers that reached hotter temperatures were more difficult to liftoff and had lower yield with less than half of the structures in Figure 2-7 surviving the processing. Control of the chamber temperature, by such means as an external cooler, would help reduce the heat and its deleterious effects. Due to budget and time constraints, the crucible approach was not further pursued.

In addition to reconfiguring the evaporator for indium deposition, a gold crucible was installed to passivate the indium before removal from the evaporator. By passivating the indium with gold, the oxidation of the indium could be averted. As a result, the oxide-cleaning step could be eliminated and the oxides present in the final joint could be reduced. The wafers that were processed with the gold formed a gold-indium passivating intermetallic, Au/In_2. However, the intermetallic layer did not completely passivate the indium as demonstrated during the reflow process, Section 3.2.3.

Test structures were also created to explore the use of resistance heating to reflow the solder. A localized heating technique allows for tacking of individual fibers without exposing the rest of the chip, including prior solder joints, to the full reflow temperature. Localized heating can be done with a laser welder [84]. However, laser welders require significant capitalization investment in tooling and training. A resistance reflow technique can be performed in virtually any lab and is an active area of research. The layout of the localized heat test structures is shown in Figure 2-10.

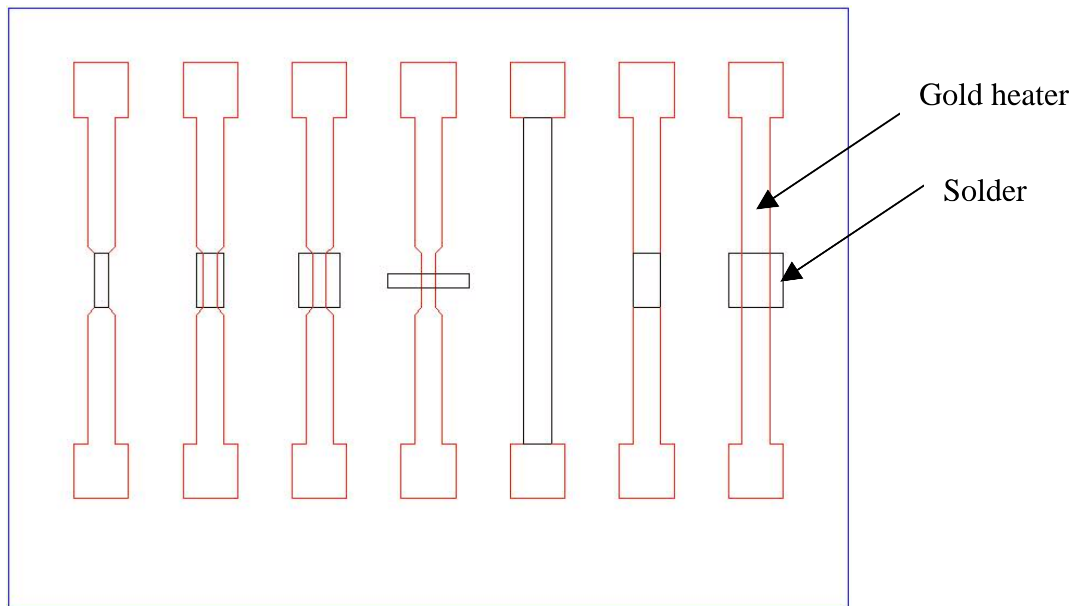


Figure 2-10: Localized heat test structure chip layout

The thickness of the heaters is 1000 Å in the Cr/Au metallization and 5000 Å in the TiW/Au metallization. Two widths were explored for heating, 125 µm and 250 µm. The solder was deposited over the heater and in some instances overplated beyond the heater. Structures on the fabricated chip are shown in Figure 2-11.

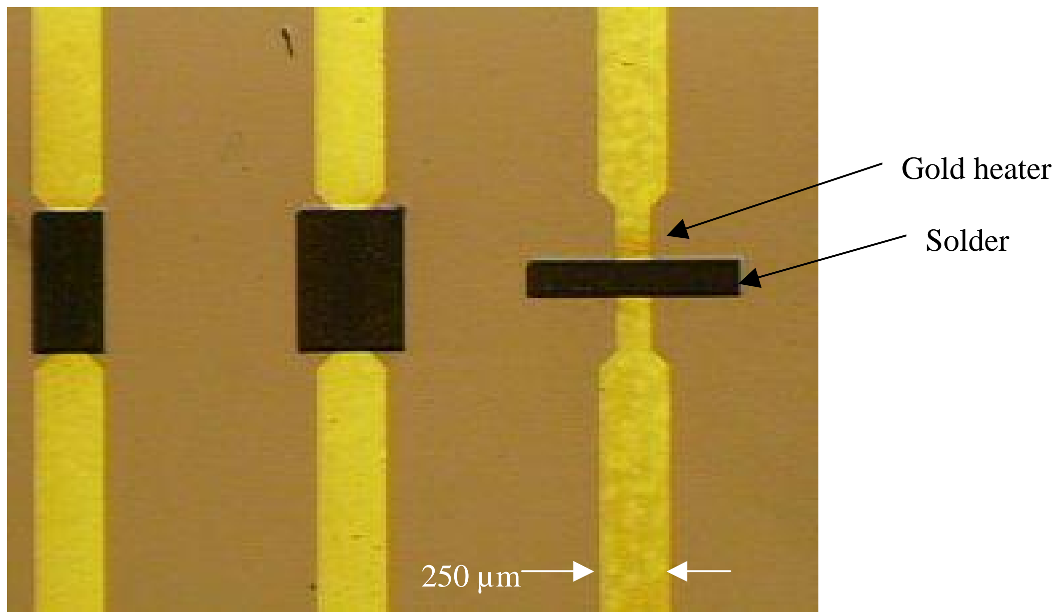


Figure 2-11: Structures on a localized heat test structure chip

2.6 Device and cap chip process flow

Having addressed the techniques to deposit the metallization and solder on the top mesa of the wafer, the focus turns to integrating the metallization process with the DRIE, including the metallization of the etched channel. Before the process flow was selected, several methods to form the seal ring of metal were considered. The formation of this seal is somewhat unique to this approach in that the seal crosses a DRIE trench. This requires a seal ring that spans the top mesa, the sidewalls of the fiber groove, and the floor of the fiber groove. The complete seal ring could not be formed until after the DRIE steps since metallization is needed in the channels that necessarily cross the seal ring. Metallization on the top mesa could be formed before the DRI etch, and then the groove metallization could be completed after the DRI etch. The undermetallization of

the sidewalls and bottom of the fiber channels is the key to the success of the presented approach. The sidewalls and bottom of a thin groove 130 µm wide and 100 µm deep must be covered with a contiguous layer of metal. A sputtering process was selected to deposit the metal in the channels because of the higher energy associated with sputtering. Evaporation is line of sight dependent and would not coat the walls nearly as well as a sputtering technique [2].

Having selected a sputtering technique to deposit this metal layer, there still remained several candidate methods to complete the seal ring in the DRIE trench. Although not considered exclusively, dry processing was preferred in this post DRIE step to reduce issues presented by wet processing. In addition, post DRIE steps that do not require contact with the wafer can be more readily integrated into the MEMS fabrication process. Three primary methods to mask the layer were considered:

- Liftoff mask
- Blanket coat, then etch away undesired metal
- Shadow mask

The liftoff technique was deemed to be unsuitable due to the sidewall coverage of the mask itself from the sputtering process. The metal on the sidewall effectively masks the mask during its removal. The metal-coated sidewalls further complicate liftoff since the metal must be torn to remove the mask. Thus this wet process was ruled out.

A blanket coat of the undermetallization would provide the best coverage of the channel sidewalls. Without using a mask during deposition, this technique eliminates the issue of undesirable shadowing effects of the mask. After the blanket coat of metal, the

wafer is then masked to protect the area where the metal is to remain. An etchant is then introduced to remove the unwanted metal. Finally the mask is stripped away. Although this is a wet process, it was explored due to the potential for superior sidewall coverage. Because this method was not the design of choice, the layout was not designed specifically for this technique. As a result, the mask was not able to protect the thin width of metal in the channels and this method was not further pursued due to additional costs for new masks and the fact that it is a wet process.

The shadow mask technique provides the greatest flexibility with regards to process integration. It can be done in a completely dry process and can be performed on released or unreleased parts. For these reasons, a shadow mask deposition to complete the seal ring was selected. However, the shadow mask process does not lend itself well to formation of a continuous ring. Three approaches were identified that utilized a shadow mask deposition technique to complete the seal ring:

- One shadow mask to from entire seal with bridges to hold the internal mask feature in place
- Two shadow masks; each forming half of the seal ring
- A lift mask before DRIE combined with a post DRIE shadow mask

The use of one shadow mask to form the entire seal ring is challenging since the inside region of the ring must be masked and this part of the mask must be attached to the rest of the mask. Small bridges can be used to hold the internal ring in place, but these bridges mask a portion of the ring. The process could be tailored to have a large spread of the metal through the mask to eventually cover the areas masked by the bridging. Due

to the fragility of the bridges and the uncertaincy of the spreading of the metal as it passed through the shadow mask, this approach was not pursued.

The use of two shadow masks is a viable method for formation of the seal ring. The primary disadvantage to this method is that it adds another process step after the DRIE. This approach was not pursued despite its viability.

The liftoff process to deposit the metal on the top mesa combined with a shadow mask technique to deposit the metal in the fiber channels was selected for this dissertation. The liftoff process reduces the number of processing steps after the DRIE step and is already utilized in the fabrication process of the S&A. This metallization has been proven robust for wire bonding. In addition, the fine resolution of the liftoff process is useful for definition of fine features, such as metrology structures. The mask layout to form the chip-level hermetic seal test structures is shown in Figure 2-12.

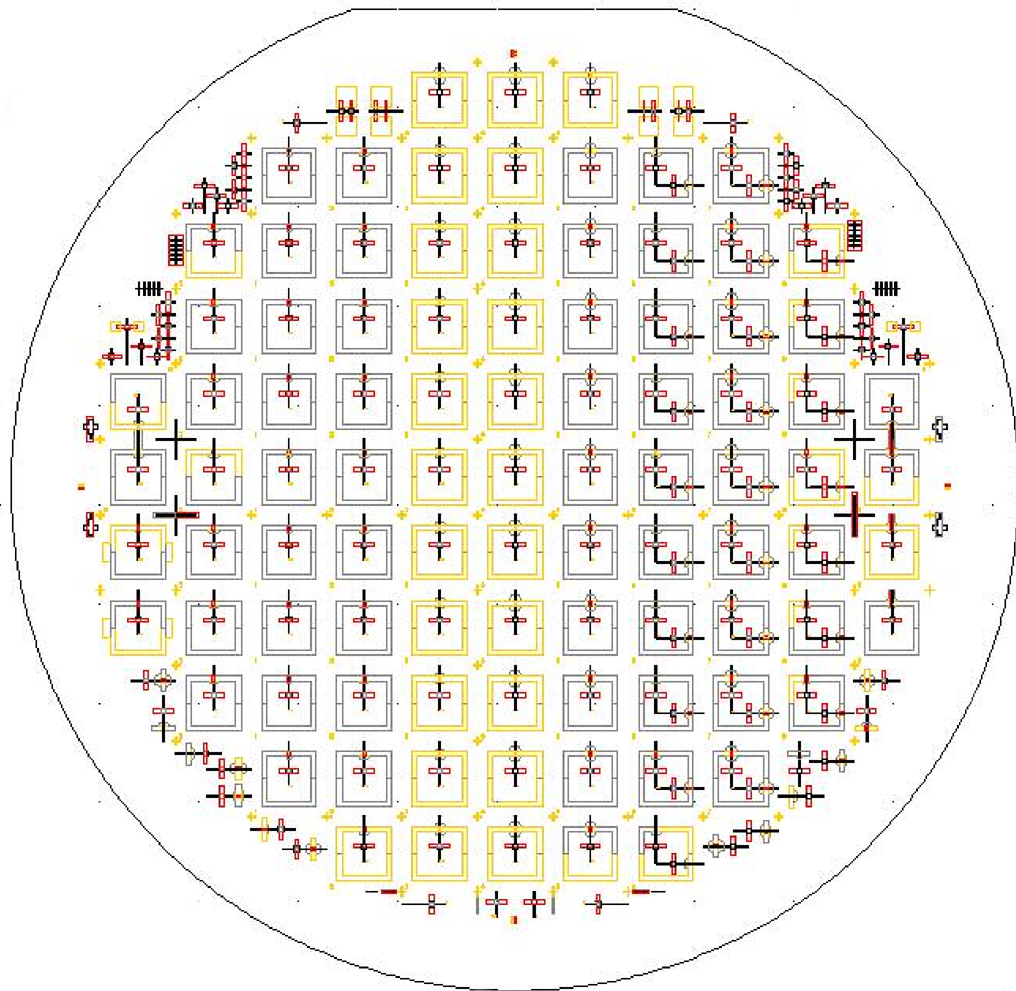
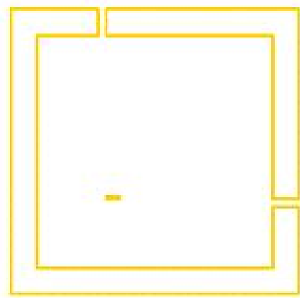


Figure 2-12: DRIE chip-level package layout

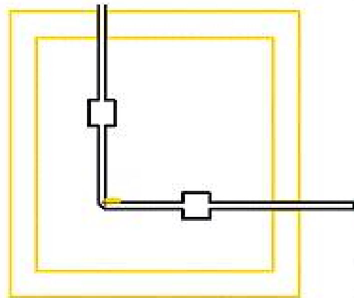
Top chip and bottom chips were fabricated from the same layout. The bottom chips were fabricated in 100 μm silicon and the top chips were fabricated in 25 μm silicon. The layout can be broken down into three general categories. The layout includes single fiber chips, dual fiber chips, and test structure chips. Sixty-six single fiber packages were fabricated per wafer. The single fiber layouts simplify the hermetic sealing process to

allow quicker and more precise assessment of the factors governing the formation of a hermetic seal. Twenty-six dual fiber chips were included in the layout. The dual fiber chips include a reflector to verify the passage of the light bounces off a microstructure to a receiving fiber. The dual fiber chips also provide a convenient monitor of chip status during environmental conditioning. The remaining chips include various test structures to allow for fiber assembly trials as well as metrology structures to assess the fabrication process.

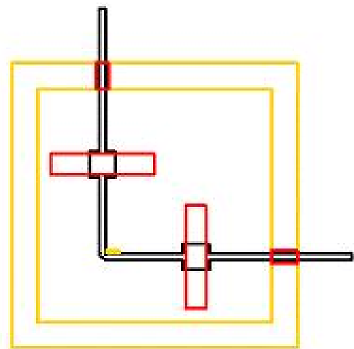
The process flow selected to form the seal ring in depicted graphically in Figure 2-13.



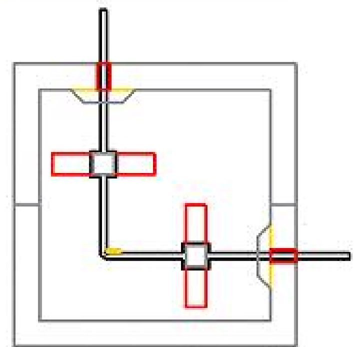
1. Metallization on top mesa (liftoff metal)



2. DRI etch of fiber trenches



3. Completion of seal ring (shadow mask)



4. Solder deposition (2 shadow masks)

Figure 2-13: Process flow to make seal ring

A complete seal ring is not possible with a single shadow mask. Therefore, two masks are required to make the gold seal ring and another two masks are required to make the solder seal ring. A majority of gold seal ring was first completed using a liftoff process. A liftoff process was used for this step since it is already used to define the bond pads for the MEMS S&A. Next, the fiber channels were made using the MEMS S&A DRIE step. Next a shadow mask of adhesion metal and gold was sputtered onto the chip to complete the seal ring and to provide metallization for tacking the fiber in place, Figure 2-14. Finally, the solder is evaporated through a series of shadow masks to complete the solder seal ring and provide solder for tacking of the fiber.

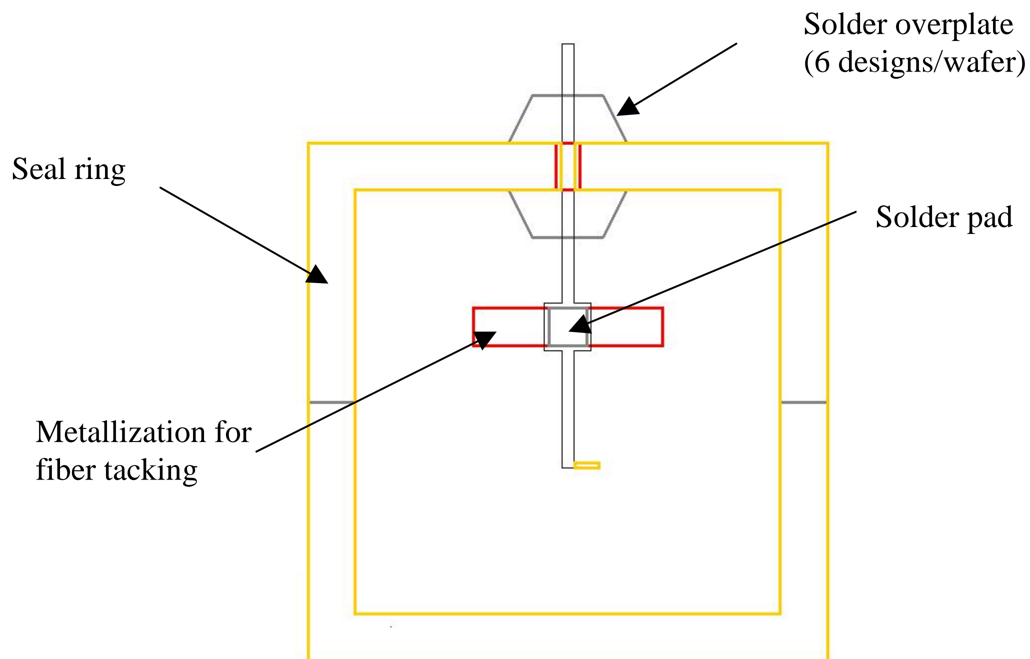


Figure 2-14: DRIE chip-level seal test structure, 1 fiber

The mask to selectively deposit the metallization in the DRI etched channels was iterated to improve sidewall coverage. The primary function of the mask is to prevent the deposition of the metal in unwanted areas. It does, however, provide additional shading of the sidewalls of the high aspect ratio fiber channels. The mask can inhibit the deposition of metal on the sidewalls by reducing the cone of angles that passes through the mask, Figure 2-15.

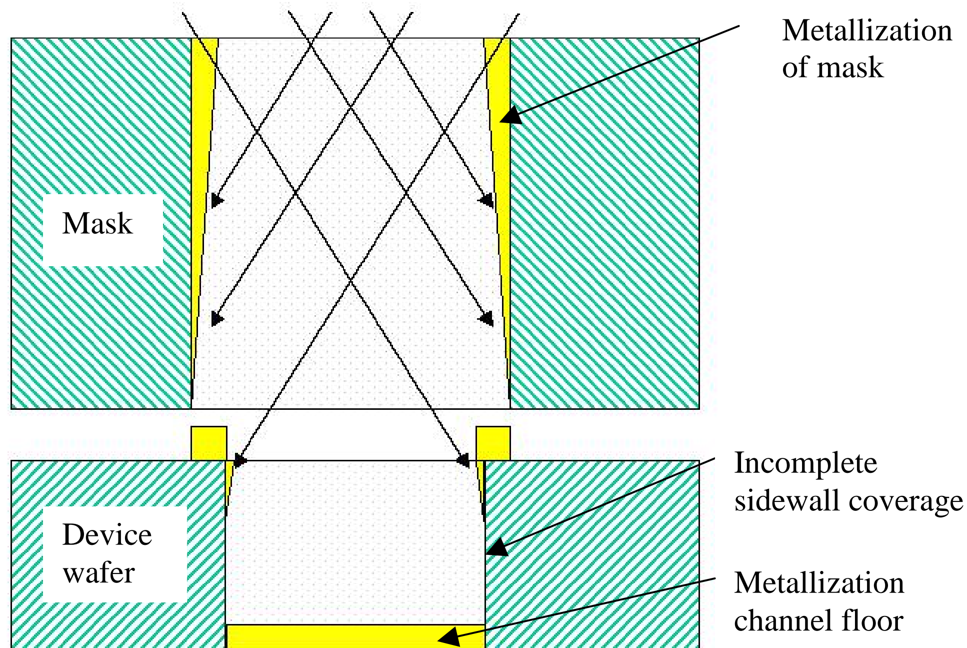


Figure 2-15: Effect of thick mask on sidewall coverage

The mask has to be thick enough to withstand handling, but thin enough not to detrimentally interfere with the sidewall coverage of the device wafer. Initial runs were performed with 600 μm thick DRIE wafer as the mask. The features etched in the DRIE

mask were the same size as the desired features on the device wafer. A small percentage of the metal reached the bottom of the channel, but the sidewalls of the device wafer were not covered at all. The sidewalls of the mask were covered approximately 200 µm down as shown in Figure 2-8.

To cover the 100 µm deep sidewalls in the device wafer with this approach, an alternative masking technique was required. The following masking techniques were identified as alternative methods to deposit metal on the channel sidewalls:

- Thinner DRIE silicon mask
- KOH etched silicon mask
- Thin, more ductile metal mask supported by a DRIE silicon mask
- Two sided DRI etched SOI mask

The thinner 100 µm DRI etched silicon mask was deemed too fragile for handling.

The KOH etched mask was an attractive alternative since the silicon is preferably etched along its crystallographic plane, a 54.7° angle. The slope of the sidewall serves as a relief cut that would lessen the undesirable sidewall shadowing effect. A through hole would still be required. The through hole could be made with a timed KOH etch, but the accuracy would suffer. For improved accuracy, a DRI etch could be used to make the through hole. This approach should be sufficient for this application, but was not pursued due to facility capability mismatch.

A metal mask in beryllium copper could be readily made at JHU/APL. A 50 µm thick beryllium copper layer was etched to form the desired windows for metal deposition and bonded to a 300 µm thick silicon handle wafer layer with larger windows

surrounding the holes in the beryllium copper. As a result, the shadow effect of the mask was limited to the 50 µm thick portion of the mask.

To evaluate the coating of the metal on the sidewall, metrology structures were designed into the layout of the DRIE wafer, Figure 2-16.

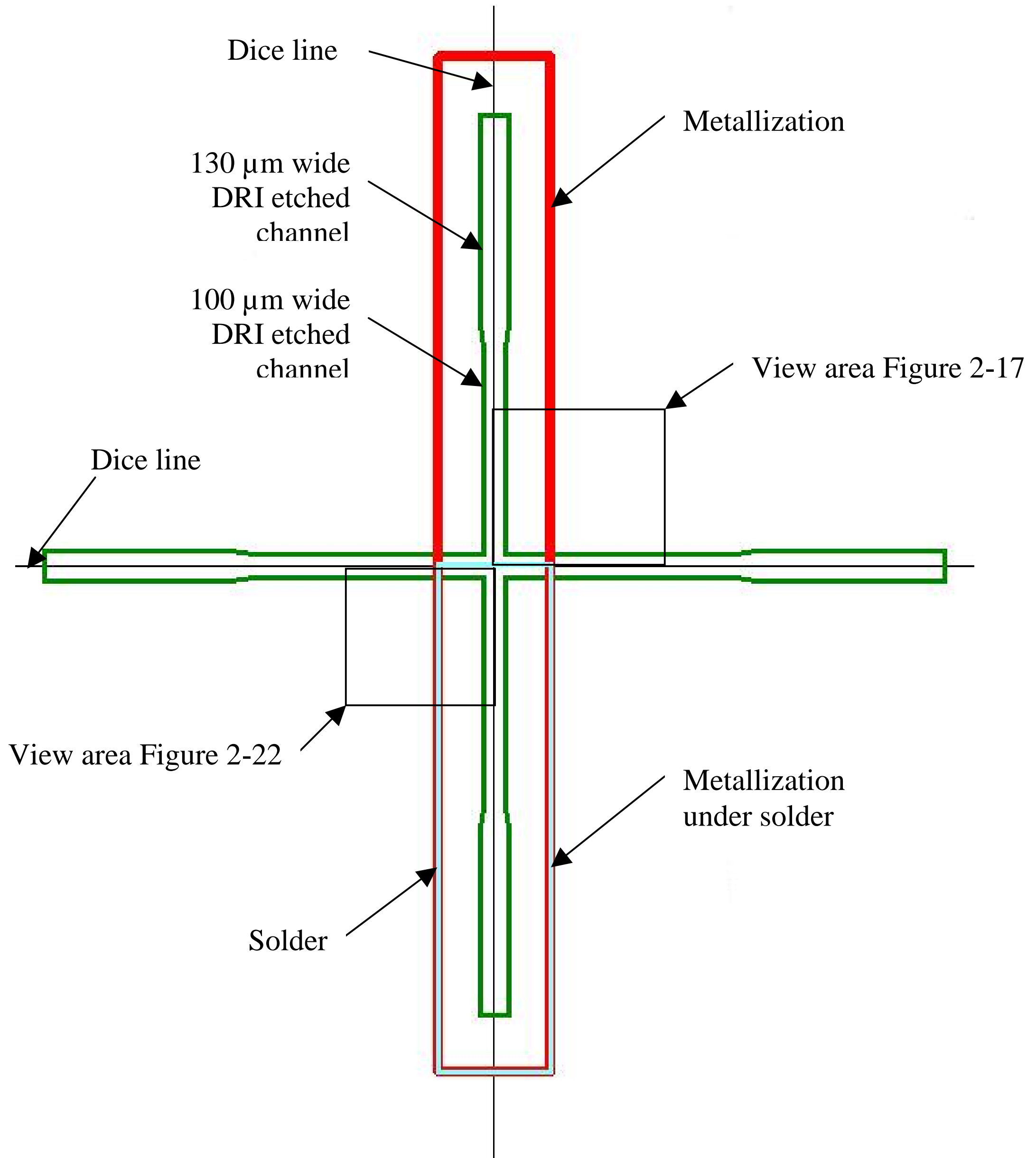


Figure 2-16: DRIE metallization and solder deposition metrology structure

The wafers masked with the beryllium cooper wafer resulted in good sidewall and floor coverage of the etched channels, Figure 2-17.

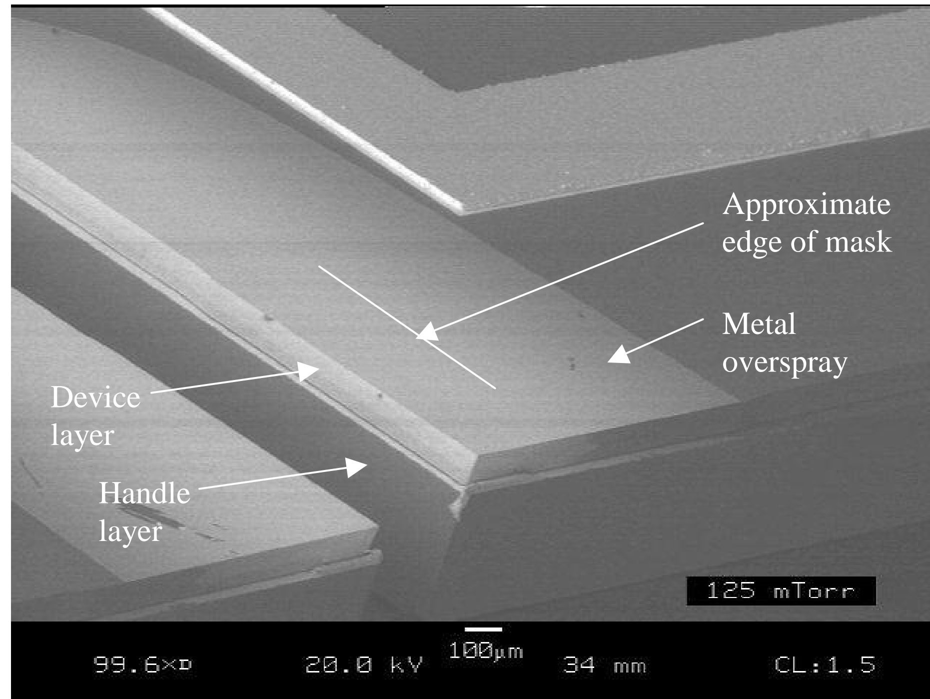


Figure 2-17: Metal coverage of metrology structure (50x)

The metallization width of 250 µm was actually approximately 1mm in this figure due to overspray from the sputtering process. The ductile beryllium copper mask was not perfectly adhered to the silicon handle wafer. As a result, the metallization overspray varied over a wide range, 100 µm to 750 µm. An excellent potential fix for this issue is to use an SOI wafer as a mask. A mask made of SOI would have micron alignment tolerance and excellent adhesion between the two wafers resulting in a more consistent metallization pattern. For this dissertation, the excessive spread of the gold is not an overriding concern, because the focus is to seal the fiber in the grooves and extra metal on the top mesa does not interfere with the performance of the MEMS device.

A closer look of the metrology structure in Figure 2-17 is shown in Figure 2-18.

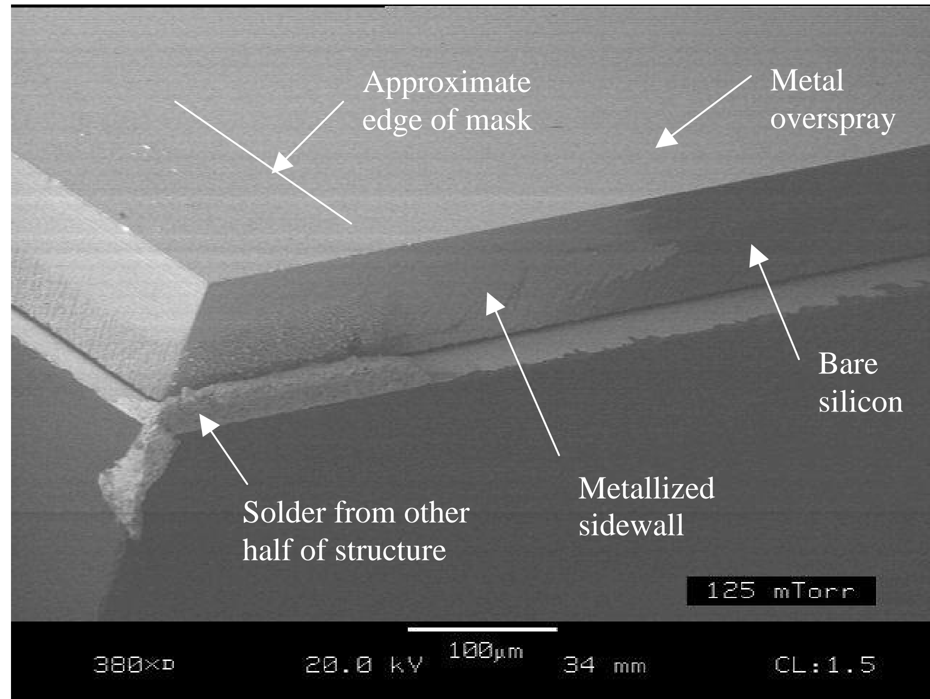


Figure 2-18: Metal coverage of metrology structure (190x)

From this view, the gold on the sidewall can be seen to extend far beyond the area defined by the mask. It is also apparent that the gold covered the sidewall and floor of the channel. Note that the channel width in this section of the structure, 100 µm, is smaller than the fiber channel width, 130 µm. To get a more comprehensive understanding of the sidewall coverage, consider a higher magnification of the metrology stucture, Figure 2-19.

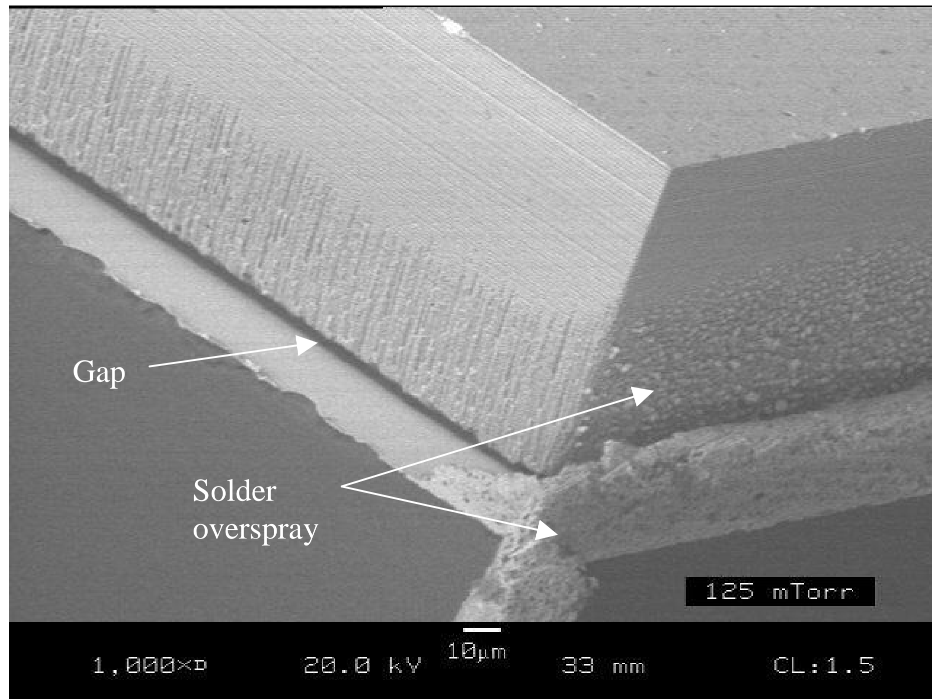


Figure 2-19: Metal coverage of metrology structure (500x)

Here the gold can clearly be seen to cover both the sidewall and channel floors. The surface roughness of the wall on the left half of the image changes significantly approximately half way down the wall. Structures that were analyzed without metallization show a similar pattern, Figure 2-20. Hence the roughness is due to the DRIE processing.

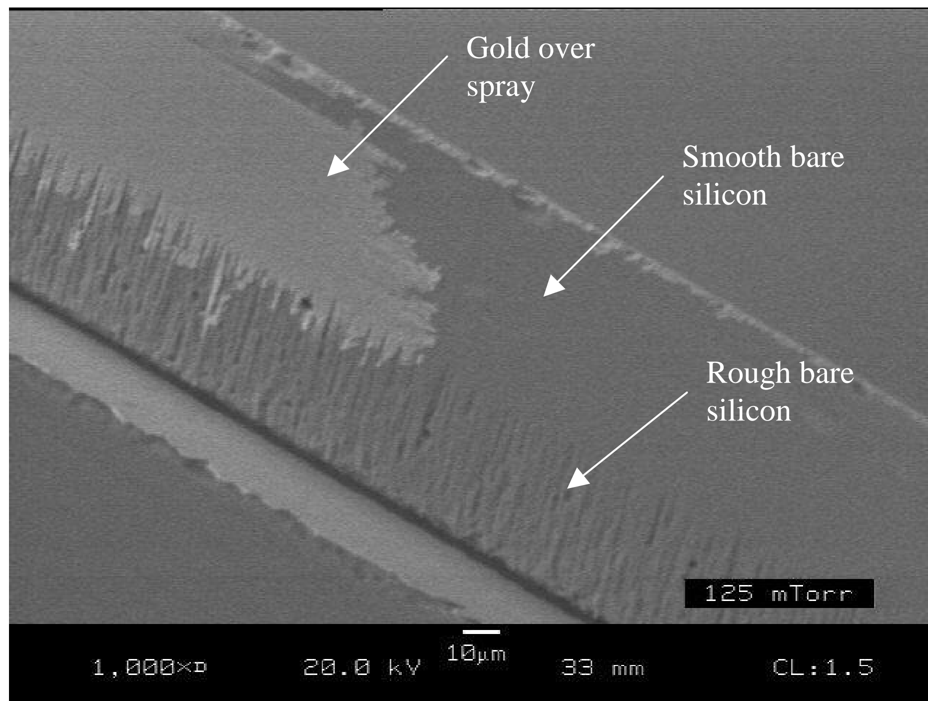


Figure 2-20: Surface roughness of DRIE silicon wall

A gap can be seen between the sidewall and the floor of the channel. This gap is a result of the buried oxide removal during the HF dip. The intent of the HF dip is to remove the field oxide (that is, the oxide that is not covered by silicon). However, the HF dip undercuts the silicon structures. Undercutting is exacerbated by excessive exposure time to the HF. In this case, the undercutting is larger than desired. The 2 µm buried oxide layer was too thick for the metal to bridge, Figure 2-19.

The right wall in Figure 2-19 is also interesting. The wall was splattered with solder that spread beyond the mask definition. Note that the area viewed in Figure 2-19, the upper right quadrant of Figure 2-16, was not intentionally covered with solder.

The deposition of the indium was the next critical step to realize the design goal. Recall that complete coverage of the fiber channels was not critical for this step. With

the metal in place, the solder will flow to selectively wet the metallized areas. Therefore, an evaporative deposition process was sufficient to get indium on the face of the chips. Excess solder was evaporated to provide enough material to completely cover the metallization during reflow. A sputtering process could have also been used. However, indium deposition equipment must be dedicated to indium and a suitable set-up for sputtering was not readily available. A lift off technique was used to remove unwanted indium. This wet process was used for expediency. Future runs could readily be performed with a shadow mask to provide a dry deposition step. The deposition metrology structure with indium in shown in Figure 2-21.

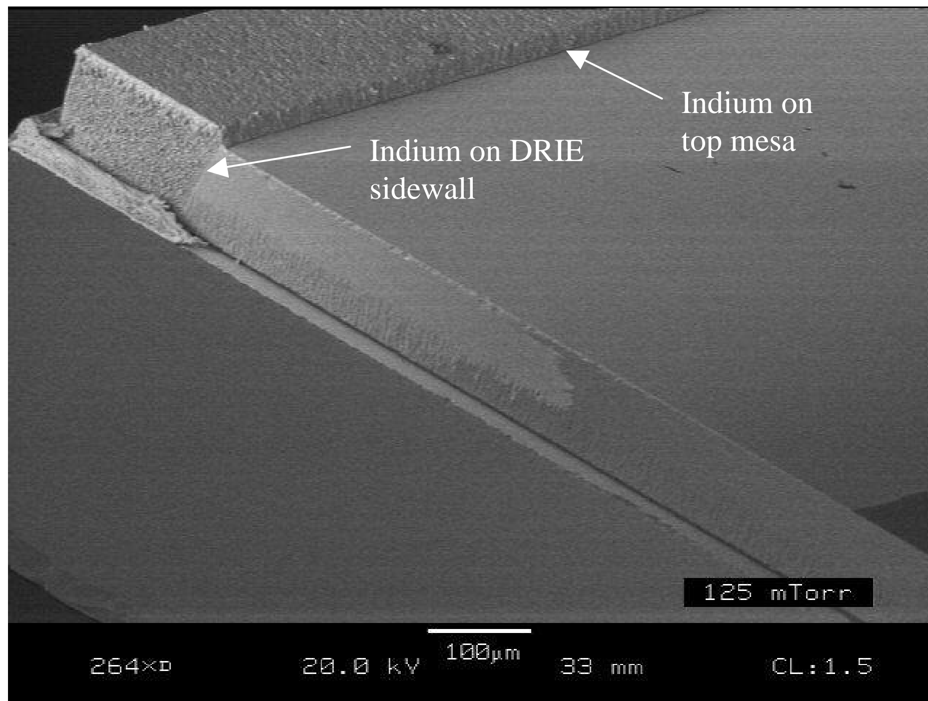


Figure 2-21: Solder coverage of metrology structure (132x)

The view in this figure is looking down the bottom left quadrant of the metrology structure shown in Figure 2-16. A 15 µm thick solder layer can be seen on the top mesa of the chip. The mask for the metallization and the solder were the same geometry. Clearly gold sputtered through the shadow mask spread far beyond the liftoff masked solder on the top mesa of the chip. Again, the gold can also be seen to extend far beyond the mask window on the sidewall.

A higher magnification of the solder in the channel is shown in Figure 2-22.

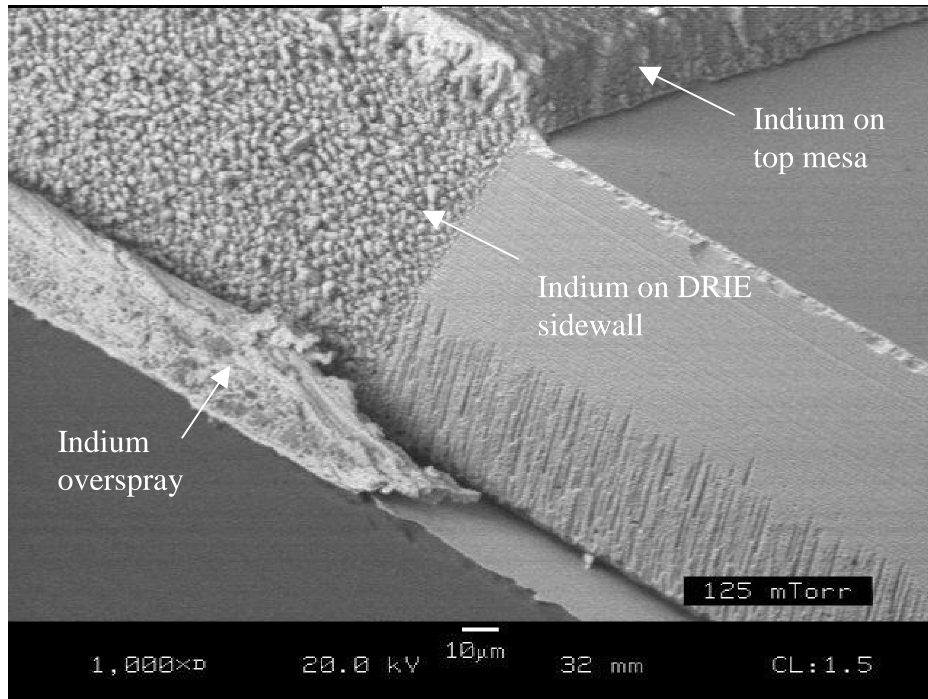


Figure 2-22: Solder coverage of metrology structure (500x)

This view again shows the thick layer of solder deposited on the top mesa. More interesting, the evaporated solder also covered the sidewall. The thickness of the solder on the sidewall is an order of magnitude less than that of the top mesa. This presence of the solder on the sidewall is akin to pre-tinning surfaces before soldering and should

enhance the reflow of the solder during the assembly phase. The evaporation process is considered to be line of sight dependent, so the coating of the sidewall was not expected. The coating may be sufficient to bridge the gap that remained from the buried oxide etch, Figure 2-23.

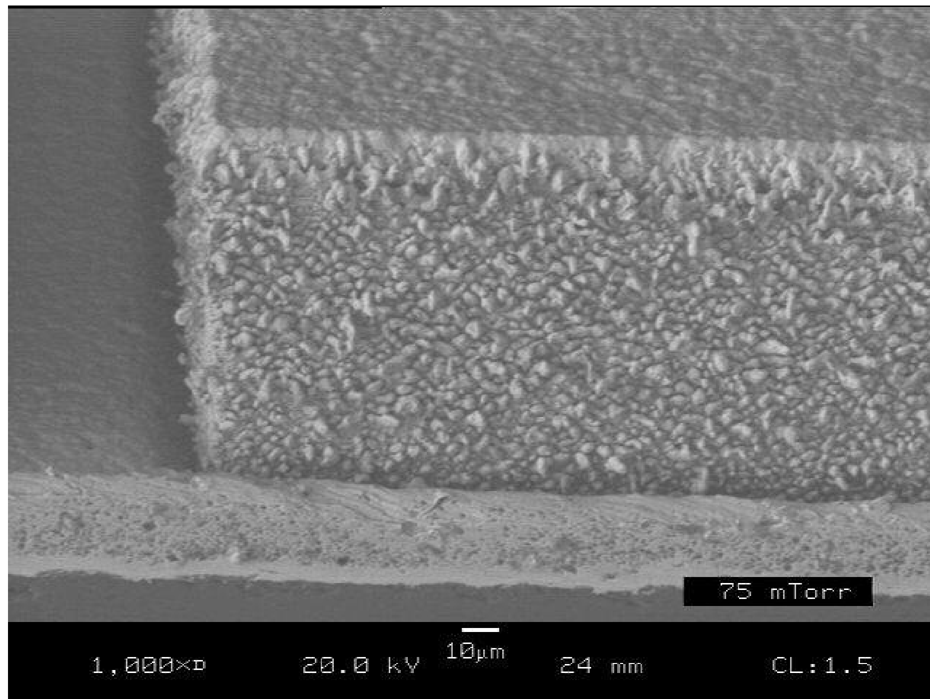


Figure 2-23: Solder coverage of buried oxide gap (500x)

Next, consider the dicing process. A flood coat was used to protect structures during dicing. Alternatively, this wet process could be substituted with a scribe and break technique. A second HF dip to release the parts was not performed in this study, but may be performed early or late in the process flow so long as dry processing is used. The second HF dip is an added complication that is not expected to affect yield and is outside the scope of work of the present effort.

The general process flow to fabricate the seal ring with a fiber channel crossing the seal is as follows:

1. Lift off chrome gold undermetallization to form most of gold ring
2. DRIE at MEMSCAP
3. Wafers sent to JHU/APL
4. HF dip to clean and remove field oxide
5. Sputter chrome gold undermetallization to metallize channels and finish seal ring
6. Evaporate indium
7. Liftoff indium by stripping resist
8. Clean
9. Flood coat for dicing
10. Dice
11. Strip flood coat
12. HF dip (if releasing parts)

2.7 Fluxless soldering

In a traditional soldering process, a flux is used to remove oxides from the solder and the surface metallization in order to allow the solder to wet the undermetallization. Although the fluxes are very effective, they leave behind an organic residue, which can lead to contamination and corrosion inside the package. The residue is typically cleaned with a solvent, which oftn still leaves behind residue and introduces compatibility

questions between the solvent and all other exposed materials. Low residue fluxes, called "no clean" fluxes, have been introduced to the market to eliminate the solvent cleaning step. However, the no clean fluxes still leave behind residue, just less. Cleaning of the flux residue is exceeding more difficult with the presence of the small MEMS structures.

Liquids and organics adversely affect many MEMS. Microstructures that are suspended above the substrate, as is the case with the S&A chip, are prone to stiction related failures when exposed to liquids [85, 86, 87]. Liquid that is introduced into the microstructure area is drawn between the suspended structures and the substrate due to the capillary forces. As the liquid dries, the capillary forces pull the suspended structure to the substrate. Once these two highly polished surfaces come together, the van der Waals forces hold them together in a phenomenon called stiction. The liquid can also act as a vehicle to bring other particulates into the microstructure area. If a liquid is introduced during the packaging process, the device can be supercritically dried [88] or the device may possibly be designed to withstand the capillary forces or to avoid stiction. For the approach here, liquids are not introduced into the microstructure area during packaging. Organics also pose additional reliability concerns concerning the MEMS devices. The organics can out-gas and redeposit in the microstructure area, adversely affecting device performance. Alternatively, the out-gassed species may redeposit on optical surfaces, such as mirrors and fiber faces. Fluxes, clean or no clean, are liquids that leave behind organics. These fluxes are not to be utilized in scenarios where the flux may enter microstructure area. Due to the adverse effects of liquid fluxes, a fluxless soldering process was implemented for the present effort.

Without the aid of a flux to remove the oxides present on the solder and the undermetallization, these oxides must be eliminated through other means. As stated in the previous section, a gold coating is used in this effort to protect the wetable surface from oxidation. The solder can also be coated with gold to protect it from oxidation. Alternatively, the solder can be cleaned of oxides before the soldering process and the atmosphere can be controlled to prevent further oxidation or even to remove oxides that grew after the cleaning process. A nitrogen atmosphere is inert in that it has very little oxygen content and little reaction will take place between the specimen and the atmosphere. Under the right conditions, a reducing atmosphere, such as hydrogen, will react with and remove the oxide from the metal.

The condition for spontaneous reduction of the metal oxide to the base metal can be expressed through the Gibbs free energy. The change in Gibbs free energy is conceptually the maximum energy that can be extracted from a reaction. The change in Gibbs free energy for a reaction at a constant temperature can be expressed by the Gibbs-Helmholtz equation:

$$\Delta G = \Delta H - T\Delta S \tag{2.3}$$

Where ΔG is the change in Gibbs free energy, ΔH is the change in enthalpy, T is the temperature, and ΔS is the change of entropy of a given reaction. A reaction is in thermodynamic equilibrium when the change in Gibbs free energy is zero, $\Delta G = 0$. If the Gibbs free energy is less than zero, the reaction is spontaneous, that is it proceeds to the right without outside intervention. Nonspontaneous reactions need a constant source of

supplied energy to sustain the reaction. Although the Gibbs free energy determines if the reaction is spontaneous, it does not provide information on reaction rates.

Like internal energy and enthalpy, Gibbs free energy is a thermodynamic potential used to characterize reactions. The absolute value of thermodynamic potentials is arbitrary, but the change in the quantity is a property of the compound. In most references and for this work, the thermodynamic properties are referenced to 298K and 1 atmosphere. Gibbs free energy of formation for various materials can be found in thermodynamic reference and textbooks [89] and are reported here for the compounds of interest to the dissertation, Table 2-1.

Table 2-1: Thermodynamic properties of selected compounds (298K, 1 atm, 1 mole)

Substance	Enthalpy of formation, ΔH_f^o (kJ)	Gibbs free energy of formation, ΔG_f^o (kJ)	Entropy (J/K)	Specific heat (J/K)
In_2O_3	-925.79	-830.68	104.2	92
In	0	0	57.82	26.74
O_2	0	0	205.14	29.38
H_2	0	0	130.68	28.82
H_2O (g)	-241.82	-228.57	188.83	33.58

The Gibbs free energy change for a reaction is calculated from the Gibbs free energy of formation of each of the compounds in the reaction.

$$\Delta G^o = \sum_{\text{reactants}} n\Delta G_f^o - \sum_{\text{products}} n\Delta G_f^o \tag{2.4}$$

Where ΔG^o is the change in the Gibbs free energy of the reaction at standard conditions, n is the number of moles of the compound, and ΔG_f^o is the Gibbs free energy of

formation of the compound at standard conditions. The Gibbs free energy can be calculated at elevated temperatures using (2.3) provided that Gibbs free energy of formation of each of the products and reactants are available at the temperatures of interest. This is often the case for common compounds, such as H_2 and O_2, but is not the case for less common compounds like indium or indium oxide. To obtain the Gibbs free energy for a reaction at temperatures other than standard, first substitute (2.3) into (2.4) to obtain an expression in terms of temperature, enthalpy, and entropy.

$$\Delta G = \sum_{\text{products}} n\Delta H - \sum_{\text{reactants}} n\Delta H - T\left(\sum_{\text{products}} n\Delta S - \sum_{\text{reactants}} n\Delta S \right) \tag{2.5}$$

The enthalpy and entropy change due to temperature change can be accurately approximated by the following relations:

$$\Delta H = C\Delta T \tag{2.6}$$

$$\Delta S = C \ln\left(\frac{T_2}{T_1} \right) \tag{2.7}$$

where C is the specific heat, ΔT is the change in temperature, T_2 is the temperature final temperature, and T_1 is the initial temperature.

Consider the reduction of indium oxide, which can be expressed by the following reaction.

$$2In_2O_3 \Leftrightarrow 4In + 3O_2 \tag{2.8}$$

The Gibbs free energy for the above reaction can be expressed as:

$$\Delta G^o = -2\Delta G_f^o In_2O_3 \tag{2.9}$$

The Gibbs free energy change for the reduction of indium oxide reduces to the Gibbs free energy of formation for indium oxide because the other terms go to zero. Equation (2.9) was derived based on a reaction involving two moles of indium oxide. Typically values for Gibbs free energy are reported on a per mole basis. For consistency, the reduction of indium oxide can be expressed on a per mole basis as:

$$\Delta G^o = -\Delta G_f^o In_2O_3 \tag{2.10}$$

The Gibbs free energy for the indium reduction equation at elevated temperatures can be obtained by expressing (2.5) in terms of the reaction in (2.8) with

$$\begin{aligned}\Delta H = {} & 4(H_f(In) + C(In)\Delta T) + 3(H_f(O_2) + C(O_2)\Delta T) - \\ & 2(H_f(In_2O_3) + C(In_2O_3)\Delta T)\end{aligned} \tag{2.11}$$

$$\begin{aligned}\Delta S = {} & 4\left(S(In) + C(In)\ln\left(\frac{T_2}{T_1}\right)\right) + \left(S(O_2) + C(O_2)\ln\left(\frac{T_2}{T_1}\right)\right) + \\ & \left(S(In_2O_3) + C(In_2O_3)\ln\left(\frac{T_2}{T_1}\right)\right)\end{aligned} \tag{2.12}$$

Having established a method to calculate Gibbs free energy at various temperatures, the parameters to establish the thermodynamic conditions for the oxide reduction can be established. This can be graphically depicted using an Ellingham diagram. The Ellingham diagram for the oxidation/reduction of tin and indium oxides is shown in Figure 2-24. The tin reaction was included in this diagram due to related efforts in fluxless soldering using tin as well as indium-based alloys.

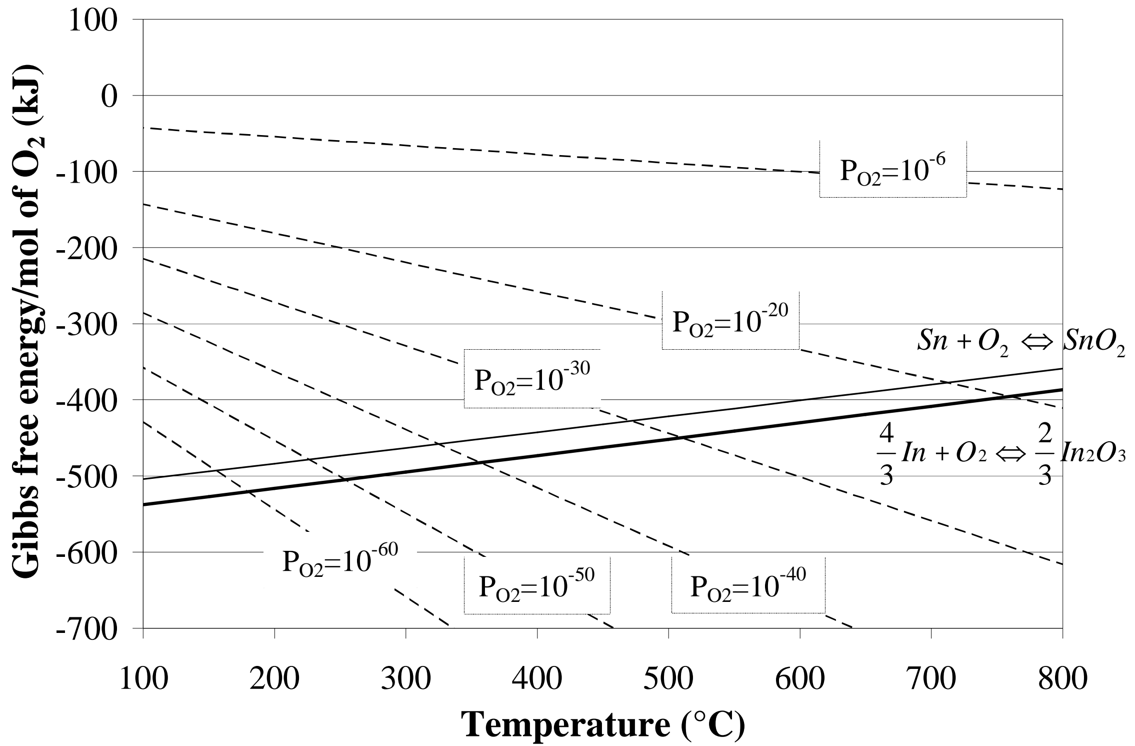


Figure 2-24: Ellingham diagram for indium and tin oxide reduction

The Ellingham diagram is useful in visualizing the conditions needed for a reaction to be thermodynamically favorable. The solid curves are plots of the Gibbs free energy for the reactions of indium with oxygen and tin with oxygen. The dotted lines are the oxygen partial pressure curves for the reduction of the oxide. The decomposition pressure for the oxide can be calculated from the following relationship:

$$\Delta G = RT \ln(K_p) \tag{2.13}$$

where R is the universal gas constant, T is the temperature, and K_p is the equilibrium constant for the reaction. K_p is the ratio of the partial pressure of the products raised to the power of the number of moles of each product in the reaction to the partial pressure of

the reactants raised to the power of the number of moles of each product in the reaction. For the case of indium oxide, K_p can be expressed by:

$$K_p = \frac{P_{O_2}{}^3 P_{In}{}^4}{P_{In_2O_3}{}^2} \quad (2.14)$$

Since indium and indium oxides are solids, (2.12) reduces to:

$$K_p = P_{O_2}{}^3 \quad (2.15)$$

Equation (2.15) is written for a reaction with three moles of O_2. The values reported for Gibbs free energy are typically supplied per mole of oxygen, (2.4) and thus (2.14) could have been written to reflect this, but was not for the sake of simplicity. With that in mind (2.14) can be rewritten assuming that only 1 mole of oxygen is present in the reaction:

$$K_p = P_{O_2} \quad (2.16)$$

Written in this form, the equation is valid for the reduction of all metal oxides. Substituting (2.16) into (2.13).

$$\Delta G = RT \ln(P_{O_2}) \quad (2.17)$$

Equation (2.17) can be used to calculate the decomposition pressure.

$$P_{O_2} = e^{(\Delta G / RT)} \quad (2.18)$$

Alternatively, the decomposition pressure can be viewed graphically via (2.17). The family of curves from (2.17) are plotted as dotted lines in the Ellingham diagram. Normalized to one mole of O_2, these curves are independent of the metal oxide reaction. The intersection of the Gibbs free energy curve for the reaction and the partial pressure curve determines the equilibrium condition for the reaction. In other words, the

intersection of the two curves represents the disassociation temperature and pressure for the reaction. Temperature and pressure below this intersection are favorable to reducing the oxide. Conversely, temperature and pressure above this point are favorable to oxidizing the metal. From the Ellingham diagram, it is clear that the reduction of the oxide is more favorable as the temperature is increased and as the oxygen partial pressure is reduced. Also, note that the tin oxide is more readily reduced than indium oxide.

There are practical limitations to both the maximum process temperature and the minimum oxygen partial pressures. The disassociation temperature and oxygen partial pressure required to reduce indium oxide are summarized in Table 2-2.

Table 2-2: Disassociation temperature and pressure of indium oxide

Temperature (°C)	Partial Pressure O_2 (-)
25	$1.2x10^{-97}$
100	$6.4x10^{-76}$
200	$1.2x10^{-57}$
300	$9.0x10^{-46}$
400	$2.1x10^{-37}$
500	$3.3x10^{-31}$
600	$2.0x10^{-26}$
700	$1.3x10^{-22}$
800	$1. 6x10^{-19}$
900	$6.0x10^{-17}$
1000	$8.8x10^{-15}$

For the case of indium, the oxygen partial pressure must be below 10^{-37} for the reduction of oxides to be thermodynamically favorable at 400°C. Oxygen partial pressure of this order of magnitude is not achievable in most industrial or laboratory environments. Oxygen free nitrogen gas bottles are typically only guaranteed to have oxygen content below 10^{-6} atmospheres. It is worth mentioning that the reduction can take place at more modest levels than predicted by the Gibbs free energy due to other factors, such as dissolution of the oxide into the molten metal. However, such an environment favors oxidation and much greater care is needed to prohibit excessive oxide formation.

Reducing indium oxide in an inert environment is not practical. However, using a reducing gas, such as hydrogen, is a viable method for scrubbing oxides from metals if the activation energy is low enough and high process temperatures are acceptable. The hydrogen reacts with the ambient oxygen to form water vapor:

$$2H_2 + O_2 \Leftrightarrow 2H_2O \quad (2.19)$$

The Gibbs free energy for reaction of hydrogen and oxygen to form water vapor can be calculated from thermodynamic steam tables using (2.3). The equilibrium constant can then be calculated from (2.13). The equilibrium constant can then be used to find the amount of hydrogen necessary to obtain the desired partial pressure of oxygen.

The equilibrium constant for the reaction in (2.19) can be expressed as:

$$K_p = \frac{P_{H_2O}{}^2}{P_{H_2}{}^2 P_{O_2}} \quad (2.20)$$

Rearranging to solve for the partial pressure of oxygen:

$$P_{O_2} = \frac{P_{H_2O}{}^2}{P_{H_2}{}^2 K_p} \quad (2.21)$$

For the case of a reducing environment, the partial pressure of the oxygen can be reduced by increasing the ratio of hydrogen to water vapor in the reflow environment. Increasing the temperature, which increases the equilibrium constant, can also lower the partial pressure of oxygen. The effects of temperature on the reaction constant and ratio of hydrogen to water vapor needed to reach the disassociation pressure of oxygen to reduce indium and tin oxide in summarized in Table 2-3.

Table 2-3: Ratio of hydrogen to water vapor for thermodynamically favorable reduction of indium oxide and tin oxide

Temperature	Disassociation Pressure, P_{O2}		Equilibrium constant, K_p	$\frac{P_{H_2}}{P_{H_2O}}$ for oxide redux	
	Indium	Tin		Indium	Tin
(°C)	(atm)	(atm)			
100	$1.0x10^{-76}$	3.0×10^{-71}	1.5×10^{64}	324,388	1,506
150	1.0×10^{-65}	1.2×10^{-61}	3.6×10^{55}	52,117	485
200	1.2×10^{-57}	4.5×10^{-54}	1.6×10^{49}	7,388	119
250	3.8×10^{-51}	6.0×10^{-48}	6.5×10^{43}	2,022	51
300	$9.0 \times 10^{--46}$	$7.0 \times 10^{--43}$	3.6×10^{39}	554	20
350	3.0×10^{-41}	1.2×10^{-38}	7.3×10^{35}	216	11
400	2.1×10^{-37}	5.1×10^{-35}	6.6×10^{32}	86	5
450	4.3×10^{-32}	6.8×10^{-32}	1.3×10^{30}	42	3
500	3.3×10^{-31}	3.5×10^{-29}	6.5×10^{27}	21	2

A typical bottled gas containing 5% H_2 and 95 % N_2 will has a frost point of –70°C. This corresponds to 0.0002% water vapor content and thus hydrogen to water vapor ratio of 25,000. According to the above analysis, the hydrogen reducing gas appears to be a viable method to reduce the oxides from the indium or tin. However, the above analysis assumes that the entire chamber is at the elevated temperature. In the

present effort, the heat is applied by a hot plate. In the final design, the intent is to use a localized heating technique to obtain the solder reflow. Without using a globally heated environment, there will exist a large temperature gradient in the air surrounding the solder sample. This will lead to a convective recirculation zone and entrain oxygen to the solder sample. For the oxygen in the ambient environment to reduce oxide to a level for fluxless soldering of indium, the surrounding temperature must be approximately 200°C.

From the above thermodynamic analysis, the fluxless soldering of indium appears to be feasible. While the above analysis provides an important understanding of the factors that govern the fluxless soldering process, it also serves as a worst case bound of the process environment requirements. Other factors, such as oxide dissolution, further support the viability of a fluxless soldering process. In fact indium can be bonded to itself without reflow using a room temperature cold weld. At elevated temperatures, indium may be bonded, with pressure, in the presence of oxides. The pressure acts to break the solid oxide and then allows the molten indium to wet the under metallization. This can lead to conglomerations of oxides in the joint and also inhibits the surface tension flow desired. However, if the oxide layer is sufficiently thin, pressure is not needed to pierce the oxide layer. In this case, the oxide is dissolved into the joint and does not impede the flow of the solder. With the understanding of the governing thermodynamics, the cleaning and the reflow environment can be selected to prevent excessively thick oxide layer formation. In the soldering process employed here, the reducing environment does not necessarily reduce the indium oxides, rather it need only slow down the oxidation reaction such that the oxide can be dissolved into the joint

allowing the solder to flow to its minimal energy state. Molten indium readily dissolves up to 20 Å of indium oxide at 210°C [65].

Cleaning can remove the native oxides from the solder. After this oxide reduction, the sample will begin to grow an oxide layer when exposed to oxygen. The thickness of the oxide layer is primarily dependent on the exposure temperature and time of the metal to oxygen. Higher temperatures and longer exposure time result in a thicker oxide layer.

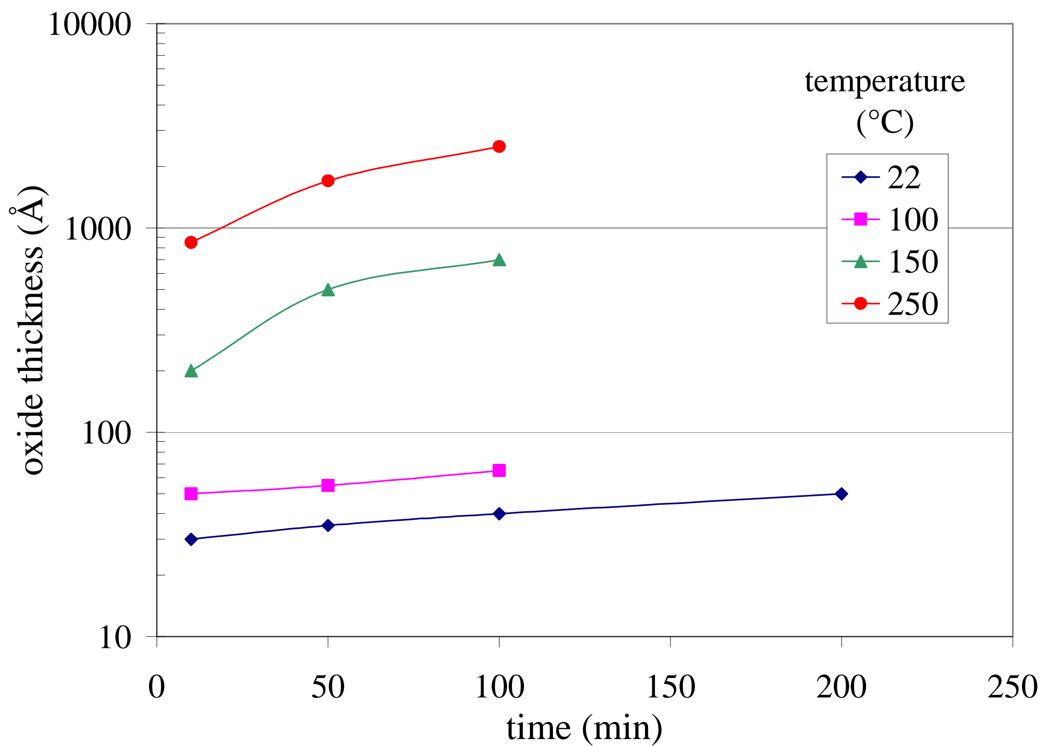


Figure 2-25: Indium oxide layer thickness growth on InSn film as a function of exposure temperature and time to ambient oxygen, adapted from Kuhmann [67]

The indium has a tendency to self-passivate, limiting the growth of the oxide film. The Pilling-Bedworth equation is used to quantify the passivation quality of metal [90]:

$$P\text{-}B = \frac{(M_{oxide})(\rho_{metal})}{n(M_{metal})(\rho_{oxide})} \tag{2.22}$$

where *P-B* is the Pulling-Bedworth ratio, *M* is the molecular weight, ρ is the density, and *n* is the number of metal atoms in the oxide. The data used to calculate the *P-B* for indium is summarized in Table 2-4 [91].

Table 2-4: Material property data for indium and indium oxide

Material	Molecular weight (g/mol)	Density (g/cm^3)
In	114.8	7.31
In_2O_3	277.6	7.18

The *P-B* ratio for indium calculated from (2.22) and values listed by West [92] are listed in Table 2-5.

Table 2-5: Pilling-Bedworth ratio for indium and selected common metal oxides

Material	*P-B* ratio
In-In_2O_3	1.2
Al-Al_2O_3	1.3
Ti-TiO_2	1.5
Fe-Fe_2O_3	2.1

With *P-B* ratio of 1, the volume of the metal and the metal oxide are identical and thus little stress is incurred. Oxides with a P-B ratio below 2 are typically passivating. Oxides with a P-B ratio above 2 typically flake and allow further oxidation of the exposed metal.

The *P-B* ratio of indium is closer to 1 than titanium and aluminum, materials often used in applications where oxidation resistance is important.

2.8 Cleaning

The solder samples must be cleaned prior to reflow. Organic matter that may have inadvertently been deposited onto the solder must be removed. In addition, the oxide layer that naturally forms on the metal must be removed to achieve a reliable solder joint. For the surface tension driven solder flow process, further emphasis on oxide removal is necessary to allow free movement of the solder. The indium oxide that forms on the solder has a much higher melting point (1900°C) than the indium solder and forms solid films on the molten solder that prevents solder movement.

The samples can be wet or dry cleaned. For MEMS applications, dry clean is preferred. A March PLASMOD plasma cleaner was installed in the Indian Head clean room for the removal of both organics and oxides. Oxygen plasma, which acts chemically, effectively removes organics from indium. Argon plasma, which acts physically, effectively removes oxides from indium. The cleaning process can elevate the temperature of the sample. Introduction of oxygen to the sample at this elevated temperature can create a thicker, more tenacious oxide layer than existed before the cleaning process began. To prevent oxide excessive formation, the plasma cleaner was modified to substitute inert gas for air during the purge cycle upon completion of cleaning. The plasma cleaning process requires a balance between power, gas partial

pressure, and exposure time to achieve the oxide free surface without elevating the temperature of the solder to the point of reflow. The use of argon plasma to remove oxides for fluxless soldering has been demonstrated [93]. Since the dry cleaning process has already been demonstrated, the tuning of this process was not emphasized for this effort.

Wet cleaning was used as an expedient method to reliably clean non-MEMS test structures. In addition, the wet cleaning eliminates several variables, such as sample temperature rise during cleaning, inherent in the dry cleaning process. Hence, the wet cleaning process provided a quick, consistent, room temperature cleaning process. The following cleaning schedule was used for wet cleaning:

1. Soak in acetone for 10 minutes.
2. Soak in 10% hydrochloric acid solution for 10 minutes.
3. Thoroughly rinse twice in isopropyl alcohol.
4. Rinse with acetone.
5. Dry thoroughly with inert gas.

2.9 Heat application and assembly

For samples that required manipulation during assembly (e.g., packages with fibers), the soldering process was performed in a glove box to allow control over the solder environment while still allowing for manual manipulation of the hardware. For the

assembly of the fibers, the glove box approach provides the greatest flexibility in handling and aligning the hardware.

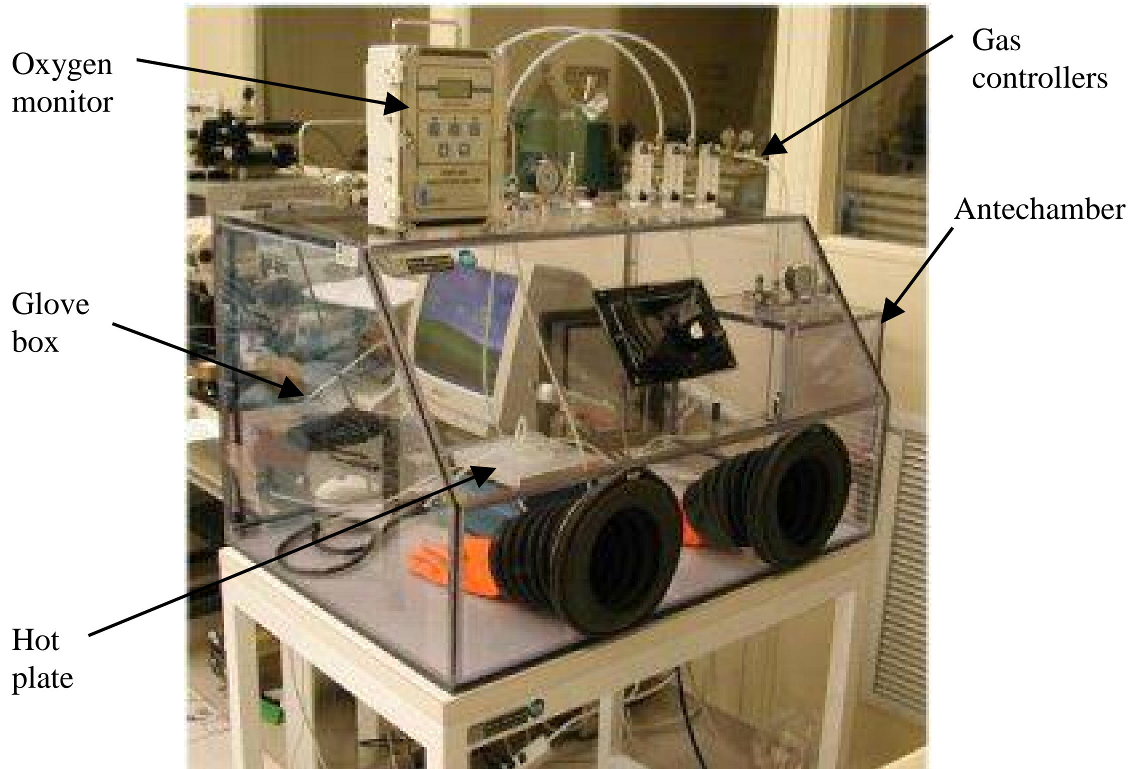


Figure 2-26: Glove box set-up for reflow

The glove box used to perform the research in this dissertation, a Terra Universal model 200, is shown in Figure 2-26. The glove box requires a several hour purge at 5SCFH of an oxygen free gas to get the oxygen content below 1000 ppm. A port was machined into the top of the housing to provide a connection to an oxygen sensor. The oxygen analyzer, an Alpha Omega Instruments series 3000, was configured to measure oxygen content below 1000 ppm with a resolution below 0.1 ppm in the 10 ppm range. The glove box was also outfitted with two process gas ports, one for nitrogen and one for the hydrogen reducing gas. The chamber is equipped with an antechamber to allow pass

through of hardware without compromising the environment of the glove box. Another port was machined into the back of the glove box to allow a USB cable feed through to enable the installation of a digital microscope inside the glove box, Figure 2-27.

For most of the present study, heat was typically applied using a programmable hot plate. The hotplate, a Barnstead Dataplate series 730, was installed inside the glove box, Figure 2-27.

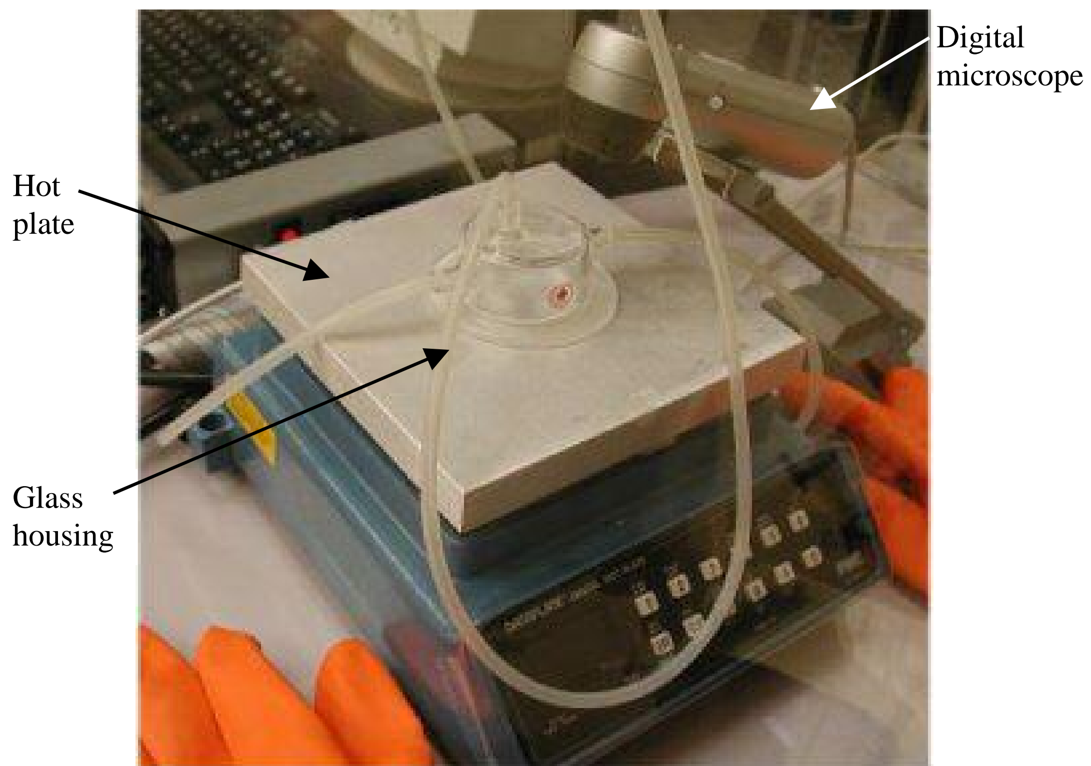


Figure 2-27: Programmable hot plate with reflow housing

The hot plate has a 6-inch square stage capable of achieving 400°C. In cases that the hot plate was not used, a localized Joule heating technique was used to reflow the solder. The entire environment heated was not heated during this study.

For studies that did not involve complex assembly, the soldering was performed using a glass housing with an aluminum base on a programmable hot plate, Figure 2-27. The base of the housing was made of aluminum for good thermal coupling between the solder coupon and the fixture. The glass housing allowed for rapid control of the reflow environment and is optically clear to allow *in-situ* monitoring of the soldering process with a digital microscope. The glass housing has three ports. One port was available for vacuum, a second port for process gas inlet, and the final port for a gas monitor. The process gas was plumbed through one of the side ports to allow the reducing gas or nitrogen to blanket the sample. The flow rate was typically set to approximately 10 cubic feet per hour (SCFH) initially to purge the chamber then lowered to 5 SCFH during reflow to reduce airflow effects. The top port was connected to the oxygen analyzer for measurement of the environment purity. It was determined that the environment inside the glass chamber stabilized within 10 minutes without the use of a vacuum, so this port was not used for most of the present work.

Experiments were performed to determine the best way to apply the heat to the sample while using the hot plate. Samples were placed in the glass fixture and sealed then placed on a cold hot plate. Then the hot plate was heated to the process temperature. Alternatively, the sample was placed in the glass fixture and was then loaded onto the hot plate already at the process temperature. The effects of process temperature were also addressed through process variations and evaluation of the reflowed solder. Although the indium reflows at 160°C, the hardware is brought up to temperatures as great as 400°C to

allow for rapid rise in temperature to prevent the growth of the oxide layer in the environment that is potentially thermodynamically favorable to oxidation of the solder.

To assemble chips together, a fixture was made to provide alignment between the chips. A typical alignment fixture, Figure 2-28, used in the present effort features relief cuts in the corners and posts for tweezers interface.

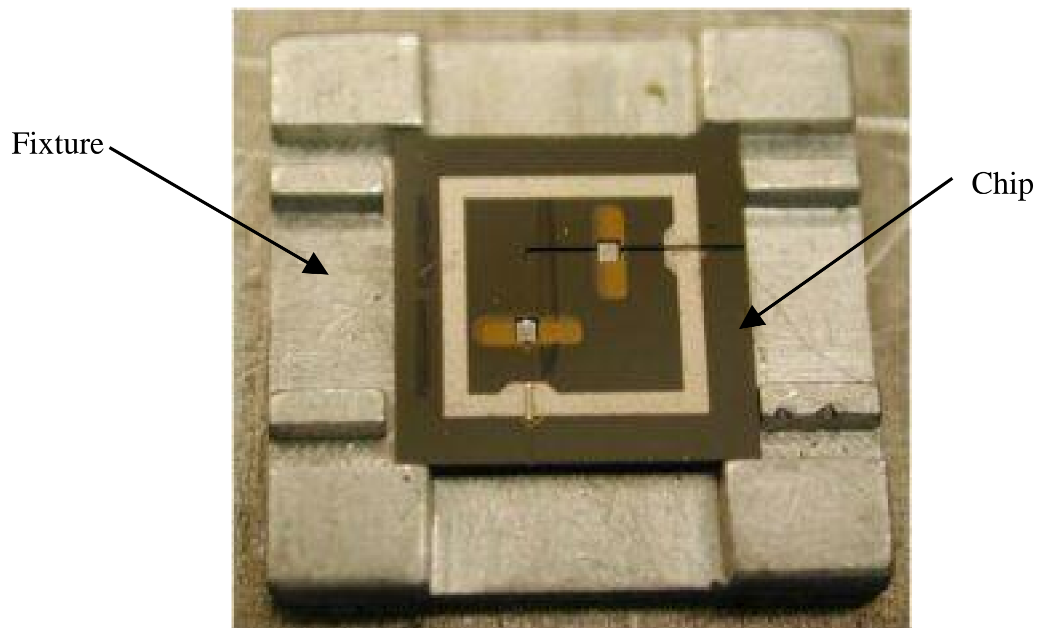


Figure 2-28: Chip alignment fixture

The top chip protrudes from the top of the fixture to allow placement of a weight when needed. For chip assemblies involving fibers, the bottom chip was placed in a fixture to provide an approximate location. The fiber is laid in the groove of the bottom chip and can be tacked in place by localized reflow of the solder or via a small quantity of adhesive. For the present effort the exact fiber position was not critical, so the fibers were not necessarily fixed in the groove prior to final reflow.

2.10 Leak rate of gases

In this section the technique used to evaluate the hermeticity of IC packages is studied to assess its applicability to small volume MEMS packages. In addition, the moisture ingress rates are studied to define the level of protection required to ensure a condensate free package throughout its life. The influence of the leak path geometry on leak rate is also presented.

2.10.1 Military standard for hermetic seal evaluation

A hermetic seal can be conceptually thought of as being impervious to moisture. MIL-STD-883 provides a quantitative definition and measurement technique for validating a hermetic seal [94]. The protocol specified in MIL-STD-883 requires that the package first be exposed to pressurized helium for several hours to force helium into the package. The package is then transferred to a mass spectrometer where the helium leak rate from the package can be detected. Helium was selected as the detection gas due to its small molecular size, inertness, and ease of detection. Test method 1014.10 of MIL-STD-883 requires the measured leak rate of helium not to exceed a specified value, typically 5 x 10^{-8} atm-cm^3/s, when the package is exposed to specified conditions. The conditions for the leak test vary depending on package internal volume and test method used. The acceptable leak rates as defined by MIL-STD-883 for the fixed test method (test condition A_1) are reported here for reference, Table 2-6.

Table 2-6: MIL-STD-883 fine leak test rejection criteria for selected package volumes (Test method 1014.1 test condition A_1)

Package volume, V (cm^3)	Bomb condition			Reject limit, R_1 (atm-cm^3/s He)
	Pressure, P_E (psia)	Minimum exposure time, t_1 (hours)	Maximum dwell time, t_2 (hours)	
<0.05	75	2	1	5×10^{-8}
0.05 to <0.5	75	4	1	5×10^{-8}
0.5 to <1.0	45	2	1	1×10^{-7}

Alternatively, a flexible method can be used (test condition A_2) and can result in the acceptance of a package that was rejected under the fixed test method. Under the flexible method, the test coordinator can select the bombing parameters, which are input into a formula to calculate the acceptable standard leak rate. If the fixed parameters are used in the flexible formula, the acceptance level is generally more lenient for the flexible method. For this dissertation, only the more stringent fixed method will be considered in analyzing the acceptable leak path size.

The true leak rate is defined in the literature from the reference point of a "pure" gas at one atmosphere of pressure inside the package. In measuring the leak rate from a package, it is difficult to directly measure the true leak rate, which would require that the measurement be performed with 1 atmosphere of helium inside the package. The amount of helium that enters the package during the bombing phase is not typically directly measurable. Furthermore, it is not possible to quantify the amount of helium that leaks from the package between the bombing and detection phases of leak testing. As a result, there exists a discrepancy between the true leak rate and the measured leak rate. The measured leak rate and the true leak rate are related as follows:

$$L_{gas} = \frac{R_{gas}}{pp_{gas}} \quad (2.23)$$

where L_{gas} is the true leak rate of the gas, R_{gas} is the measured leak rate of the gas, and pp_{gas} is the partial pressure of the gas inside the package. The true leak rate expressed in terms of air, termed the standard leak rate, can be calculated from the Howel-Mann equation [95].

$$R_m = \frac{L_{air} P_E}{P_o} \left(\frac{M_A}{M} \right)^{0.5} \left(1 - e^{\frac{L_{air} t_1}{V P_o} \left(\frac{M_A}{M} \right)^{0.5}} \right) \left(e^{\frac{L_{air} t_2}{V P_o} \left(\frac{M_A}{M} \right)^{0.5}} \right) \quad (2.24)$$

where

R_m is measured leak rate

L_{air} is the equivalent leak rate of air, termed standard leak rate

P_E is the exposure pressure of helium

P_o is the atmosphere pressure

M_A is the molecular weight of air

M is the molecular weight of the tracer gas, helium

t_1 is the exposure time in seconds

t_2 is the dwell time between pressure exposure and leak detection

V is the internal volume of the package

Substituting for atmosphere pressure (1 atm) and the molecular weight of helium (4g) and air (28.7g), The Howell-Mann equation reduces to:

$$R_m = 2.679 L_{air} P_E \left(1 - e^{-2.679 L t_1 / V} \right) \left(e^{-2.679 L t_2 / V} \right) \quad (2.25)$$

The true leak rate of helium can be calculated from the standard leak rate using the following relation:

$$\frac{L_1}{L_2} = \sqrt{\frac{M_2}{M_1}} \tag{2.26}$$

where L_1 and M_1 is the leak rate and molecular weight of gas 1 and L_2 and M_2 is the leak rate and molecular weight of gas 2. From (2.26), the true leak rate of helium can be expressed in terms of the standard leak rate:

$$L_{He} = 2.679 L_{air} \tag{2.27}$$

Substituting (2.27) into (2.25) yields a relationship between the measured leak rate and the true helium leak rate:

$$R_m = L_{HE} P_E \left(1 - e^{-L_{HE} t_1 / V}\right)\left(e^{-L_{HE} t_2 / V}\right) \tag{2.28}$$

The rejection leak rate for packages based on MIL-STD-883 varies depending on package volume. Note from Table 2-6 that the rejection leak rate is not continuous at certain package volumes. The rejection leak rate, displayed in terms of true helium leak rate, is plotted as a function of package volume in Figure 2-29.

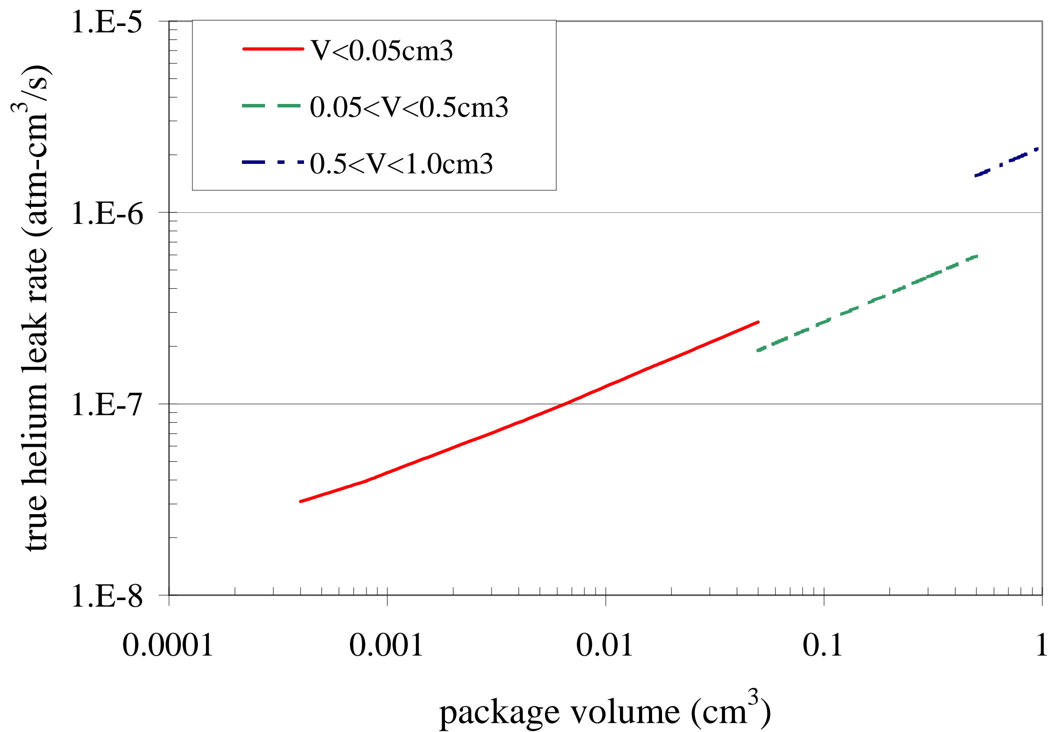


Figure 2-29: MIL-STD-883 rejection limit of true leak rate of helium as a function of volume (test condition A_1)

The test structures used in this dissertation have internal dimensions of 4.5 mm x 4.5 mm x 30 µm by design. For these dimensions, the package internal volume is approximately 0.0006 cm^3. The actual internal volume may be significantly different than the designed volume. While the in-plane dimensions are precisely controlled; the 30 µm standoff between the chips can vary due to variations in the deposition thickness of the indium during fabrication and the flow of the indium during assembly. During reflow, solder can lift the chips creating a larger standoff between the chips. Alternatively, pressure applied during reflow can act to reduce the standoff between the

chips. The accuracy of the internal volume of the package is not critical to the analysis, especially considering the variability in the rejection leak rates with regards to volume.

The internal volume also affects the ability to detect leaks. Very small packages, those with a volume an order of magnitude less than listed in the MIL-STD-883 ($0.05 cm^3$), can lose a large percentage of the helium in the transfer from the bomb to the leak detection chamber. Figure 2-30 shows the pressure inside a $0.0006 cm^3$ package as it is transferred from the bombing chamber to the detection chamber. It assumes that the package was completely filled with helium to 5 atm in the bombing phase.

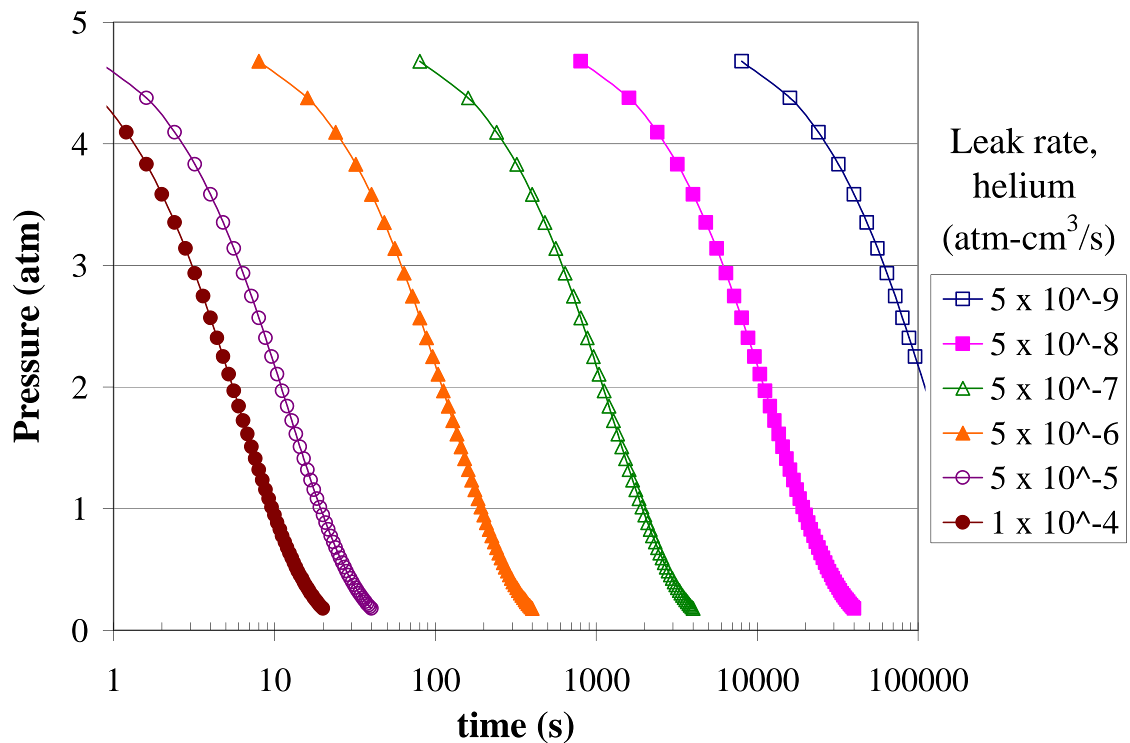


Figure 2-30: Helium leak rate from a $0.0006 cm^3$ package initially at 5 atm

The fine leak test is supposed to detect leaks smaller than 1 x 10^{-4} atm-cm^3/s. Leaks greater than that are detected via a gross leak test. Note that virtually all the helium would leak out of a package with a leak rate of 5 x 10^{-5} atm-cm^3/s within 40 seconds. The transfer time between chambers is on the order of minutes. A package of this volume, completely filled with helium during the bombing phase, would pass the leak test because there would be insufficient helium remaining in the package in the detection phase. As a result, the military standard fails to accurately screen packages of very small volumes.

2.10.2 Effects of leak path size

To better understand the effects of the rejection leak rate specification on the allowable defect size, consider the factors that govern the leak rate. The leak rate can be expressed by the conductance of the leak path by the following relationship:

$$Q = F(P_2 - P_1) \tag{2.29}$$

where Q is the leak rate, F is the conductance, P_2 is the pressure of gas on the inside of the package and P_1 is the pressure of the gas on the outside of the package.

The physics governing the conductance depends on the ratio of the mean free path to the leak cross-section dimensions and the pressure gradient across the package. Molecular and viscous flows are the two primary mechanisms that transport gas through a small leak channel. Molecular transport acts to equalize the partial pressure of each gas

inside the package with that on the outside the package. This transport occurs without a pressure difference between the inside and the outside of the package. Rather, this flow is driven by a difference in partial pressure of each individual gas. Viscous flow requires a pressure gradient across the package boundary of the package. The viscous flow cannot be ignored during the package bombing in leak testing or in rapid temperature cycling, where a pressure gradient across the package seal can occur. When considering long-term reliability for Navy fuzing applications, the focus is the effects of long-term storage on the device. During long-term storage, pressure gradients across the package are negligible.

Therefore, the analysis can focus upon the molecular transport of a gas through a small channel. First, consider the smallest leak rate possible. The smallest conductance will take place in a channel of length zero with a diameter equal to that of the molecule of interest. This conductance through an orifice is given by [96]:

$$F_o = 3638\sqrt{\frac{T}{M}}A \tag{2.30}$$

where F_o is the conductance of the orifice in cm^3/s, or minimum conductance rate, T is the absolute temperature in Kelvin, and M is the molecular weight in grams and A is the area of the channel in cm^2. The true leak rate can be calculated by substituting (2.30) into (2.29). By definition, the true leak rate is referenced to a helium pressure difference of 1 atmosphere. As a result, the conductance and leak rate are equal since the pressure gradient across the package is 1 atmosphere. The minimum leak rate for a particular gas can be calculated by substituting the temperature and molecular weight of the gas and setting the diameter of the orifice to the diameter of the gas molecule. A comparison of

the theoretical minimum leak rates for selected gases at 300K is summarized in Table 2-7.

Table 2-7: Theoretical minimum leak rate of selected gases

Gas	Molecular weight (gr)	Molecule diameter (cm)	Minimum leak rate (atm-cm^3/s)
Helium	4	2.2 x 10^{-8}	1.20 x 10^{-11}
Water	18	3.2 x 10^{-8}	1.19 x 10^{-11}
Air	28.7	3.7 x 10^{-8}	1.26 x 10^{-11}

If the leak rate is less than that specified in Table 2-7, then the gas will not leak into the package [97]. As a result, a larger leak cross section can retard ingress of the gas if the path length is increased. This relationship can be calculated by considering the molecular conductance of a rectangular channel [97]:

$$F_m = \frac{9.7a^2b^2}{(a+b)l}\sqrt{\frac{T}{M}} \qquad (2.31)$$

where F_m is the molecular conductance in cm^3/s, a and b are the cross-sectional dimensions of the channel in centimeters, l is the length of seal (that is, the length along the axis of leak channel) in centimeters, T is the absolute temperature in Kelvin, and M is the molecular weight of the gas in grams. In the test structures used in this dissertation, the length of the seal is 500 µm. The true leak rates of helium, based on a 500 µm seal, as a function of a square cross-section leak path is shown in Figure 2-31.

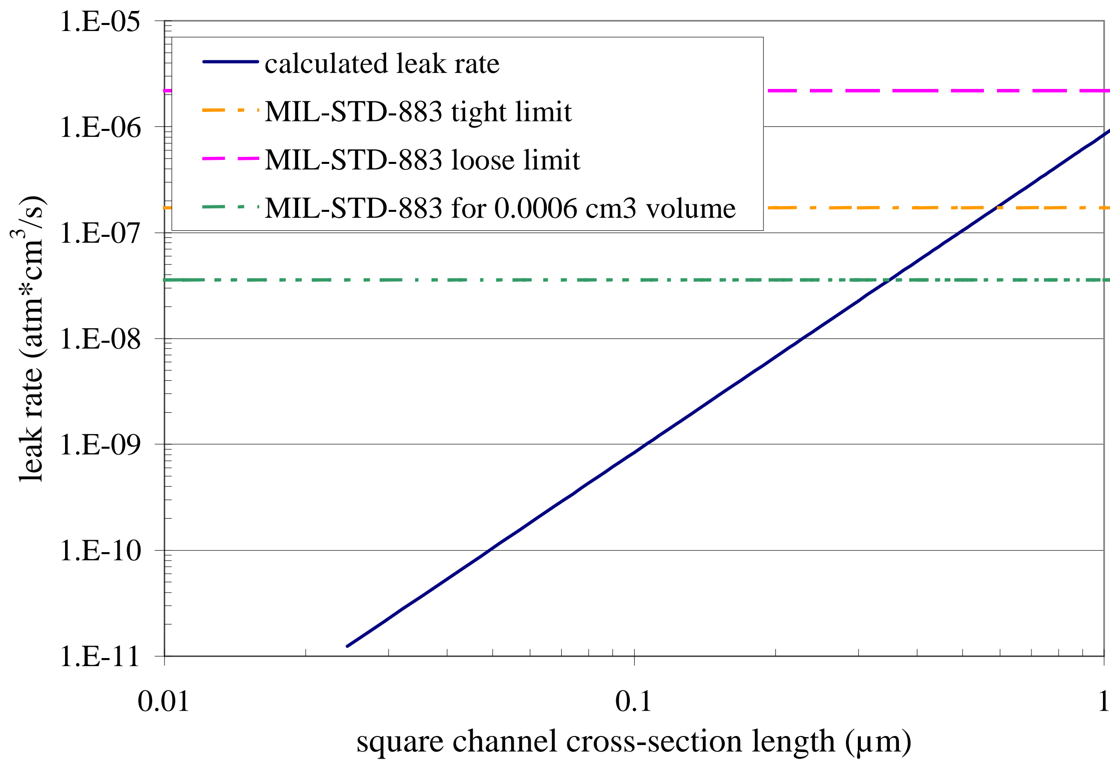


Figure 2-31: Theoretical true leak rate of helium as a function of leak path cross-section (500µm seal)

Note that the minimum leak rate for a 500 µm seal has a leak path with a 0.026 µm square cross section. A leak path smaller than this would not permit helium to pass into the package. From Figure 2-31, for the volume considered in this dissertation, 0.0006 cm^3, a 0.4 µm leak path meets the MIL-STD-883 standard. Other package volumes, with different leak rate acceptance criteria under the standard, can have more or less stringent acceptance criteria with regards to acceptable leak path geometry. The tight and loose limits plotted in the figure are the maximum and minimum rejection limits over the volume range of 0.05 cm^3 to 1cm^3 based on true leak rate of helium. Note that there is a wide variation in the defect size that will pass the leak test, the square channel may have

to be as small as 0.4 µm on a side or may be as large as 1.3 µm. This discrepancy is a direct result of the variation in the acceptable leak test limits in the military specification and the influence of package volume on acceptance criteria.

2.10.3 Determination of acceptable leak rate

The understanding of the military specification is important in that it provides a background on the scrutiny that the packages undergo before acceptance. However, it does not address if the test is too stringent or perhaps too lenient in its pass-fail criteria. The purpose of this section is to address the level of protection required to ensure that that the moisture level in the package does not reach unacceptable levels over the life of the package.

Consider next, the time for moisture to cross the seal boundary as a function of time and leak rate. The amount of water that leaks into a package can be calculated from the following relationship [97]:

$$Q_{H_2O} = p_{H_2O}\left(1 - e^{\frac{L_{H_2O}t}{V}}\right) \tag{2.32}$$

where Q_{H_2O} is the pressure of water that has leaked into the package, p_{H_2O} is the initial difference in partial pressure of water inside and the water vapor outside the package, L_{H_2O} is the true leak rate of water vapor in atm-cm^3/s, t is the time in seconds, and V is the internal package volume in cm^3. The dependence of leak rate of water into the package on channel size and package volume is shown in Figure 2-32.

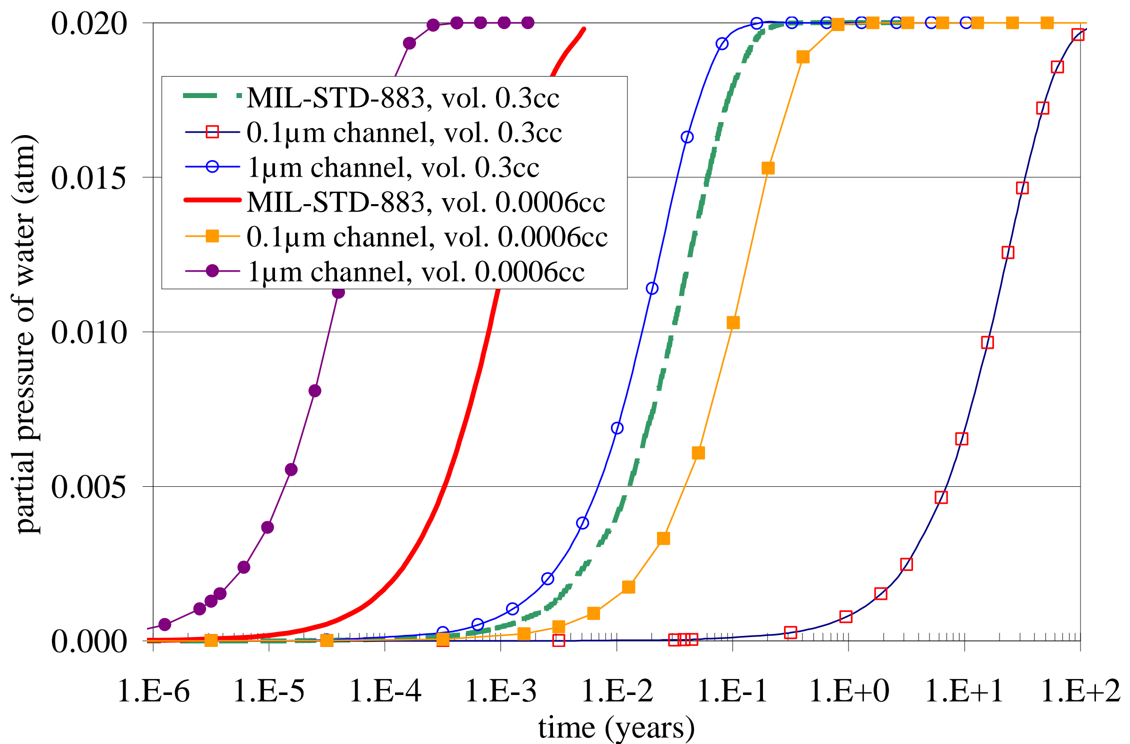


Figure 2-32: Migration of moisture into a sealed package

The curves in Figure 2-32, calculated using (2.32), are based on initial conditions of zero initial water vapor in the package and external moisture content of 0.02 atmospheres of water vapor in the air. The partial pressure used in these calculations represents the yearly average content over the past 18 years in Florida [98]. The leak rates to generate the leak channel curves were calculated by substituting a package seal length of 500 µm into (2.31). The military standard curves were calculated by first converting the measured leak rate limit to a true leak rate of water via (2.26) and (2.28). Next, the true leak rate of water military limit was substituted into (2.32).

There are several interesting points to make from Figure 2-32. First, the military standard does not provide an adequate screening method to ensure that water vapor will not enter the package. This concern is more apparent as the package internal volume shrinks. Considering the case of an internal volume 0.3 cm^3, a package that passes the military standard can allow the water vapor pressure inside the package to reach equilibrium (i.e., the partial pressures are within 1% of each other) with the external environment in 81 days. For the case with a 0.0006 cm^3 internal volume, a hermetic package may reach equilibrium within 2 days. In the examples cited in Figure 2-32, air with 0.02 atm partial pressure of water vapor has a dew point of 16°C (62°F). Clearly, equilibrium with the external water vapor environment must be avoided to provide adequate protection to the device inside the package. Smaller volume packages must adhere to a much stricter standard if moisture inside the package is to be avoided. However, even the large volume packages fail to fully protect moisture ingress over a several year time span.

The second interesting point to note from Figure 2-32 is the effect of the leak path size on the leak rate. A 1µm square leak path fails to meet the military specification for both the 0.3 cm^3 and 0.0006 cm^3 packages. A 0.1 µm leak path will pass the leak test criteria for both volumes considered. However, 0.1 µm leak path provide 3 orders of magnitude longer time to water vapor equilibrium than the standard dictates for a 0.3 cm^3 package and less than an order of magnitude advantage for the 0.0006 cm^3 package. Hence, the acceptable leak path in the smaller volume package must be smaller than its larger package counterpart.

It was just demonstrated that the military specification does not ensure that moisture will not enter the package over a several year time frame. However, IC packages for military applications historically have been qualified to this standard to ensure long-term reliability. The discrepancy lies in the relevant failure mechanisms of the IC packages versus that of MEMS packages. For IC packages, moisture in the package accelerates and in some cases initiates corrosion. The corrosion process occurs over a long period of time. The hermetic seal does not necessarily prevent corrosion, but it prevents corrosion related failures during the package life by slowing the onset and the rate of corrosion. Hence, the deleterious effects of the moisture in these cases are mostly due to long-term exposure of the device to moisture. In the case of MEMS, the deleterious moisture effects can be immediate. Moderate temperature changes, such as those often experienced over a typical day, can result in condensation inside the package and immediate stiction failure of the MEMS device.

Having established that the hermetic seal defined by MIL-STD-883 is not strict enough to prevent moisture related failure throughout the life of the MEMS packaged considered in this dissertation, the next question to address is the level of protection that is required. A package with an internal water partial pressure of 0.006 atm will condense at 0°C. Therefore, it is desired to maintain the water vapor content below this level. The time it takes for the package internal environment to reach a specified partial pressure of water can be calculated by rearranging (2.32).

$$t = -\frac{V}{L}\left[\ln\left(1 - \frac{Qin}{\Delta P}\right)\right] \tag{2.33}$$

The time for the package to reach an unacceptable moisture level, based on an internal pressure limit of 0.006 atm and an external pressure of 0.02 atm, as a function of leak rate is shown in Figure 2-33.

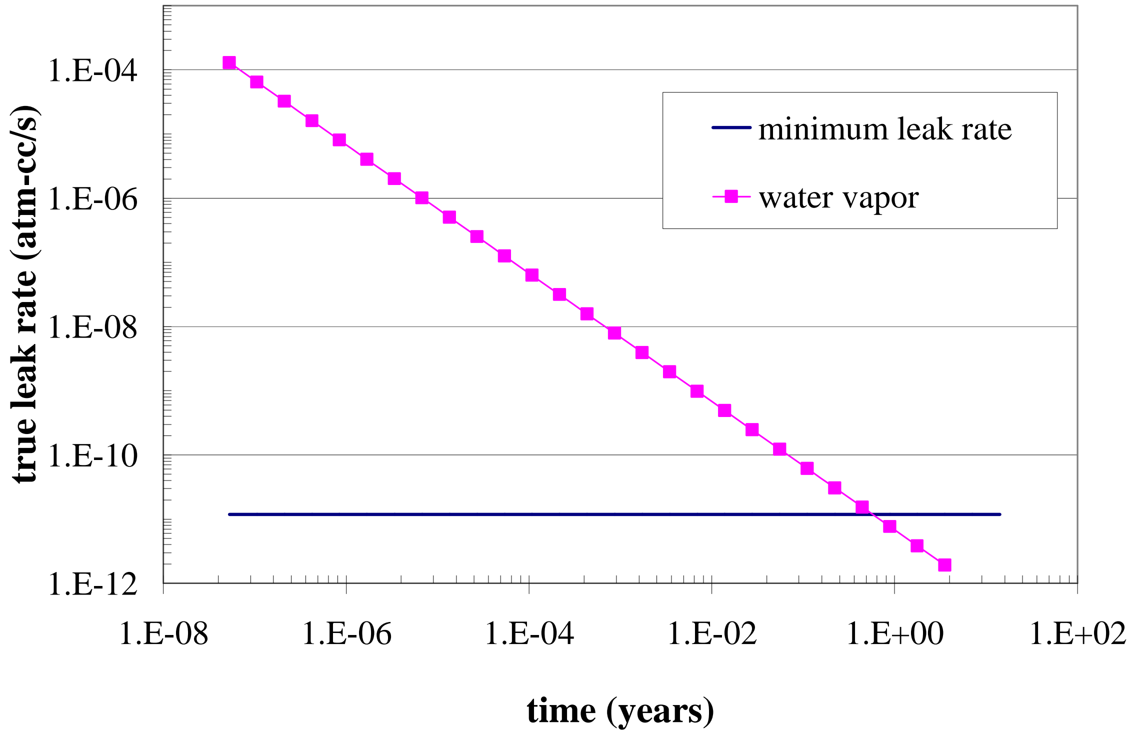


Figure 2-33: Time for package to reach unacceptable moisture level

To achieve a life of twenty years, the true water leak rate must be below 5 x 10^{-13} atm-cm^3/s. This leak rate is more than two orders of magnitude below the minimum leak rate of water vapor (Table 2-7). Hence, the package seal that adequately protects the device from moisture ingress over a one-year time frame will provide indefinite protection. However, testing the seal integrity is another issue. The equivalent true leak

rate of helium, calculated from (2.26), is 2.5 x 10^{-11} atm-cm^3/s, below the typical helium detector limit of 5 x 10^{-10}. To be able to accurately assess the integrity, alternative seal evaluation techniques need to be developed that are outside the scope of this thesis.

2.11 Summary

In this chapter the approach to seal two chips with an optical fiber crossing the seal was presented. Several processes to fabricate the chips were identified and evaluated, resulting in a process flow for chip fabrication. A particular emphasis was placed on metallization of the high aspect ratio sidewalls of the fiber channels. This contribution is fundamental to facilitating a seal at the interfaces between the fiber and the chips. This chapter also addressed the thermodynamic conditions that govern the fluxless soldering process in different atmospheres. The means used to assemble and reflow the hardware is presented with a focus on understanding the implications of the techniques on the soldering process. At the end of this chapter, the test conditions that used to assess the hermeticity of packages are scrutinized for small volume packages. It is found that the standard is not capable of accurately screening small volume packages. In addition, if the parameters in the standard could be modified to properly assess the hermeticity, the resolution of the leak detectors would still lack the ability to detect sufficiently small leaks that are large enough to allow an unacceptable moisture ingress rate into the package. This chapter concludes that the military standard is an inadequate tool to assess the package seal integrity.

CHAPTER 3: EXPERIMENTAL RESULTS & MODELING

In this chapter the results of the soldering experimentation are discussed. The fluxless soldering process is evaluated through a series of increasingly complex experiments. To develop a quick inexpensive method to assess the fluxless soldering process, experiments were first performed using bare indium wire and flux coated preforms. The preforms are ordered to the customer specifications, in this case a 0.062 inch diameter pure indium disc, 0.020 inch thick. After suitable fluxless soldering process parameters were established with the indium wire samples, the process was extended to overplated chips with various metallization schemes, as outlined in Section 2.4. These test structures were used to explore the effects of the undermetallization and gold content on the solder flow and the resulting solder joint quality. In addition, the test structures were necessary to extend the fluxless soldering process to planar structures, that is structures with a high surface area to volume ratio. High surface area structures, utilized in the design concept presented in Section 2.1, oxidize more readily and are thus more difficult to reflow properly with a fluxless soldering process. Next, the fluxless soldering process is extended to bonding chips with planar solder structures. The integrity of the joined chips is assessed through die shear and inspection. Finally, the pairs of chips with a metallized fiber sandwiched in-between are joined with the fluxless soldering process.

The latter half of the chapter deals with the modeling of the solder during and after the reflow. An energy minimization software tool called Surface Evolver was used to predict the final shape and the stability of the reflowed solder joint. First, the model of

one-sided solder joints is studied to broaden the understanding of the solder behavior during reflow and to reflect the test structures discussed in Section 3.2. Then the model of the solder joint that seals the fiber in the channel is discussed. This model was used to provide a deeper comprehension of the solder behavior as it fills voids in the fiber channel and to provide guidance in the design of the solder joint.

3.1 Manually applied solder to wetable and non-wetable surfaces

To first demonstrate and validate the cleaning process and reflow environments, test reflows were performed with indium wire and flux coated indium preform discs. Flux coated indium samples readily formed balls on bare silicon regardless of reflow environment and profile (Figure 3-1).

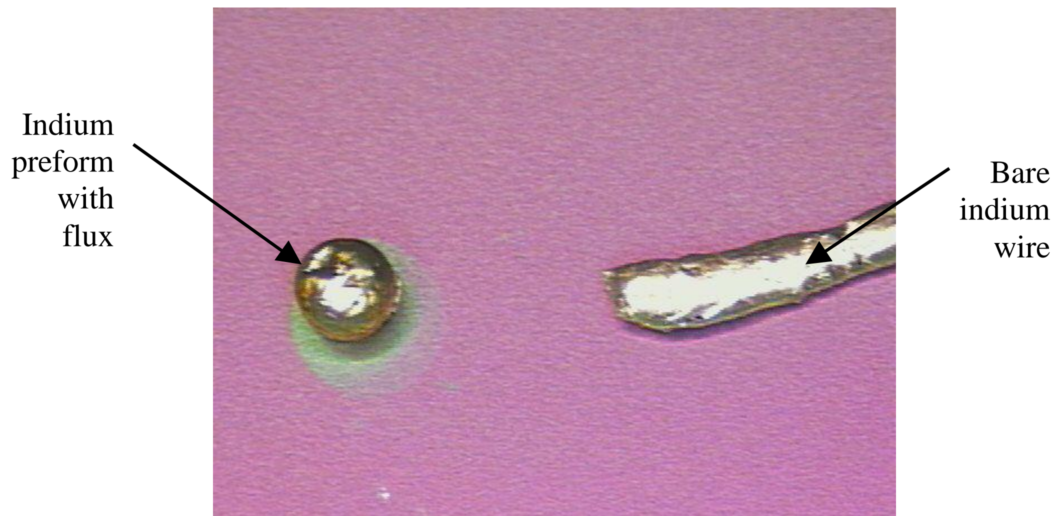


Figure 3-1: Reflow results of flux indium and indium wire on silicon

The indium does not typically wet to bare silicon. In the absence of the wetting forces between the solder and the substrate, the surface forces of the molten solder dominate. Upon reflow, the molten solder will act to minimize its energy state by reducing its surface area to a minimum by forming a spherical shape. The formation of the spherical shape is contingent on the solder achieving a completely molten state. If an oxide skin is present, the solder will not become completely molten until a much higher temperature (i.e., 1900°C). The solder can, however, achieve a lower energy state if the oxide skin is not present during the reflow or is sufficiently thin such that it is consumed by the joint and does not obstruct the solder reflow. In the case of the fluxed performs, the flux effectively removed the oxides during the reflow. The flux is designed to remove the oxide skin and performed as expected. The reflow of the flux samples provides an example of how the solder should behave on the silicon samples if the oxide skin is effectively removed.

Bare indium wires were reflowed on bare silicon with a variety of cleaning and temperature profiles. The primary difference between these samples and the fluxed performs is the absence of the flux vehicle. Hence, the oxide must be removed from the samples through pre-cleaning and handling, during the reflow with a reducing gas, or both. The following three factors significantly affected the ability to flow the indium wire into a sphere:

1. Cleaning and removal of the initial oxide
2. The amount of oxygen in the reflow environment
3. Exposure time to oxygen before reflow

In the absence of a flux, indium wire samples (Figure 3-1) often retained their shape after reflow. The oxide skin formed on these samples was thick enough to prevent the surface tension forces of the molten solder from reducing the solder sample to a spherical shape. Cleaning the indium wire is essential for removing the oxides. A 10% HCl soak for 10 minutes with an isopropyl rinse effectively removed the indium oxide. Since indium readily reforms a thin oxide layer, additional care is required to get an oxide-free reflow. Oxides present during the reflow process form a thicker, more tenacious bond due to the elevated temperature. Samples that were not cleaned of the native oxide typically did not reflow into a spherical shape.

The heat rate affected the reflow due to the accelerated oxidation rate of indium at elevated temperatures. Samples that were heated slowly in the presence of oxygen (>1000 ppm) did not reflow to spherical shape. The amount of time above the melting temperature of the solder typically did not influence the reflow results. Samples that did not reflow within 1-2 seconds after exposure to temperatures above the melting point of the bulk solder typically retained their cylindrical shape.

The reducing gas was ineffective even at dwell times as long as 1 hour and at process temperatures as high as 400°C. Higher temperature and longer dwell times were not attempted since 400°C and 1-hour dwell can be considered upper bounds on the process parameters. The 400°C limit was selected for two reasons. First, the manufacturer of the wafers uses this as a maximum process temperature to avoid delamination of the gold layer from the chromium. Second, the hot plate used in the

present effort has a maximum temperature of 400°C. Commercial sources for programmable hot plates capable of temperatures above 400°C were not identified. The intent of this effort is to minimize the specialized infrastructure needed to perform the assembly of the hardware to lend itself to commercial acceptance. With regards to the process time, machine time must be kept to a minimum to maximize throughput. In commercial applications, in particular large quantity applications, every second of machine time affects throughput and thus cost. One-hour process time was viewed as at least an order of magnitude too long for a large quantity commercial application and as a worst case bound for small quantity applications, such as the Navy S&A.

To determine if the environment was close to being thermodynamically favorable for reducing the indium oxide, the experiment was repeated with AuSn eutectic solder. Recall from the analysis in Chapter 2 that the AuSn oxide is thermodynamically favorable to reduction at 400°C if the ratio of hydrogen to water is on the order of 5, as opposed to the 86 needed for indium oxide. However, the AuSn cylinders did not form a sphere even after 1 hour at 400°C, despite the fact that the hydrogen to water ratio from the supply was on the order of 2500. The oxygen content in the atmosphere during the reflow was measured to be on the order of 100 ppm. Note that this is far above the limit for oxide reduction of indium or tin. However, the oxygen content is measured several feet downstream of the sample. From the analysis in chapter two, it can be understood that the some of oxygen is consumed by the reducing gas at an elevated temperature reverts back to pure oxygen by the time it passes through the oxygen sensor. This highlights the issue of oxygen entrainment into the sample from the chosen heating

method. Although the heat is applied globally, in that it is applied to the entire chip, the entire environment is not heated. Thus, the thermodynamic conditions for oxide reduction of indium or tin were not met with the heating approach selected for this study.

With the understanding that the process gas was unable to effectively reduce the oxides, the fluxless soldering process proposed here is not unfeasible. Rather than try to use the reducing gas to scrub the oxides that were present, the environment was controlled to prevent formation of the thicker, more tenacious oxide that forms at elevated temperatures with ample oxygen supply. By having an extremely thin initial oxide and limiting the formation of additional oxides, the solder joint can consume the oxide without impeding the flow of the solder. This approach hinges on a fast heat time to limit exposure time in the thermodynamically favorable oxidation environment.

Using a rapid heat technique, the bare indium wire samples successfully achieved their lower energy spherical shape on silicon (Figure 3-2).

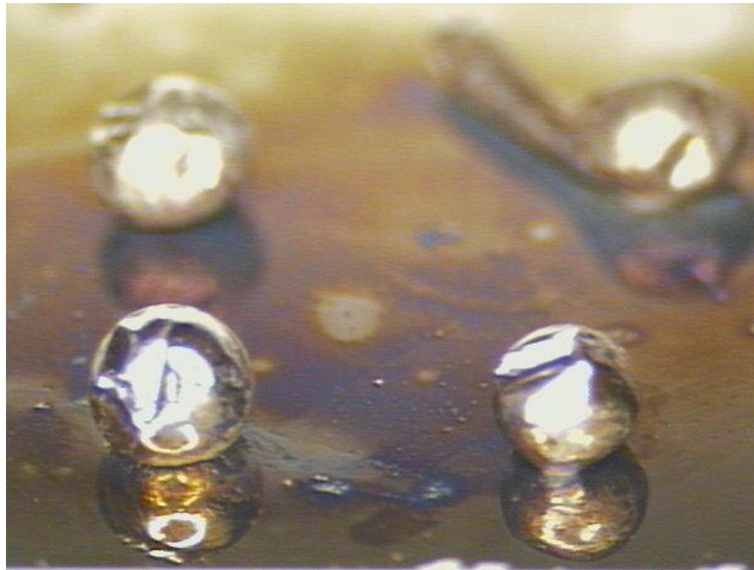


Figure 3-2: Bare indium wire samples after reflow

To obtain a fast heat rate, the samples were placed directly on a preheated hot plate. However, higher heat rates could be effectively obtained with lasers, which are commonly used in MOEMS packaging applications. The reflow results of 10% HCl clean bare indium wire samples are summarized in Table 3-1.

Table 3-1: Indium wire reflow results on bare silicon in a reducing environment

Temperature (°C)	Number of samples evolving to a spherical shape
200	1 of 3
250	3 of 3
300	4 of 4
350	5 of 6

The samples that formed spheres did so within two seconds of contact with the substrate. At higher temperatures, wires that did not form balls immediately would

sometimes slowly (on the order of tens seconds) form more of an oval shape. Samples reflowed at higher temperatures were more likely to flow into a spherical shape. Two factors influenced this result, both dealing with oxide formation. First, the higher temperature plate results in a faster heat rate to the solder reflow temperature. The high heat rate prevents thickening of the oxide layer at elevated temperatures. The second factor that resulted in better reflow at a higher temperature is that the oxygen content in the atmosphere surrounding the plate is reduced due to the action of the reducing gas.

Gold-tin eutectic wire was reflowed in a similar manner as the indium samples in Table 3-1. However, the samples were not cleaned prior to reflow. The results are summarized in Table 3-2.

Table 3-2: Gold-tin wire reflow results on bare silicon in a reducing environment

Temperature (°C)	Number of samples evolving to a spherical shape
300	0 of 4
350	3 of 4
400	3 of 4

At the lower temperatures, the wire did not initially form a sphere. When the temperature was increased to 350°C, 3 of the 4 wires that were on the hot plate from the 300°C then formed a spherical shape. This is in stark contrast to the indium samples, which typically reflowed immediately upon reaching the melting temperature or not at all. This is because tin oxides are not as thermodynamically stable as the indium oxides. When the plate was brought to 400°C, 3 of the 4 samples introduced at that temperature

formed spheres. All of the samples in Table 3-2 formed spheres when the reflow fixture was agitated slightly. The agitation provided enough energy to break up the little remaining oxides.

To address wetability concerns, bare indium samples were reflowed on gold covered silicon. The indium wet the gold quickly if cleaned. If not clean of oxides, the indium wire wet to the gold at elevated temperature (300°C) after stress in the film causes a hole in the oxide skin and allows the solder to flow out (Figure 3-3).

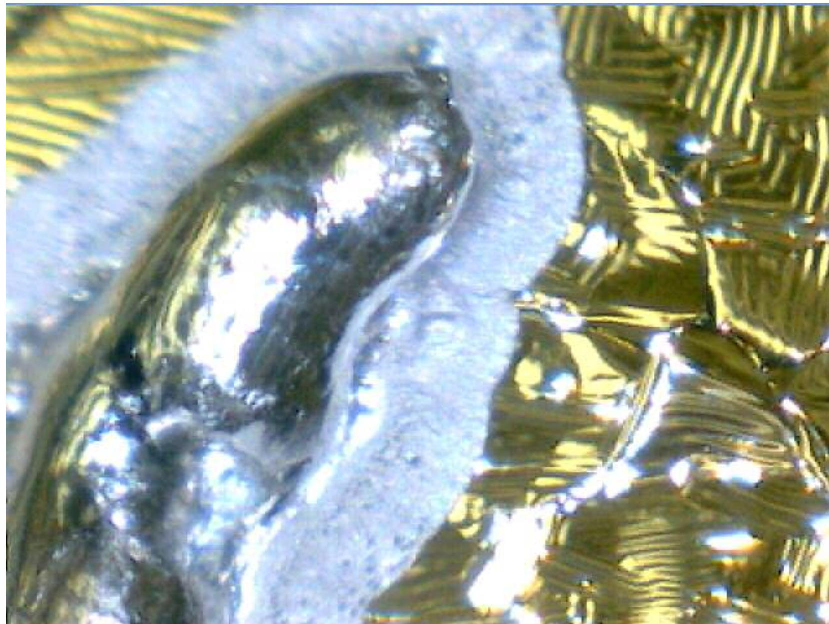


Figure 3-3: Indium flowing out of oxide bag

After sufficient time, all the molten solder would flow out of the "oxide bag", leaving a skeleton of the indium wire behind (Figure 3-4). The solder was able to wet the entire gold deposited chip due to the protective atmosphere. The indium that flows out of the oxide skin does not oxidize, yet the inert or reducing environment is unable to scrub

away the oxide bag. This further illustrates the importance of cleaning and the prevention of oxide formation before and during the solder reflow.

Figure 3-4: Oxide bag after complete reflow

3.2 Open faced solder test coupons

Solder test coupons were designed to validate the concept of using surface tension forces to fill voids. Indium solder pads were designed to be, in some cases, larger than the metallized pad (Section 2.5). These structures were reflowed open faced, that is they were not bonded to other structures or substrates. The primary purpose was to study the flow of the solder from non-metallized areas to the metallized pads. This approach lends the samples to optical inspection of the solder joint during and after soldering. Using an open faced structure is a penalty test in that the actual system has a top chip in place,

which helps to draw the solder to the metallized pad with the additional wetting forces. The overplate structures were also used to study the solder systems outlined in Section 2.4. The effects of the relative gold content were addressed in these experiments. By depositing solder beyond the metallized pad, the quantity of gold in the final solder joint was varied without depositing different thickness layers of the indium and gold.

The behavior of the solder during reflow was studied to quantify the effect of the overplate ratio on the final solder joint geometry and is discussed in further detail below. The assessment of the processing and the reflow behavior results provides a broader understanding of the practical limits of solder overplating. More specifically, the study provides design rules to guide future designers in the limits of the amount of solder that could be drawn from off-pad locations to the metallized pad during the reflow process. Recall that the flow of the solder from non-metallized areas to metallized areas is a key part of the process to seal the round fiber in the rectangular hole. In addition, it is desirable to have a consistent thickness of solder in the seal ring. Therefore, the additional solder to fill the voids is to come from non-metallized areas. In summary, the overplate structures provide the data necessary to define the process limits to make the overplate structures, the cleaning and reflow environment to obtain a completely molten solder joint during reflow, and the design limits at which the solder will not be drawn to the metallized pad. In broader terms, these test structures were used to define the limits at which the solder was drawn to the metallized areas.

3.2.1 Initial feasibility and joint gold content

Initial samples were reflowed in the University of Maryland Electrical Engineering clean room. Samples were cleaned for 10 minutes in 10% HCl and 90% H_2 and later reflowed in a reducing gas environment, 95% N_2 and 5% H_2. These experiments demonstrated that the solder could pull in from non-metallized areas. Figure 3-5 depicts a sample with 750 µm by 750 µm by 5µm indium pad on a 500 µm square gold pad on TiW. The SEM pictures show that virtually all the solder was drawn from the bare silicon to the metallized pad. Localized off-pad balling can also be seen. The solder did not wet to the non-metallized area, i.e., the off-pad solder had a wetting angle much greater than 90°. On the metallized pad, the solder wet to the metal, having a wetting angle below 90°. Had the solder not wet the pad, a spherical shape would have been realized as opposed to the mound seen in the test coupons. However, as evident in the dewetting around the perimeter of the pad, there is room for improvement in the pad wetting. The wetting could be improved by further limiting the oxides present during the reflow or simply by increasing the quantity of solder deposited on the pad.

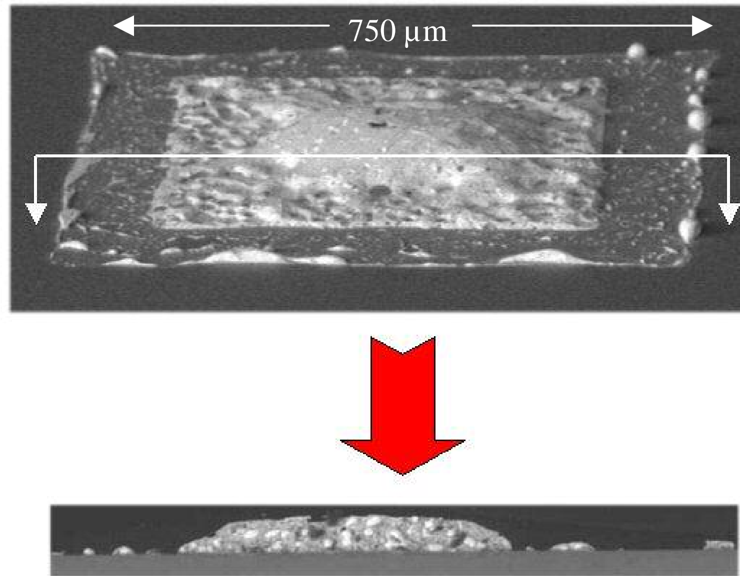


Figure 3-5: Small overplate test structure

Larger overplate structures further demonstrated the ability to use the metallized pads to define the post solder reflow geometry without a flux vehicle. Figure 3-6 depicts 1500 µm by 1500 µm by 5µm indium pad on a 500 µm square gold pad on TiW after reflow. This sample was reflowed with the same technique as the sample pictured in Figure 3-5. The larger overplate resulted in larger quantity of solder off the metallized pad. However, it also demonstrated the ability to draw solder from as far away as 500 µm with only a 5 µm film of solder. In addition, it demonstrated the ability to form much larger mounds of solder, in this case increasing the height from 5 µm to approximately 75 µm. Also note that the dewetting of the pad was greatly reduced with the presence of the additional solder.

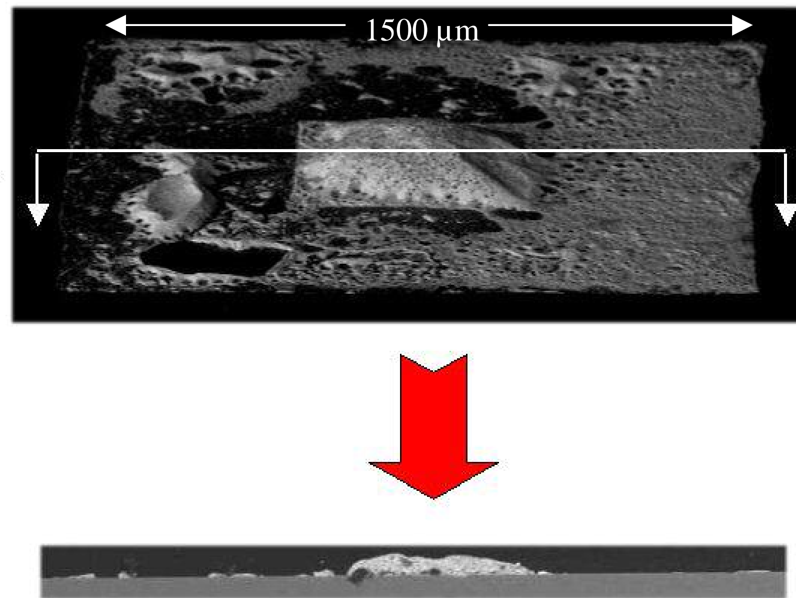


Figure 3-6: Large overplate test structure

The amount of gold in the joint was varied to study the effect of intermetallic formation. The undermetallization significantly affected the final joint shape and composition. It also impacted the ability of the solder to pull into the metallized pad. Figure 3-7 shows a post reflow of a 1500 µm by 1500 µm by 5µm indium solder pad on a 500 µm by 500 µm by 1000 Å gold pad on chromium. This sample had an overplate ratio of 100 and 0.15% gold content. Note that virtually all the solder flowed from the non-metallized area to the metallized pad. However, Figure 3-8 shows a similar test structure with a 5000 Å thick gold layer that was cleaned and reflowed concurrently with the structure in Figure 3-7. The overplate ratio for this sample was also 100, but overall gold content increased to 0.7%. Note that the solder did not flow to the metallization pad nor was it able to form a mound.

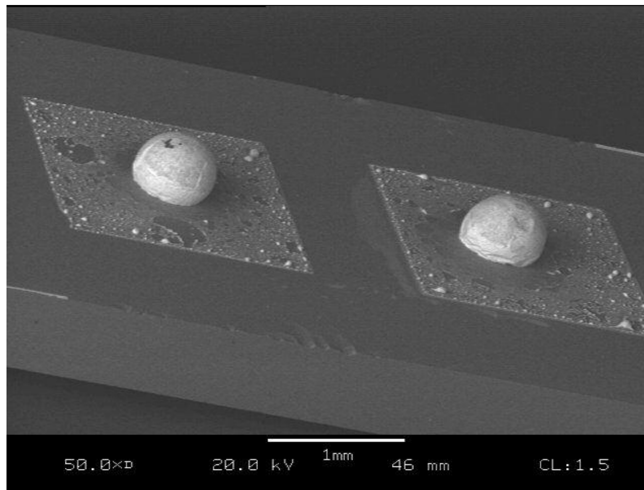


Figure 3-7: Cr/Au/In after 275°C reflow: 1000 Å gold

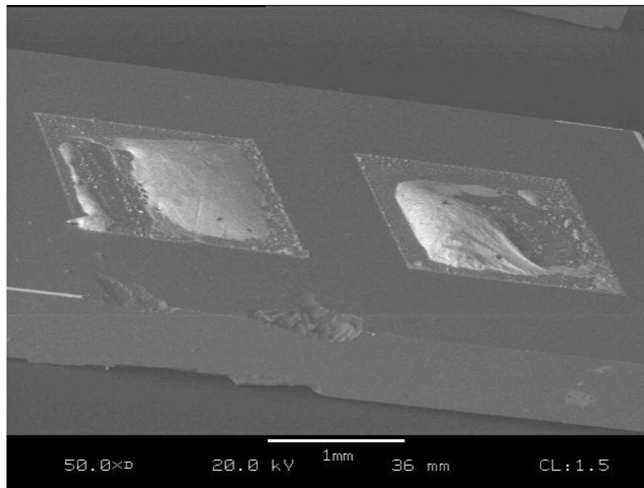


Figure 3-8: Cr/Au/In after 275°C reflow: 5000 Å gold

Several samples were cross-sectioned and analyzed on a SEM and an EDX. The SEM provided qualitative data on the reflowed solder joint and the EDX was used to identify elements in the joint. Several different cross-sectioned samples, each with a different gold content, are shown in Figure 3-9, Figure 3-10, and Figure 3-11. If the solder joint had a high content of gold like that shown in Figure 3-9, the solder joint

consisted of a large amount of the gold-indium intermetallic. An EDX analysis was performed on the sample in Figure 3-9. The bright regions are the gold indium intermetallic, Au/In_2. The dull regions, so small that they are barely visible in the image, are pure indium.

The samples with 10% gold by weight had localized regions of the intermetallic, seen as bright regions in Figure 3-10. Using the level law and the gold indium phase diagram, the amount of Au/In_2 in the solder joint can be predicted.

$$\text{phase percent} = 100 \times \frac{\text{opposite arm of lever}}{\text{total length of arm}} \tag{3.1}$$

For the 10% Au case, the Au/In_2 content in the joint is 18% by weight. For comparison with the cross-section images, the weight content can be converted to volume using the following densities:

Au: 19.32 g/cc [91]

In: 7.31g/cc [91]

Au/In_2: 10.3 g/cc (assumed)

The resulting volume percentage, or area percentage, of Au/In_2 is approximately 17%. The area of bright regions, identified as Au/In_2 using EDX analysis, in Figure 3-10 is roughly on the order of 15%, which agrees with the expected quantity of the intermetallic.

The 3% gold by weight samples had gold dispersed throughout the joint, undetectable with an EDX analysis.

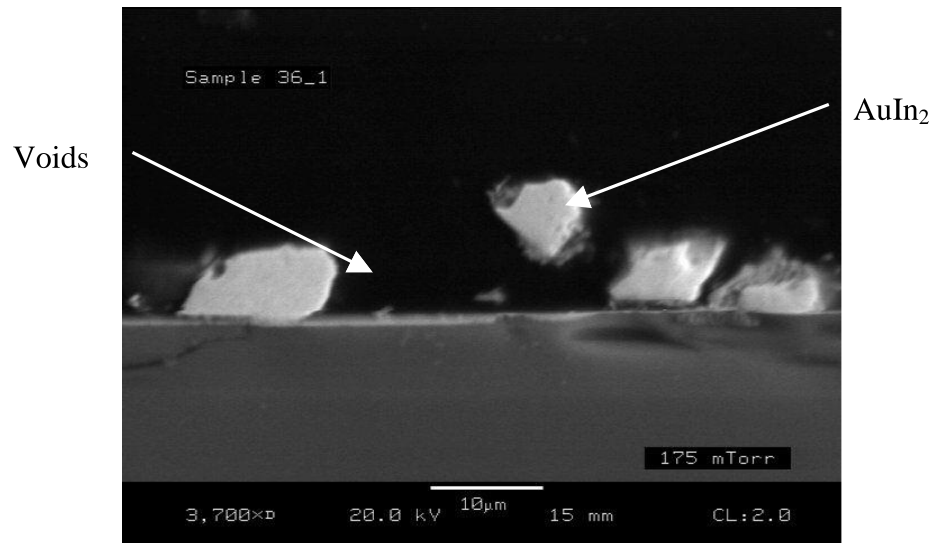


Figure 3-9: 26% Au by weight

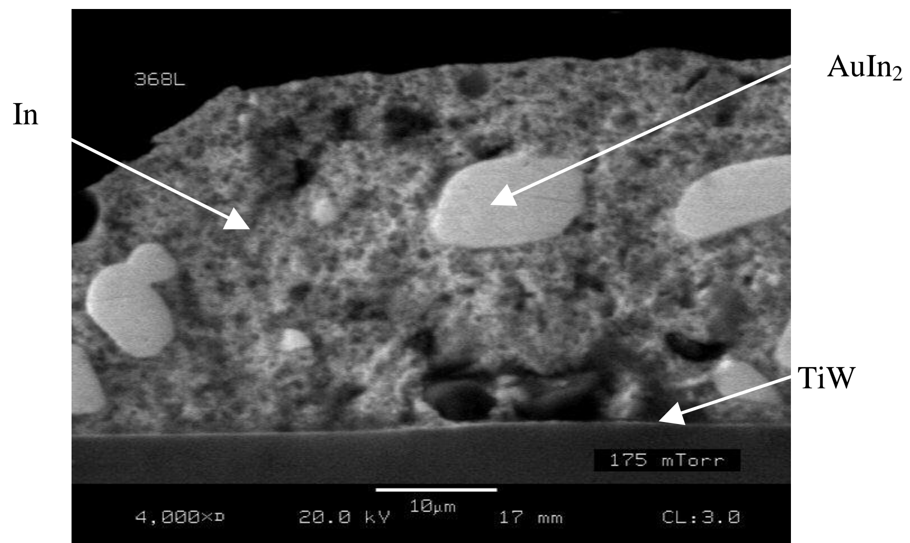


Figure 3-10: 10% Au by weight

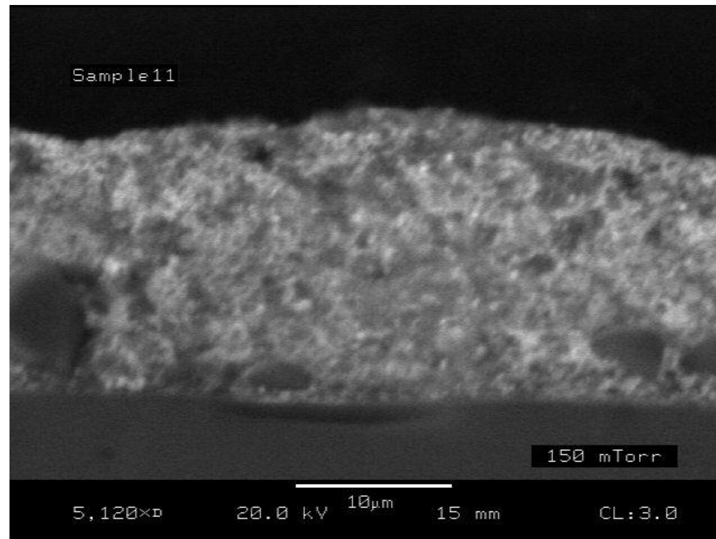


Figure 3-11: 2.8% Au by weight

The gold-indium phase diagram aids in the understanding of the intermetallic formation. If excess gold is present it is dissolved in the joint. As the gold content in the joint increases, the risk of precipitating intermetallic compounds increases. Suppose the gold content in the joint is 10%. Referring to Figure 3-12, the Au/In_2 would begin to precipitate out at approximately than 370°C. Therefore, for the reflow temperature used in the present effort, the intermetallic phase would solidify. The solid boulder of the intermetallic impedes the natural flow of the solder and may lead to separation, or tearing, of the solder. The resulting joint has non-uniform material properties and often is unable to completely flow to the metallization pad. Higher gold concentrations begin to solidify at even higher temperatures. Furthermore, higher gold content results in more $AuIn_2$ intermetallic formation at a given temperature than lower gold content joints. As a result, a lower gold concentration is desirable to reduce the adverse effects of intermetallic formation.

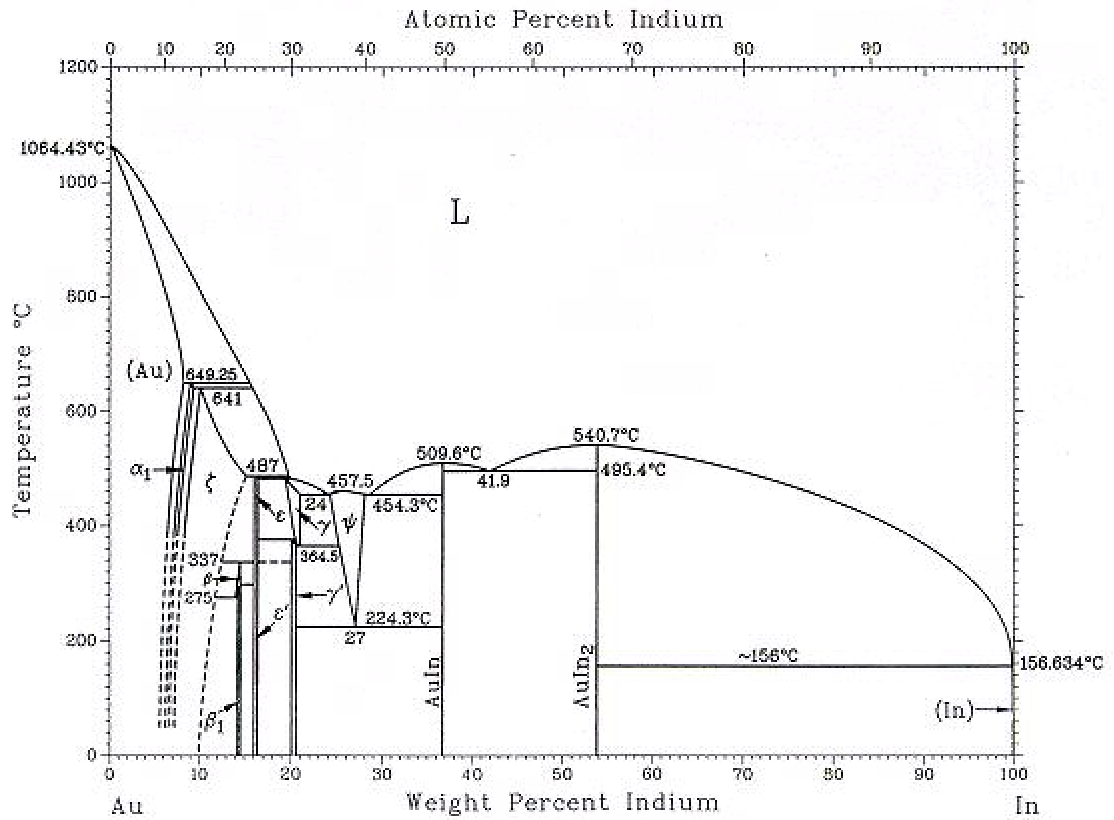


Figure 3-12: Au-In Phase Diagram

3.2.2 Multiple overplate test structure reflow results

The multiple overplate test structure chips, Figure 2-7, were fabricated using either TiW or Cr adhesion layers, which also serves as the wetting layer [99]. In the previous section, it was demonstrated that superior wetting characteristics were obtained when the Cr was passivated with a 1000 Å layer of gold as opposed to a 5000 Å layer. Therefore, the 1000 Å gold layer was used on the multiple overplate wafers that were fabricated

with a Cr adhesion layer. The TiW gold layer was maintained at 5000 Å since data did not exist to justify reducing the gold layer on this adhesion layer to 1000 Å.

In the comparisons that follow, TiW and Cr samples were cleaned and reflowed concurrently. Post reflow images of the TiW and Cr undermetallization overplate test structures are shown in Figure 3-13 and Figure 3-14, respectively.

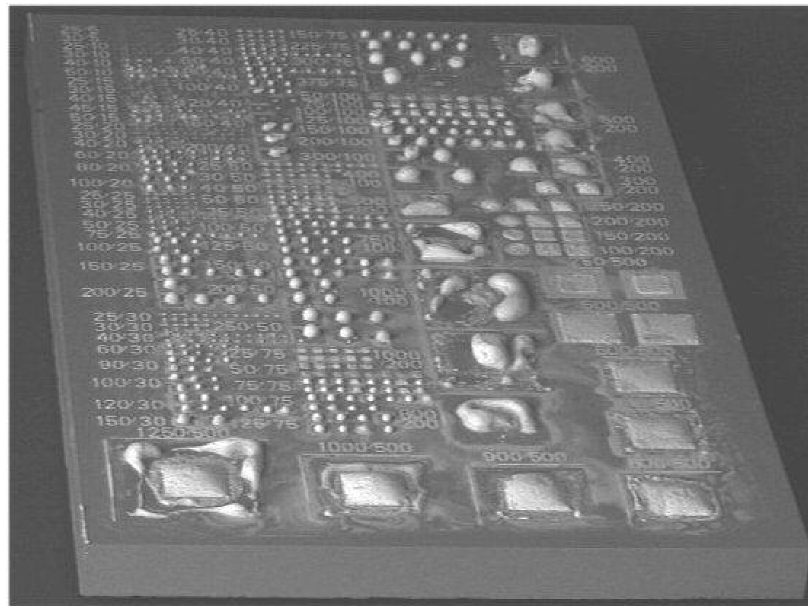


Figure 3-13: TiW/Au/In multiple overplate test structure after reflow

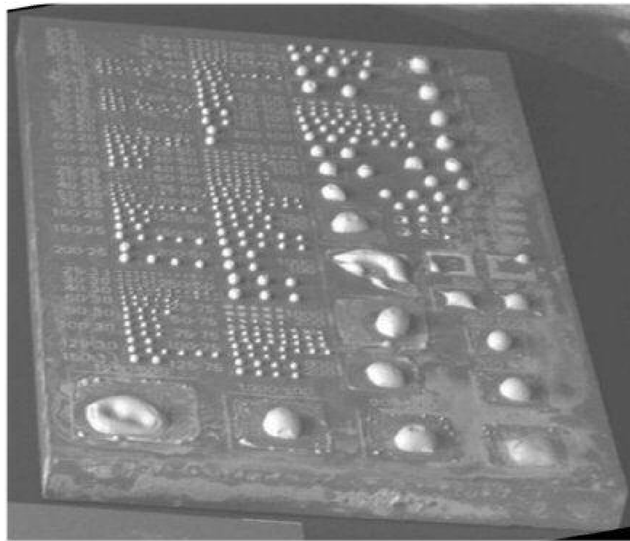


Figure 3-14: Cr/Au/In multiple overplate test structure after reflow

Both chips were reflowed with 5% H_2 reducing gas at 275°C. The results from these two chips are summarized in Figure 3-15 and Figure 3-16.

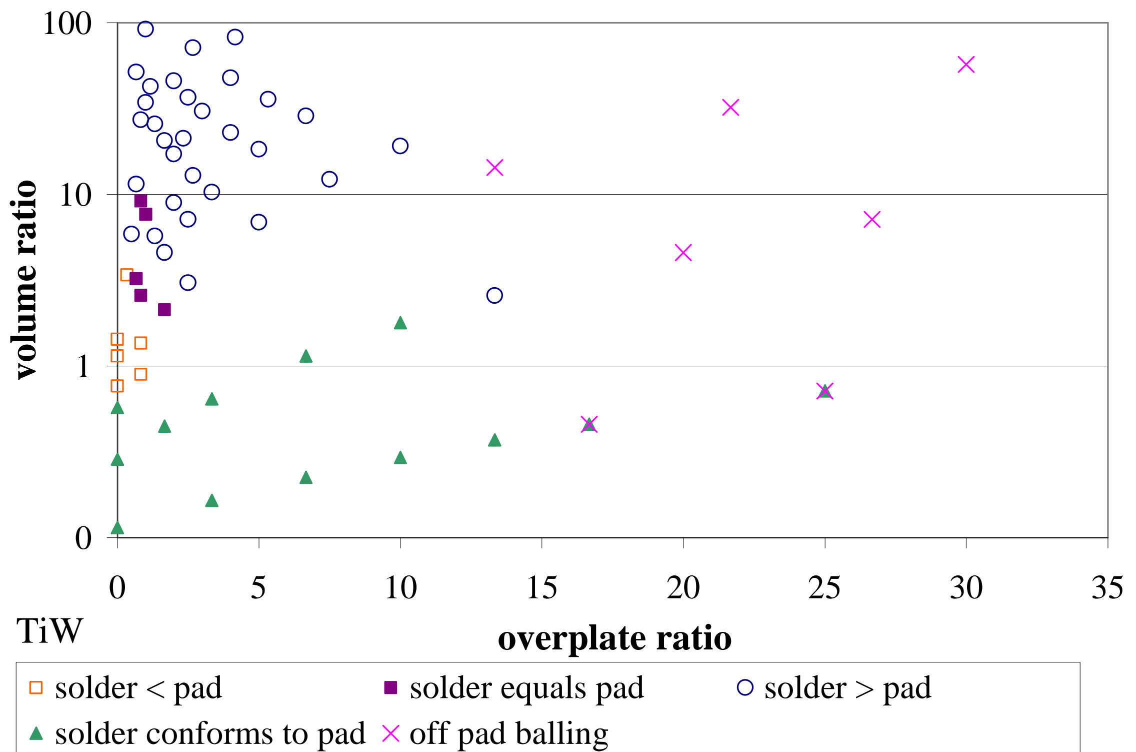


Figure 3-15: Reflowed TiW/Au/In multiple overplate test structure characterization

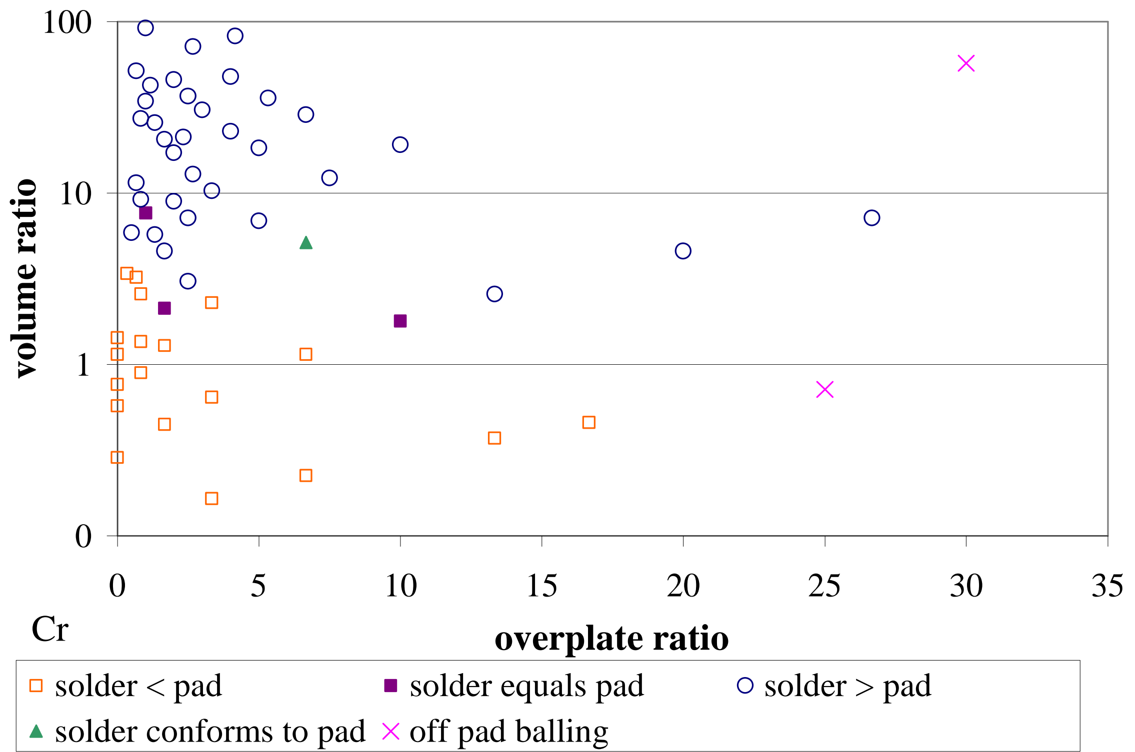


Figure3- 16: Reflowed Cr/Au/In multiple overplate test structure characterization

These figures summarize both the wetting and tearing of the solder. The data was put into categories based on the shape and position of the solder mound as outlined in Figure 3-17.

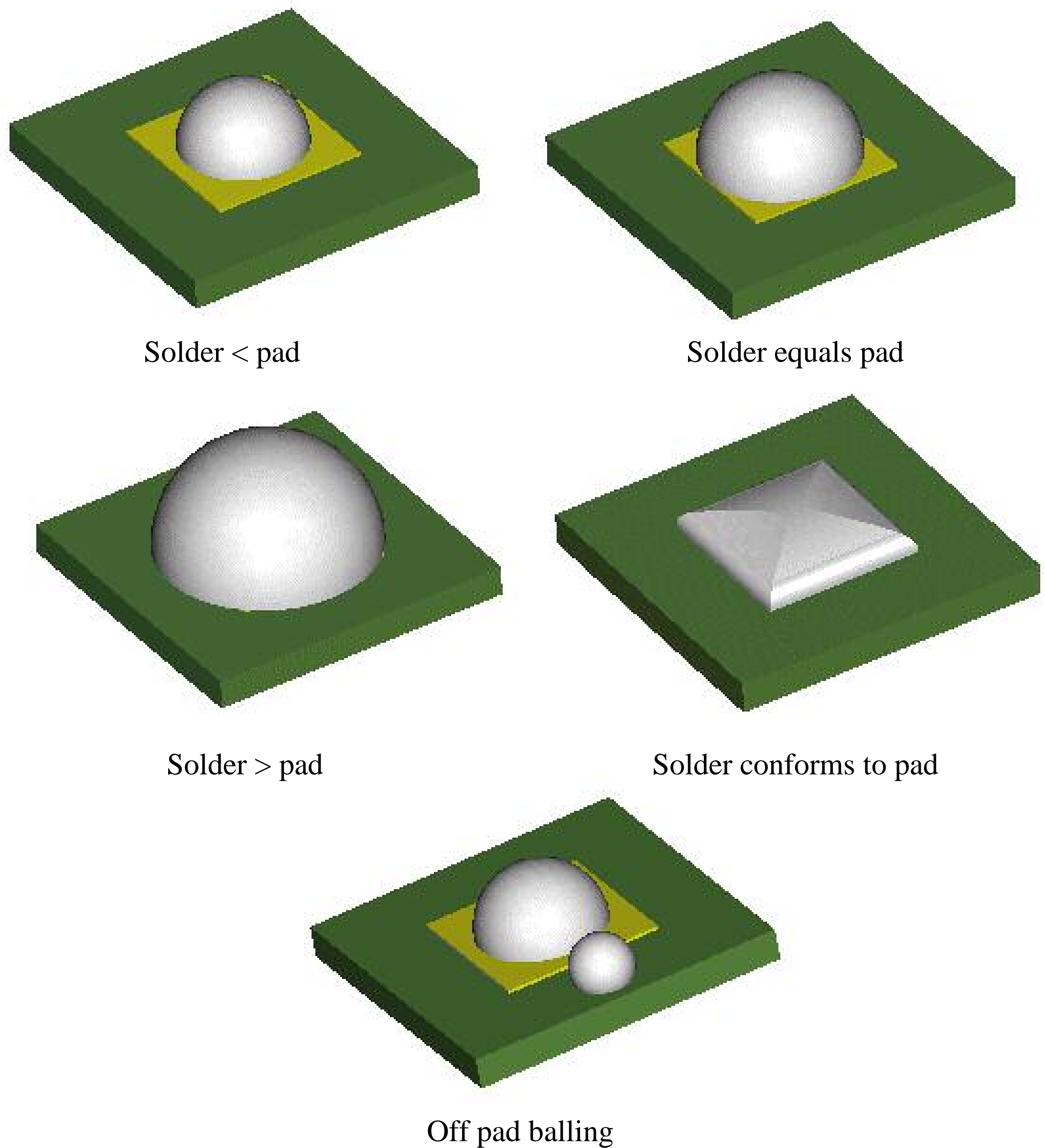


Figure 3-17: Categories post reflow shapes of open faced solder joints

The wetting characteristics are captured by the size of the solder mound on the pad. Samples that have solder mounds smaller than the metallized pad failed to completely wet the pad. Samples that conform to the pad demonstrate a strong affinity between the

solder and the pad. Samples with a mound larger than the pad have an excess of solder. The off-pad balling is indicative of a sample that tore into discrete volumes of solder, leaving a mound of solder off the pad. A more in depth analysis of off-pad balling is discussed in Sections 3.3.2.3 and 3.3.2.4.

TiW samples with volume ratios ranging from 0.2 to 1.8 and overplate ratios ranging from 0.25 to 25 typically conformed to the pad. Conforming samples with large overplate ratios, for example 16 and 25, also experienced off-pad balling. The Cr samples typically did not conform to the pad, an indication that the indium did not wet the Cr as well as it wet to the TiW.

To further illustrate the superior wetting of the indium to the TiW. Compare the results of concurrently cleaned and reflowed structures in Figure 3-18 and Figure 3-19.

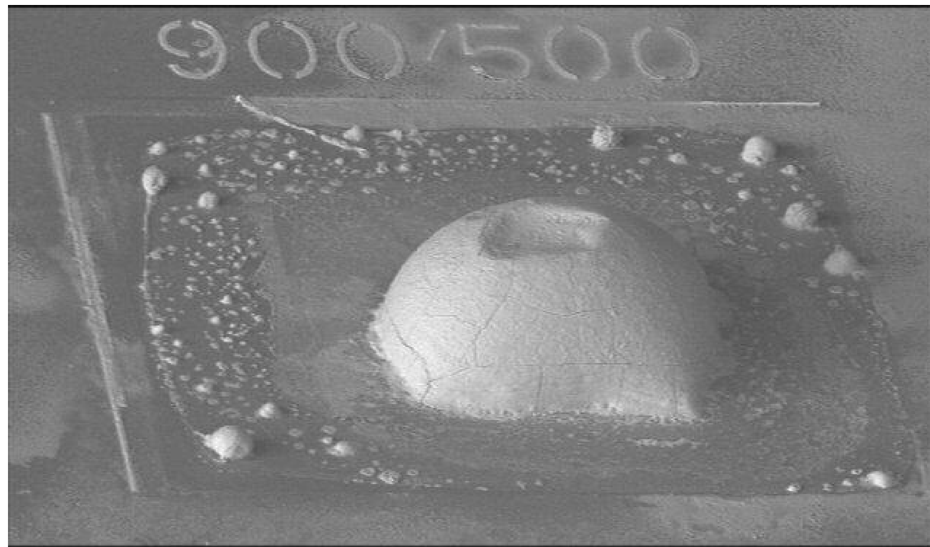


Figure 3-18: 900 x 900 x 15 μm indium on 500 x 500 μm Cr/Au pad after reflow

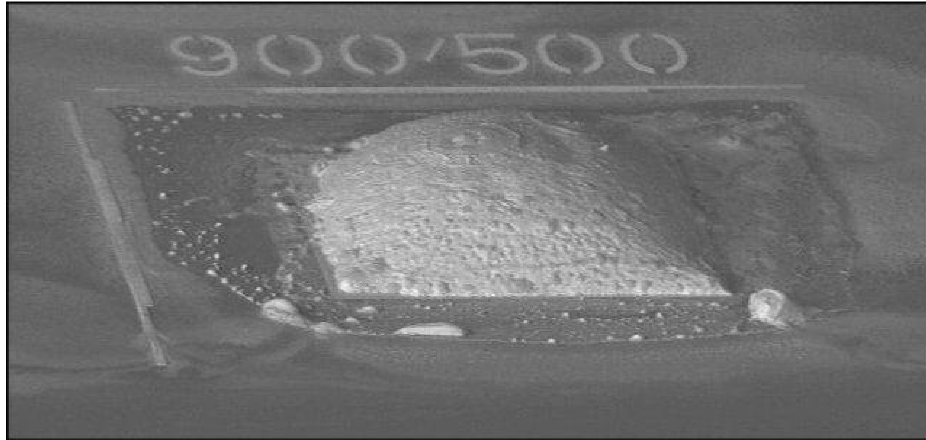


Figure 3-19: 900 x 900 x 15 µm indium on 500 x 500 µm TiW pad after reflow

The samples in Figure 3-18 and Figure 3-19 have a volume ratio of 0.4 and an overplate ratio of 13.3. The Cr sample has a wetting angle below 90°, but still failed to wet the entire pad. The TiW sample had a much lower wetting angle and conformed to the square pad.

Structures with volume ratios above 2 typically would not fit onto the metallization pad. These samples do not provide insight into the wetting properties. However, they do illustrate ability to pull large volumes of solder into small metallized regions. Figure 3-20 depicts a solder mound formed on Cr with a volume ratio of 13 and a volume ratio of 2.7.

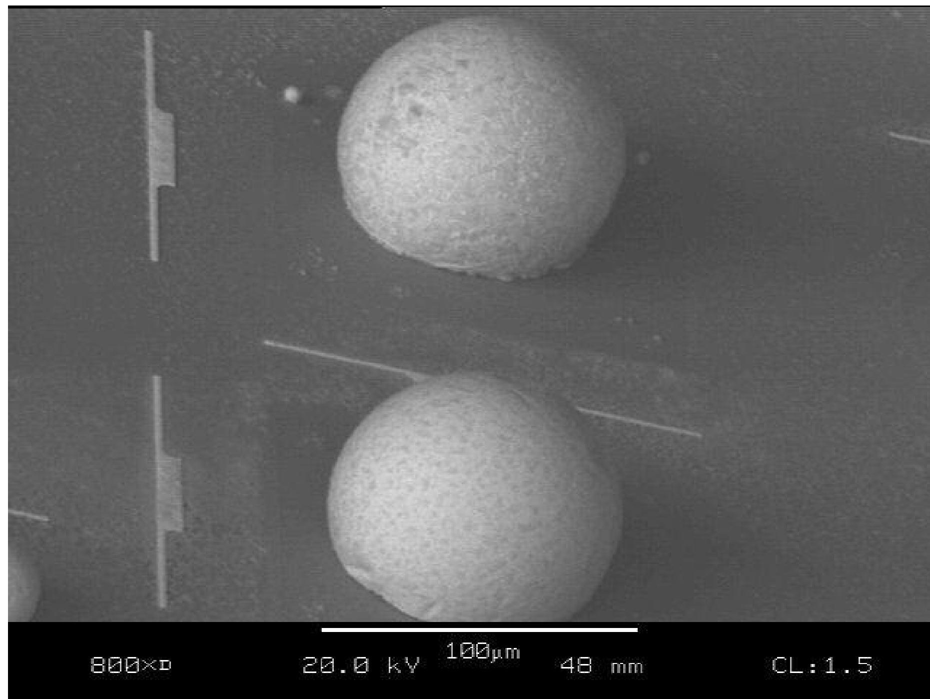


Figure 3-20: Mound spanning metallization pad and beyond

Note that virtually all of the solder has pulled in to form a mound, leaving very little solder behind. Clearly the oxide did not inhibit the solder flow and the solder did not tear despite the large overplate ratio. Also note that the wetting angle between the indium and silicon is greater approximately 135°. These large solder volume structures have a tendency to leave less solder off of the metallized pad. This is due to the lower gold concentration in the solder joint. Recall that the higher gold concentration results in precipitation of solid intermetallics during the reflow process.

Referring back to Figure 3-13 and Figure 3-14, note that the TiW samples experienced more off-pad balling than the Cr sample. However, neither suffered from significant off-pad balling for overplate ratios below 15. An example of significant off-pad balling is shown in Figure 3-21.

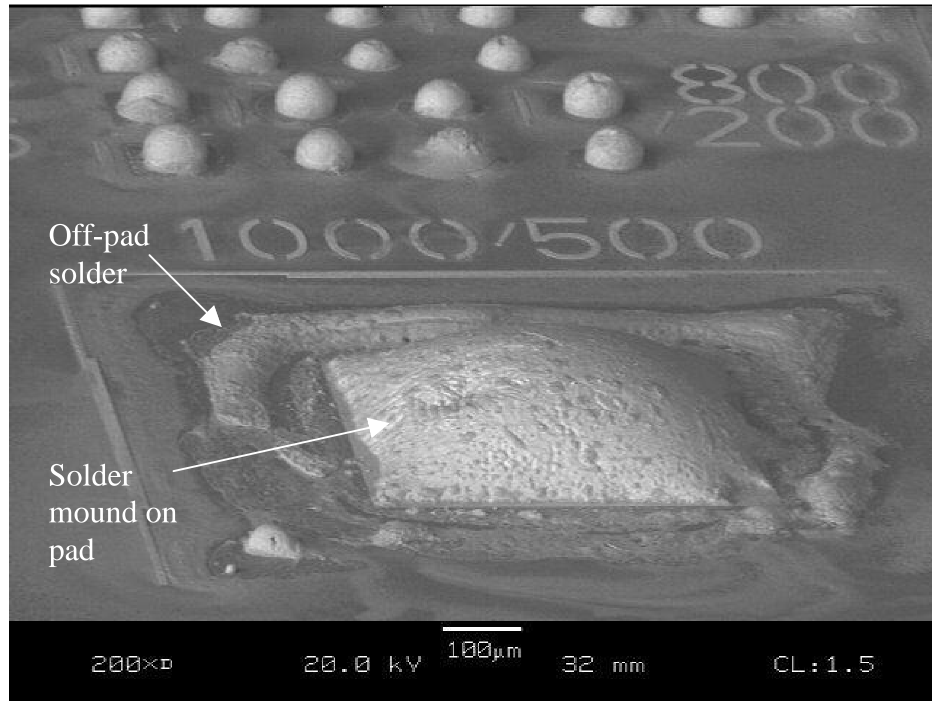


Figure 3-21: Off-pad balling of solder

Chromium samples did not exhibit off-pad balling until the overplate ratio reached 25. Two factors may have contributed to the higher incidence of off-pad balling of the TiW structures. First the thickness of the gold layer on TiW structures is 5 times that of the Cr structures (5000 Å versus 1000 Å). The intermetallic region does not melt at as low of a temperature as the pure indium and can lead to tearing of the solder. The torn solder then balls up in place. Another source of the solder tearing to form localized balls is that the TiW structures have stronger wetting forces, which could act alone to separate the molten indium.

Another interesting result of the solder reflow of the multiple overplate test coupon is the effect of metallization pad size. The structures with larger metallization pads had a greater tendency to be completely filled with solder, Figure 3-22.

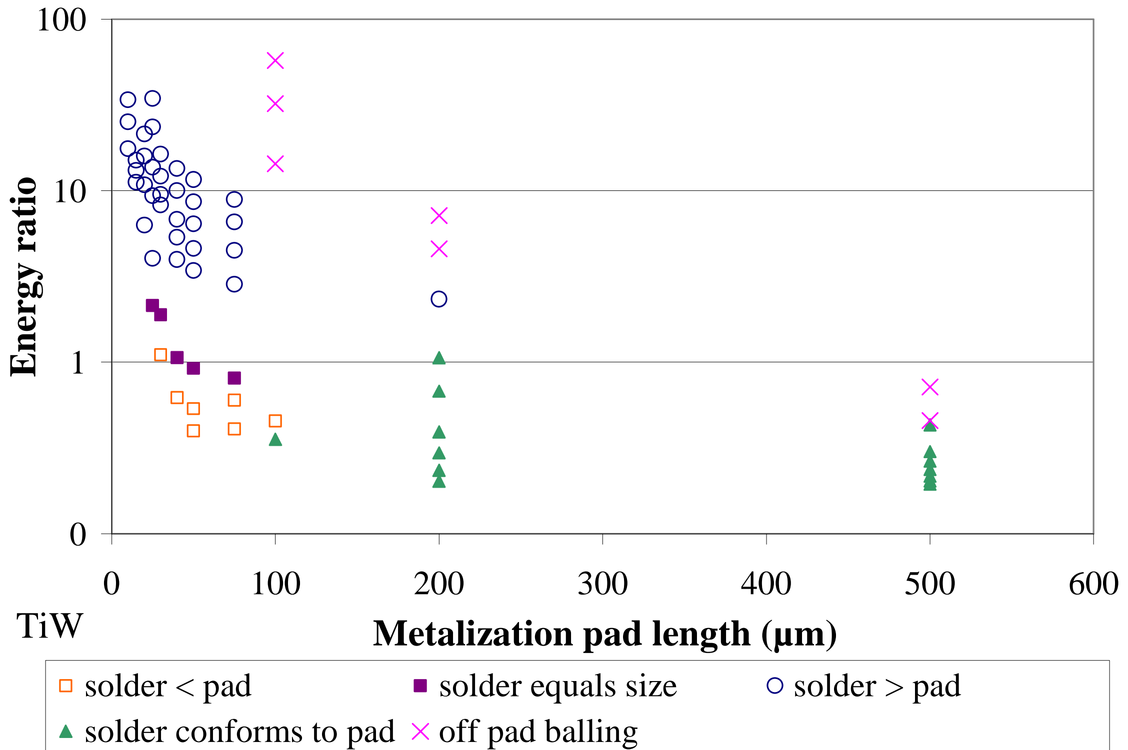


Figure 3-22: Pad size effects on solder wetting

Considering the results in Figure 3-22 as representative of other samples, the solder did not conform to pads with metallization dimensions below 100 µm. Conversely, the solder conformed to the pad in the majority of the structures with metallization pads greater than 100um. The volume ratio cannot be used alone to predict structures that will conform to the pads. The results are further explored in the modeling section.

3.2.3 Gold evaporated on indium

Both Cr and TiW metallized wafers were coated with indium and then gold. The gold coating was approximately 1000 Å thick. In order to completely eliminate oxide formation in the evaporation chamber, two changes were required in the deposition process: the indium boat was replaced with a crucible to increase the volume of indium, and a gold deposition system was added. Due to funding constraints these changes were made simultaneously. Attempts to reflow both the Cr and TiW metallized wafers without cleaning failed. Several chips were then cleaned with different soak times in a 10% HCl solution, with 10 minutes being the maximum exposure time. In some cases, the cleaning solution etched away the undermetallization, which already suffered from yield loses as described in Section 2.5. The gold indium passivation layer was etched off the remaining structures leaving an oxide free indium pad behind. However, etching off the passivation layer negates the benefit of introducing it in the first place. In addition, the gold passivation layer reduces yields significantly. To investigate the failure of the gold to passivate the indium, samples were inspected in a SEM. A TiW sample is shown in Figure 3-23.

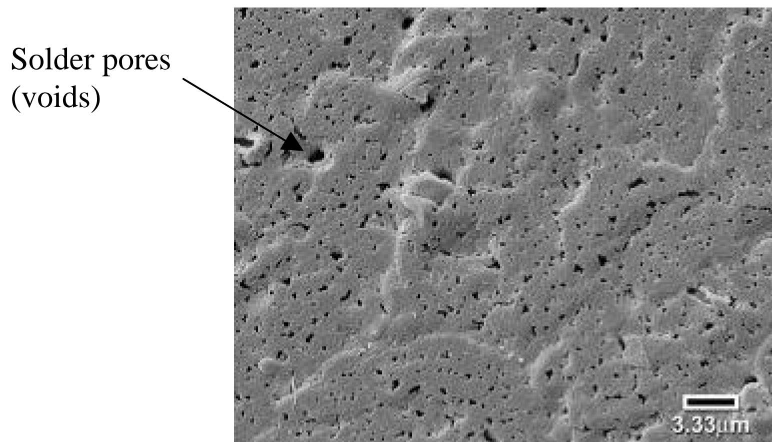


Figure 3-23: TiW/Au/In/Au test structure on pad, crucible deposited indium

Large holes on the order of a 1 µm can be seen in the surface of the indium in Figure 3-11. Clearly the 1000 Å gold layer was unable to passivate a surface of this porosity. Alternatively, runs that were performed with the indium boat rather than the crucible did not result in such large pores in the surface of the indium, Figure 3-24 and Figure 3-25.

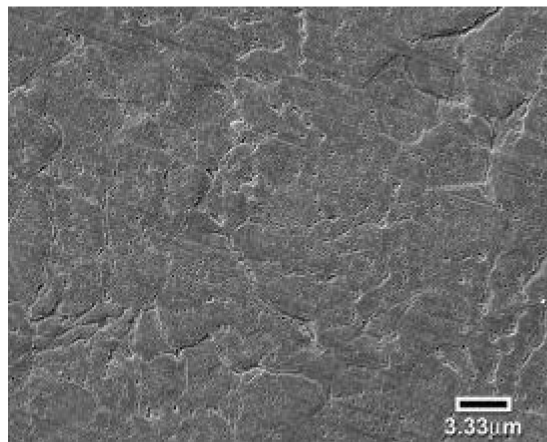


Figure 3-24: Cr/Au/In surface on pad, boat deposited indium

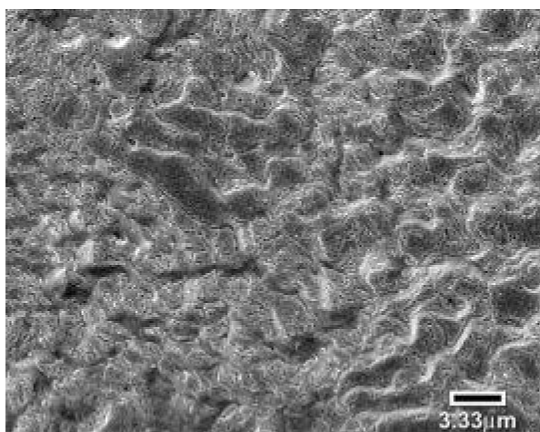


Figure 3-25: TiWIn surface on pad (DRIE wafer), boat deposited indium

The gold passivation technique lends itself better to the boat approach for indium deposition. However, the solder volume in the boat deposition technique limits the indium thickness to only 5 μm. With gold layers above and below the indium, the gold content of the joint is higher than the desired 3% gold by weight (5% gold by weight for a 1000 Å gold layers with 5 μm indium layer). With additional processing experimentation, the temperature during deposition of the indium using the crucible could be reduced, to both improve yield and reduce porosity to enable adequate gold passivation.

3.2.4 Localized heating reflow results

The resistive heating test structures were reflowed in the reducing environment after cleaning in 10% hydrochloric acid. The current was increased until a reflow of solder was achieved on the 125 μm heaters. For the Cr/Au samples, current below 500

mA failed to reflow the test structures. However, 700 mA reflowed the solder on both the 125 µm and 250 µm gold heaters. The reflow of the solder on a Cr/Au chip is shown in Figure 3-26.

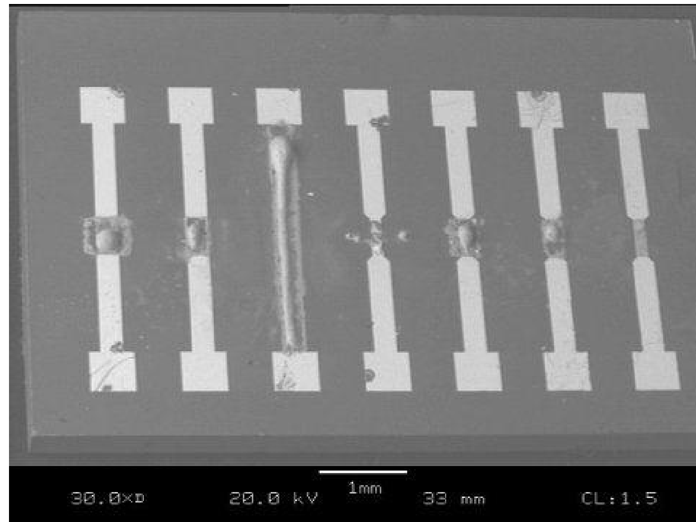


Figure 3-26: Localized reflow test chip: after reflow

A close-up of one of the reflowed structures is shown in Figure 3-27.

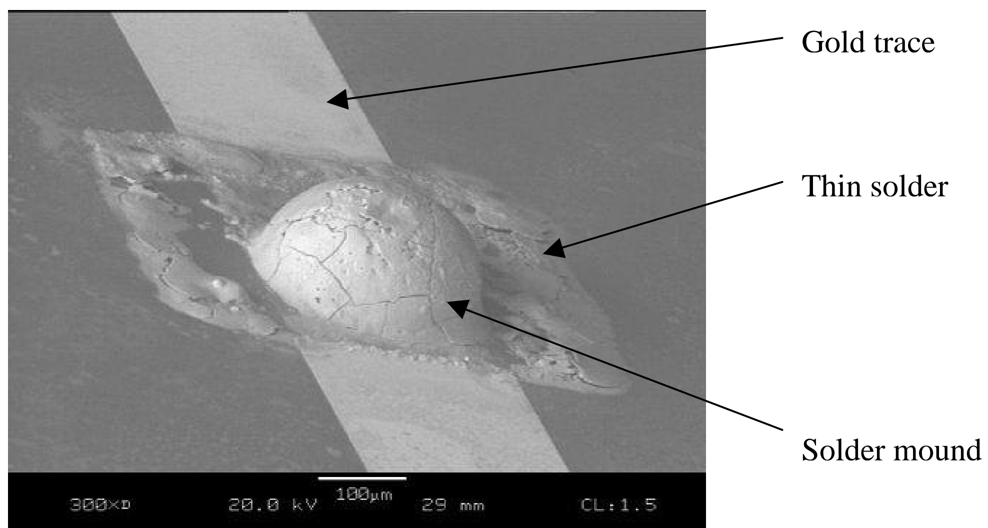


Figure 3-27: Close-up of localized reflow solder mound

Note that most of the solder pulled in from the non-metallized area to the metallized area. This characteristic was true of all of the locally reflowed solder joints.

3.3 Modeling

The solder geometry and energy state after reflow was modeled using Surface Evolver [71]. Surface Evolver is software developed at Susquehanna University by Kenneth Brakke to study the surfaces shaped by surface tension and other energies, such as gravitational potential energy. It evolves a user define shape to a minimal energy state constrained by user applied boundary conditions.

Three models for the open faced structures are presented in this section. First, the open faced structures are modeled assuming perfect wetting to the pad without any wetting off-pad. Next, open faced structures are modeled, but are not forced to wet the entire metallization pad and do not wet off-pad. Finally, a model for the case where the solder preferably wets the metallization pad, but also wets the non-metallized areas is presented.

A model of the solder joint formed between the fiber and the channel is presented. The stability of this solder joint and the factors that affect the potential for dewetting are discussed.

Surface Evolver uses its own language to define the geometry, boundary conditions, material properties, and external loading on the fluid under study. A user

manual is available on-line [71]. A text editor was used to create the data files for input into the surface evolver program. After the model is loaded into Surface Evolver, the model is evolved through a series of iterations of the fluid shape by the program and refinements and corrections of the mesh by the user. Due to saddle points, the model has to be iterated properly to evolve the fluid to its minimal energy state.

3.3.1 Young's wetting model

The affinity of a liquid droplet for a solid surface can be characterized by the contact angle formed at the liquid, solid, and vapor interface. The contact angle, θ, is measured between the liquid and the solid, Figure 3-28. During reflow, the liquid solder will flow to its equilibrium shape defined by the contact angle.

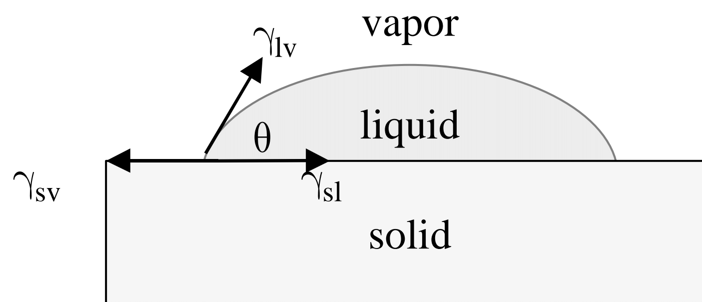


Figure 3-28: Surface tension forces and wetting angle of a solid-liquid-vapor interface

A force balance of Figure 3-28 results in the classical wetting model, called Young's equation [100]:

$$\gamma_{lv} \cos\theta = \gamma_{sv} - \gamma_{sl} \tag{3.2}$$

Where γ_{lv} is the surface tension between the fluid and the vapor, γ_{sv} is the surface tension between the solid and the vapor, and γ_{sl} is the surface tension between the solid and the liquid, and θ is the wetting angle. The surface tension is typically reported as force/length. In the world of solder modeling, the surface tension is often conceptualized as an energy density, or energy per area. In the literature, (3.2) is referred to as both a force balance, a vector quantity necessary to derive the equation, and as an energy balance for conceptualization. Equation (3.2) assumes that there is no chemical interaction between the liquid, and the solid and vapor surroundings. Further analysis of (3.1) results in a qualitative understanding of the wetting angle and its effect on the final joint shape. If $\gamma_{sv} > \gamma_{sl}$, then the solder will spread until equilibrium is achieved. However, if $\gamma_{sv} < \gamma_{sl}$, then the solder will retract until equilibrium is achieved. To better understand the quantities that affect the wetting angle, (3.2) can be rearranged in terms of the wetting angle:

$$\cos\theta = \frac{\gamma_{sv} - \gamma_{sl}}{\gamma_{1v}} \tag{3.3}$$

If the angle is less than 90°, than the fluid "wets" the surface. Conceptually, a hemispherical mound of fluid would spread to increase its contact area with the surface. Fluids that have wetting angles above 90°, but below 180°, are considered to have partially wet the substrate.

The wetting area can readily controlled by the solid vapor surface tension. Metallization, which can have a large solid-vapor surface tension, is patterned onto a substrate such as silicon. The surface tension between the silicon and the vapor is small, thus the solder does not wet to this material and will tend to retract away from it (force balance favors a retraction of the solder). Conversely, the surface tension between the metallization and the vapor is large, thus favoring a spreading of the solder onto this material.

One of the metrics in the evaluation of a “good” solder joint is the wetting angle. Although it cannot be used to predict bond strength, a low wetting angle is indicative of good affinity of the solder for the undermetallization. More specifically, wetting angle is an indicator of the cleanliness of the soldering process, which does influence the strength of the final joint. Consider again the equation for the wetting angle, (3.3). The wetting angle can be decreased by increasing the surface tension between the solid and the vapor, or by decreasing the surface tension between the liquid and the solid or vapor. Oxidation is the primary source of wetting problems and hence the wide spread use of fluxes. Oxides, and other contaminants, on the pad to be wetted decrease the surface tension between the solid and the vapor and thus increase the wetting angle on the metallization. It follows that cleaning is instrumental in maintaining both a metallization area that is conducive to wetting and solder that is capable of spreading. Other factors also affect the wetting angle of the solder. The surface coefficients are properties of the temperature, pressure, and the material themselves. Generally speaking, higher temperatures and lower pressures result in lower wetting angles. Confinement of large amounts of solder

to a metallization pad also will increase the wetting angle, but in this case wetting angle is not a relevant measurement technique of the affinity of the solder to the metal.

The wetting equation (3.1) has been demonstrated to be invalid in practical applications [83, 101]. The assumptions involved in the derivation of the wetting equation, neglecting hydrodynamic forces and interaction between the materials involved, break down when trying to use measured surface tension coefficients to calculate the wetting angle. More complex models have been developed [102], but again their ability to predict wetting angle has been disappointing. As a result, wetting angles are obtained empirically. Although Young's equation does not provide quantitative information about the relationship between the surface tensions and the wetting angles due to the broad assumptions needed to arrive at Young's equation, it is useful in providing a qualitative understanding of the factors that govern the wetting process.

Consider again (3.2), only this time from an energy perspective. The right hand side of (3.2) is the surface energy change per area at the solid-fluid interface due to the flow of the solder. Thus the surface tension of the solid-vapor interface and the wetting angle govern the energy change from the surface wetting. Combined with the energy change from the change in surface area of the fluid-vapor interface, the final joint shape can be predicted through an energy balance. Surface Evolver was used to predict the final shape and energy state of the solder by balancing these energies as well as other energy sources, such as gravity.

From the energy balance, the forces acting on the liquid solder can be calculated as well. The wetting force between the solder and the solid can be calculated by multiplying

(3.2) by the characteristic wetting length normal to the direction of the force.

$$F = \gamma_{lv} l \cos\theta \tag{3.4}$$

Where F is the force and l is the characteristic length of the solder pad (side length on a square pad or diameter on a round pad).

3.3.2 Surface Evolver modeling

Surface evolver models can be interrogated to report energy, force, pressure, and geometry of the evolved shape. Several models were used to analyze the open faced solder test structures. The first model, called "vol2.fe" in Appendix B, allowed the solder to flow without constraints to its wetting area. This model provided insight to the behavior of the solder, but failed to accurately predict the final solder shape and energy state for most practical applications due to lack of confinement to the wetting surface. However, the energy state of the solder in this model is used to normalize the energy in successive models thus providing a useful comparison of the final solder shape stability.

The second model, called "wetfix.fe" in Appendix B, constrained the solder to completely wet the metallization pad. This model is valid for samples that had sufficient solder volume in the vicinity of the metallization pad. For structures in which the spread area at equilibrium was less than the metallization area, incomplete wetting of the pad occurred and the assumption, and thus the model for complete pad wetting, is invalidated. For these cases, the previous model with condition of complete wetting relaxed provides a measure of the likelihood of the retraction of the solder from the metallization pad.

Next, two additional models are presented to address the wetability of the silicon, which is considered completely unwetable in the previous models. These models are also included in Appendix B as “tearnew.fe” and “varwet2.fe”. Lastly, the model of the solder between the fiber and the fiber groove is presented and discussed.

3.3.2.1 Open face solder joint; solder free to pull in

Consider first the model where the solder is permitted to pull in. Figure 3-29 shows the solder shape before reflow and after reflow with two different wetting angles.

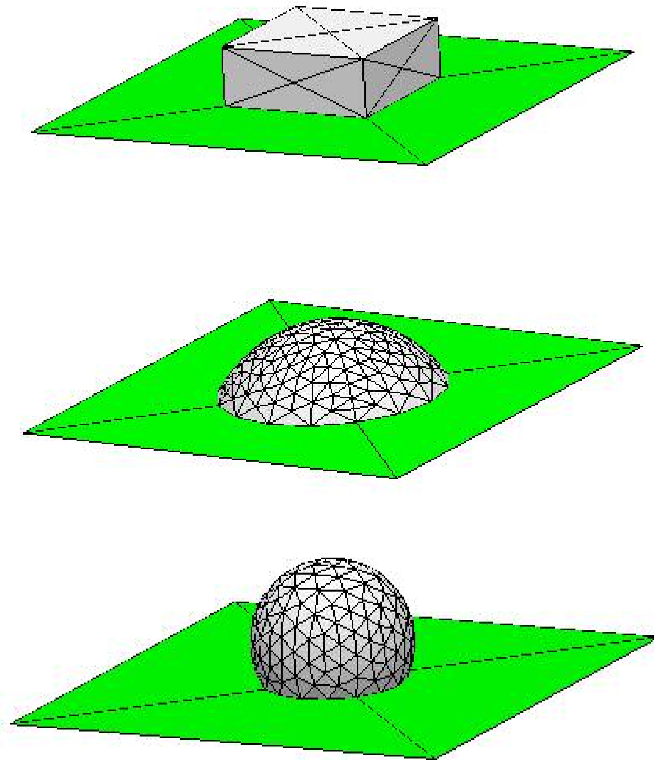


Figure 3-29: Surface Evolver model results with solder free to wet entire surface: before reflow (top), 60° wet angle (middle), and 120° wet angle (bottom)

Clearly, the solder can be seen to flow to a half mound shape. If the wetting angle is 90°, then the mound is a hemisphere shape. The diameter of the solder mound for various wetting angles and volumes are shown in Figure 3-30.

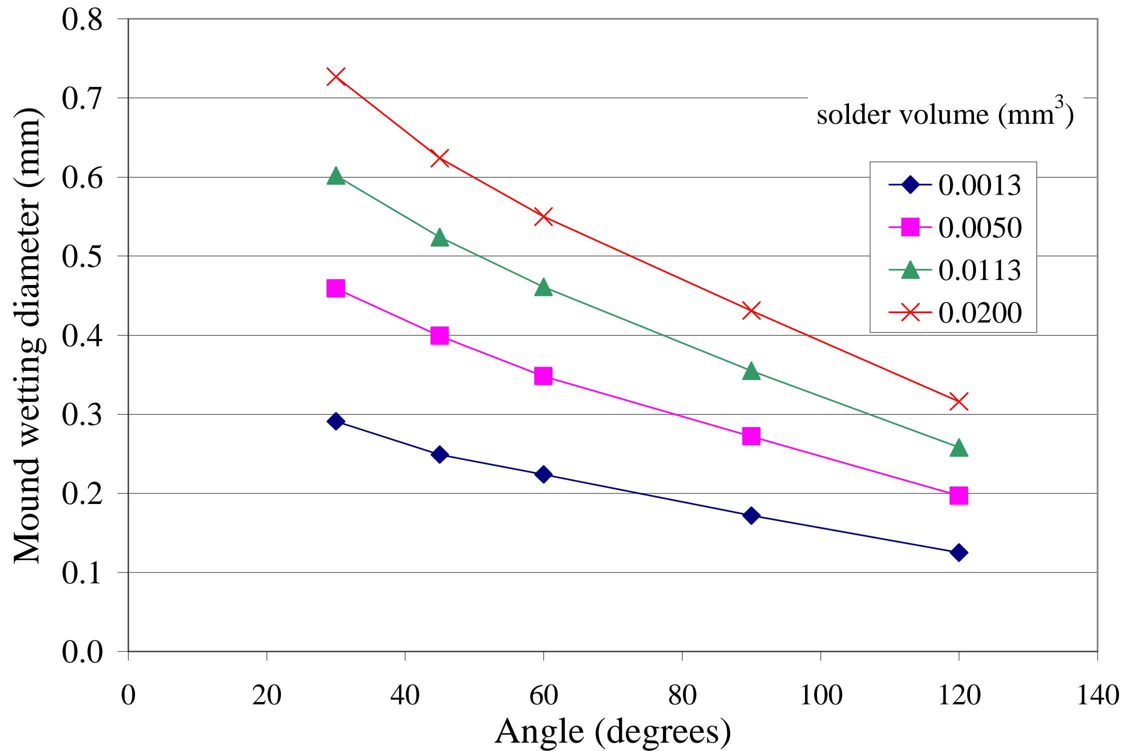


Figure 3-30: Effect of wetting angle and volume on wetting diameter (from open face model with free boundary conditions)

As expected, the wetting diameter decreases as the wetting angle is increased. The wetting diameter for a given solder volume with 120° wetting angle is less half of an equivalent volume solder mound with a 30° wetting angle. This translates to less than a quarter of the area, thus reducing the bond strength of the resultant solder joint. This relationship holds independent of the solder volume.

To investigate the shape dependence on volume, the solder mound diameter is normalized by the volume of the solder (Figure 3-31).

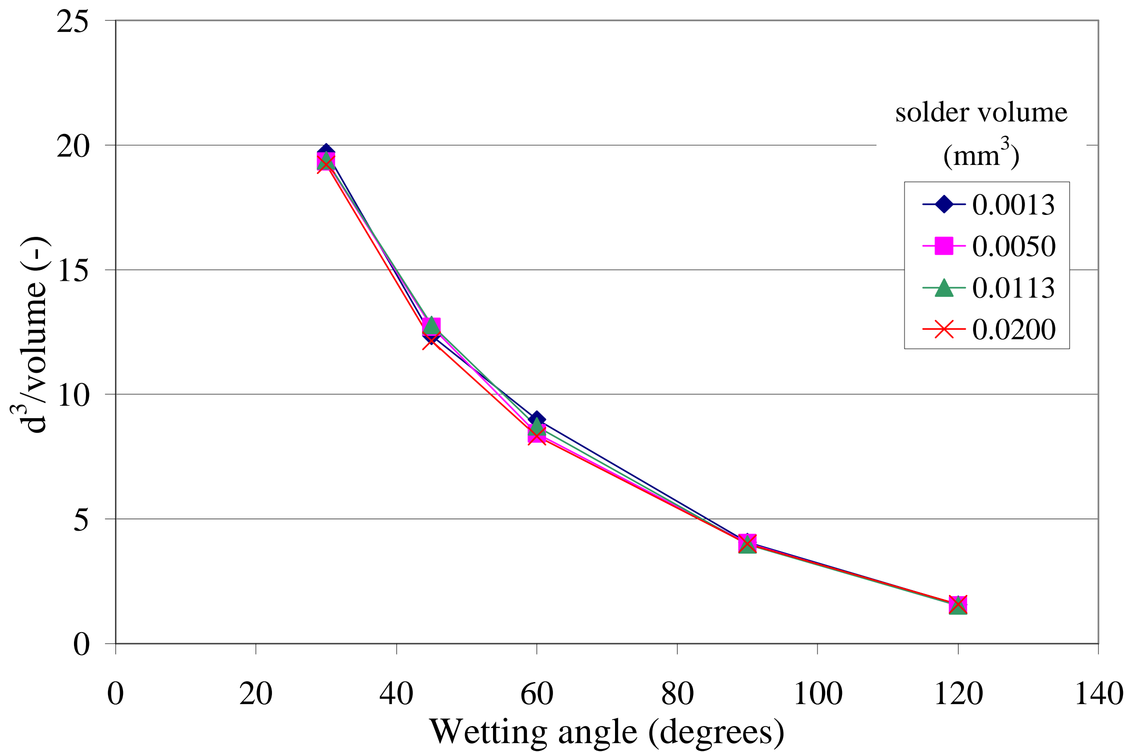


Figure 3-31: Normalization of solder mound diameter by solder volume (from open face model with free boundary conditions)

For the model presented here, the shape of the solder is independent of the solder volume. This holds true for a mound of solder free to wet an infinite flat surface in the absence of gravity or other body forces. For the solder volumes of interest in this dissertation, the gravity body force plays an insignificant role in shape and energy state of the solder and is thus neglected.

The energy dependence of the final fluid solder shape on the wetting angle and volume is shown in Figure 3-32.

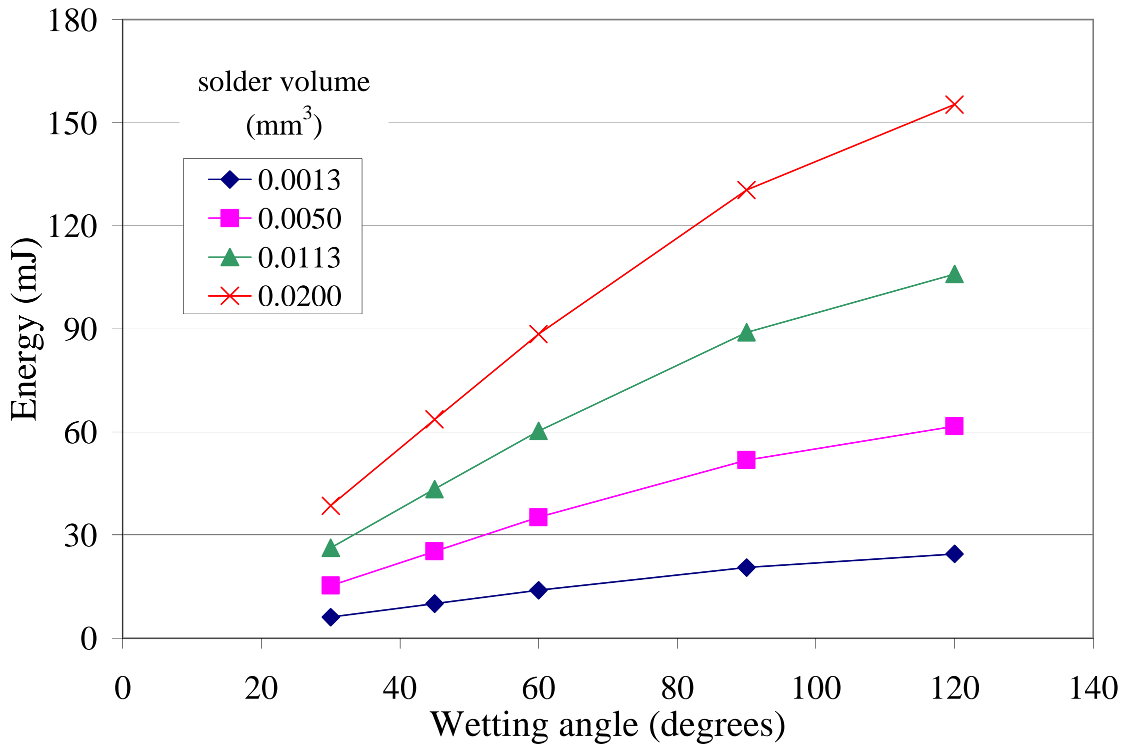


Figure 3-32: Effect of wetting angle and solder volume on fluid solder energy (from open face model with free boundary conditions)

In addition to reducing the bond area of the solder joint, larger wetting angles also result in a higher energy state and thus higher stress in the fluid solder mound. A solder mound with a 120° wetting diameter has over three times the energy of an equivalent solder mound with a 30° wetting angle. Larger volume solder joints have more energy merely due their size. The dominant source of energy in a fluid solder joint results from surface area effects.

To get an effective comparison between the different solder volumes, the energy can be normalized by the energy of a hemisphere with an equivalent volume. The surface

energy of a solder mounds results from the energy between the solder and the vapor and the solder and the solid.

$$E_{surf} = E_{lv} + E_{sl} \tag{3.5}$$

Where E_{surf} is the total surface energy of the fluid solder, E_{lv} is the energy between the liquid solder and the vapor, and E_{sl} is the energy between the solid metallization pad and the liquid solder. The energy between the fluid solder and the metallization pad can be derived from the wetting equation:

$$E_{sl} = \gamma_{sl} A_{wet} \cos\theta \tag{3.6}$$

Where γ_{sl} is the surface tension between the solid and the liquid, A_{wet} is the area wetted by the solder. For the case of a hemisphere, the wetting angle is 90° and the energy between the solder and the metallization pad goes to zero. Equation (3.5) then reduces to

$$E_{surf} = E_{lv} \tag{3.7}$$

The energy between the solder and the vapor is given by:

$$E_{lv} = \gamma_{sl} A_{surf} \tag{3.8}$$

Where the A_{surf} is the area between the solder and the vapor. The surface area can be expressed in terms of volume resulting in an expression of the surface energy of a hemispherical mound in terms of volume.

$$E_{lv} = 2\pi \left(\frac{3V}{2\pi}\right)^{2/3} \tag{3.9}$$

Where V is the volume of the solder. Equation (3.9) was used to normalize the energy output of the surface evolver model, Figure 3-33.

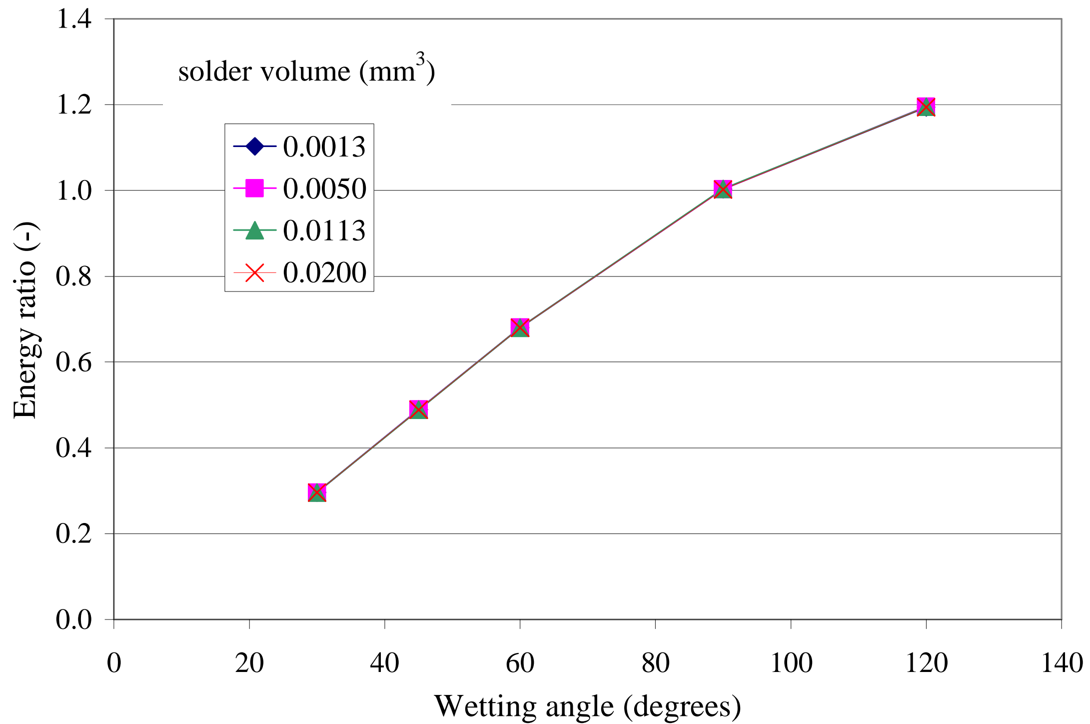


Figure 3-33: Energy normalized by the energy of an equivalent volume wetted hemispherical mound (from open face model with free boundary conditions)

The energy ratio for all the solder volumes collapses onto a single curve. This agrees with the conclusion from Figure 3-31 that solder shape is independent of the solder volume. Note that the energy ratio at 90° wetting angle has an energy ratio of one as expected. In considering solder joint stabilities, the energy ratio can be used to express the relative energy state of the solder. This tool provides a normalization tool to predict instability of a solder shape independent of the solder volume. An excessive relative energy state can lead to dewetting of the pad or tearing of the solder.

3.3.2.2 Open face solder joint; solder forced to wet pad

Next, consider the model where the solder is forced to wet the entire pad. The displacement constraints placed on the solder prevent it from pulling in to evolve into a lower energy state. The energy states predicted by this model are depicted in Figure 3-34.

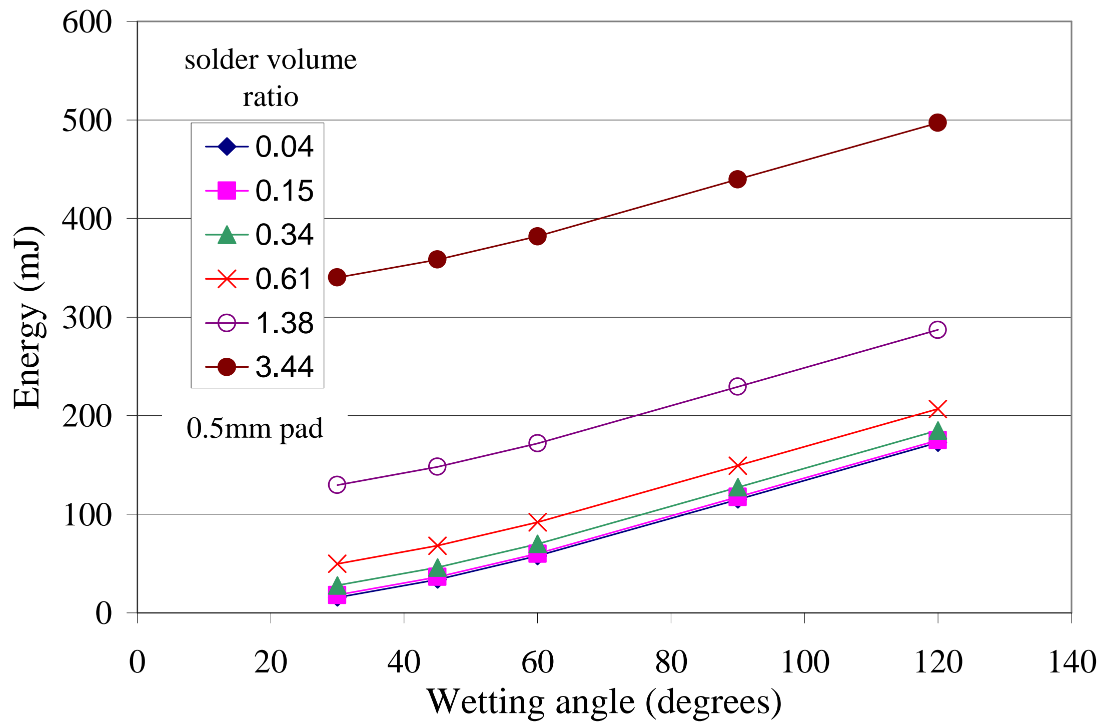


Figure 3-34: Effect of wetting angle and solder volume on fluid solder energy (from open face model with solder forced to wet metallization pad)

A new term, volume ratio, is introduced in Figure 3-34. The volume ratio is defined as the ratio of the solder volume to the volume of a hemispherical mound that is inscribed on the square metallization pad. This ratio provides a more insightful means to understand the effects of the relative amount of solder on the pad. For example, a joint

with a solder volume ratio of 2 would have 2 times the amount of solder necessary on a pad to from a hemisphere. In comparing the energy results from the free boundary condition model, Figure 3-32, to the fixed boundary model, Figure 3-34, note that the energy level is much higher for the fixed boundary condition. Both models indicate that the energy increases as the volume increases.

To better interpret the model energy results, the data can be normalized by the energy of an equivalent hemispherical mound of solder, Figure 3-35. Note that the both the energy and volume normalizations used reference the state of a hemispherical mound.

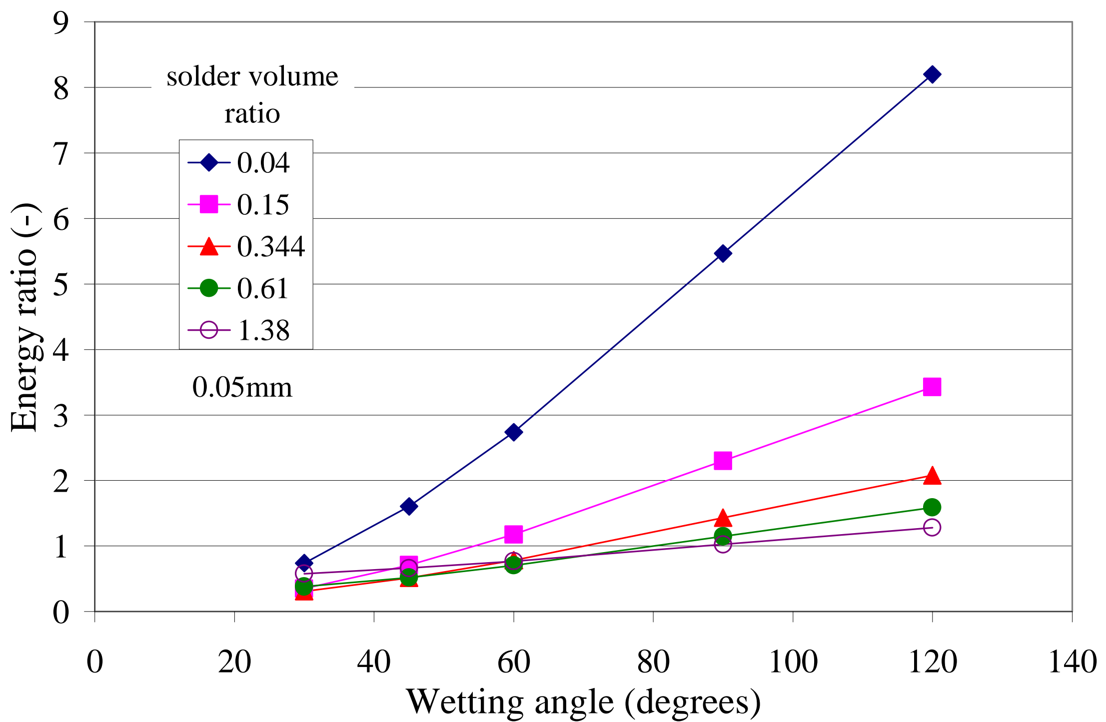


Figure 3-35: Energy ratio of solder on a 0.5mm pad (from open face model with fixed boundary conditions)

For the cases analyzed, the energy of the solder in the fixed case can now be seen to be as much as nine times greater than if the solder was allowed to flow to a hemispherical shape. For the fixed boundary condition, the energy ratios in the fluid solder increases as the solder volume decreases. This is due to the fact that the dominant source of energy is between the solder and the metallization. It can be deduced from this result that a superior wetting angle is needed to wet a given solder pad with less solder.

Next, consider the effects of volume ratio on the energy ratio. A joint with a volume ratio much less than 1 does not have sufficient solder to form a mound. If good wetting is not achieved, the solder depraved pads have a very high relative energy state, as indicated by the 0.04 volume ration curve. Conversely, a joint with a volume ratio of 1 or more can form more of a taller mound shape. Consider the case where the solder volume is much less than what is needed to form a hemispherical mound on the pad. The shape of the solder joint for a volume ratio of 0.04 is shown in Figure 3-36.

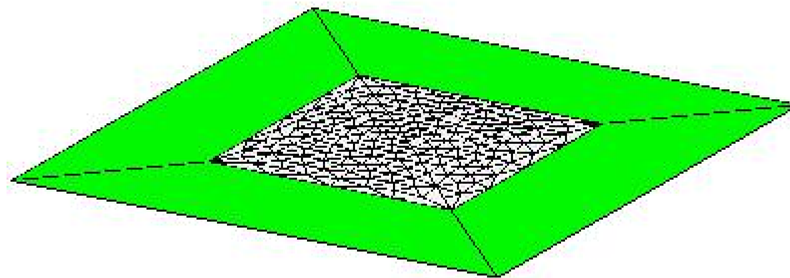


Figure 3-36: Open face model shape prediction for solder constrained to metallization pad; volume ratio 0.04

For this volume ratio, the shape is essentially the same for all the wetting angles. However, if good wetting is not achieved between the metallization and the solder, the

energy state of the fluid is large in comparison to hemispherical mound of the same volume. These excessive forces can then lead to a dewetting of the pad as seen in the experimental portion of this effort, particularly with the chromium samples. If excellent wetting is achieved (e.g., <30°), even the smallest volume ratio reported in Figure 3-35 can have a lower energy state than its hemisphere equivalent (energy ratio < 1).

Next, consider the case where there is sufficient solder to form a more of a mound shape (volume ratios from 0.3 to 1.4). Figure 3-37 shows the model prediction for the shape of the solder with a volume ratio 0.6.

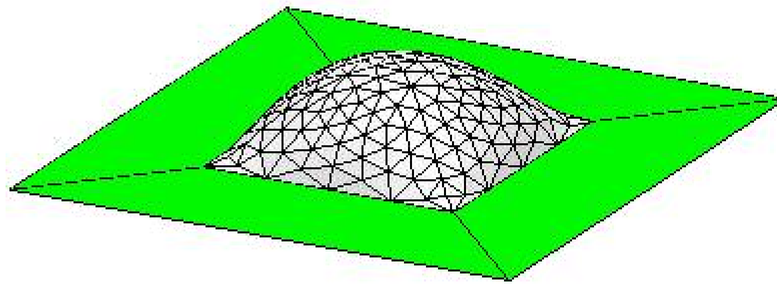


Figure 3-37: Open face model shape prediction for solder constrained to metallization pad; volume ratio 0.6

The wetting angle at the perimeter of the pad can be observed. However, the energy of the fluid solder in this case is less dependent on the quality of the wetting, see Figure 3-35. For these cases with a moderate volume of solder, the surface forces between the solder and the vapor dominate the solder pad forces.

At this point it is interesting to compare the model results to the experimental results of the open faced solder test structures. Since the wetability is dependent on several factors (cleanliness, heat rate, oxygen content, temperature, etc.), determining an

energy level the solder will dewet the pad is not feasible strictly with an energy based modeling tool. The open faced structures shown in Figure 3-38 are identical samples that were reflowed in a slightly different environment. The sample on the left completely wet the metallization pad, while the sample on the right pulled in to a diameter smaller than the metallization pad. The sample on the left had a greater affinity for the metallization, so its minimal energy state was to conform to the pad. The primary factor in the dewetting is the formation of oxides on the metallization. This illustrates the interdependency of the wetting angle, energy state, and shape of the solder.

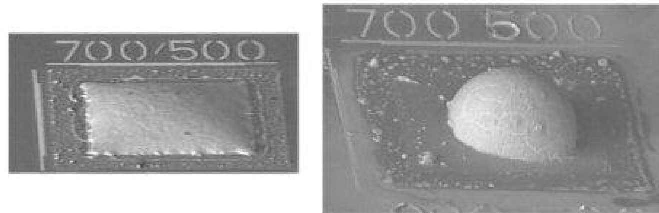


Figure 3-38: Identical design reflow samples with different wetting results (700x700x15µm In pad on 500µm square Cr/Au pad)

However, the energy model is an excellent comparative tool that can guide the designer in the design of a solder joint to minimize the likelihood of dewetting. The geometry of the metallization pad and the volume of solder should be tailored to maintain the energy ratio to reasonable levels. The higher the energy in the solder joint, the more likely the solder is to retract and dewet the pad.

The results for a 0.5mm metallization pad having been presented, consider next the effect of the pad size on the energy content on the fluid solder. The model with the

solder forced to wet the undermetallization was performed on a 0.05 mm and 0.1 mm square pad. When the energy and volume were normalized to those of a hemisphere of equivalent volume, the results collapsed to a single curve, Figure 3-39.

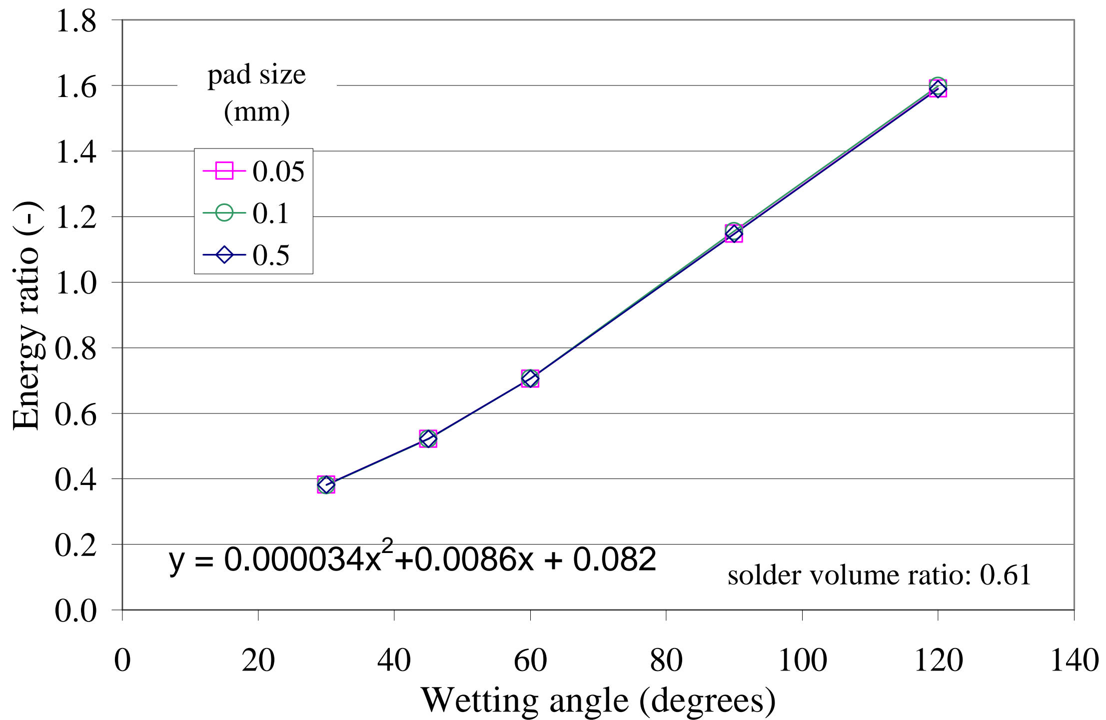


Figure 3-39: Energy ratio of solder as a function of pad size (from Surface Evolver model with fixed boundary conditions)

From Figure 3-39, it can be established that the model presented here can be generically applied to square pads of various dimensions without rerunning the Surface Evolver model. Recall from the discussion concerning Figure 3-33, it was established that the free boundary condition modeling results presented were applicable across the solder volume range of interest if the data was normalized in the fashion presented. It can now be concluded that the output of the fixed boundary condition model can be applied to the

entire range of metallization pad dimensions explored in this dissertation. Perhaps most interestingly, the model predicts that dewetting is not a function of pad size or solder volume. The key parameters are the following:

1. Energy ratio: defined as the ratio of the energy of the resultant fluid solder shape and the energy of a fluid solder hemisphere of the same volume
2. Volume ratio: defined as the ratio of the actual volume of solder on the pad and the volume of a hemisphere inscribed on the pad.

Consider next the reflow results of the multiple overplate solder test structures that were discussed in Section 3.2.2. Recall that the volume ratio was not sufficient to provide guidance on the tendency of the solder to conform to the pad, Figure 3-22. However, the volume ratio coupled with the energy ratio provides a means to predict the post reflow solder shape, Figure 3-40.

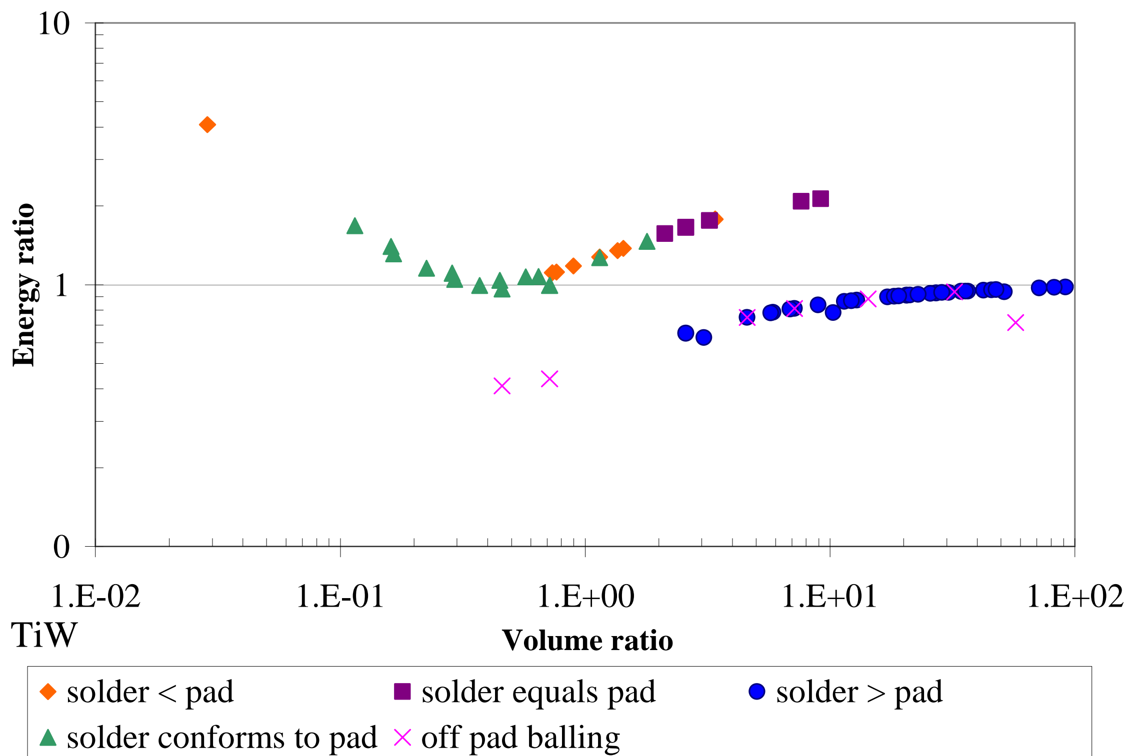


Figure 3-40: Effects of energy and volume ratio on post reflow solder geometry

The solder tends to conform to the pad for energy ratios below 2. If the energy ratio is larger than 2, the solder will dewet the pad (too little volume) or form a mound much larger than the pad (too much volume). For the energy ratio to remain below 2, the volume ratio should be between 0.1 and 2.

3.3.2.3 Open face solder joint; variable wetting angles; single volume

Next, consider the model where the silicon is not a perfect non-wetting surface (that is, the wetting angle is other than 180°). The first attempt to model off-pad wetting was to model the solder as one discrete volume of solder on a substrate with a varying wetting

angle.   A conditional statement was added to the constraints input data to define two distinctly different wetting schemes, Appendix B.4. The results of the model for several off-pad wetting angles and for 45° and 60° wetting angles on the pad are plotted in Figure 3-41.

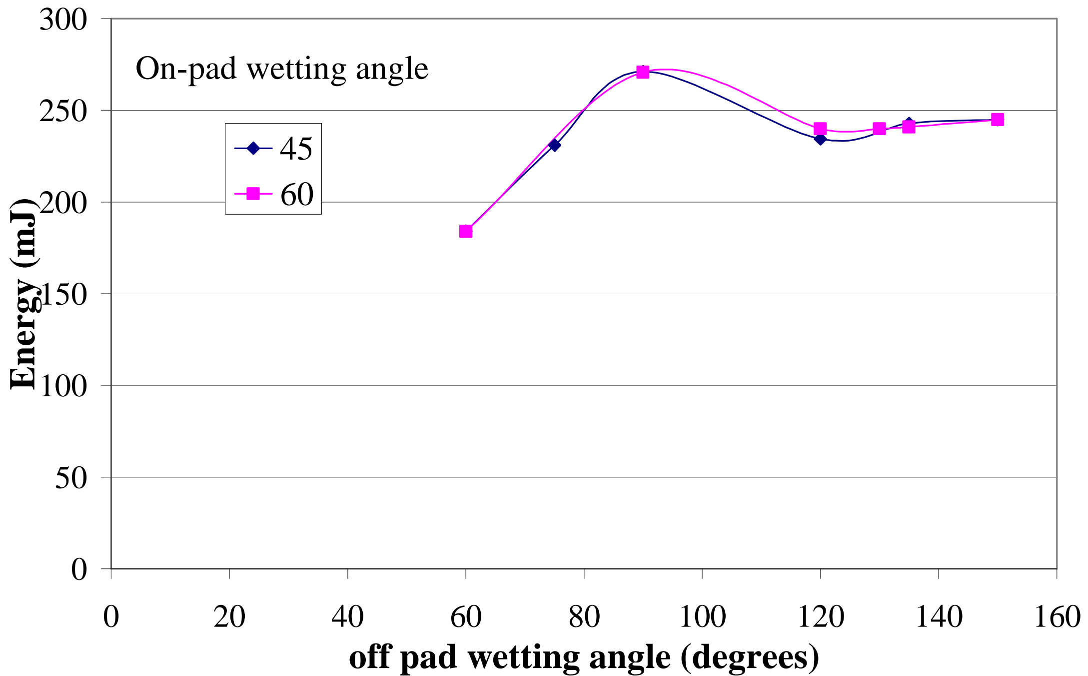


Figure 3-41: Single volume, discrete wetting angle model results

This model failed to properly calculate the energy of the solder that contacts the substrate. If the solder was entirely on the metallization pad, the correct energy was reported. If the solder spanned the metallization pad and the silicon, the energy is not calculated properly. Note that the energy of identical solder joints with different wetting angles result in the same energy state. The actual energy is not independent of the

wetting angle on the pad. A lower wetting angle should result in a lower energy state for the solder. The source of this error was looked into further. The energy can be broken down into two components, the energy between the solder and the surrounding air and the energy from the solder pad interface.

$$E_{total} = E_{gas} + E_{wet} \tag{3.10}$$

The energy for the solder gas interface can be calculated from the surface area calculated in the model:

$$E_{gas} = \gamma A_s \tag{3.11}$$

Where γ is the surface tension between the solder and the surrounding vapor and A_s is the surface area of the exposed solder joint. The wetting energy can be derived from the wetting equation:

$$E_{wet} = \gamma A_{wet} \cos\theta \tag{3.12}$$

Where A_{wet} is the wetted area. For a surface with two discrete wetting angles, the energy can be calculated from the following relationship:

$$E_{wet} = \gamma A_{wet_1} \cos(\theta_1) + \gamma A_{wet_2} \cos(\theta_2) \tag{3.13}$$

where the subscript 1 denotes the area with one wetting angle and subscript 2 denotes the area with a different wetting angle. These above equations were used to break down the energy components from the Surface Evolver model, Figure 3-42.

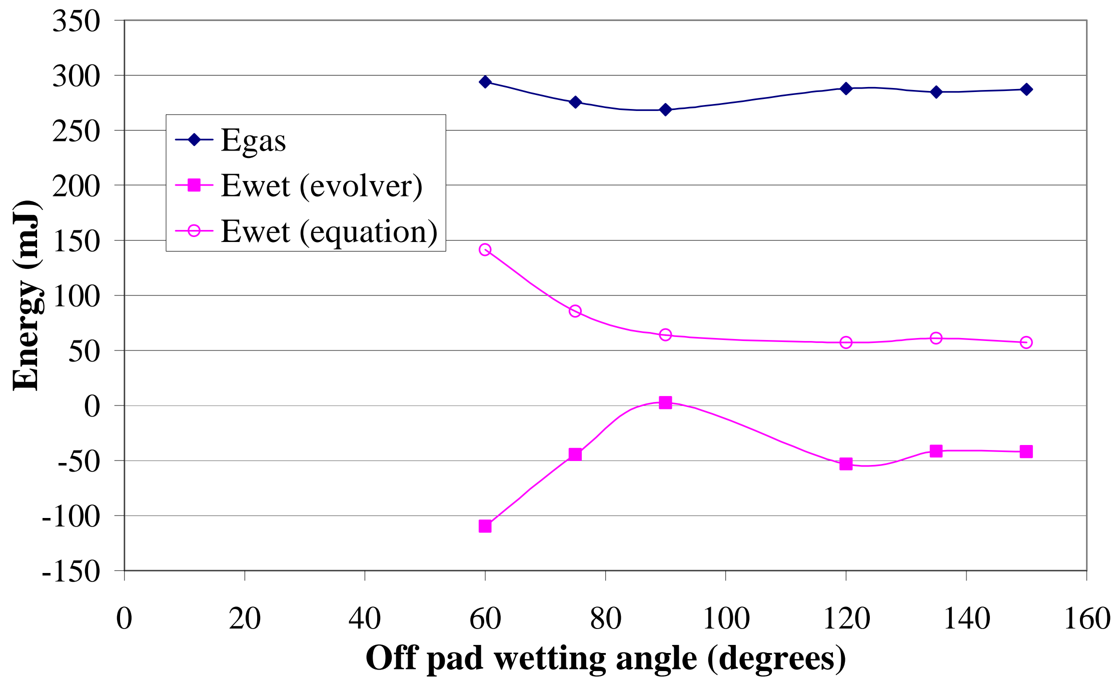


Figure 3-42: Energy components of the variable wetting angle model (45° on pad wetting angle)

Clearly, the wetting energy cannot be neglected and thus does not account for the model discrepancy. Also, note that the model reporting of the wetting energy is significantly different than that calculated by (3.13). Since Evolver uses the wetting energy to predict the final shape of the solder, the discrepancy cannot be corrected in the model output data. It is concluded that Surface Evolver is not able to properly evolve a single volume of solder wetting a surface with two distinct wetting angles. An alternate approach was taken in the next section using several discrete solder volumes.

3.3.2.4 Open face solder joint; variable wetting angles; discrete volumes

The model was constructed by defining a square area, representing the metallization pad, with one wetting angle and the surrounding area with another wetting angle. If the surrounding area is given a wetting angle of 180°, then the result should be the same as free boundary condition model. Figure 3-43 shows the variable wetting angle model results for a 45° wetting angle on the pad and 180° off-pad.

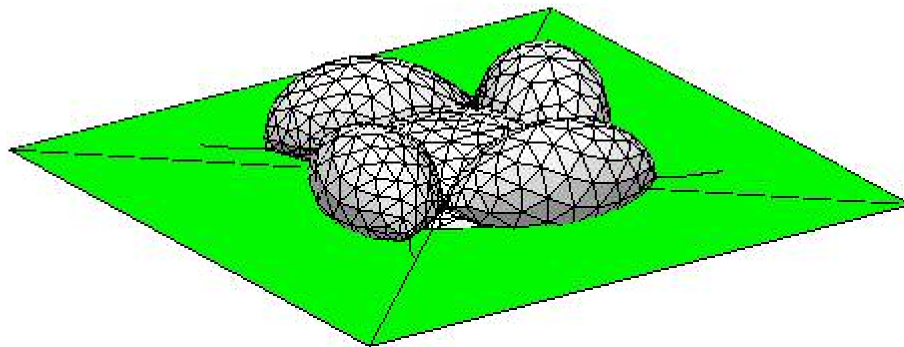


Figure 3-43: Variable wetting model with 180° off-pad wetting angle; ggg iteration scheme [details of iteration schemes is documented in Appendix B]

The final shape and energy state of the fluid solder was very sensitive to the iteration scheme used to evolve the fluid. Figure 3-44 shows the same model with a different iteration scheme.

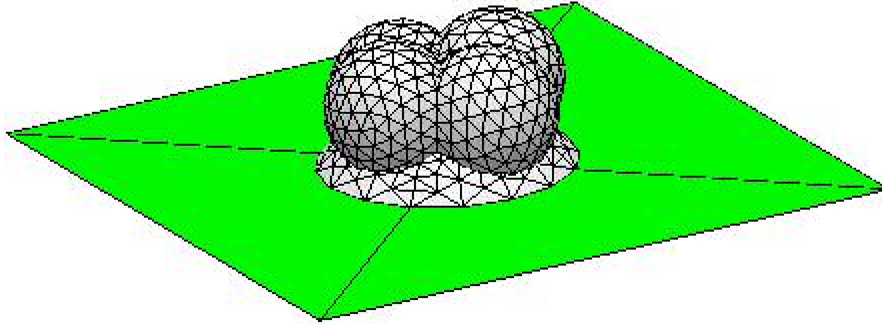


Figure 3-44: Variable wetting model with 180° off-pad wetting angle; gg2 followed by ggg iteration scheme

The shape and the energy are clearly seen to vary in these scenarios. Even in the case where the silicon is given a 180° wetting angle, perfect non-wetting, Surface Evolver was easily fooled into following an incorrect path. Surface Evolver likely has difficulties in evolving the shape of the solder due to local minima that exist. In addition, the solder was modeled as discreet entities over each area. Therefore, Surface Evolver simply minimized the energy of each discreet volume of solder as opposed to the entire system. Even with these issues, the model does reveal some interesting points. First and foremost is that care must be taken when interpreting Surface Evolver results. Second, the final energy state and shape of the solder can be changed by small perturbations in the boundary conditions, such as those due to contaminants or oxides.

In the modeling of the silicon as partially wetting, the final shape of the solder is very unpredictable both experimentally and theoretically. The wide variety of predicted localized minimum energy states might reflect instabilities in the model. However, the experimental results showed that the off-pad wetting was random in nature. Subtle

differences in surface topography or contaminants could drive the off-pad wetting shape to its final form. The effects of the wetting angle off-pad are shown in Figure 3-45 and Figure 3-46.

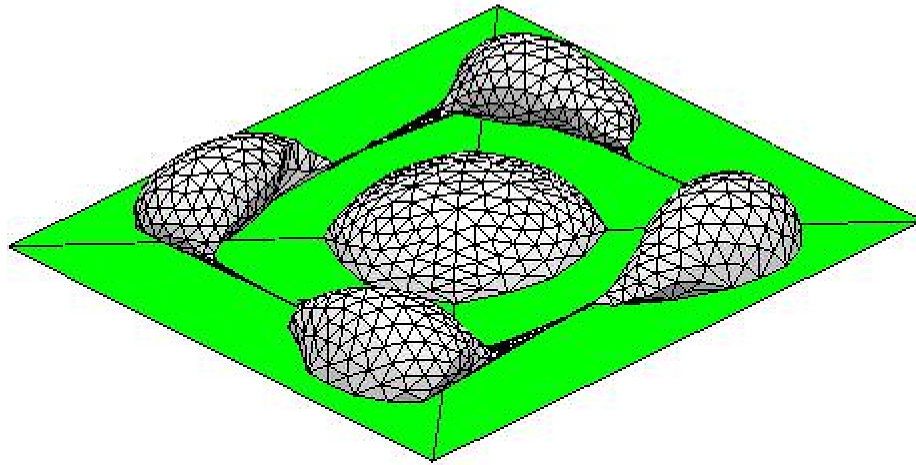


Figure 3-45: Variable wetting model with 60° off-pad wetting angle

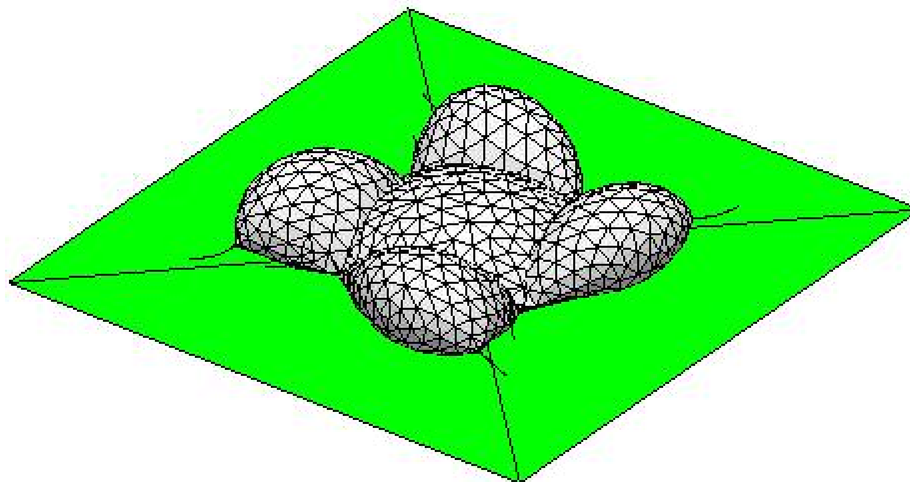


Figure 3-46: Variable wetting model with 120° off-pad wetting angle

The affinity of the solder to the surface affects the final shape of the solder. However, the final shape of the solder for off-pad modeling was too difficult to predict with this model approach. With that caveat aside, the experimental results (Figure 3-47) with off-pad wetting of the solder are fairly accurately captured by the model (Figure 3-45).

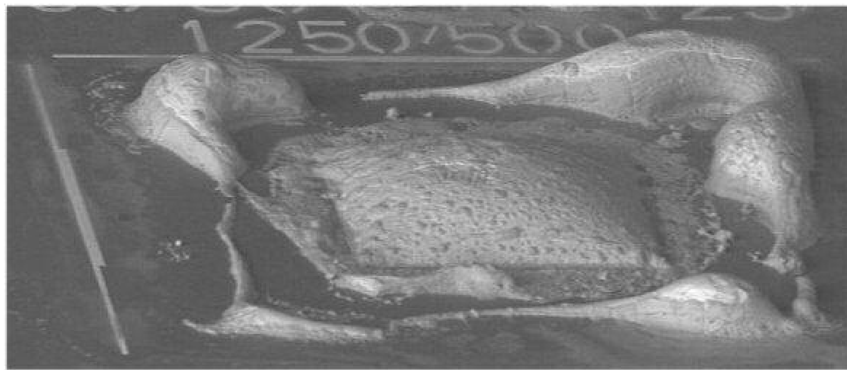


Figure 3-47: Off-pad wetting (1250μm In pad on 500μm TiW/Au pad)

Note that the wetting angle on the pad is much smaller than the off-pad wetting angle. The discrete solder volume model thus can accurately describe the off-pad wetting phenomena seen in some of the reflow experiments. In other experiments, all of the solder pulls into the pad. In this scenario, the off-pad model is not valid. Rather the free or forced boundary condition model is applicable. The factors that govern the off-pad wetting are likely due to oxide and/or intermetallic formation. Both compounds have a higher melting temperature than the indium. These compounds can remain a solid during the reflow process and cause the solder to tear into discrete solder volumes that coalesce off the metallization pad.

This concludes the energy modeling discussion of open faced solder joints. The models provide insight to the wetting phenomena without having to consider the many effects of process variables. The models illustrate that good wetting, achieved through cleanliness and oxidation control, is critical to avoidance of pad dewetting in scenarios with a relatively small volume of solder on the pad. In scenarios with sufficient solder, the wetting conditions can be relaxed without sacrificing the wetting area. An off-pad wetting model was introduced and aided in the understanding of the solder behavior during reflow and further emphasized the importance of cleanliness in the soldering process. In the next section, the energy modeling is extended to the fiber-groove interface.

3.3.2.5 Fiber in a rectangular groove

The model, "arc2.fe", for calculating the energy and shape of the solder that fills the area between a fiber and the square groove is provided in Appendix B.5. For this model the solder was constrained to wet the metallized surfaces only. Instabilities in the model required this additional constraint. The solder shape before reflow is shown in Figure 3-48.

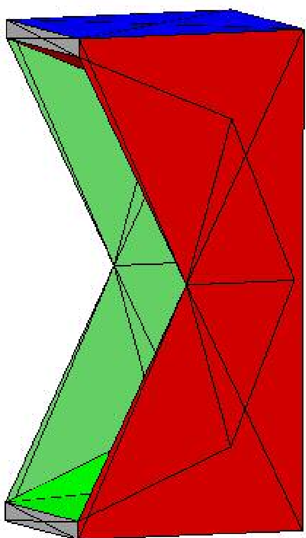


Figure 3-48: Solder in groove before reflow

Note that the exact shape of the solder before reflow is not critical. Evolver, being an energy minimization tool, acts to reduce the energy of a prescribed volume of solder given a set of constraints. Theoretically, the final energy and shape of the solder is independent of the initial shape of the solder. However, due to numerical instabilities in the evolution of the solder model, it is prudent to begin with an initial guess for the model of the solder that is approximately its end shape. The shape of the solder after reflow is dependent on both the wetting angle and the deposited solder volume. The effects of wetting angle on the final shape and energy state of the solder were compared through a series of numerical evolutions. To aid in the understanding of the model results, the volume of solder is normalized by the amount of solder to fill the volume between the fiber and the etched channel in the silicon. The shape of the final solder joint for this condition is shown in Figure 3-49.

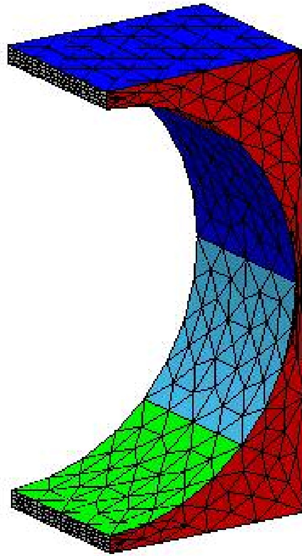


Figure 3-49: Solder shape in fiber-groove interface with a nominal solder volume

The amount of solder deposited in the metallized area can be greater than or less than the amount need to form the structure shown in Figure 3-49. The shape of the final joint predicted by the model for a solder depraved joint and a joint with excess solder are shown in Figure 3-50 and Figure 3-51, respectively.

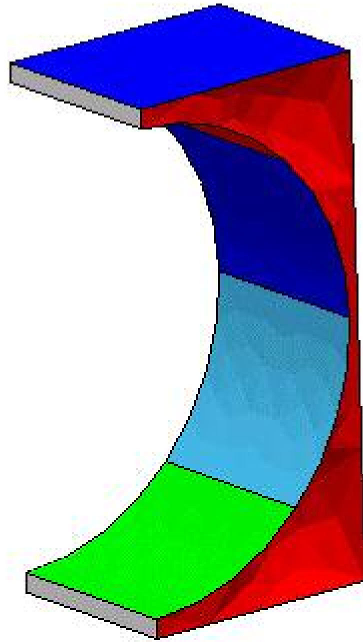


Figure 3-50: Solder shape in fiber-groove interface with 20% less than nominal solder volume (solder deprived)

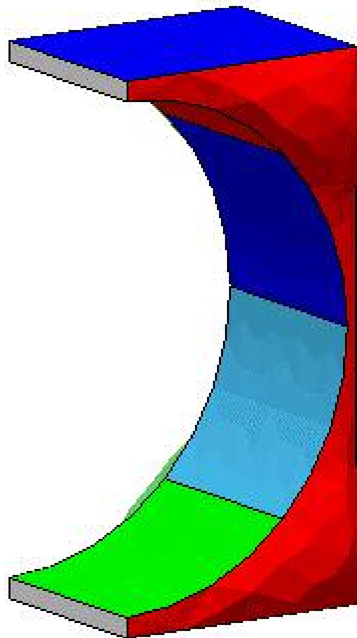


Figure 3-51: Solder shape in fiber-groove interface with 20% more than nominal solder volume (excess solder)

The solder can be seen to form a concave surface if insufficient solder is available and form a convex surface if additional solder is available. The effects of the volume on the energy of the fluid solder are plotted in Figure 3-52.

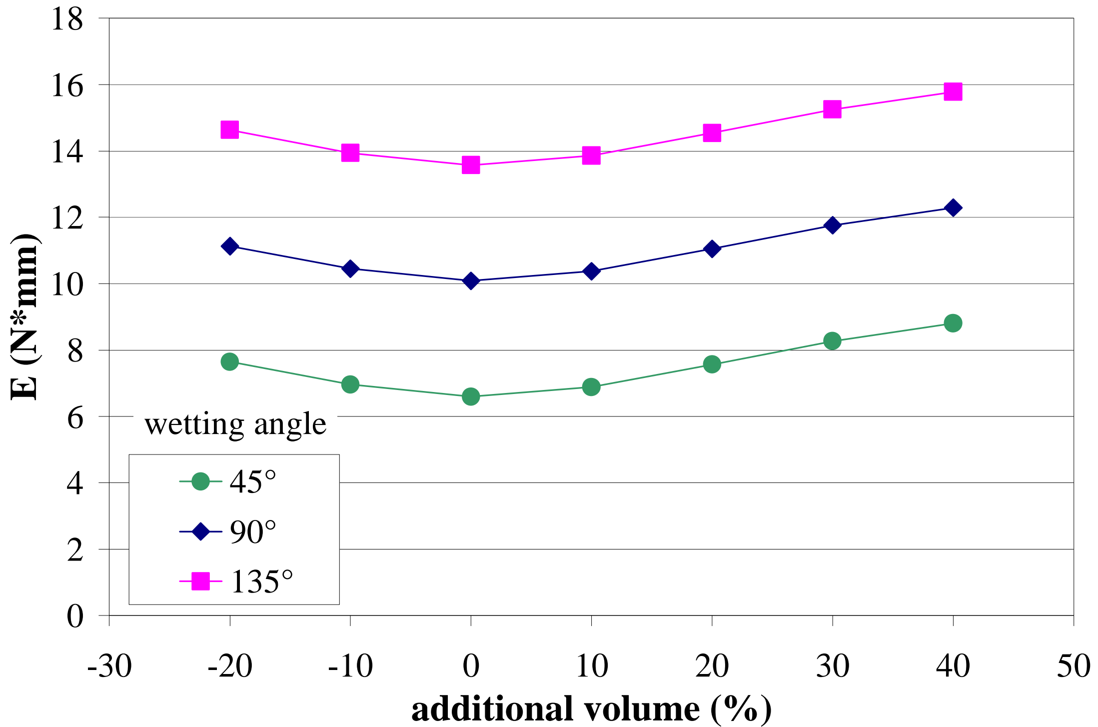


Figure 3-52: Effects of wetting angle and solder volume on solder energy (fiber-groove model)

The wetting angle has a significant effect on the energy of the solder joint, in some cases doubling the energy in the solder joint. The volume of solder in the joint affects the final energy by less than 15% over the ranges modeled. In the previous section it was shown that the energy ratio was a key parameter in predicting the final shape of the solder joint. The normalized energy is plotted in Figure 3-53.

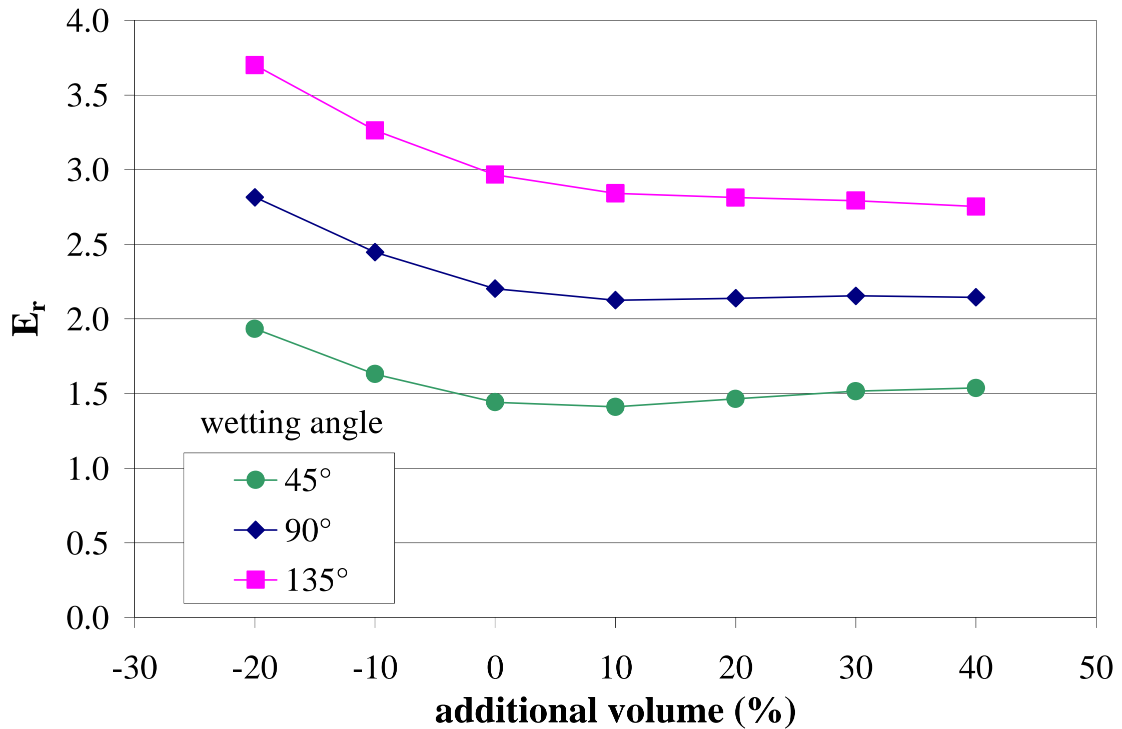


Figure 3-53: Effects of wetting angle and solder volume on solder energy ratio (fiber-groove model)

The energy ratio changes less than 10% as the volume is increased from nominal to 40% above nominal. However, a solder joint with less than the nominal volume results in a higher energy state solder joint, increasing sharply as the volume is reduced. Recall from the previous section that solder joist with higher energy ratios are more likely to not conform to the pad. This lack of conforming, which manifests itself in dewetting, results in a smaller weaker solder joint. More critically, the dewetting can create a leak path in the most severe cases.

CHAPTER 4: TEST AND EVALUATION

In this chapter the environmental stress qualification testing and evaluation of the assembled die-level packages complete with metallized fibers is discussed. Several techniques were implemented to evaluate the integrity of the chip-level package. The evaluation criteria included metrology, fiber pull, die shear, and environmental conditioning. The results of these tests are discussed in more detail in the sections that follow.

4.1 Inspection

After reflow, the chip assemblies were inspected on the optical microscope. An assembled chip-level test structure is shown in Figure 4-1.

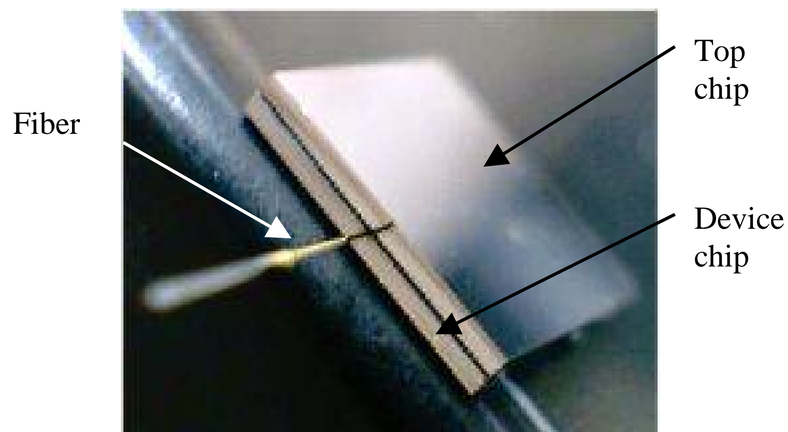


Figure 4-1: Assembled chip-level package test structure

Many of the structures suffered from misalignment between the two chips as large as 30µm. In theses cases, the fiber and the groove in the top chip did not engage. Recall the 125µm diameter fiber protrudes 25µm from the 100µm deep channel in the device chip. The 30µm thick solder layer sometimes resulted in fiber not keying off the groove in the top chip. This alignment issue could be fixed by making the groove deeper in the device layer, an approach that is now implemented in the present S&A design.

The spacing between the chips was not as planar as desired, often ranging from 50µm to 80µm. Note that the spacing was much larger than the 30µm design solder layer. During the reflow, the solder pulled in to form a lower energy state. As the solder pulls in, it increases the standoff between the chips. Applying a load during the solder reflow can reduce this effect.

To obtain visual access to the fiber-channel interface, several assemblies were separated by die shear or die peeling. An SEM picture of a sample that was die sheared along the fiber axis is shown in Figure 4-2.

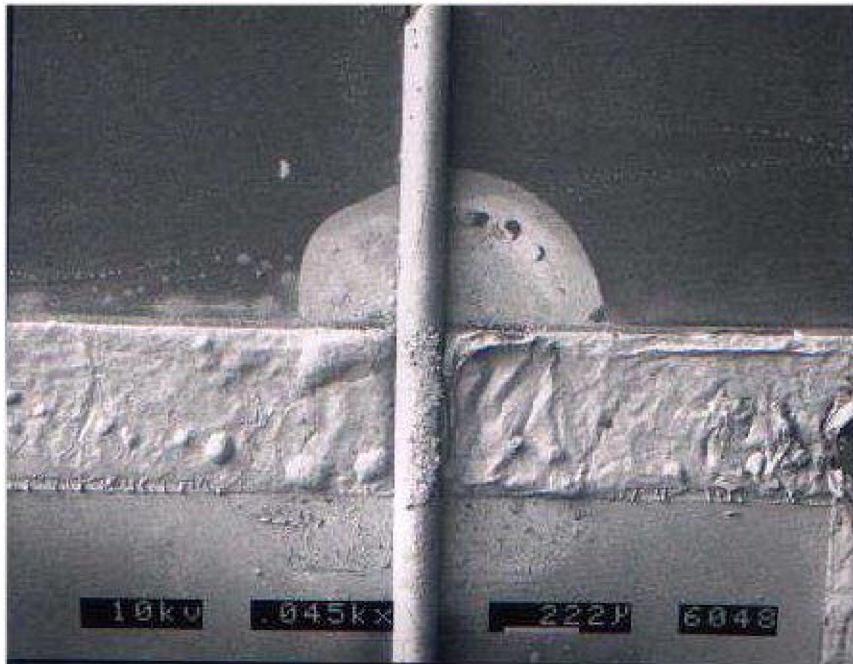


Figure 4-2: Fiber in the groove of device chip after die shear

The fiber remained in the groove of the device chip shown in the figure and can be seen to be wetted by the solder through the seal ring area. The corresponding groove on the top chip is shown in Figure 4-3.

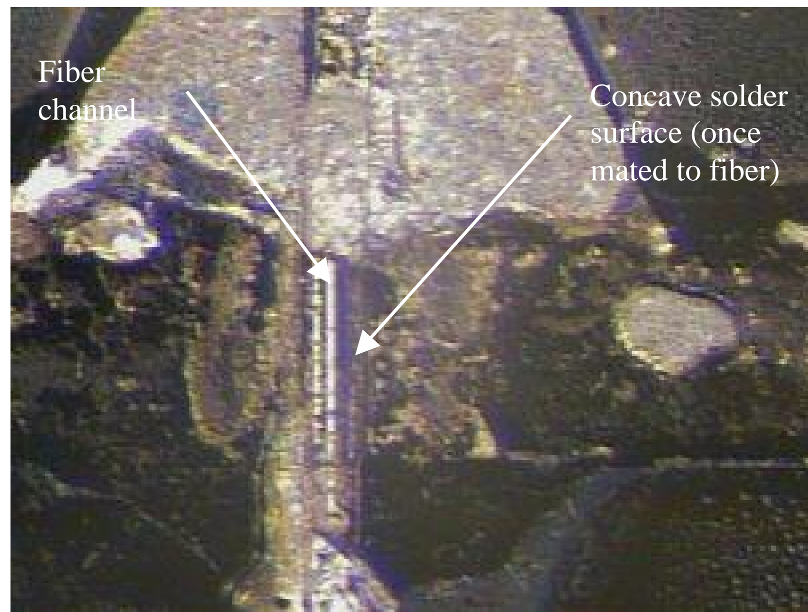


Figure 4-3: Top chip fiber groove after die shear

Note that the solder in the groove has a concave shape indicating that the solder flowed to fill the void between the fiber and the groove.

4.2 Fiber pull tests

The pigtailed fibers were loaded to assess the integrity of the fiber-to-chip bond. A pair of locking scissors was clamped to the fiber. Weights were suspended from the scissors to load the fiber as shown in Figure 4-4.

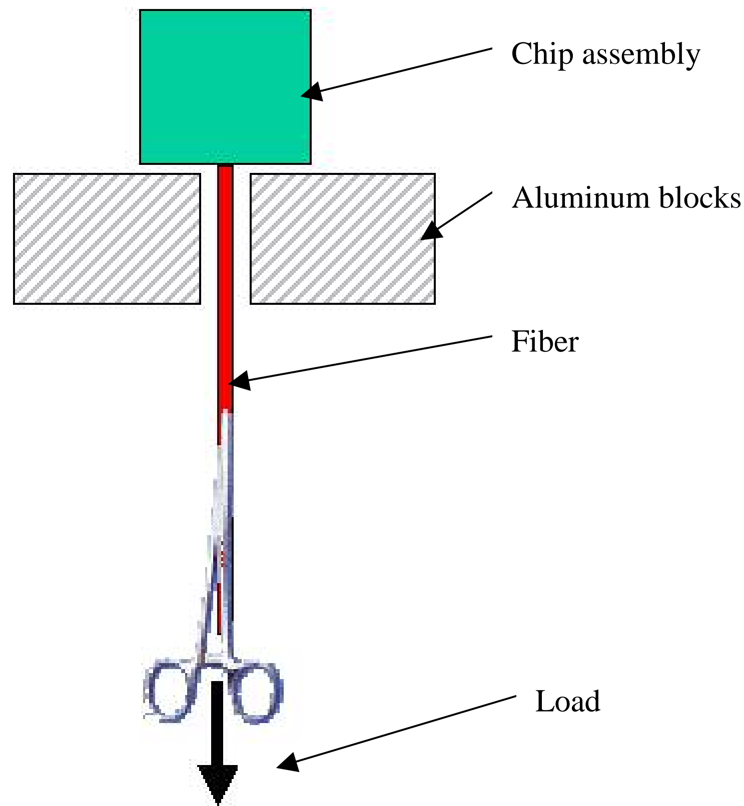


Figure 4-4: Fiber pull test set-up

Two samples were destructively tested in this fashion. Both samples held a 354 gram weight (3.3 N) and sheared when loaded with a 554 gram weight (5.2 N). In both cases, the solder appeared to fail, as opposed to the interface at the solder to metallization, Figure 4-5.

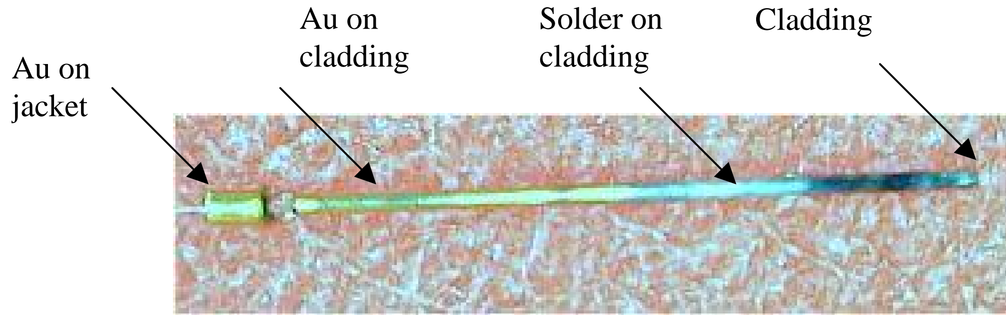


Figure 4-5: Fiber after destructive pull test

Note from Figure 4-5 that the solder wetted the fiber and that it remained bonded to the fiber even after the pull test. Solder was also remaining on the chip. Hence, the bulk solder failed as opposed to an adhesion metallization failure or a brittle intermetallic failure.

Assuming the solder wet completely across the 0.5 mm wide solder seal ring; the two results above correspond to a shear strength of the joint between 16.7 and 26.7 MPa. The tensile and shear strength of indium is far below this value. MATWEB reports an ultimate tensile stress limit of 4.5 MPa [91]. Indium Corporation reports an ultimate tensile strength of 1.9 MPa and an ultimate shear strength of 6.5 MPa [103]. The strength of the solder joint indicates that a solid bond was formed between the fibers and the chips in the test samples since the failure strength of the bond appears to be much greater than that of the bulk indium. The greater strength is due to the thin layer of solder that is present, and from the compressive force that exists between the bonded chips. Regardless, the strength of the fiber attachment is not a performance driver since strain

relief will be utilized to mitigate fiber stress in tactical applications. However, a strong bond is indicative of good wetting.[1]

4.3 Die shear

Die shear was performed on several samples to assess the chip-to-chip bond integrity. In the die shear test, a load is applied parallel to one of the orthogonal in-plane directions of the bonded chip pairs. A load cell was used to measure the force applied to the chip pair. Finally, the shear stress is calculated from the load at failure and the bond area. Four chip assemblies were sheared along the fiber axis. The results are summarized in Table 4-1.

Table 4-1: Die shear results

Sample #	Bond pressure (kPa)	Failure load (N)	Failure stress (MPa)
1	0	13.8	1.4
2	0	37.5	3.8
3	0	25.2	2.5
4	10	50.4	5.0

MIL-STD-883 test method 2019.5 requires the minimum bond strength in die shear to be 1.24 MPa for the 2x failure criteria [94]. The "2x" refers to the shear load at which the bond fails. Samples that pass the 2x criteria automatically pass the standard. Lower

[1] Having established the approximate strength of properly wetted fiber interconnects, the fiber pull test can be used to screen for latent defects in the soldering process. To non-destructively validate the bond between the fiber and the chips, bonded assemblies were qualified by loading the assembly with a 0.5N

shear stress levels are acceptable under this standard (1x and 1.25x) if other acceptance criteria are met. All tested samples exceeded the 2x limit in MIL-STD-883. The shear stress level agrees with that found by other researchers using pure indium solder, such as 2.6 MPa in Cheng's soldering process [104]. The use of pressure to join the chips increases the mechanical strength of the bond, as demonstrated with sample 4 in Table 4-1. The stress in the solder at failure, 5 MPa, is in the range of the 4.5MPa ultimate strength of pure indium solder.

4.4 Highly accelerated life testing (HALT)

The scope of the HALT, performed for NSWC Indian Head by Sandia National Labs, was two-fold. From a Sandia perspective, the test series was to demonstrate and establish expertise in the application of HALT to MEMS. From an NSWC Indian Head perspective, the purpose of the test was to assess the robustness of the MEMS device and packages. The HALT is designed to uncover latent defects in the design, fabrication, or assembly of electronic devices in a short amount of time. The test recipes are not standard. Rather they are typically set according to the application. HALT generally includes the following sequence of tests:

1. Thermal stress
2. Rapid temperature transitions
3. Vibration stress

---

load. The stress in the solder joint at 0.5N is 2.7MPa, which is on the order of the strength of the bulk indium. Of the several samples that were subjected to the 0.5N load, none failed.

4. Combined temperature and vibration stress

Failures are expected and actually intended. HALT failures highlight weaknesses in the device allowing the designer to address potential areas of concern.

Several chip-level packages with 2 fibers,

Figure 4-6, were prepared with the intention of subjecting them to HALT. Unfortunately, machine time availability limited the scope of the testing and only two samples were tested.

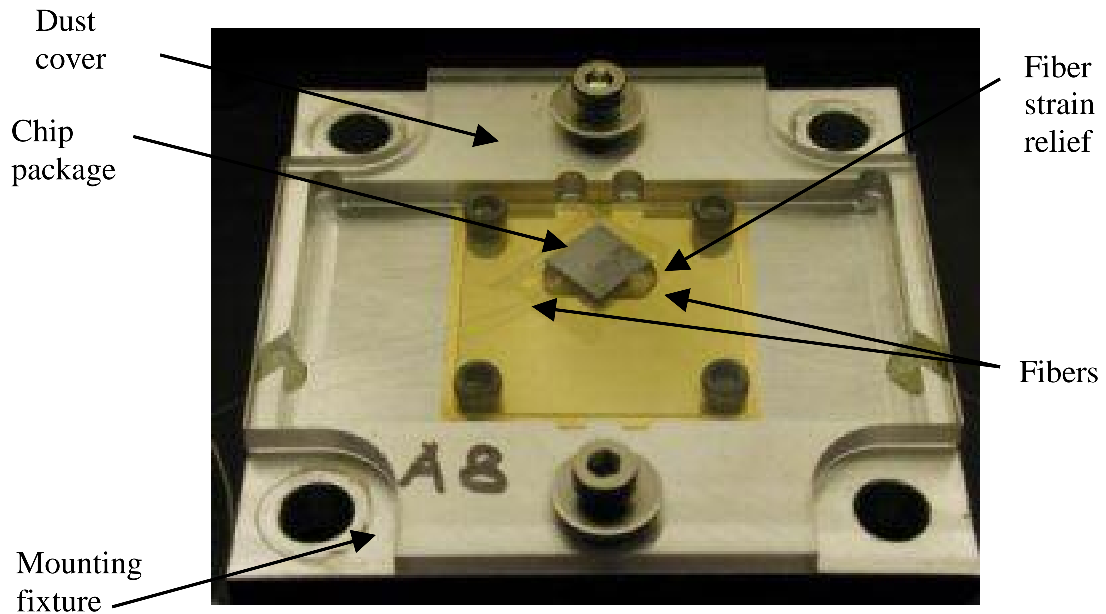


Figure 4-6: Chip-level package with 2 fibers in HALT test fixture

The chip assembly was bonded to a Kovar® lid to reduce effects of coefficient of thermal expansion (CTE) mismatches, Table 4-2. The data in table came from MatWeb [91] for indium, Kovar®, and aluminum and from Petersen for silicon [105]. The Kovar® lid was

bolted to an aluminum fixture that interfaced with the HALT chamber. Adhesive was added to the assembly where the fiber exits the chip assembly to provide strain relief. Two fibers were used so that light could be transmitted into an inlet fiber and detected exiting the output fiber after the light reflects off a MEMS structure inside the package.

Table 4-2: Coefficient of thermal expansion of materials in HALT test

Material	CTE (µm/(m -°C))
Silicon	2.33
Indium	33
Kovar®	5.86
Aluminum	23.6

The test levels were selected to stress the hardware beyond levels the assembly sees in a tactical application. The test conditions are summarized in Table 4-3.

Table 4-3: HALT test parameters

Test	Conditions		
	Level	Steps	Dwell time (min)
Hot step	100°C	10°	10
Cold step	-100°C	10°	10
Vibration	60g_{rms} random, 10-20kHz,	5$_{grms}$	5
Hot vibration	Vibration: 15, 30, 45 g_{rms} Temperature: 80, 90,100°C		10
Cold vibration	Vibration: 15, 30, 40 g_{rms} Temperature: -80, -90, -100°C		10
Hot/cold vibration	Vibration: 60 g_{rms} Temperature: -90, 100°C	10$_{grms}$	5

A sample power spectral density of the random vibration is shown in Figure 4-7.

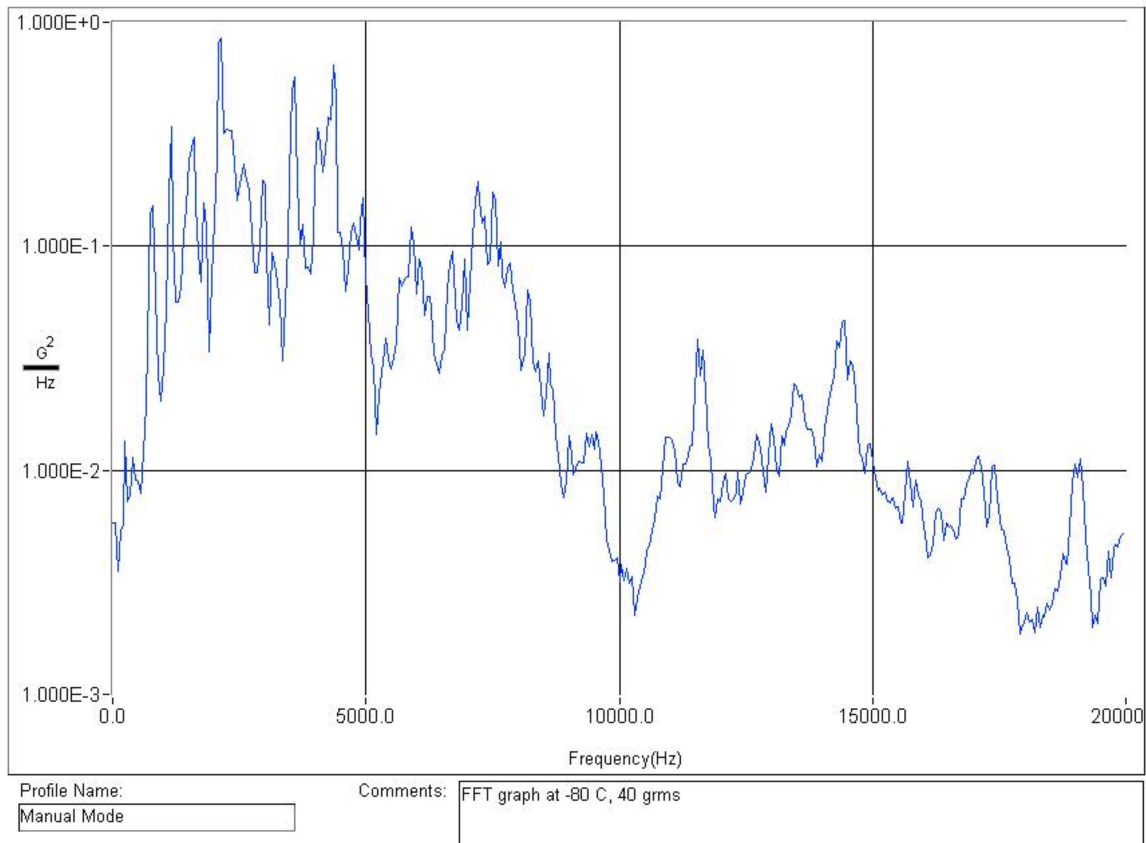


Figure 4-7: Sample power spectral density of random vibration test (40 g_{rms})

The hot and cold tests were skipped. Past experience lent confidence that these tests were not severe enough to cause failures. The first sample was subjected to the hot vibration and cold vibration tests. Note that the package is subjected to the same temperature extremes that it would have been in the hot step and cold step tests. This package survived these tests with no loss of optical transmission efficiency. The light transmitted through the fiber pair did vary with temperature, but returned to the nominal value at

room temperature. The transmission efficiency loss at extreme temperature is most likely due to changes in the index of refraction in the fibers and the reflectivity of the silicon (additional tests could be designed to verify this assertion, but were outside the scope of the present effort). After these tests, the fiber was inadvertently broken at the strain relief. A second package was introduced for the last test, hot/cold vibration. This package survived this test without a loss in optical transmission efficiency.

The HALT testing is designed to produce failures so that weak points in the design can be addressed and strengthened, if necessary. The tests subject the hardware to temperature and vibration levels far in excess of the expected levels in the tactical application. The HALT series failed to catastrophically damage the chip-level packages. From a vibration and temperature perspective, the packages appear to be robust from both a military and telecommunication standard.

CHAPTER 5: SUMMARY

MEMS research continues to yield novel devices that offer an exciting glimpse into the future. For MEMS to continue its rapid proliferation, packaging solutions and technologies must mature. The unique ways in which many of the MEMS are required to interact with their environment has been an impediment to the development of a common, standard package. Furthermore, the commercial implementation of new MEMS devices is hampered by the lack of standard processes and specialty packaging tools. A potential solution to this problem is to develop standard interconnect designs that result in a tool set that can be implemented in the microsystem design to facilitate the packaging process.

This chapter summarizes the conclusions and contributions from the research presented in this dissertation. In addition, recommendations are presented to further develop the technology for military and commercial acceptance.

5.1 Summary and Conclusions

This dissertation addresses the need to seal an optical fiber between two micromachined chips at the chip perimeter. The result of this effort is the definition of the design and process to seal an optical fiber across the package boundary at the chip-level using commonly available batch fabrication techniques.

A novel optical fiber interconnect design concept was presented. A fabrication sequence was identified to provide a contiguous metal ring across high aspect ratio

grooves machined using DRIE. The deposition of solder was improved to facilitate plating beyond the metallization pads in order to provide sufficient solder volume to fill voids between the round fiber and the rectangular DRIE groove. The micro-machining methods implemented are all common batch fabrication techniques and lend themselves to integration into most DRIE fabrication sequences.

A fluxless soldering process was analyzed and demonstrated. The process requires a fast heating rate to prevent further oxidation during the reflow cycle. The reducing gas, 5% H_2 and 95% N_2, was shown to be an insufficient oxide reducer at the soldering temperatures, but slowed the oxidation rate of the metal enough to allow the surface tension forces to act and the metallization pads to be wetted. The fluxless soldering process was demonstrated with multiple overplate test structure chips.

The experimental results indicated that the size of the metallization pad had an effect on the quality of wetting. The size effect was explored using a surface energy minimization tool, Surface Evolver. A model was written to predict the final shape and energy state of open faced solder joints. The model revealed that volume and energy ratios could be used to predict the final shape of the solder joint. In addition, these variables provide the solder joint designer an understanding of the quality of wetting required for the solder to conform to the metallization pad.

Having established the fluxless soldering technique, a Surface Evolver model of the solder at the fiber-chip interface was generated. The volume of solder was selected to optimize the success of sealing the fiber between the two chips. The chip-level packages

were assembled with fibers crossing the seal interface. The robustness of the package was demonstrated through fiber pull, die shear, and highly accelerated life testing.

The design of this package, with a fiber housed in a groove in the chip and sealed at the chip-level, was filed for a patent in January of 2003 [79]. The proof of concept of this interconnect was demonstrated in this dissertation.

5.2 Contributions

The primary contribution of this dissertation is a design and method to seal a metallized optical fiber between two chips without the use of a flux. To date, no such package has been reported, with or without the use of fluxes. In addition to this umbrella contribution, several smaller contributions are also realized. First, a method to deposit a contiguous metal layer onto all the surfaces of a MEMS fabricated groove has been demonstrated. The effects of both evaporation and sputtering techniques with regard to sidewall coverage are reported. Second, a Surface Evolver model was generated to predict the flow of solder on a surface with a variable wetting angle. The parameters governing the stability of a solder geometry are determined through correlation of energy modeling with the results of a parametric experimental study. Third, the behavior of high aspect ratio indium solder during reflow, especially with regards to fluxless soldering, has been examined. The geometric constraints that result in off pad localization to solder are reported. Fourth, a Surface Evolver model was generated to predict the stability of a solder joint between a round fiber and a faceted groove. Finally, the method to robustly

join a fiber between two chips is defined and then demonstrated through destructive testing.

5.3 Recommendations

Several follow-on efforts would greatly benefit this research. Most importantly, an accurate leak detection method for small volume packages should be identified and incorporated into the design. Humidity, pressure, lid deflection, or dew point sensors are viable techniques to assess the package hermeticity. The effect of harsh environments, such as vibration and temperature extremes, should be quantified from a leak rate perspective. For proper function through the life of the package, the package should ultimately have a leak rate much smaller than the military standard specification. Improved hermeticity measurement techniques would benefit the MEMS industry, especially for small internal volume and vacuum packaging applications.

Another area that would benefit from additional research is the development of a dry cleaning process. Plasma cleaning is an excellent method to remove oxides from surfaces. The literature is devoid of recipes to remove oxides from any surfaces, no less metals of interest in this dissertation. A parametric study of the effects of background pressure, gas pressure, gas species, and RF power on oxide etching rates and sample temperature would reduce process variations due to over or under etching of the metals in the cleaning process.

The under etching of the buried oxide layer creates a potential leak path. The process to remove the field oxide at the bottom of the channel should be optimized to reduce the under etching. Alternatively, changes to process sequence should be explored. For instance, the HF etch could be performed after the indium is deposited. Although indium is readily etched in HF, initial tests indicate that indium oxide passivates the indium, preventing etching of the indium. As a result, the oxide layer would not be under etched and this potential leak path would be eliminated.

Finally, the approach should be demonstrated on a fully processed MEMS chip. The package demonstrated in this dissertation did not have movable microstructures. Care was taken to insure that the process developed in this dissertation would be compatible with the process used to fabricate the MEMS S&A, however subtle changes can often have a profound effect on MEMS device yield and on soldering processes.

APPENDIX A: MEMS-BASED SAFETY AND ARMING SYSTEM

The application discussed in this dissertation is the Safety and Arming (S&A) device described in [14] and [15] for use in undersea torpedoes in which two chips containing DRIE MEMS structures are bonded together and operate reliably after many years of storage in extreme environmental conditions. The requirements of the S&A system are to safely and reliably arm and detonate the weapon, but only after all safety criteria are met and the weapon has reached its intended target. The MEMS S&A system is shown in Figure 0-1 and Figure 0-2.

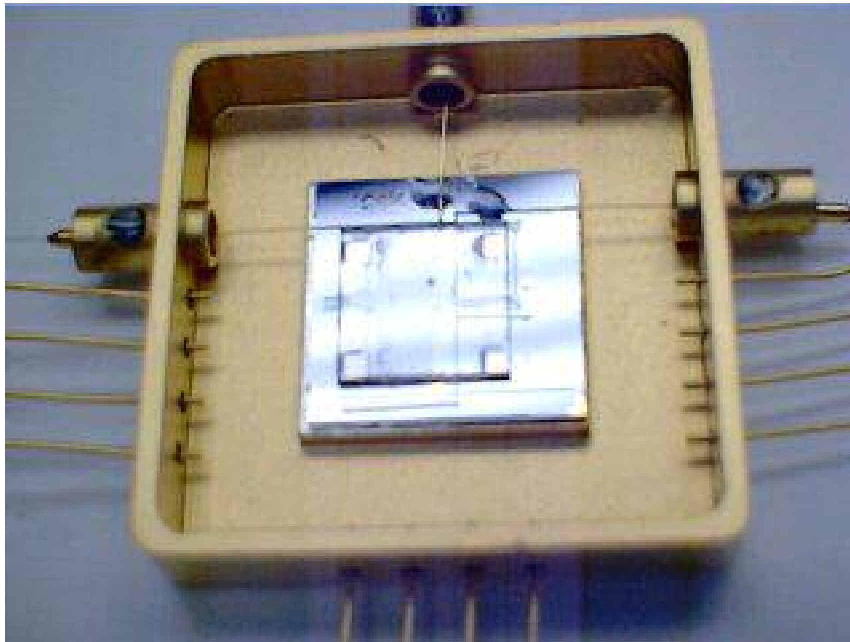


Figure 0-1: MEMS S&A chip in a Kovar® package

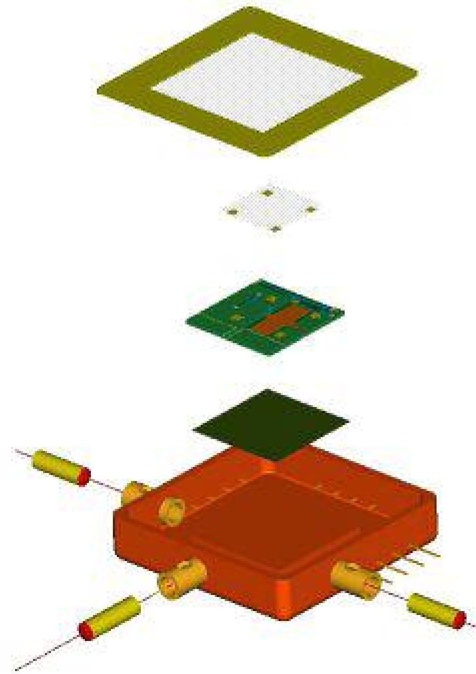


Figure 0-2: MEMS S&A exploded view

The MEMS components include the S&A chip and deflection delimiter. The operation and construction of the S&A system has been discussed in [14] and [15], and a picture of the system can be found on the cover of [106]. A deflection delimiter is introduced to limit out-of-plane (z-axis) compliance of several structures. The delimiter ensures that the locks on the barrier are not violated by z-axis displacement between structures. The deflection delimiter must allow for in-plane movement of all structures, but prevent z-axis movement of selected structures. In addition, the delimiter must allow for wire bonding and fiber optic cable routing and mounting.

APPENDIX B: SURFACE EVOLVER MODEL FILES

This section documents the programs that were written for Surface Evolver [107]. The different models that are discussed in this dissertation are separated into different sub-sections in this Appendix. Comments are included in the input files to assist the reader in understanding the purpose of the lines of code.

B.1: Vol2.fe

```
// vol2.fe
// open faced solder joint, free to pull in
// update 3/11/04
// Evolver data for drop of prescribed volume sitting on plane with gravity.
// Solder NOT forced to wet to pad; can move in
// Contact angle with plane can be varied.
// convert high aspect volume to lower aspect volume to ease model evolution

parameter angle = 90.0    // interior angle between plane and surface, degrees
parameter tens = 460.0
parameter pad_act  = 2.0
parameter thick_act = .0082
parameter scaleit = .25
parameter pad  = scaleit*pad_act
parameter thick = (1/(scaleit^2))*thick_act
gravity_constant 0  // start with gravity off

#define WALLT  tens*(-cos(angle*pi/180))  // virtual tension of facet on plane
//define evolve routine
#define ggg
g5;r;u;V;g20;u;V;g20;u;V;u;V;g20;u;V;u;V;g20;u;V;u;V;u;V;r;u;V;u;V;g40;u;V;u;V;g4
0;u;V;u;V;g40
#define ggg2
u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;
u;V;g5
#define ggg3
r;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V
;u;V;g5
//define parameters of interest
#define maxh print max(vertex where not fixed,z)
#define dia print 2*max(vertex where not fixed,(x^2+y^2+z^2)^0.5)
```

```
#define wetdia print 2*max(vertex where z=0, (x^2+y^2)^0.5)
#define area2 print sum(facet where tension > 0, area)  //gives surface area of solder
(eliminates display areas)
keep_macros

constraint 1   /* account for energy between solder and wetable surface */
formula: x3 = 0
energy:  // for contact angle
e1: -(WALLT*y)
e2: 0
e3: 0

//define geometry for solder and display surfaces
vertices
1   -pad/2  -pad/2 0.0 constraint 1
2    pad/2  -pad/2 0.0 constraint 1
3    pad/2   pad/2 0.0 constraint 1
4   -pad/2   pad/2 0.0 constraint 1
5   -pad/2  -pad/2   thick
6    pad/2  -pad/2   thick
7    pad/2   pad/2   thick
8   -pad/2   pad/2   thick
9    pad + 0.1    pad + 0.1   0.0  fixed   /* for wetable surface display */
10   pad + 0.1  -(pad + 0.1)  0.0  fixed
11 -(pad + 0.1) -(pad + 0.1)  0.0  fixed
12 -(pad + 0.1)   pad + 0.1   0.0  fixed

edges  /* given by endpoints and attribute */
1   1 2    constraint 1 /* 4 edges on plane */
2   2 3    constraint 1
3   3 4    constraint 1
4   4 1    constraint 1
5   5 6
6   6 7
7   7 8
8   8 5
9   1 5
10  2 6
11  3 7
12  4 8
13  9 10   fixed  no_refine /* for wetable surface display */
14 10 11   fixed  no_refine
15 11 12   fixed  no_refine
16 12  9   fixed  no_refine
```

```
faces  /* given by oriented edge loop */
1   1 10 -5  -9  tension tens
2   2 11 -6 -10  tension tens
3   3 12 -7 -11  tension tens
4   4  9 -8 -12  tension tens
5   5  6  7   8  tension tens
7  13 14 15  16  no_refine color green density 0 fixed /* for wetable surface display */

bodies  /* one body, defined by its oriented faces */
1   1 2 3 4 5   volume thick*pad^2  density 0.008
```

B.2: Wetfix.fe

```
// wetfix.fe
// open faced solder mound forced to wet to pad
// last updated 3/13/04;
// Evolver data for drop of prescribed volume sitting on plane with gravity.
// Contact angle with plane can be varied.
parameter angle = 30    // interior angle between plane and surface, degrees
parameter tens = 460.0
parameter solderpad = 0.1786
parameter pad  = 0.1
parameter thick = .005

gravity_constant 0  // set gravity to zero

#define WALLT  (-tens*cos(angle*pi/180))  // virtual tension of facet on plane

//define evolve routine
#define ggg
g5;r;u;V;g20;u;V;g20;u;V;u;V;g20;u;V;u;V;g20;u;V;u;V;u;V;r;u;V;u;V;g40;u;V;u;V;g4
0;u;V;u;V;g40
#define ggg2
u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;
u;V;g5
#define ggg3
r;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V
;u;V;g5
//defined values of interest
#define maxh print max(vertex where not fixed,z)
#define dia print 2*max(vertex where not fixed,x)
#define area2 print sum(facet where tension > 0, area)  //gives surface area of solder
(eliminates display areas)
#define padw print 2*max(vertex where z=0, x)
keep_macros

constraint 1   /* account for energy between solder and metallization pad */
formula: x3 = 0
energy:  // for contact angle
e1: -(WALLT*y)
e2: 0
e3: 0

//define geometry for solder and display surfaces
vertices
```

```
1   -pad/2 -pad/2 0.0  constraint 1
2    pad/2 -pad/2 0.0  constraint 1
3    pad/2  pad/2 0.0  constraint 1
4   -pad/2  pad/2 0.0  constraint 1
5   -(solderpad/2) -(solderpad/2) thick
6    (solderpad/2) -(solderpad/2) thick
7    (solderpad/2)  (solderpad/2) thick
8   -(solderpad/2)  (solderpad/2) thick
9   1.0  1.0 0.0  fixed       /* display substrate */
10  1.0 -1.0 0.0  fixed
11 -1.0 -1.0 0.0  fixed
12 -1.0  1.0 0.0  fixed
13  -pad/2 -pad/2 0.0  fixed  /* display metallization pad */
14   pad/2 -pad/2 0.0  fixed
15   pad/2  pad/2 0.0  fixed
16  -pad/2  pad/2 0.0  fixed

edges  /* given by endpoints and attribute */
1   1 2    fixed constraint 1 /* 4 edges on plane */
2   2 3    fixed constraint 1
3   3 4    fixed constraint 1
4   4 1    fixed constraint 1
1   1 2          constraint 1 /* 4 edges on plane */
2   2 3          constraint 1
3   3 4          constraint 1
4   4 1          constraint 1
5   5 6
6   6 7
7   7 8
8   8 5
9   1 5
10  2 6
11  3 7
12  4 8
13  9 10   fixed no_refine /* display substrate */
14 10 11   fixed no_refine
15 11 12   fixed no_refine
16 12  9   fixed no_refine
17 13 14   fixed no_refine /* display metallization pad */
18 14 15   fixed no_refine
19 15 16   fixed no_refine
20 16 13   fixed no_refine

faces  /* given by oriented edge loop */
```

```
1   1 10 -5  -9 tension tens
2   2 11 -6 -10 tension tens
3   3 12 -7 -11 tension tens
4   4  9 -8 -12 tension tens
5   5  6  7   8 tension tens
7  13 14 15  16 no_refine color green density 0 fixed /* display substrate */
8  17 18 19  20 no_refine color yellow density 0 fixed /* display metallization pad */

bodies  /* one body, defined by its oriented faces */
1   1 2 3 4 5   volume thick *(solderpad)^2
```

B.3 tearnew.fe

```
// tearnew.fe
// Update 3/11/04
// Evolver data for drop of prescribed volume sitting on plane
// Solder NOT forced to wet metallization
// Wetting angle of metallization and substrate can be prescribed
// Solder modeled as discrete volumes
// Contact angle with plane can be varied.
// Try to fix tearold instability.  Eliminate vertex sharing with different wet angles

PARAMETER angle1 = 45    // interior angle between plane and metallization, degrees
PARAMETER tens = 460.0   // surface tension of indium
parameter pad_act  = 1.0  // dimension of solder pad
parameter thick = .05     // thickness of solder
parameter angle2 = 120    // wetting angle on substrate
PARAMETER width1 = 0.5    // metallization pad
PARAMETER width2 = (pad_act-width1)/2  //portion of substrate with deposited solder

gravity_constant 0  // neglect gravitational effects

#define WALLT1  tens*(-cos(angle1*pi/180))  // virtual tension of facet on plane, on
metallization
#define WALLT2  tens*(-cos(angle2*pi/180))  // virtual tension of solder facet on plane,
off metal

//define evolution routines
#define ggg
g5;r;u;V;g20;u;V;g20;u;V;u;V;g20;u;V;u;V;g20;u;V;u;V;u;V;r;u;V;u;V;g40;u;V;u;V;g1
0
#define ggg2
u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;
u;V;g5
#define ggg3
r;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V
;u;V;g5
#define maxh print max(vertex where not fixed,z)
//define values of interest
#define dia print 2*max(vertex where not fixed,(x^2+y^2+z^2)^0.5)
#define area2 print sum(facet where tension > 0, area)  //gives surface area of solder
(eliminates display areas)
keep_macros

constraint 1   /* account for energy between solder and metallization pad */
```

```
formula: x3 = 0
energy:  // for contact angle
e1: -(WALLT1*y)
e2: 0
e3: 0
constraint 2   /* account for energy between solder and substrate */
formula: x3 = 0
energy:  // for contact angle
e1: -(WALLT2*y)
e2: 0
e3: 0
constraint 3
formula: x3 = 0

vertices
1   -width1/2  -width1/2 0.0 constraint 1
111 -width1/2  -width1/2 0.0 constraint 2
2    width1/2  -width1/2 0.0 constraint 1
22   width1/2  -width1/2 0.0 constraint 2
3    width1/2   width1/2 0.0 constraint 1
33   width1/2   width1/2 0.0 constraint 2
4   -width1/2   width1/2 0.0 constraint 1
44  -width1/2   width1/2 0.0 constraint 2
5   -width1/2  -width1/2   thick
55  -width1/2  -width1/2   thick
6    width1/2  -width1/2   thick
66   width1/2  -width1/2   thick
7    width1/2   width1/2   thick
77   width1/2   width1/2   thick
8   -width1/2   width1/2   thick
88  -width1/2   width1/2   thick
9    width1 + 0.1    width1 + 0.1   0.0  fixed   /* display substrate */
10   width1 + 0.1  -(width1 + 0.1)  0.0  fixed
11 -(width1 + 0.1) -(width1 + 0.1)  0.0  fixed
12 -(width1 + 0.1)   width1 + 0.1   0.0  fixed
100  -(width1/2+width2)  -(width1/2+width2) 0.0 constraint 2
101  -(width1/2)         -(width1/2+width2) 0.0 constraint 2
102   (width1/2+width2)  -(width1/2+width2) 0.0 constraint 2
103   (width1/2+width2)  -(width1/2)        0.0 constraint 2
104   (width1/2+width2)   (width1/2+width2) 0.0 constraint 2
105   (width1/2)          (width1/2+width2) 0.0 constraint 2
106  -(width1/2+width2)   (width1/2+width2) 0.0 constraint 2
107  -(width1/2+width2)   (width1/2)        0.0 constraint 2
200  -(width1/2+width2)  -(width1/2+width2) thick
```

```
201  -(width1/2)         -(width1/2+width2) thick
202   (width1/2+width2)  -(width1/2+width2) thick
203   (width1/2+width2)  -(width1/2)        thick
204   (width1/2+width2)   (width1/2+width2) thick
205   (width1/2)          (width1/2+width2) thick
206  -(width1/2+width2)   (width1/2+width2) thick
207  -(width1/2+width2)   (width1/2)        thick

edges  /* given by endpoints and attribute */
1   1 2    constraint 1 /* 4 edges on plane */
91  111 22 constraint 2
2   2 3    constraint 1
92  22 33  constraint 2
3   3 4    constraint 1
93   33 44 constraint 2
4   4 1    constraint 1
94 44 111  constraint 2
5   5 6
95 55 66
6   6 7
96 66 77
7   7 8
97 77 88
8   8 5
98  88 55
9   1 5
99 111 55
10  2 6
910 22 66
11  3 7
911 33 77
12   4 8
912  44 88
13  9 10   fixed  no_refine /* display substrate */
14 10 11   fixed  no_refine
15 11 12   fixed  no_refine
16 12  9   fixed  no_refine
100 100 101    constraint 2
101 101 102    constraint 2
102 102 103    constraint 2
103 103 104    constraint 2
104 104 105    constraint 2
105 105 106    constraint 2
106 106 107    constraint 2
```

```
107 107 100    constraint 2
200 200 201
201 201 202
202 202 203
203 203 204
204 204 205
205 205 206
206 206 207
207 207 200
300 100 200
301 101 201
302 102 202
303 103 203
304 104 204
305 105 205
306 106 206
307 107 207
400 101 111
401 103 22
402 105 33
403 107 44
500 201 55
501 203 66
502 205 77
503 207 88


faces  /* given by oriented edge loop */
1   1 10 -5  -9  tension tens
2   2 11 -6 -10  tension tens
3   3 12 -7 -11  tension tens
4   4  9 -8 -12  tension tens
5   5  6  7   8  tension tens
7  13 14 15  16  no_refine color green density 0 fixed /* display substrate */
101 100 301 -200 -300           tension tens
102 400 -94 912 98 -500 -301tension tens
103 -403 307 503 -912           tension tens
104 300 -207 -307 107           tension tens
105-100 -107 403 94 -400        tension tens
106 200 500 -98 -503 207        tension tens
201 101 302 -201 -301           tension tens
202 102 303 -202 -302           tension tens
203 401 -91 99 95 -501 -303  tension tens
204 -400 301 500 -99            tension tens
```

```
205 -101 400 91 -401 -102     tension tens
206 201 202 501 -95 -500      tension tens
301 103 304 -203 -303         tension tens
302 104 305 -204 -304         tension tens
303 402 -92 910 96 -502 -305          tension tens
304 -910 -401 303 501                 tension tens
305 401 92 -402 -104 –103             tension tens
306 -501 203 204 502 –96              tension tens
401 403 -93 911 97 -503 –307          tension tens
402 -402 305 502 -911                 tension tens
403 105 306 -205 -305                 tension tens
404 -206 -306 106 307                 tension tens
405 93 -403 -106 -105 402             tension tens
406 -97 -502 205 206 503              tension tens

bodies  /* one body, defined by its oriented faces */
1   1 2 3 4 5   volume thick*width1^2  density 0.008
2 101 102 103 104 105 106 volume thick*width2*(width1+width2)
3 201 202 203 204 205 206 volume thick*width2*(width1+width2)
4 301 302 303 304 305 306 volume thick*width2*(width1+width2)
5 401 402 403 404 405 406 volume thick*width2*(width1+width2)
```

B.4: Varwet2.fe

```
// varwet.fe
// update 3/08/04
// Evolver data for drop of prescribed volume sitting on plane with gravity.
// Solder NOT forced to wet pad; can move in
// Contact angle on metal and off metal can be varied.

PARAMETER angle1 = 45   // interior angle between plane and surface, degrees
PARAMETER tens = 460
parameter pad  = 2.558  // dimension of solder pad
parameter thick = .005  // thickness of solder
parameter angle2 = 135   // wetting angle on substrate
PARAMETER metal = 0.5   // metallization pad diameter

gravity_constant 0  // start with gravity off

#define WALLT1  tens*(-cos(angle1*pi/180))  // virtual tension of facet on plane, on
metallization
#define WALLT2  tens*(-cos(angle2*pi/180))  // virtual tension of solder facet on plane,
off metal

//define evolve routine
#define gogo r; u; g 20; r; g 20; r; g 20; V; u; g 20;
#define ggg
g5;r;u;V;g20;u;V;g20;u;V;u;V;g20;u;V;u;V;g20;u;V;u;V;u;V;r;u;V;u;V;g40;u;V;u;V;g1
0
#define ggg2
u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;
u;V;g5
#define ggg3
r;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V
;u;V;g5
#define maxh print max(vertex where not fixed,z)
#define dia print 2*max(vertex where not fixed,(x^2+y^2+z^2)^0.5)
#define wetdia print 2*max(vertex where z=0, (x^2+y^2)^0.5)
#define area2 print sum(facet where tension > 0, area)  //gives surface area of solder
(eliminates display areas)
keep_macros

BOUNDARY 1 PARAMETERS 1 /*for display of metallization pad*/
x1: (metal/2)*cos(p1)
x2: (metal/2)*sin(p1)
x3: -0.1
```

```
constraint 1   /* account for energy between solder and wetted surfaces */
formula: z = 0
energy:  // for contact angle
e1: -y*((x^2 + y^2) < (metal/2)^2 ? WALLT1 : WALLT2)
//e1: -(y*WALLT2)
e2: 0
e3: 0

constraint 3 /*
formula: x3 = 0

constraint 4   /* offset display of metal pad so it can be seen */
formula: x3=-.01

constraint 5 /* for display of round metal pad */
formula: x1^2 + x2^2 = metal^2/4

vertices
1   -pad/2  -pad/2 0.0 constraint 1
2    pad/2  -pad/2 0.0 constraint 1
3    pad/2   pad/2 0.0 constraint 1
4   -pad/2   pad/2 0.0 constraint 1
5   -pad/2  -pad/2   thick
6    pad/2  -pad/2   thick
7    pad/2   pad/2   thick
8   -pad/2   pad/2   thick
//9    pad + 0.1    pad + 0.1   -0.02  fixed   /* for substrate display */
//10   pad + 0.1  -(pad + 0.1)  -0.02  fixed
//11 -(pad + 0.1) -(pad + 0.1)  -0.02  fixed
//12 -(pad + 0.1)   pad + 0.1   -0.02  fixed
//20  5*pi/4 boundary 1 fixed  /*metallization pad round*/
//21  7*pi/4 boundary 1 fixed
//22    pi/4 boundary 1 fixed
//23  3*pi/4 boundary 1 fixed

edges  /* given by endpoints and attribute */
1   1 2    constraint 1 /* 4 edges on plane */
2   2 3    constraint 1
3   3 4    constraint 1
4   4 1    constraint 1
5   5 6
6   6 7
7   7 8
8   8 5
```

```
9   1 5
10  2 6
11  3 7
12  4 8
//13  9 10   fixed  no_refine /* for substrate display */
//14 10 11   fixed  no_refine
//15 11 12   fixed  no_refine
//16 12  9   fixed  no_refine
//20 20 21 boundary 1 /*constraint 4 5 metallization pad round*/
//21 21 22 boundary 1 /*constraint 4 5 */
//22 22 23 boundary 1 /*constraint 4 5 */
//23 23 20 boundary 1 /*constraint 4 5 */

faces  /* given by oriented edge loop */
1   1 10 -5 -9   tension tens
2   2 11 -6 -10  tension tens
3   3 12 -7 -11  tension tens
4   4  9 -8 -12  tension tens
5   5  6  7   8  tension tens
//7  13 14 15  16  no_refine color green density 0 fixed /* substrate display */
//10 20 21 22 23  no_refine color red density 0 fixed /* metallization pad display */

bodies  /* one body, defined by its oriented faces */
1   1 2 3 4 5   volume thick*pad^2  density 0.008
```

B.5 Arc2t.fe

```
// arc2t.fe
// Evolver data half fiber in half channel

parameter angle = 45    // interior angle between plane and surface, degrees
parameter tens = 460
parameter chan  = 0.130
parameter dia = 0.125
parameter width = .05
parameter thick = .005
parameter stand = .005
parameter ve = -0.000000  // extra volume to reduce energy state

gravity_constant 0  // gravity negligible

//define evolve routine
#define gogo r; u; g 20; r; g 20; r; g 20; V; u; g 20;
#define ggg
g5;r;u;V;g20;u;V;g20;u;V;u;V;g20;u;V;u;V;g20;u;V;u;V;u;V;r;u;V;u;V;g40;u;V;u;V;g1
0
#define ggg2
u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;
u;V;g5
#define ggg3
r;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V;u;V;g5;u;V
;u;V;g5
keep_macros

BOUNDARY 1 PARAMETERS 1
x1: (dia/2)*cos(p1)
x2: -width/2
x3: (dia/2)*sin(p1)

BOUNDARY 2 PARAMETERS 1
x1: (dia/2)*cos(p1)
x2: width/2
x3: (dia/2)*sin(p1)

#define WALLT  (-tens*cos(angle*pi/180))  // virtual tension of facet on plane

constraint 1   /* the table top */
formula: x3 = -dia/2 -stand
energy:  // for contact angle
```

```
e1: -(WALLT*y)
e2: 0
e3: 0

constraint 2   /* solder conforms to fiber */
formula: x1*x1 + x3*x3 = dia*dia/4

constraint 3   /* solder conforms to top chip*/
formula: x3 = dia/2 +stand
//e1: -(WALLT*y)
//e2: 0
//e3: 0

constraint 4 /* solder conforms to side wall*/
formula: x1 = chan/2
energy:  // for contact angle
e1: -(WALLT*y)
e2: 0
e3: 0

constraint 5 /* solder centerline*/
formula: x1 = 0.0

vertices
1   0.0     -width/2  -dia/2-stand   fixed constraint 1  /* 4 vertices on plane */
2   chan/2  -width/2  -dia/2-stand   fixed constraint 1
3   chan/2   width/2  -dia/2-stand   fixed constraint 1
4   0.0      width/2  -dia/2-stand   fixed constraint 1
5   0.0     -width/2   dia/2+stand   fixed
6   chan/2  -width/2   dia/2+stand   fixed
7   chan/2   width/2   dia/2+stand   fixed
8   0.0      width/2   dia/2+stand   fixed
9   -pi/4 boundary 1 fixed
10  0.0   boundary 1 fixed
11   pi/4 boundary 1 fixed
12  -pi/4 boundary 2 fixed
13  0.0   boundary 2 fixed
14   pi/4 boundary 2 fixed
15  0.0  -width/2 -dia/2 fixed
16  0.0   width/2 -dia/2 fixed
17  0.0  -width/2  dia/2 fixed
18  0.0   width/2  dia/2 fixed
//30  0.25  0.25 -dia/2-stand  fixed   /* for table top */
//31  0.25 -0.25 -dia/2-stand  fixed
```

```
//32 -0.25 -0.25 -dia/2-stand  fixed
//33 -0.25  0.25 -dia/2-stand  fixed

edges  /* given by endpoints and attribute */
1   1  2     fixed constraint 1 /* 4 edges on plane */
2   2  3     fixed constraint 1
3   3  4     fixed constraint 1
4   4  1     fixed constraint 1
5   5  6     fixed
6   6  7     fixed
7   7  8     fixed
8   8  5     fixed constraint 3,5
9   15  9    fixed constraint 2
10  9  10    fixed constraint 2
11  10 11    fixed constraint 2
12  11 17    fixed constraint 2
13  16  12   fixed constraint 2
14  12 13    fixed constraint 2
15  13 14    fixed constraint 2
16  14 18    fixed constraint 2
17  2   6    fixed
18  3   7    fixed
19  9  12    fixed
20  10 13    fixed
21  11 14    fixed
22  16 15    fixed constraint 5
23  1  15    fixed constraint 5
24  4  16    fixed constraint 5
25  17 18    fixed constraint 5
26  17 5     fixed constraint 5
27  18 8     fixed constraint 5
//30  30 31  no_refine fixed  /* for table top */
//31  31 32  no_refine fixed
//32  32 33  no_refine fixed
//33  33 30  no_refine fixed

faces  /* given by oriented edge loop */
1   1 17  -5 -26 -12 -11 -10 -9 -23 tension tens   color red
2   2 18  -6 -17  tension tens constraint 4        color yellow
3   3 24  13  14 15 16 27 -7 -18    tension tens   //constraint 7 color lightgreen
5   5 6 7 8       tension tens constraint 3        color blue
6   -1 -4 -3 -2    tension tens constraint 1
7   22 9 19 -13    tension tens constraint 2       color green
8   -19 10 20 -14  tension tens constraint 2       color lightblue
```

```
9   -20 11 21 -15  tension tens constraint 2        color blue
10  -21 12 25 -16  tension tens //constraint 6        color red
11  23 -22 -24 4   constraint 5
12  26 -8 -27 -25  constraint 5
//30  30 31 32 33  no_refine color green density 0.008 fixed /* table top for display */

bodies  /* one body, defined by its oriented faces */
1 1 2 3 5 6 7 8 9 10 11 12  volume  0.5*width*((dia+2*stand)*chan - 3.14*dia^2/4)+ve
density 0
```

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