ABSTRACT

Title of Dissertation: Electronic Properties of Carbon Nanotubes studied in
Field-Effect Transistor Geometries

Tobias Dürkop, Doctor of Philosophy, 2004

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Due to their outstanding properties carbon nanotubes have attracted considerable research effort during the last decade. While they serve as an example of a 1-dimensional electron system allowing one to study fundamental quantum effects nanotubes—especially semiconducting nanotubes—are an interesting candidate for next-generation transistor application with the potential to replace silicon-based devices.

I have fabricated nanotubes using chemical vapor deposition techniques with various catalysts and gas mixtures. The nanotubes produced with these techniques vary in length from 100 nm to several hundreds of micrometers. While data taken on shorter metallic and semiconducting devices show Coulomb blockade effects, the main part of this work is concerned with measurements that shed light on the intrinsic properties of semiconducting nanotubes.

On devices with lengths of more than 300 μm I have carried out measurements of the intrinsic hole mobility as well as the device-specific field-effect mobility. The mobility

measured on these nanotube devices at room temperature exceeds that of any semiconductor known previously.

Another important consideration in nanotube transistor applications are hysteresis effects. I present measurements on the time scales involved in some of these hysteresis effects and a possible application of the hysteresis for memory devices.

Electronic Properties of Carbon Nanotubes studied in

Field-Effect Transistor Geometries

by

Tobias Dürkop

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Chapter 1

Introduction

Carbon and its compounds have long been known to have an immense variety of uses and applications. As oil, natural gas or coal, carbon is used to deliver most of the energy used today. Materials made of carbon compounds have been used in cutting edge technology in all ages. For example the compound known as "wood" is stable enough to be formed into the image of a large horse facilitating one of the most important military victories known [1]. The same compound also allowed the construction of such things as ships, which were indispensable for the first Europeans to travel to America, ultimately resulting in the constitution of the USA, which is written on yet another carbon compound called "paper".

Compared to the number of uses for carbon compounds the number of applications for elemental carbon have been limited, possibly due to the fact that for most of the time there were only two known forms of elemental carbon, i. e. diamond and graphite.

Recently, however, more forms of elemental carbon have been discovered. Despite early (1970) theoretical predictions (for references and more details see [2]), which sug-

gested icosahedral clusters of 60 C-atoms to be chemically stable, these clusters known as fullerenes or Buckminsterfullerenes were not found experimentally before 1985 [3]. In 1991 another form of elemental carbon was discovered by S. Iijima [4] (for more details see chapter 2): Carbon Nanotubes. Carbon nanotubes can be metallic and semiconducting making them an interesting and promising material for many future applications including applications as transistors.

While metallic nanotubes can be incorporated in devices like single electron transistors and quantum dots showing quantum behavior at low temperatures and single electron effects even at room temperatures [5], semiconducting nanotubes can be used as field-effect transistors potentially replacing silicon-based devices in future computers.

This work focuses on various aspects of nanotubes in transistor applications. Single electron transistors are being investigated as a background for the experiments on nanotube field-effect transistors and to obtain better knowledge of the methods of device fabrication that are used. The experiments on semiconducting nanotube devices aim to gain a better understanding of the fundamental properties of conduction in semiconducting nanotubes. Experiments on devices made from "ultralong" ($> 300\,\mu$m) nanotubes are presented. The main result of these experiments is that charge carriers in nanotubes (holes) have an intrinsic mobility at room temperature that is higher than in any other semiconductor and show remarkably long mean free paths of several micrometers. Another aspect of the behavior of nanotube transistors is the presence of hysteresis. Some investigations of temperature dependence and long term behavior of this hysteresis are being presented together with a possible application of the hysteresis in memory elements.

Chapter 2

Nanotube Basics

2.1 Historical Overview

Already before 1980 there were some experimental observations of thin carbon fibers or tubes produced by decomposing hydrocarbons in the presence of some form of catalyst [6, 7, 8]. The discovery of fullerenes in 1985 by Kroto et al. [3] increased the general interest in structures consisting of elemental carbon starting a significant amount of research activity. A good overview of the research on fullerenes can be found in [2].

However, research on carbon nanotubes (CNTs)[1] did not seriously begin until multi-walled carbon nanotubes (MWNT), initially dubbed "helical microtubules of graphitic carbon" [4], were discovered by S. Iijima while researching methods of producing fullerenes. Using transmission electron microscopy (TEM) he discovered unusual fibers in the soot produced by an arc discharge between carbon electrodes, and identified them as seamless, concentrically nested, tubular sheets of graphite. Theoretical predictions about structure

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[1]A list of abbreviations used throughout the text can be found in appendix A on page 96.

and electronic properties of CNTs followed quickly [9, 10, 11, 12]. Soon methods were developed to produce single-walled carbon nanotubes (SWNT), i. e. nanotubes that consist of only a single sheet of graphite, by Iijima [13] and Bethune [14]. The production of SWNT in large quantities by laser ablation [15] finally spurred intense research on this material, revealing outstanding electrical, thermal and mechanical properties.

2.2   Nanotube Properties

This work deals mainly with various aspects of the electronic properties of carbon nanotubes. Accordingly their remarkable properties in other areas will not be treated in any detail. However, for completeness some of them shall at least be mentioned here.

Young's modulus for graphite is strongly anisotropic due to its layered structure consisting of stacked sheets of single atomic thickness ("graphene" sheets) that are loosely bound to each other. While the out-of-plane value, i. e. the value perpendicular to the sheets ($\sim 1\,\mathrm{GPa}$ [16]) is low compared to many other materials, the structure of a nanotube (see section 2.2.1) allows for a value over 1000 times higher because its properties are derived from the much higher in-plane modulus of graphite. Using different techniques Treacy et al. [17] and Wong et al. [18] have found Young's modulus in nanotubes to be $1.8\,\mathrm{TPa}$ and $1.2\,\mathrm{TPa}$, respectively. Later measurements by various groups (for an overview of the mechanical properties of CNTs see for example [16]) essentially found values within the limits given by the measurements mentioned. Although measurements of the tensile strength of CNTs report less consistent results between 10 and $60\,\mathrm{GPa}$ [19, 20, 21] it is clear that nanotubes are remarkably strong, in fact so strong that the idea
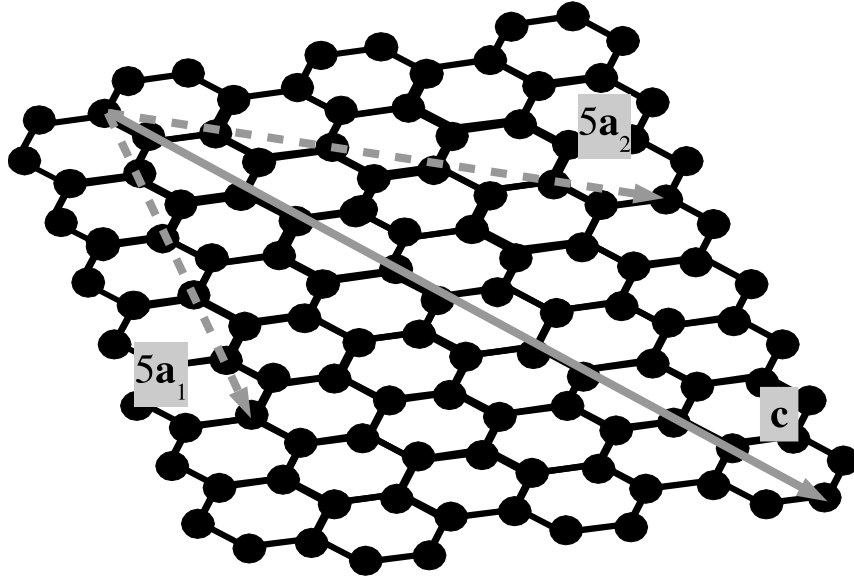
Figure 2.1: Hexagonal lattice of a graphene sheet: The dashed arrows indicate the directions of a common choice of basis vectors $\mathbf{a}_1$ and $\mathbf{a}_2$ to define chiral (or rollup) vectors in a carbon nanotube. The solid arrow shows the chiral vector $\mathbf{c} = 5\mathbf{a}_1 + 5\mathbf{a}_2$ for a (5,5)-armchair tube.

of using nanotube-based cables for an elevator into space [22] is being dreamed about.

2.2.1 Structure

To understand the atomic structure of a carbon nanotube it is best to start by looking at so-called graphene, which is nothing but a single sheet of graphite. The carbon atoms in graphene are sp^2-hybridized and arranged in a hexagonal lattice. Figure 2.1 shows an example of such a lattice. To form a carbon nanotube such a graphene sheet is rolled up into a seamless tube as verified by high-resolution transmission electron microscopy (TEM) and scanning tunneling microscopy (STM) [23]. To characterize the way in which the tube is rolled up one uses the chiral (or rollup) vector $\mathbf{c}$, which points around the circumference of a nanotube describing what unit cell of the graphene lattice is mapped
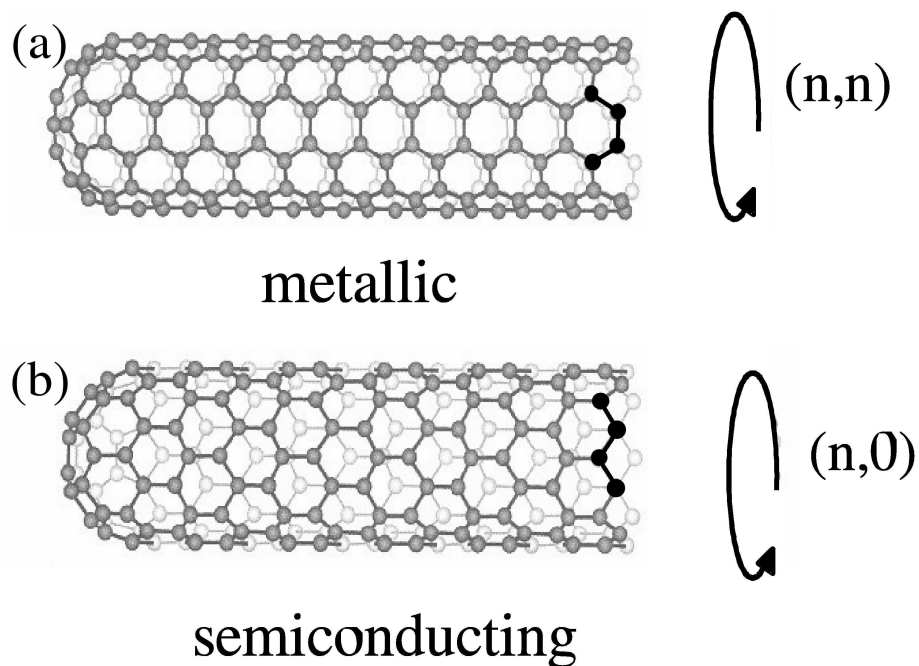
Figure 2.2: Examples of different types of nanotubes: (a) Metallic (*n*,*n*)-nanotube (see also section 2.2.2). The configuration of bonds along the chiral vector (emphasized in black) resembles an armchair. (b) Semiconducting (*n*,0)-nanotube. Here the bonds are in a zigzag configuration along the chiral vector.

onto itself by rolling up the sheet. Using the basis vectors $\mathbf{a}_1$ and $\mathbf{a}_2$ as illustrated in

figure 2.1 the chiral vector is given by $\mathbf{c} = n\mathbf{a}_1 + m\mathbf{a}_2$, usually written simply as (*n*,*m*). The

choice of *n* and *m* determines the properties of a nanotube. The so-called chirality of a

nanotube is measured by its chiral angle θ, which is the angle between $\mathbf{a}_1$ and $\mathbf{c}$. Figure 2.2

shows two examples for carbon nanotubes: Figure 2.2(a) shows a so-called "armchair"

tube that has a chiral angle of $\theta = 30°$ and indices (*n*,*n*). The nanotube in figure 2.2(b)

is a "zigzag" tube with indices (*n*,0) and a chiral angle of $\theta = 0°$ [11]. Although there is

no evidence that common methods of nanotube synthesis (see section 2.3) produce these

special types of nanotubes more frequently than so-called chiral nanotubes, which have

arbitrary indices n and m, these two special configurations have attracted more research attention than others due to their higher degree of symmetry, which allows for easier theoretical treatment.

The diameter d of a nanotube is given by the length of $\mathbf{c}$ divided by π [11]:

$$d = \frac{|\mathbf{c}|}{\pi} = \frac{\sqrt{(n\mathbf{a}_1 + n\mathbf{a}_2)^2}}{\pi} = \frac{\sqrt{3}a\sqrt{n^2 + nm + m^2}}{\pi}, \qquad (2.1)$$

where a is the length of the carbon-carbon bond (1.42 Å).

2.2.2 Electronic Properties

The next important question is how a nanotube's chirality influences its the electronic properties. As an introduction we first look at the band structure of graphene. The first tight-binding calculations including only the π- and π^*-orbitals of graphene were presented by P. R. Wallace as early as 1947 [24]. They serve well as a simplified model to understand the basic features of the transformation from graphene to a carbon nanotube. Figure 2.3(a) shows a simplified model of the graphene bands near the Fermi level (marked by the plane defined by the hexagon). In this low energy region the valence as well as the conduction band can be approximated by cones whose slopes are given by the Fermi velocity $v_F = 8.1 \times 10^{-5}$ m/s [25] and whose apices meet at the K-point of the graphene Brillouin zone. This picture ignores the trigonal warping of the graphite lattice [26, 27], as well as the behavior at higher energies.

When rolling the graphene into a nanotube an additional quantization is imposed on the electron wave functions: $k_c \cdot c = 2\pi i$. Here k_c is the circumferential component of the electron wave vector, c is the magnitude of $\mathbf{c}$ and i is an integer. This additional condition
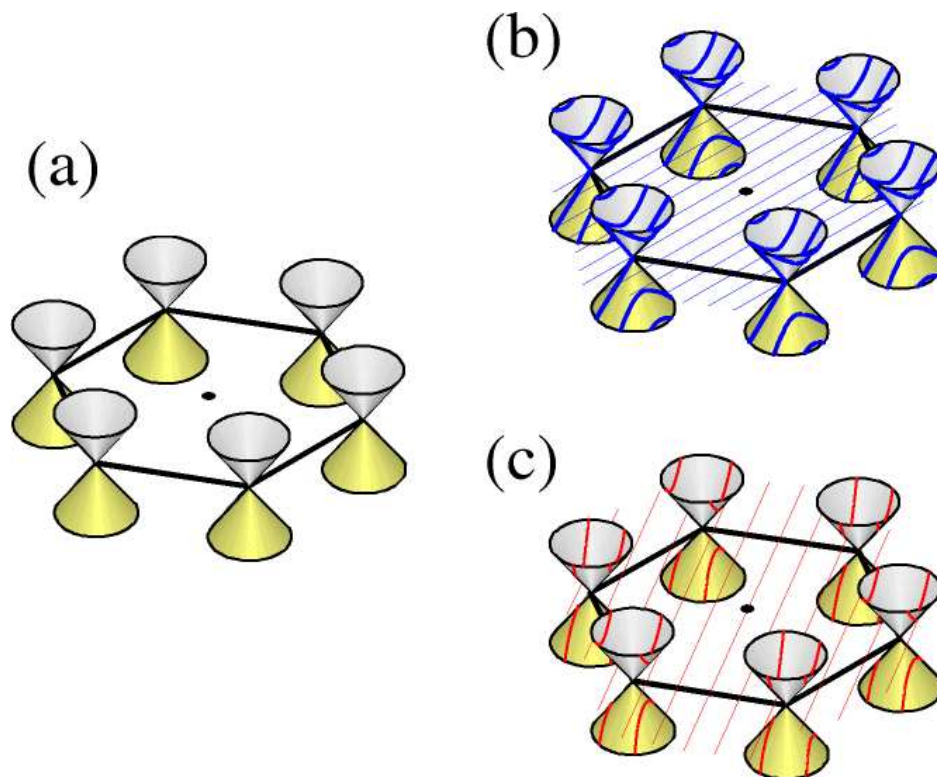
Figure 2.3: Schematic view of the band structures of (a) graphene, (b) a metallic carbon nanotube and (c) a semiconducting carbon nanotube. The black hexagons represent the plane of the Fermi level in 2D momentum space. Near the Fermi level the conduction band (grey) and valence band (yellow) in graphene are cone shaped with the cones' apices meeting at the Fermi-energy. When rolling up the graphene into a CNT another quantization condition is imposed onto this band structure, essentially cutting slices out of the band structure. If these slices pass through the apices of the cones—blue slices in (b)—the CNT is metallic; otherwise—red slices in (c)—the CNT is semiconducting.
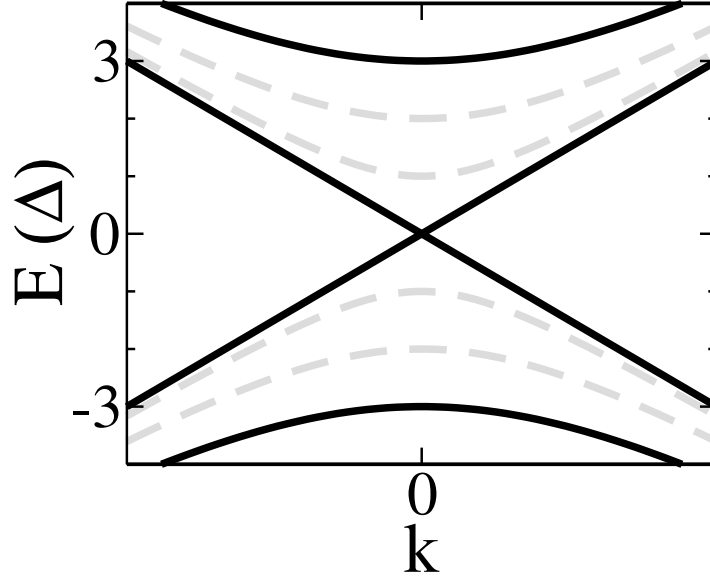
Figure 2.4: Nanotube and structure: The subbands shown as black straight lines are present in a metallic nanotube while the bands drawn as grey dashed lines are present in a semiconducting nanotube of the same diameter. The bands have been calculated using the hyperbolic approximation presented in formula 2.2.

effectively cuts slices out of the cone shaped band structure. Depending on the chirality of the particular nanotube these slices can either pass through the cones' apices to form the linear bands of a metallic nanotube or miss the apices and form hyperbolic bands and a band gap. It can be shown [11, 10] that nanotubes are metallic, if the indices n and m fulfill the relationship $n - m = 3i$ where i is a whole number. The shape of the bands as a function of the wave number k can then be calculated using

$$E(\Delta) = \pm\sqrt{\left(\frac{\hbar v_F k}{2}\right)^2 + (\nu\Delta)^2}. \tag{2.2}$$

In this equation E is measured relative to E_F, the Fermi energy. The semiconducting band gap E_g is given by 2Δ, while v_F is the Fermi velocity. The integer $\nu = 0, 1, 2, \ldots$ counts the subbands. The result of this calculation is sketched in figure 2.4. The first bands present in a metallic tube are the bands with $\nu = 0, 3$, whereas the lowest energy bands in
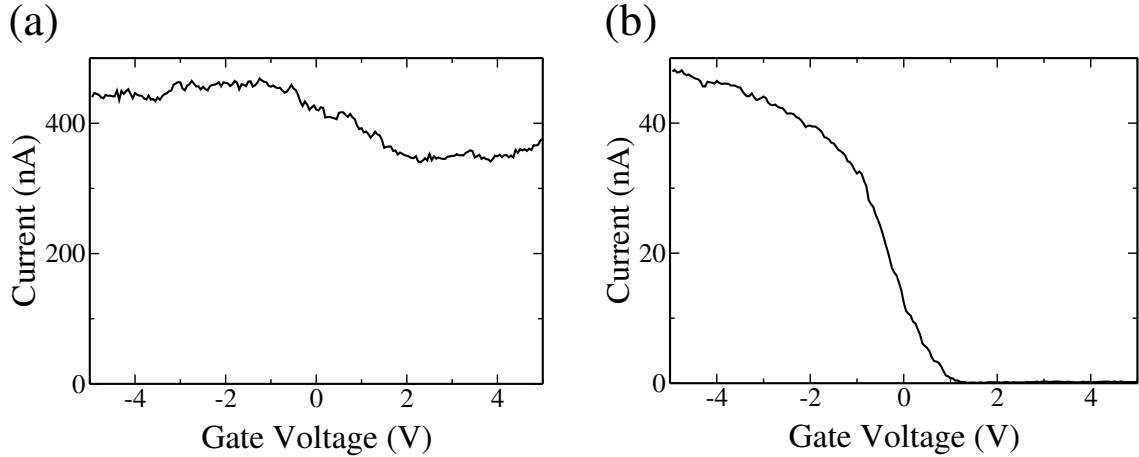
Figure 2.5: Examples for the behavior of carbon nanotube devices at room temperature. A constant bias voltage is applied across the device. The source-drain current I is shown as a function of applied gate voltage V_g. A schematic of these devices is shown in figure 3.1. (a) Metallic nanotube device: Ideally the current should not show any V_g-dependence. However, a small variation is quite typical. (b) Semiconducting nanotube device: The current turns off completely as V_g goes from negative to positive. This p-channel behavior, which is typical for as-prepared nanotube devices, is probably caused by doping through atmospheric oxygen. (See also figure 3.1 in section 3.1.)

a semiconducting tube have $\nu = 1, 2$ [10].

Within this picture to first order [28] the size of the bandgap is inversely proportional to the nanotube diameter $E_g = 2\Delta \approx 0.7/d$, where E_g is in electron-Volts if the diameter d is given in Ångström. Taking into account the curvature of the graphene when rolled into a nanotube one also gets a contribution to the band gap that is proportional to d^{-2}. This effect also causes a small band gap of around 0.05 eV [10, 28] or less in "metallic" nanotubes with indices other than (n,n), i. e. in "metallic" nanotubes that are not armchair tubes.

It took researchers several years for nanotube fabrication methods (see section 2.3 on page 14) to be able to supply carbon nanotubes in sufficient quantity and quality, which

was necessary to obtain experimental verification for these early predictions about the nanotubes' electronic structure.

In 1997 the first groups reported successful fabrication of devices from single carbon nanotubes or bundles of few nanotubes [29, 30]. Both groups report transport measurements on devices that are metallic at room temperature, i. e. their I-V curves are Ohmic, and their resistance does not depend on an applied gate voltage. At low temperatures they exhibit Coulomb blockade behavior (for more details see section 5 on page 57) acting as single-electron transistors (SETs). Devices that incorporated semiconducting nanotubes followed shortly after [31]. Such a device behaves in a way similar to a traditional field-effect transistor (FET); its resistance can be switched by several orders of magnitude [32] depending on the applied gate voltage V_g.

Figure 2.5 shows examples of the behavior of nanotube devices. The tube in figure 2.5(a) shows metallic behavior. While applying a bias (or source-drain) voltage V_{sd} of 10 mV the current through the device is about 400 nA roughly independent of applied gate voltage V_g. Figure 2.5(b) shows an example for a semiconducting nanotube device often called tubeFET. For the same V_{sd} a strongly V_g-dependent current can be seen. Device resistances of 25 kΩ for the tube and 200 kΩ for the semiconducting device are typical for devices with good contacts.

Transport measurements on nanotube devices can verify the existence of metallic and semiconducting CNTs, give information about low energy excitations in a device [30, 29], and even show the existence of the small bandgap in non-armchair metallic nanotubes [33]. They cannot, however, show the details of the band structure. To investigate the de-

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tails of the band structure and verify the theoretical predictions made in [10, 9, 11] there are two types of commonly used measurement techniques. The first technique is called scanning tunneling spectroscopy (STS) and uses a scanning tunneling microscope (STM) to locally probe the density of states (DOS). According to Saito et al. [12] the DOS contains $1/\sqrt{E}$ singularities, so-called van-Hove singularities at the onset of new subbands. The positions and spacing of these singularities are correlated with the chirality of a nanotube. Using STS Odom et al. and Wildöer et al. [34, 35] have verified these predictions. Their experiments even allowed for identification of the chirality of individual nanotubes by using the real-space information gained from STM combined with the band structure information from STS-measurements. Unfortunately this type of STM-measurements require the nanotubes to be on a conducting substrate, e. g. gold. Since nanotube devices have to be on an insulating substrate it is impossible to use use these techniques to identify nanotubes that are parts of devices (unless someone clever finds a method to do it anyway).

The second group of experiments suitable for giving detailed insight into the nanotube band structure is based on optical techniques. Because Raman scattering from nanotubes is enhanced if the system is excited by photons in resonance with a transition between van Hove singularities, it is possible to use Raman spectroscopy to investigate the nanotube electronic structure as well as their phonon spectrum [36, 37]. Recent progress has allowed Raman spectroscopy investigations on individual nanotubes [38]; combined knowledge of the electron and phonon spectra allow unique determination of the indices (*n,m*) of individual nanotubes. Transitions between van Hove singularities are also observed in

the excitation and emission spectra in fluorescence experiments on semiconducting nanotubes in solution. Recently Bachilo et. al. [39] have been able to map the position of absorption and emission peaks in fluorescence spectroscopy onto particular chiralities of semiconducting nanotubes. Raman spectroscopy and fluorescence spectroscopy together have since been performed on single nanotubes to verify the (n,m) assignments [40].

2.3   Fabrication of Carbon Nanotubes

There are two fundamentally different types of methods of growing carbon nanotubes for device fabrication. The first class of methods tends to produce large amounts (of course the term "large" is relative; here it refers to gram-amounts at best) of nanotubes usually as nanotube-containing soot (see section 2.3.1), from which the nanotubes are deposited onto substrates for device fabrication after being purified. The second class of methods synthesizes the nanotubes directly on some substrate by first depositing some kind of catalyst and then exposing it to carbon-containing feedstock gas (see section 2.3.2).

2.3.1   Bulk Methods

Arc-Discharge Evaporation

Arc-discharge evaporation was the first technique used to produce carbon nanotubes [4]. It was derived from similar techniques used for the production of fullerenes [41]. In this method the carbon nanotubes are grown by a d. c. arc-discharge between two carbon electrodes in a vessel filled with an inert gas (e. g. argon at 100 torr [4]). This technique

was also used as the first method to produce single-walled carbon nanotubes (SWNT) [14, 13] using electrodes that contained Fe, Ni or Co catalyst and Ar or He as the inert gas in the reactor. Unfortunately the nanotube yield of such an arc-discharge tends to be fairly low so that arc-discharge evaporation is no longer used for nanotube production.

Laser Ablation

Laser ablation was the first method that allowed production of large quantities of carbon nanotubes [15]. In this method a carbon target doped with powdered Ni and Co as catalyst is heated to 1000°C in vacuum and then bombarded with laser pulses. This method results in a high yield of SWNTs with a narrow diameter distribution. With this method of synthesis the nanotubes are usually clustered together in ropes several hundreds of Ångström thick [42, 43] which need to be separated into single tubes and purified, if they are supposed to be used for electronic devices. Although there are many methods for purifying nanotubes, most prominently the method described in [44] which uses nitric acid to cleanse the nanotube soot from catalyst impurities and amorphous carbon and ultrasound to separate individual nanotubes from the ropes, all these methods either fail to completely remove impurities or leave relatively short pieces of nanotubes with relatively high numbers of defects.

HiPCO

Recently the so-called HiPCO-process of producing nanotubes in bulk amounts has become more and more popular. It has further increased the yield of nanotube production to several grams per day. HiPCO, which was first presented by Bronikowski et al. [45],

stands for **Hi**gh **P**ressure decomposition of **CO** (carbon monoxide). In this method CO-gas with a small amount of iron pentacarbonyl ($Fe(CO)_5$) added is injected into a reactor at high temperatures (900–1100°C) and high pressures (30–50 atm) [45, 46]. The $Fe(CO)_5$ decomposes during the injection and forms the nanoparticles that are required to act as catalyst, while the CO is the feedstock gas that provides the carbon for the nanotube growth. Just like nanotubes grown by laser ablation HiPCO tubes need to be purified before being used for device fabrication [47].

2.3.2   Chemical Vapor Deposition

Catalysts

To grow carbon nanotubes using any form of chemical vapor deposition technique (CVD) the first step is to prepare the catalyst. For the growth of nanotubes — especially for SWNTs — it is essential to obtain catalyst particles that have diameters in the nanometer range. The earliest published method of achieving such nanoparticles [48] used a rather complicated and time consuming process of impregnating Al_2O_3 particles with an metal-organic compound using a methanol solution, baking the catalyst, grinding it and finally passing it through a sieve. The metals used were Mo, Ni and Co with a mixture of Ni and Co producing the highest nanotube yield. This kind of catalyst is called "supported catalyst" [49]. Presumably the Al_2O_3 acts as a support for the transition metal catalyst ensuring it to have the right particle size or more generally the large surface curvature necessary for nanotube growth.

Improved methods of catalyst preparation as well as experiments with different metal-

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organic compounds of Fe, Ni, Co and Mo and various combinations of them together with different support materials (Al_2O_3 and SiO_2) have been presented in [50, 51, 52]. A significant improvement was the ability to control the location of catalyst particles on the substrate surface [53]: By using electron-beam lithography techniques[2] Kong et al. were able to create well-defined patterns of catalyst particles on their substrates, essentially controlling the locations in which nanotubes would grow. Another improvement was a simplified technique of catalyst preparation [54]. In this method substrates are dipped into a solution of $Fe(NO_3)_3$ (ferric nitrate) in 2-propanol followed by a dip into hexanes causing the $Fe(NO_3)_3$ to precipitate out of of solution forming nanoclusters on the substrate surface. An advantage of this method is its speed and ease of use. Its main disadvantage is bad control over the size of iron-nanoclusters formed and subsequently the diameter of nanotubes grown. One successful attempt of controlling the size distribution is the use of monodispersed metal-cluster containing organic molecules as demonstrated in [55].

Nanotube Growth

After depositing the catalyst the next step is the actual nanotube growth. The simplest and most common method is to place the samples inside a tube furnace as shown in figure 2.6. An oven like this has been used in most publications investigating CVD-grown CNTs. During the growth process the samples are usually heated to the growth temperature (600°C–1200°C) with some inert gas flowing through the oven, in some cases

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[2]Covering the substrate with e-beam resist (PMMA), writing patterns into the resist with an SEM, developing the resist, depositing the catalyst onto the substrate and removing the remaining PMMA together with the undesired catalyst. For details see also section 4.2
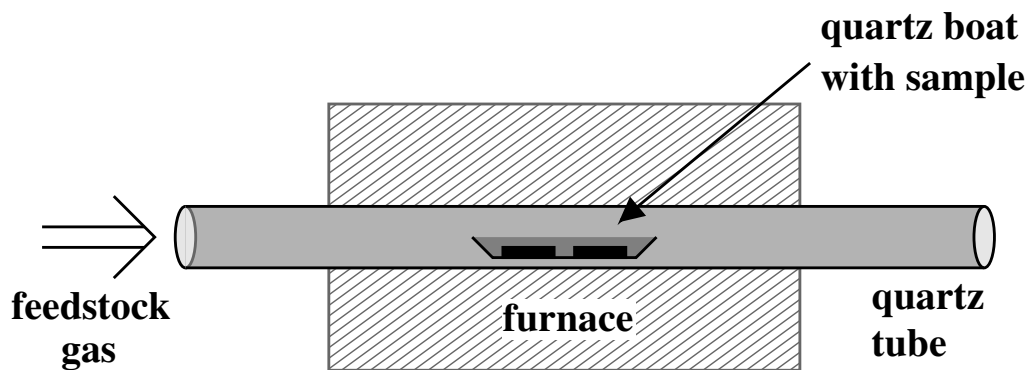
Figure 2.6: Schematic setup of a tube furnace as used for nanotube growth. The carbon containing feedstock gas flows through a quartz tube that is enclosed by the furnace. The samples are placed inside a quartz boat in the center of the quartz tube.

with added H_2 to reduce the catalyst [54]. After reaching the growth temperature the gas flow is switched to the actual feedstock gas sometimes together with the inert gas. Initially CO was used as the feedstock gas [48]. Later different gases were used, too: CH_4 [50, 54], CH_4 mixed with C_2H_4 producing exceptionally long tubes [56], pure C_2H_4 [57] or even C_2H_2 [58]. For successful nanotube growth it is generally true that the lower the feedstock gas' carbon content and the more thermically stable it is the higher the growth temperature and the feedstock gas' partial pressure needs to be. A more detailed overview of various growth methods can be found in [49].

Chapter 3

Nanotube Devices

3.1 Methods for Device Fabrication

Although there are many different types of nanotube-based nanodevices notably mechanical devices (for a review of nanotube-based mechanical devices see e. g. [59]) and field-emission devices (see e. g. [60]) this work will focus on nanotube transistors and derived devices. The archetypical nanotube transistor is shown in figure 3.1: The nanotube is contacted by a source and a drain contact while the gate electrode—electrically insulated from the tube—can be used to manipulate the nanotube's electronic structure. Depending on the particular method of nanotube fabrication (see section 2.3) there are different ways in which a nanotube transistor can be structured. However, most publications on nanotube transistors report the use of a degenerately doped Si-substrate with a comparatively thick (100 nm–500 nm) thermally grown oxide layer (see e. g. [30, 32, 61, 62, 63, 64, 65, 66]). This kind of substrate is readily available and can be used with bulk-produced nanotubes as well as nanotubes grown directly on the substrate by CVD-methods. If doped highly,

Source   **Drain**
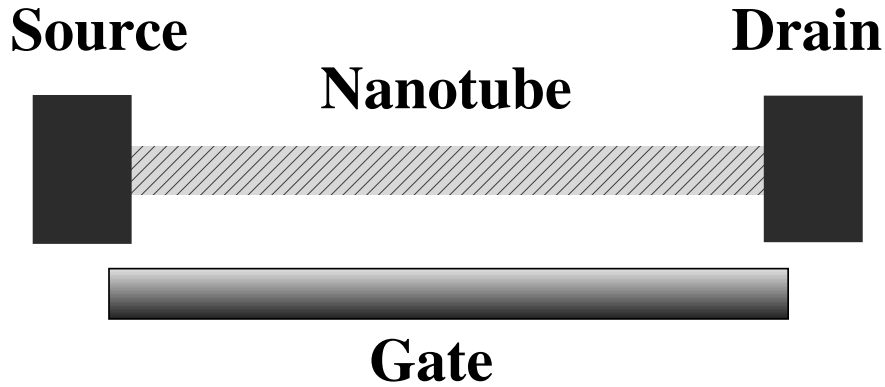
Nanotube

Gate

Figure 3.1: Schematic of a nanotube transistor. The nanotube acts as a channel between source and drain contacts. The gate is used to control the resistance of the channel. By applying a voltage to the gate it is possible to control the resistance of the device.

the Si-substrate stays conductive even at low temperatures making it usable as a so-called back-gate with the SiO_2 as a stable, if low-κ, gate-dielectric.

Bulk-produced nanotubes (laser-ablation or HiPCO)—after being purified—are usually deposited onto samples by suspending them in an organic solvent (chloroform, dichloroethane,...) and then spin-coating the substrate with the nanotubes to create an even distribution of nanotubes over the substrate surface. This method allows manufacturing two different configurations for the source and drain contacts. By creating the contacts before depositing the nanotubes (e. g. [31]) one can achieve so-called bulk-contacted nanotubes, whereas depositing the contacts onto the nanotubes creates end-contacted nanotubes (e. g. [67]). In this context "end-contacted" refers to the fact that depositing contact material on top of the nanotube normally destroys the nanotube electronic structure underneath the contacts. It only remains unchanged between the contacts with its ends at the contacts. This configuration usually guarantees a lower contact resistance than achievable in bulk-contacted devices. Furthermore the device characteristics of both types of devices

are slightly different in the low-temperature regime (see e. g. [68]).

Since gold, the most commonly used contact material, melts at temperatures below those needed for nanotube-CVD, it is impossible to grow nanotubes on top of gold contacts. Therefore by far the most common method of contacting CVD-grown nanotubes is to deposit contacts onto the tubes (see e. g. [69, 70, 71]). Often the contacts are annealed to lower contact resistance [72]. Only few researchers have presented experiments in which the contacts were prepared before nanotube growth as in [73]. While such an approach is desirable for integration of nanotubes into electronics the devices produced with these methods often have undesirable characteristics (small on-off ratio, high contact resistance) [74].

Several studies have tried to optimize the material used for the contacts. From the choices of material made in the earliest publications (Cr/Au [30] or Pt [29]) only the Cr/Au-contacts have been used widely. In this type of contacts the chromium layer is a thin ($\sim$ 1–3 nm) adhesion layer that facilitates adhesion of the gold to SiO_2. It has been found thatăan adhesion layer of Ti [75], especially when annealed, allows deposition of smooth films of many metals onto carbon nanotubes because Ti forms titanium carbide at the interface with the nanotube. For this reason Ti/Au-contacts are another frequently used combination of contact materials. Many publications investigating Schottky barriers between a nanotube and its contacts (e. g. [71, 76]) have employed this kind of contact. Pd is another material investigated in [75] that wets nanotubes well. It has been used in a recent publication [65] to produce NT-FETs with Ohmic contacts, i. e. contacts without Schottky barriers.
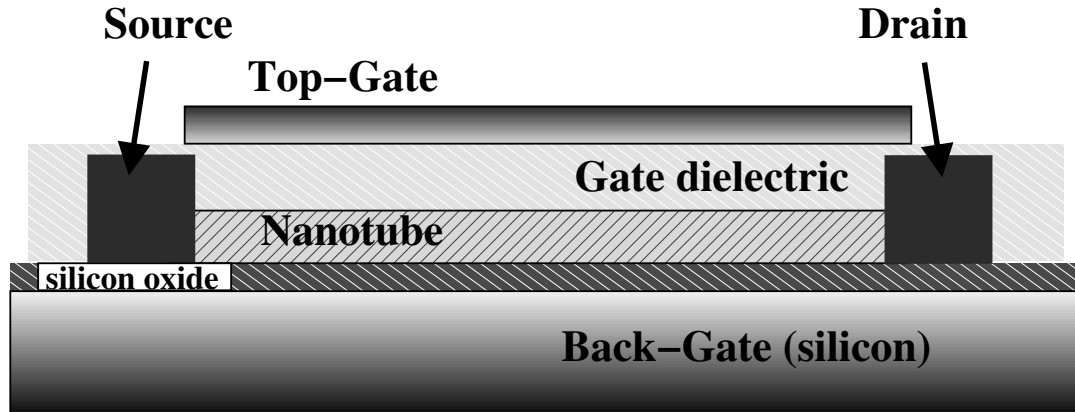
Figure 3.2: Schematic of a nanotube transistor with back- and top-gate.

The use of the "built-in" back-gate is convenient since it does not require additional fabrication steps. Its disadvantages are the fact that it is impossible to address devices on the same sample individually and the comparatively low dielectric constant of the gate dielectric SiO_2 ($\kappa \approx 4$) which limits the achievable gate capacitance and thus the transistor performance.

To address devices individually it is necessary to create separate gate electrodes for individual devices. One approach followed by Bachtold et al. [77] is to deposit nanotubes on top of Al-wires that are capped with thin Al_2O_3, which act as local back-gates. A different approach is to deposit top-gates onto nanotube devices. This approach was first used by Wind et al. [78] using the decomposition of SiH_4 and O_2 to form SiO_2 on top of nanotube devices. Generally, one of the problems in fabricating top gates is to find processes that do not destroy the nanotube. Figure 3.2 shows a schematic view of a nanotube transistor with top and back gate. The issue of increasing the gate capacitance has already been intensively studied for traditional Metal Oxide Semiconductor FETs (MOSFETs). One common approach is to use a material with a high dielectric constant κ

as the gate dielectric. Javey et al. [79] successfully fabricated top-gates out of zirconium oxide. Another material used was HfO_2 [71, 80]. The material with the highest κ used for nanotube transistors is strontium titanate ($SrTiO_3$: $\kappa \sim 175$); Kim et al. [81] have successfully used CVD to grow nanotubes directly on $SrTiO_3$-capped Si-substrates.

3.2 Low Temperature Physics: Single Electron Transistors

Unlike most of the physics investigated in this work single-electron transistors (SETs) are inherently based on phenomena occurring at low temperatures. (Researchers have managed to extend the working range of nanotube SETs up to room temperature [5, 82], but for argument's sake let's consider room temperature as an "extended low temperature" for SETs, while for FETs it is, well, room temperature.) To give a qualitative, and within limits, also quantitative description of SETs within the scope of this work it is sufficient to use a description within the framework of the so-called orthodox SET-theory as outlined in [83] following [84]. As illustrated by figure 3.3 an SET in its simplest form is a small conducting dot, usually called "island", that is connected to source and drain contacts through tunnel junctions with high but finite resistances. The total capacitance C_Σ of the island is given by the sum of its capacitances to the source contact C_s, the drain C_d and the gate C_g: $C_\Sigma = C_s + C_d + C_g$. A single charge e that tunnels onto the island has to overcome the charging energy $E_C = e^2/2C_\Sigma$. If the temperature T of the system is low enough, i. e. $k_B T \ll E_C$, tunneling onto or off the island is energetically forbidden
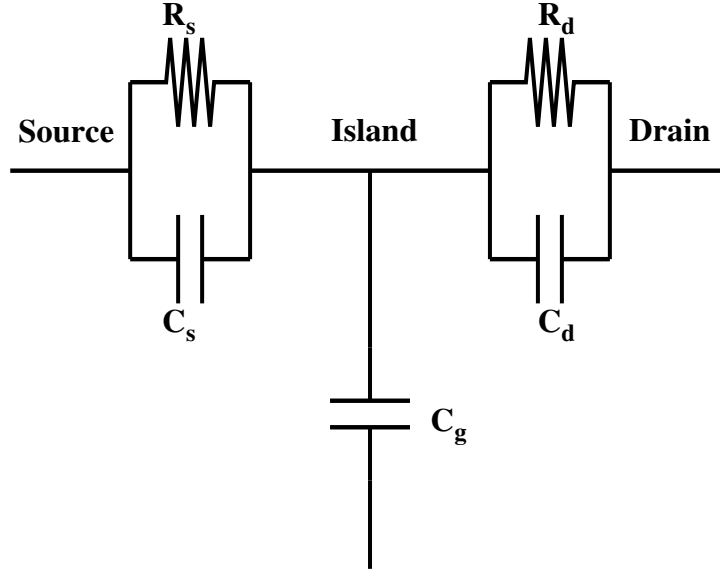
Figure 3.3: Schematic of an SET. The island is coupled to the source and drain contacts through tunnel junctions, which are characterized by the capacitances C_s, C_d and the tunnel resistances R_s, R_d between the island and the contacts. The capacitance between the gate and the island is C_g.

because of the charging energy, unless the energy can be supplied by an applied bias voltage $|V_{sd}| > e/2C_\Sigma$. This suppression of tunneling is called Coulomb blockade.

Besides the requirement on the temperature, there is a second requirement on the resistances of the tunnel junctions for Coulomb blockade to be clearly observable in a physical system. The lifetime of a charge on the island must be long enough. We can estimate the lifetime Δt by using the RC-time calculated from C_Σ and R, the lower of the resistances to source and drain, R_s and R_d: $\Delta t = RC_\Sigma$. To measure an energy difference of $\Delta E = E_C$ according Heisenberg's uncertainty relation the lifetime must fulfill $\Delta E \Delta t = e^2/2C_\Sigma \cdot 2RC_\Sigma > h$. Thus, we get two conditions to be able to observe Coulomb blockade:

$$E_C \gg k_B T$$

$$R > \frac{h}{e^2} = 25.8\,\text{k}\Omega \tag{3.1}$$
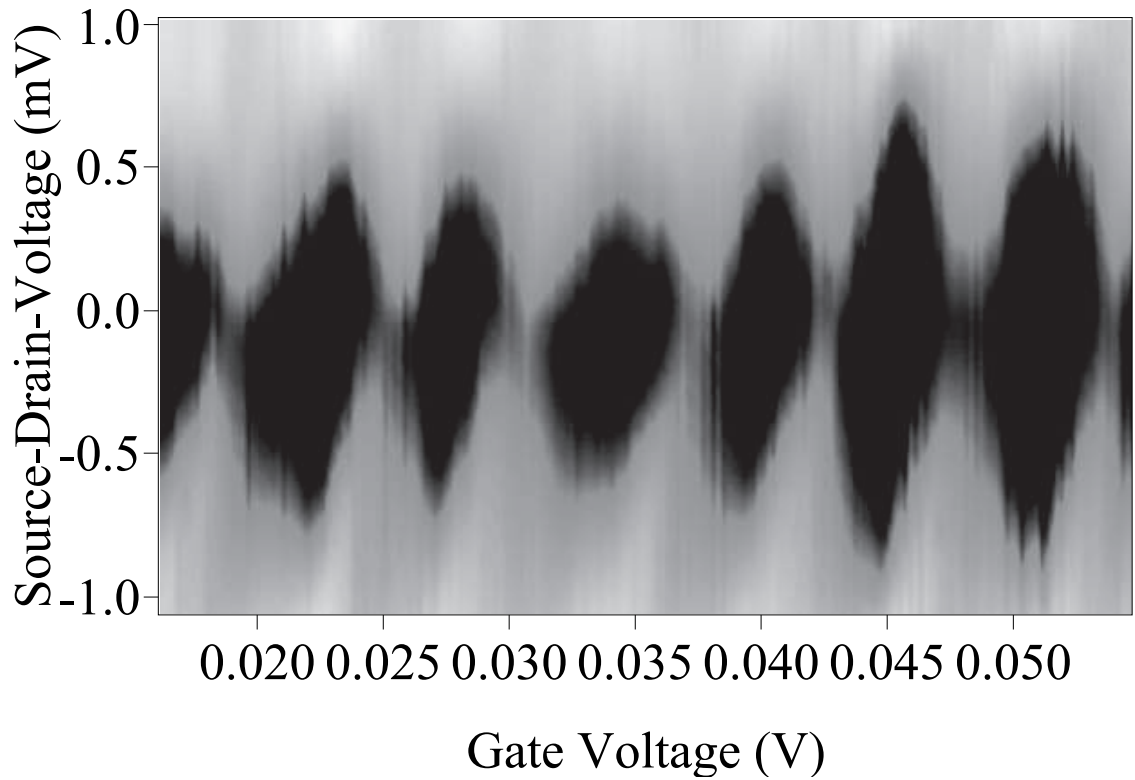
Figure 3.4: Coulomb Oscillations in a nanotube-SET measured at a temperature of 470 mK. The image shows the device conductance as it changes with V_{sd} and V_g. Darker tones indicate lower conductance. (The detailed conductance scale is shown with figure 5.5.)
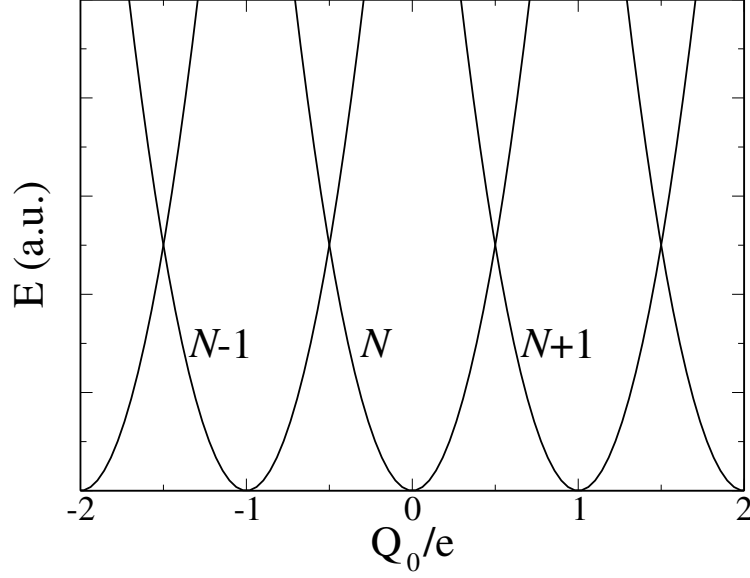
Figure 3.5: Energy of an SET as a function of the gate charge Q_0 on the island for various actual numbers N of electrons. If Q_0 reaches half integer values the energy for adjacent N is equal allowing electrons to tunnel on or off the island. The SET becomes conducting.

If these conditions are met an SET shows variations in conductance $G_{sd} = I_{sd}/V_{sd}$ that are periodic in V_g and a so-called Coulomb gap, i. e. a region in V_{sd} where the device conductance is zero. An example for this behavior is shown in figure 3.4.

To further understand this effect we take a look at the Coulomb energy U of the island. It is given by

$$U(N) = \frac{1}{2}C_s(\varphi(N) - V_{sd})^2 + \frac{1}{2}C_d\varphi^2(N) + \frac{1}{2}C_g(\varphi(N) - V_{sd})^2, \qquad (3.2)$$

where $\varphi = (C_s V_{sd} + C_g V_g - Ne)/C_\Sigma$ is the island's electrostatic potential and N the number of electrons on the island. For clarity we can separate the N-dependent from the V-dependent part of the Coulomb energy:

$$U = \frac{1}{2C_\Sigma}\left[C_g\left(C_s(V_g - V_{sd})^2 + C_d V_g^2\right) + C_s C_d V_{sd}^2 \right] + \frac{N^2 e^2}{2C_\Sigma} \qquad (3.3)$$

Now consider the limit $V_{sd} = 0$. When an electron tunnels onto the island the work done

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by the voltage source supplying V_g is given by

$$W = NeV_g \frac{C_g}{C_\Sigma}. \tag{3.4}$$

After subtracting this from U we obtain

$$E = \frac{1}{2C_\Sigma} \left[C_g(C_s + C_d)V_g^2 - 2NeC_gV_g + (Ne)^2 \right] = \frac{1}{2C_\Sigma} (C_gV_g - Ne)^2 + \text{const.} \tag{3.5}$$

The energy as a function of the number of charges on the island N for a given V_g becomes minimal for $N = C_gV_g/e$. The value $Q_0 = C_gV_g$ is often called "gate charge". Since N must be an integer it will take on the integer value closest to Q_0/e. For $Q_0/e = i + 1/2$, where i is an integer, the energy for two adjacent numbers of electrons is equal. At such a gate voltage electrons can freely tunnel on and off the island making the transistor conducting. Ideally this is repeated for all half integer values of Q_0/e. This periodicity in V_g of points at which the SET becomes conductive allows C_g to be read directly from a plot like the one shown in figure 3.4. The maximum V_{sd} at which Coulomb blockade occurs allows one to determine C_Σ of the island:

$$E_C = e|V_{sd,max}| \Rightarrow C_\Sigma = \frac{e}{2|V_{sd,max}|} \tag{3.6}$$

Starting with this classical approach it is relatively simple to obtain a complete description of simple SET-systems with metallic islands with constant (as a function of applied voltages) capacitances and resistances [85] without any quantum effects.

A quantitative description of such quantum effects is far beyond this work. However, a short introduction into the concepts behind them is useful for a qualitative understanding of some of the results presented later on. Figure 3.6 shows a quantum mechanical
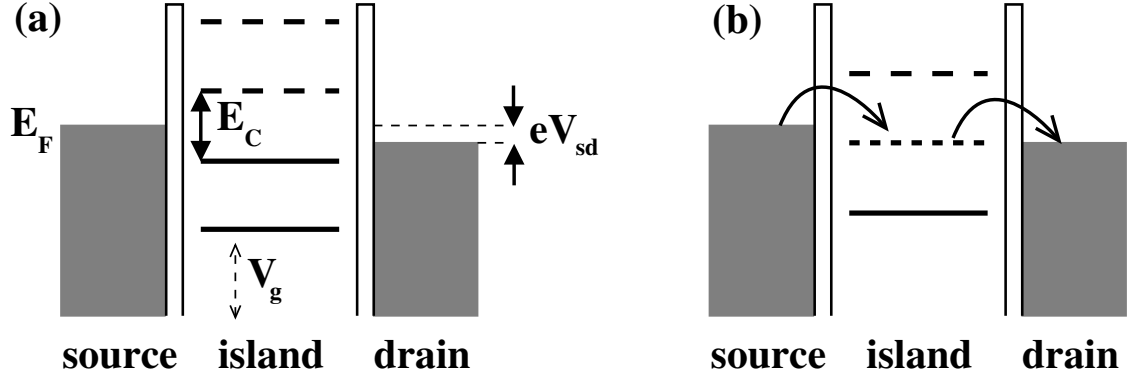
Figure 3.6: Quantum mechanical description of an SET: (a) The states in the metallic source and drain contacts are filled up to the Fermi energy. For the island the energy levels for $(N-1)$, N, $(N+1)$ and $(N+2)$ electrons are shown. An applied V_g shifts these levels relative to the contacts. In this situation none of the states is within the energy interval given by V_{sd} making it impossible for electrons to tunnel onto or off the island. The device does not conduct. (b) By applying a suitable V_g a state on the island is pushed between the Fermi levels of source and drain allowing tunneling. The SET conducts.

description of the same SET-behavior presented above. In this picture there is only one state for each number N of electrons on the SET (or quantum dot). The dot conducts when by applying a gate voltage such a state is lined up with the Fermi levels in the contacts. Figure 3.7 refines this picture by including excited states associated with each of the ground states. In addition to transitions through the ground states transitions through these excited states are possible,too. To be able to observe a transition including two states separated by an energy difference of ΔE the conditions set in equation 3.1 naturally must be met. In addition the following must hold:

$$\Delta E > k_B T$$

$$h\Gamma \ll k_B T. \tag{3.7}$$

Here $\Gamma = 1/t$ is the broadening of the state due to its lifetime t. For further and more
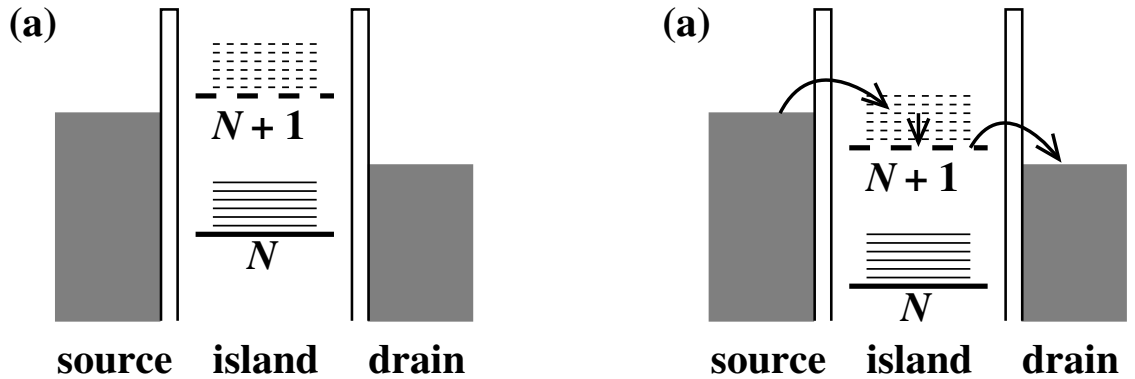
Figure 3.7: States in a quantum dot. This picture now includes various excited states (thin lines) associated with each of the N, $(N+1)$,...-electron states shown already in figure 3.6. (a) Coulomb blockade: Neither the N-electron nor the $(N+1)$-electron ground state is line up with the Fermi levels of the contacts. (b) The quantum dot conducts; an inelastic transition is shown as an example.

detailed descriptions of these quantum mechanical effects see [86].

3.3 Room Temperature Devices: Field-Effect Transistors

Field-effect transistors (FETs) have the same basic structure as the one indicated in figure 3.1. In conventional FETs the channel is not a nanotube, but a region of the substrate that can be turned conductive through field doping by a voltage applied to the gate. (For a review of traditional FET-devices see e. g. [87, 88, 89, 90].) Applications of FETs include amplifiers and logical elements in digital electronics. Switching speed and size of FETs are closely related to the achievable gate capacitance. It is expected that in the near future silicon-based devices will no longer be able to fulfill technological requirements. Carbon-nanotube FETs in which the channel is a semiconducting nanotube are promising candidates for replacing Si-based FETs.

3.3.1 Intrinsic Conductance of Nanotubes

The behavior of carbon nanotube FETs is determined by two intrinsic factors. The first is the conductance and electronic structure of the nanotube itself. The second factor is the behavior of the contact between the nanotube and the metallic source and drain electrodes. The latter will be treated in section 3.3.2.

The simplest model for describing transport properties of a material is the Drude model [91]. In its framework the conductivity σ is given by $\sigma = j/E = ne^2\tau/m$, where j is the current density, E the electric field along the material, n the carrier density in the material and τ the momentum scattering rate. The mass m of the carriers is their effective mass. For a 1D conductor like a carbon nanotube these formulae translate to $\sigma = G \cdot L$ with G being the device conductance and L the device length. The carrier density can be calculated from the number of carriers ν and the device length $n = \nu/L$. The quantity $\mu = e\tau/m = \sigma/(ne)$ is called mobility and is one of the most important parameters measuring how well a material conducts (for details see section 6.1 on page 68).

As derived in [92] the intrinsic conductance of a ballistic 1D conductor is the quantum of conductance $G_0 = e^2/h = 38.7\,\mu\text{S}$ for each mode of conductance. An SWNT has two bands and two spins per band. Therefore the maximum conductance of a single SWNT is $G_{\text{max}} = 4G_0 = 155\,\mu\text{S}$ which is equivalent to a resistance of $6.45\,\text{k}\Omega$. For a real ballistic conductor the conductance is given by $G = (G_{\text{max}}{}^{-1} + G_{\text{wire}}{}^{-1})^{-1}$, where $G_{\text{wire}} = G_{\text{max}}T/(1-T)$ and T is the transmission probability of the conductor [92]. The transmission probability can be lowered by scattering in the conductor itself (see section 6.1) and by contact resistances. The length of a conductor after which T drops to one

half resulting $G_{\mathrm{max}} = G_{\mathrm{wire}}$ is called the mean free path l. Using this definition we can use the conductance of a nanotube—provided we can distinguish it from contact effects—to calculate the mean free path:

$$l = L\frac{G_{\mathrm{wire}}}{G_{\mathrm{max}}} = L\frac{G_{\mathrm{wire}}}{155\,\mu\mathrm{S}} \tag{3.8}$$

Theoretical predictions for l in metallic nanotubes [93] ($10\,\mu\mathrm{m}$) are in good agreement with measurements by Kong et al. [94] measuring $l = 5\,\mu\mathrm{m}$. Because of high contact resistances there are few reliable measurements of l for semiconducting nanotubes. However, publications presenting results on semiconducting nanotubes with low contact resistances [72, 65] find mean free paths of at least several hundred nm in agreement with electrostatic force microscopy (EFM) studies [62].

3.3.2 The Nanotube-Metal Contact

For metallic nanotubes near-perfect transmission has been demonstrated in 2001 [95]. Until recently the lowest resistance measured in semiconducting nanotube devices was about $100\,\mathrm{k}\Omega$ with $1\,\mathrm{M}\Omega$ being more typical. This seemed to suggest the presence of some kind of intrinsic barrier either in the nanotube itself [96] or at the contacts.

Several experiments suggested these barriers to be Schottky barriers. Scanned-gate microscopy (SGM) images of semiconducting nanotubes contacted with Cr/Au-contacts [97][1] found that semiconducting nanotubes in FET-geometries react more strongly to a local gate near the contacts than in the middle of the device. Theoretical simulations of

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[1]In SGM a voltage is applied to an atomic force microscopy (AFM) tip allowing the tip to act as a local gate. The image then contains of the device response to this local gate.

the behavior of a Schottky barrier transistor [98, 99] agreed very well with experimental results on Cr/Au-contacted nanotubes on local Al/Al_2O_3-gates [77]. Experiments on Ti/Au-contacted nanotubes [100] supported the idea of barriers at the contacts. Gathering all this information Heinze et al. [76] presented a theory of the behavior of Schottky barrier NT-FETs which was corroborated by experiments on Ti/Au-contacted nanotubes presented by Appenzeller et al. [71]. An important property of a Schottky barrier transistor is the temperature dependence of the so-called subthreshold swing S, which is defined as the inverse logarithmic slope of the $G(V_g)$-curve: $S = (d\log G/dV_g)^{-1}$ [mV/decade] [87]. In a conventional MOSFET S is proportional to the temperature $S \approx 2.3k_BT/e$. In a Schottky barrier FET S should be T-independent possibly with a minor correction due to thermally assisted tunneling [101]. Indeed, this is what was found in [71].

Although the Schottky barrier model seemed conclusive, the question remained whether these Schottky barriers were intrinsic to nanotubes or caused by the choice of contact materials and treatment. Both materials Cr and Ti have work functions lower than CNTs (4.5 eV [31]). In principle the work function difference between the contacts and the nanotube should determine the characteristics of the contacts [98] since in 1D systems dipoles at the NT/contact interface cannot be screened completely [102]. Therefore a contact material with a high work function (e. g. Au, Pd, Pt) should allow for Ohmic contacts. However, Au and Pt both do not wet nanotubes such that devices with these types of contacts usually show large contact resistances. Few exceptions to this behavior have been found: Yaish et al. [103] (pure gold contacts) and Dürkop et al. [66]—although the contacts used a Cr-adhesion layer the material contacting the tubes was probably gold (see

chapter 6)—observed Ohmic contacts in nanotube FETs. On the other hand Pd has been known to wet nanotubes [75] and its work function (5.1 eV) is greater than $4.5\,\text{eV} + E_g/2$. Javey et al. have managed to reliably fabricate NT-FETs with Ohmic contacts and high device conductances (up to $0.5G_{\text{max}}$). The quality of Pd contacts is also confirmed by low temperature measurements that do not show the signature of Coulomb blockade (section 3.2), but Fabry-Perot interference as previously reported for metallic nanotube devices with high device conductance [95]. Further experiments [65] show that exposure to H_2, which is known to lower the work function of Pd [104], change the behavior of Pd-contacted NT-FETs in a way expected for the creation of a Schottky barrier.

Chapter 4

Experimental Techniques

4.1   Nanotube Growth

The carbon nanotubes for all the samples investigated in this work have been produced using CVD-techniques derived from the general methods mentioned in section 2.3.2. The furnace used is a Lindberg/Blue HTF55122A tube furnace with a 1" quartz glass tube. The maximum temperature for this furnace is 1200°C. It is controlled by an Omega CN4431 PID-temperature controller. Separate flow meters allow to control the flow of up to four different gases through the oven individually [105]. The substrate used for all samples is highly doped Si capped with 500 nm of thermally grown SiO_2. The doping level of the substrate is sufficient for the substrates to stay conducting even at temperatures below 300 mK.
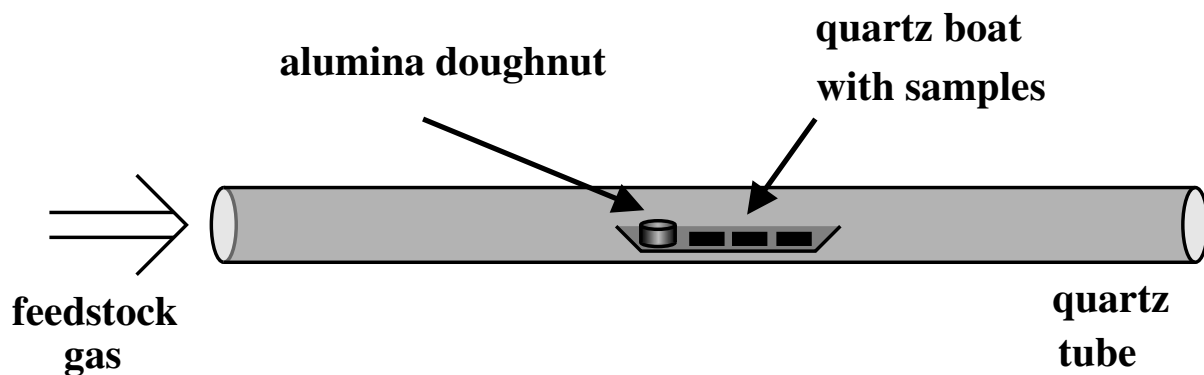
Figure 4.1: Placement of the samples and the alumina "doughnut" during nanotube growth.

4.1.1 The "Doughnut" method

The initial method used for nanotube growth used ferric nitrate ($Fe(NO_3)_3$) [54] as catalyst on the samples and an additional mixture of $Fe(NO_3)_3$ and $MoO_2(acac)_2$ [53] (for simplicity we dubbed this mixture "Dai-catalyst" after Hongjie Dai, whose research group conducted a lot of the pioneering work on CVD-grown carbon nanotubes) dripped onto a doughnut-shaped piece of porous alumina. Figure 4.1 shows the placement of the "doughnut" and the sample relative to each other in the furnace. The two catalyst solutions are prepared in the following way:

$Fe(NO_3)_3$:

   Mix anhydrous $Fe(NO_3)_3$ and 2-propanol at a concentration of $150\,\mu g/ml$ and stir for at least 1 h.

Dai-catalyst:

   Mix the following ingredients:

   1. $Fe(NO_3)_3$: 21.6 mg

2. Al_2O_3 (Degussa, average particle size 14 nm): 14.6 mg

3. $MoO_2(acac)_2$: 4.8 mg

4. Methanol: 15 ml

and stir for approximately 24 h.

After preparing the catalyst solutions the actual nanotube growth follows this procedure:

- Dice samples to approximately $1\,cm \times 0.5\,cm$.

- Blow off dust from dicing.

- Dip samples into $Fe(NO_3)_3$-solution for 5–10 seconds.

- Dip samples into hexane for 5–10 seconds.

- Blow off hexane.

- Place samples and alumina "doughnut" on quartz boat.

- Drip *one* drop of Dai-catalyst onto "doughnut".

- Place boat in furnace such that the "doughnut" is upstream of the samples.

- Flush air out of furnace[1] by flowing argon for 20 min, flow rate: 729 sccm[2].

- Heat furnace to 900°C while flowing H_2 at 531 sccm and Ar at 583.

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[1] It is equally important to flush air out of the lines carrying flammable gases before starting to heat the furnace although not mentioned in this or the recipes in the following sections.

[2] The unit "sccm" is cm^3/min at atmospheric pressure. For details see [106].

- Soak at 900°C for 3 min with unchanged flow rates.

- Flow CH_4 at 900°C with flow rate 2920 sccm for 6 min.

- Flow CH_4 at 900°C with flow rate 1042 sccm for 20 min.

- Flow Ar with 729 sccm; turn off heat.

- Go to lunch while furnace cools down (optional).

The results of this growth procedure are not very uniform: The nanotubes produced vary in diameter from below 1 nm to 20 nm, although the majority of tubes has a diameter of below 3 nm. In addition the density of nanotubes on the chip seems to depend sensitively to the amount of Dai-catalyst in the "doughnut" and the horizontal distance between the sample and the "doughnut" during growth. However, unlike the method described in section 4.1.4 the "doughnut" method mostly produces high-quality nanotubes with well-defined electronic properties.

Figure 4.2 shows an SEM-image (for a detailed analysis of the contrast mechanism of imaging nanotubes with an SEM see [107]) of nanotubes grown with the "doughnut" method. While the nanotube density on this particular sample is too high for device fabrication the image shows some features typical for the "doughnut" method. Comparison with the scale bar included in the image shows that the nanotube length is between a few μm and several ten μm. Many nanotubes show a hook-shaped bend at one end.
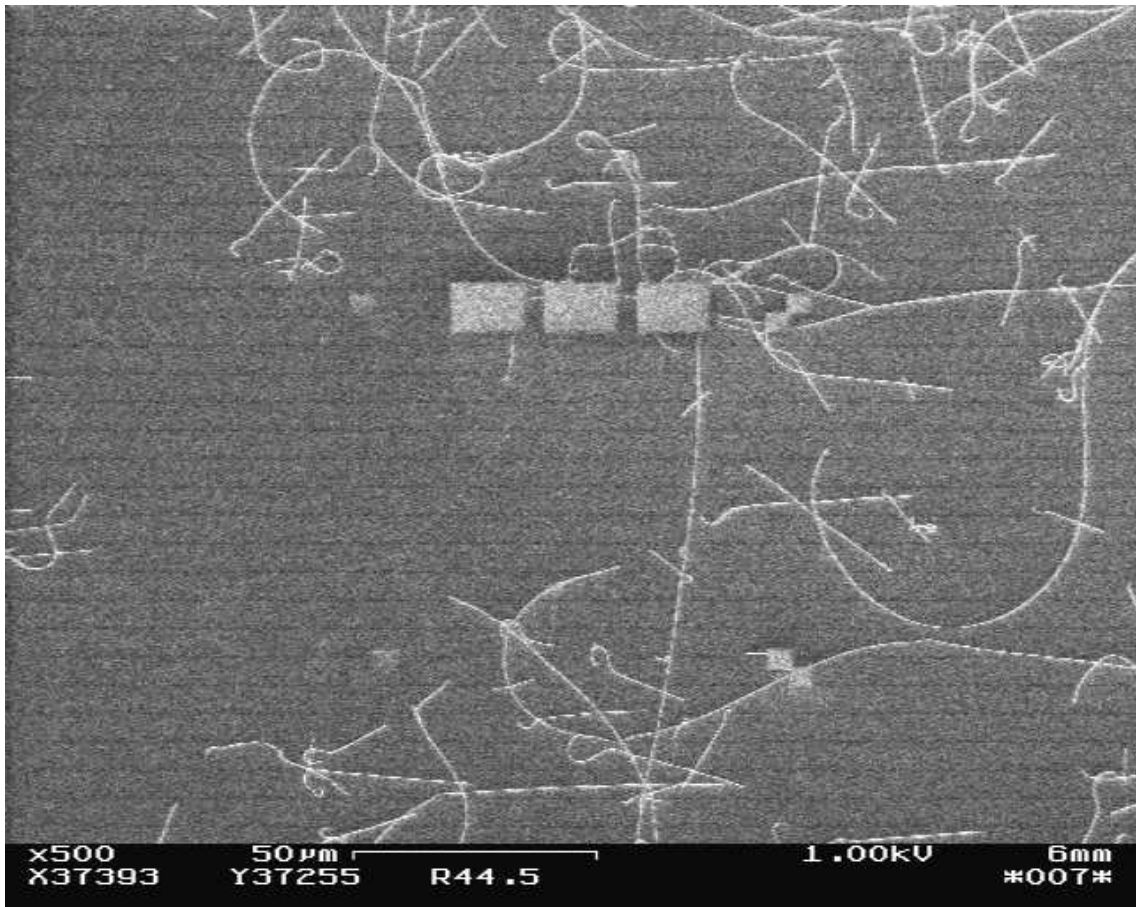
Figure 4.2: Scanning electron microscope (SEM) image of nanotubes grown with the "doughnut" method. On this particular sample the nanotube density is too high for device fabrication. The square and rectangular shaped objects are part of the alignment mark pattern explained in section 4.2.

4.1.2 Patterned Catalyst

This method of nanotube growth closely follows the method outlined by Kong et al. [53]. It uses the Dai-catalyst described in section 4.1.1 deposited directly onto the sample in patterns defined by electron-beam lithography.

The fabrication of patterned catalyst islands on the sample is carried out using the following procedure:

- Spin PMMA onto clean sample for 45 s at 6000 rpm.

- Bake sample for 5 min at 150°C.

- Carry out e-beam lithography.

- Develop samples in MIBK/IPA (1:3) solution for 70 s.

- Drip *one* drop of Dai-catalyst (see section 4.1.1) onto sample.

- Allow sample to dry in air ($\sim$ 3 min).

- Bake sample on hotplate for 5 min at 160°C.

- Immerse the sample in dichloroethane (DCE) for 45 min to lift off unwanted catalyst.

- While still immersed in DCE sonicate sample for 1 s.

- Rinse sample in Acetone, Methanol, IPA and blow dry sample.

- Place sample in quartz boat in furnace.

- Flow Ar for 20 min at 729 sccm.

- Heat furnace to 900°C while flowing Ar at 729 sccm.

- Wait 3 min at 900°C with unchanged flow.

- Flow CH_4 at 1900 sccm and H_2 at 480 sccm for 11 min.

- Flow Ar at 729 sccm during cooldown.

After experiments with several different designs for catalyst patterns [108] we found that catalyst islands with a size of $2\,\mu m \times 2\,\mu m$ produce on average one nanotube under the above growth conditions. A suitable design for catalyst patterns consist of many of these $2\,\mu m \times 2\,\mu m$ islands with a spacing of 20–30 μm between them. Although the main purpose of this growth method is to speed up device production and make it suitable for mass production of nanotube devices we found that in the framework of the production techniques we used, i. e. devices produced individually using e-beam lithography, this method of nanotube growth does not simplify device fabrication. The accuracy of positioning of the nanotubes as they grow from the catalysts island is not sufficient to skip the very time consuming step of locating individual nanotubes. Furthermore the SEM-contrast between catalyst islands and the surrounding substrate is too small to use them for alignment in subsequent processing steps requiring the fabrication of additional alignment marks after completing the nanotube growth (see also section 4.2). However, the ability to produce a predetermined density of nanotubes is a clear advantage this method has over the "doughnut" method.

An example for nanotubes grown using this method is given in figure 4.3. The image
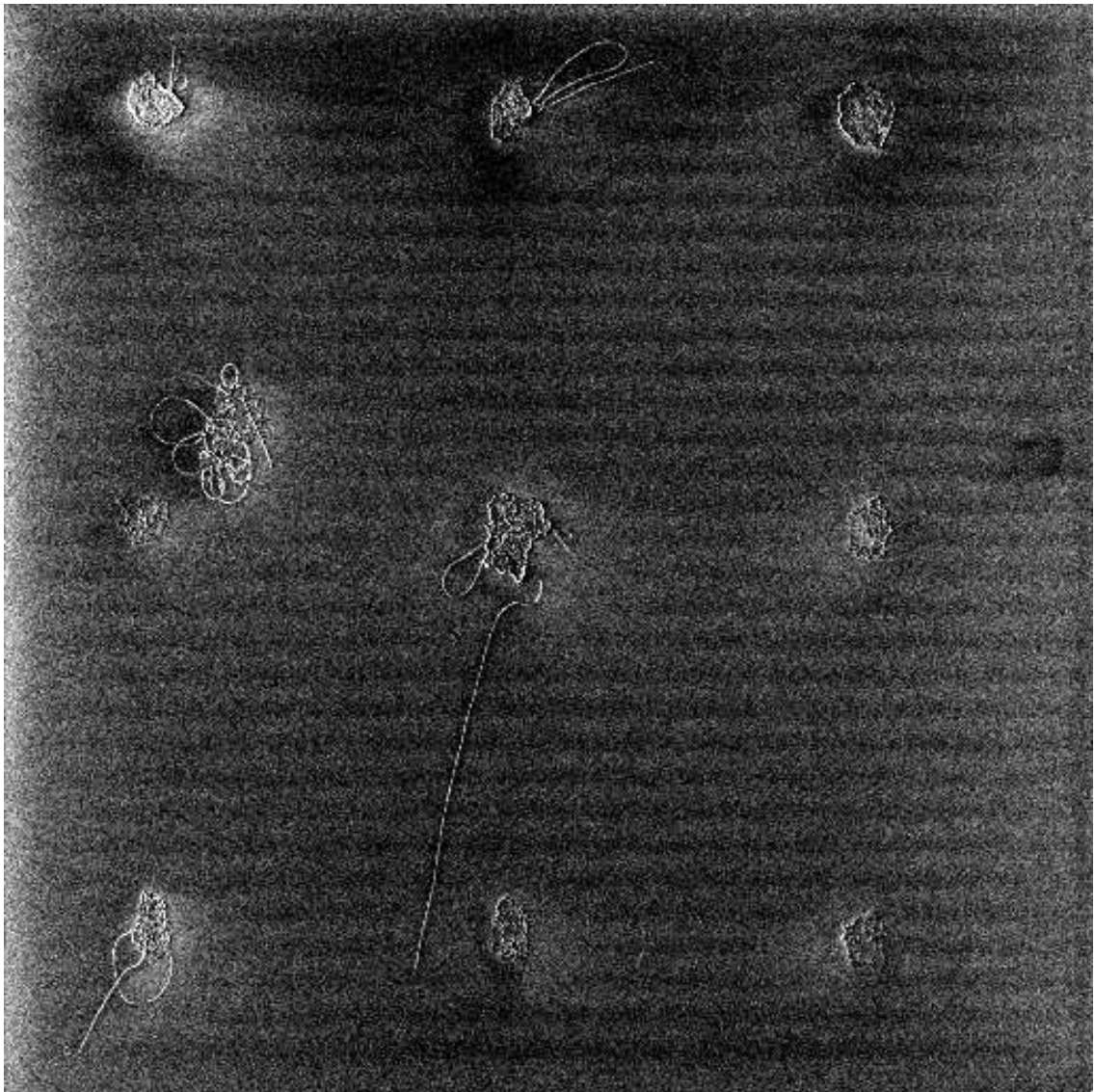
Figure 4.3: Scanning electron microscope (SEM) image of nanotubes grown from patterned catalyst islands. The island size is $2\,\mu m \times 2\,\mu m$ and the spacing between islands is $30\,\mu m$.

shows several catalyst islands most of which have produced at least one nanotube. Some of these nanotubes are up to 30 μm long and straight making them ideal for the fabrication of NT-FETs with channel length greater the mean-free path (see section 3.3.1).

4.1.3 Ultralong Nanotubes

The aim of this method of nanotube growth is to produce nanotubes with lengths over 100 μm in order to fabricate devices that allow to distinguish between contact effects and intrinsic nanotube properties. The catalyst used for the growth is the ferric nitrate catalyst used for the "doughnut" method while the gas mixture during growth is adapted from [56]. The recipe for the nanotube growth is as follows:

- Mix $Fe(NO_3)_3$-catalyst solution (see section 4.1.1) with a concentration of 30 μg/ml.

- Dip samples into $Fe(NO_3)_3$-solution for 5–10 seconds.

- Dip samples into hexane for 5–10 seconds.

- Blow off hexane.

- Place sample in quartz boat in furnace.

- Purge quartz tube by flowing Ar for 20 min at 729 sccm.

- Heat furnace to 900°C with unchanged Ar-flow.

- Soak at 900°C (Ar: 729 sccm).

- Grow tubes at 900°C for 15 min with the following flow rates:
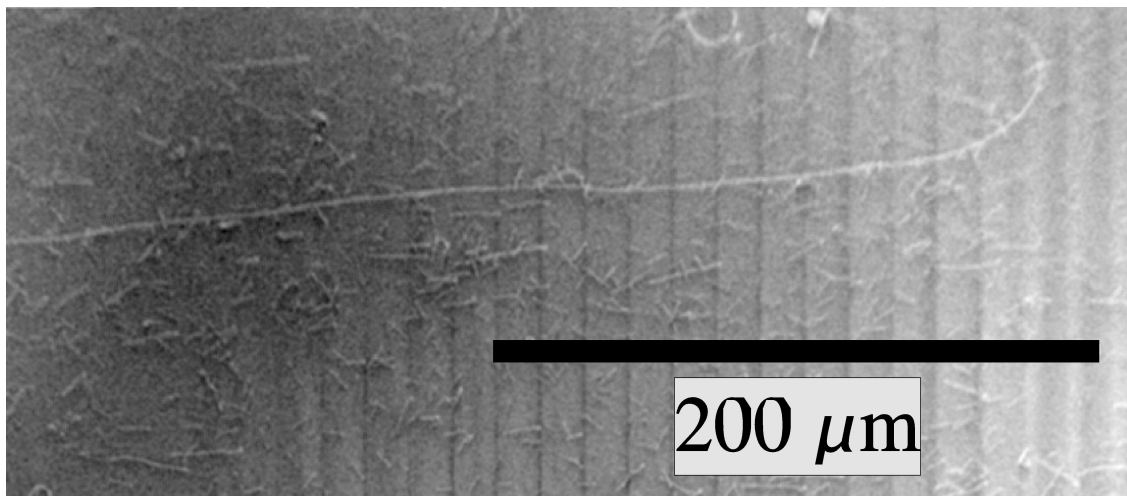
Figure 4.4: Scanning electron microscope (SEM) image of nanotubes grown with the H_2/CH_4/C_2H_4 gas mixture. One long nanotube is shown in front of a background of short tubes.

H$_2$: 500 sccm.

CH$_4$: 1200 sccm.

C$_2$H$_4$: 26 sccm.

- Cool down while flowing Ar at 729 sccm.

A sample processed in this way typically exhibits an electrically not continuous coverage of nanotubes of lengths below $10\,\mu$m with a density of 30 tubes per $100\,\mu$m $\times\,100\,\mu$m area. In addition there are about 5–10 tubes of lengths above $100\,\mu$m per mm^2. These long nanotubes are usually aligned in the direction of the gas flow during growth, an effect which has also been described in [109].

4.1.4 Thin Nanotubes

The technique of nanotube fabrication described below could not be used to provide nanotubes for device fabrication. Transistors fabricated from nanotubes that were produced with this method always showed electric properties that could not be interpreted with the models presented in section 3.

We found that the nanotubes produced using the "doughnut" method or the method for ultralong tubes would often have diameters above 2 nm. Nanotubeswith diameters above 1.5 nm can already be double- or multi-walled and our aim was to find a technique that reliably produces nanotubes with diameters too small for MWNTs. This technique is derived from the recipe for ultralong tubes, but leaves out C_2H_4 during growth and uses a slightly different method for catalyst preparation.

The detailed recipe is as follows:

- Mix $Fe(NO_3)_3$ and 2-propanol to get a concentration of 10 µg/ml.

- Stir solution for 2 h.

- Sonicate solution for 10 min.

- Dip clean samples into catalyst solution for 10 s.

- Dip samples into hexane for 10 s.

- Dry samples by blowing with N_2-gas.

- Place samples in boat in furnace.

- Purge furnace with Ar for 20 min, flow 729 sccm.

- Heat furnace to 900°C while flowing Ar at 729 sccm and H_2 at 963 sccm.

- Soak 10 min at 900°C with unchanged gas flow.

- Grow nanotubes at 900°C flowing 963 sccm of H_2 and 3135 sccm of CH_4.

- Cool down flowing Ar at 729 sccm.

A catalyst concentration of 10 μg/ml produces a density of nanotubes that would be suitable for device fabrication. A higher concentration of 50 μg/ml results in the nanotube density shown in figure 4.5. In comparison with nanotubes grown with the techniques described in the previous sections (see especially figures 4.2 and 4.3) this growth method produces nanotubes that appear "wiggly". This suggests that the tubes are less stiff than tubes grown with different techniques, i. e. their diameter is smaller. Measurements using AFM indeed confirm that the overwhelming majority of nanotubes grown with this technique have diameters of below 1 nm. Unfortunately—as demonstrated in figure 4.6—the electronic properties of this kind of tube are hard to understand. The tubes neither behave in a way expected for semiconducting tubes nor for metallic tubes nor, as can be seen for some thicker nanotubes, as if they consisted of a semiconducting tube and a metallic tube in parallel. Their behavior somewhat resembles that of small-bandgap semiconducting nanotubes ("metallic" tubes that are not armchair tubes) under applied strain [110]. While it is conceivable that a very thin nanotube grown directly on a substrate might experience strain due to interaction with the surface, it is not clear why none of the devices would exhibit clear metallic or semiconducting behavior. For this reason we abandoned this method of nanotube fabrication in favor of the techniques described in the previous
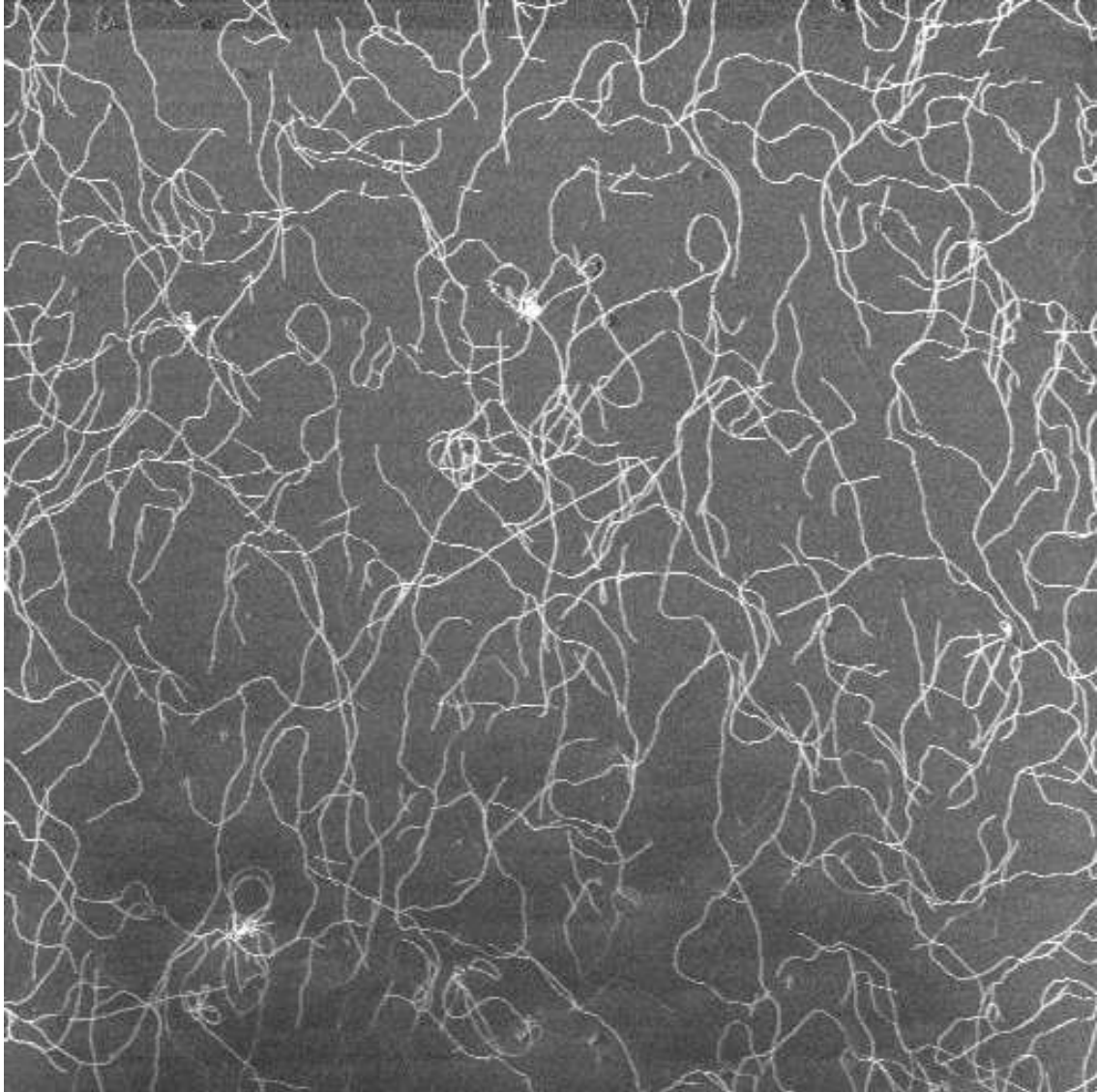
Figure 4.5: Scanning electron microscope (SEM) image of nanotubes grown with a catalyst concentration of $50\,\mu\text{g/ml}$ using the mixture for thin nanotubes. The size of the image is approximately $120\,\mu\text{m} \times 120\,\mu\text{m}$. It could not be recorded exactly due to a malfunction of the microscope.
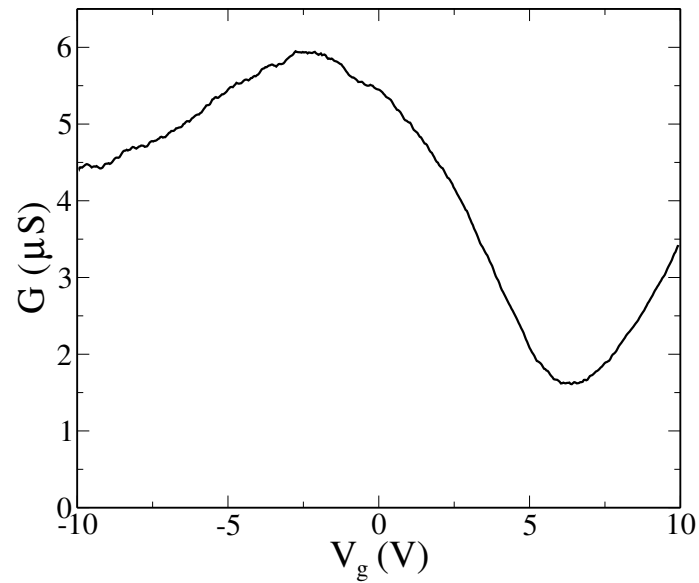
Figure 4.6: Conductance as a function of applied gate voltage for a typical device fabricated from a nanotube fabricated with the technique for thin tubes measured with a bias voltage of $V_{sd} = 10\,\mathrm{mV}$. Clearly the device does not turn off for any gate voltage as expected from a semiconducting nanotube. Unlike for metallic nanotubes, however, the conductance modulates strongly with V_g.

sections.

4.2   Device Fabrication

The first step in manufacturing nanotube devices is to find the location of individual na-

notubes in a reproducible manner. The procedure described here is derived from tech-

niques first used by Bockrath et al. [30] to fabricate nanotube devices. The first step is to

lithographically define alignment marks. Nanotubes can then be located relative to these

marks. To fabricate these marks the samples are first coated with electron-beam resist

following this recipe or slight variations thereof:

- Spin on MMA (Methyl Methacrylate) at 4000 rpm for 45 s.

- Bake sample on hotplate at 150°C for 10 min.

- Spin on PMMA at 6000 rpm for 45 s.

- Bake sample on hotplate at 150°C for 10 min.

The next step is to write the actual pattern. For this we initially used a JEOL 5400 SEM

and later a Philips XL 30 SEM both equipped with an NPGS e-beam writing system by

J. C. Nabity. An example for such an alignment mark pattern is given in figure 4.7. This

pattern was originally designed by T. Brintlinger and is optimized for nanotubes with

lengths below 10 μm. After writing several of these pattern onto a sample the sample is

developed in solution of MIBK in IPA (1:3) for 70 s to dissolve the areas of resist that had

been exposed to the e-beam, thus creating a positive mask.
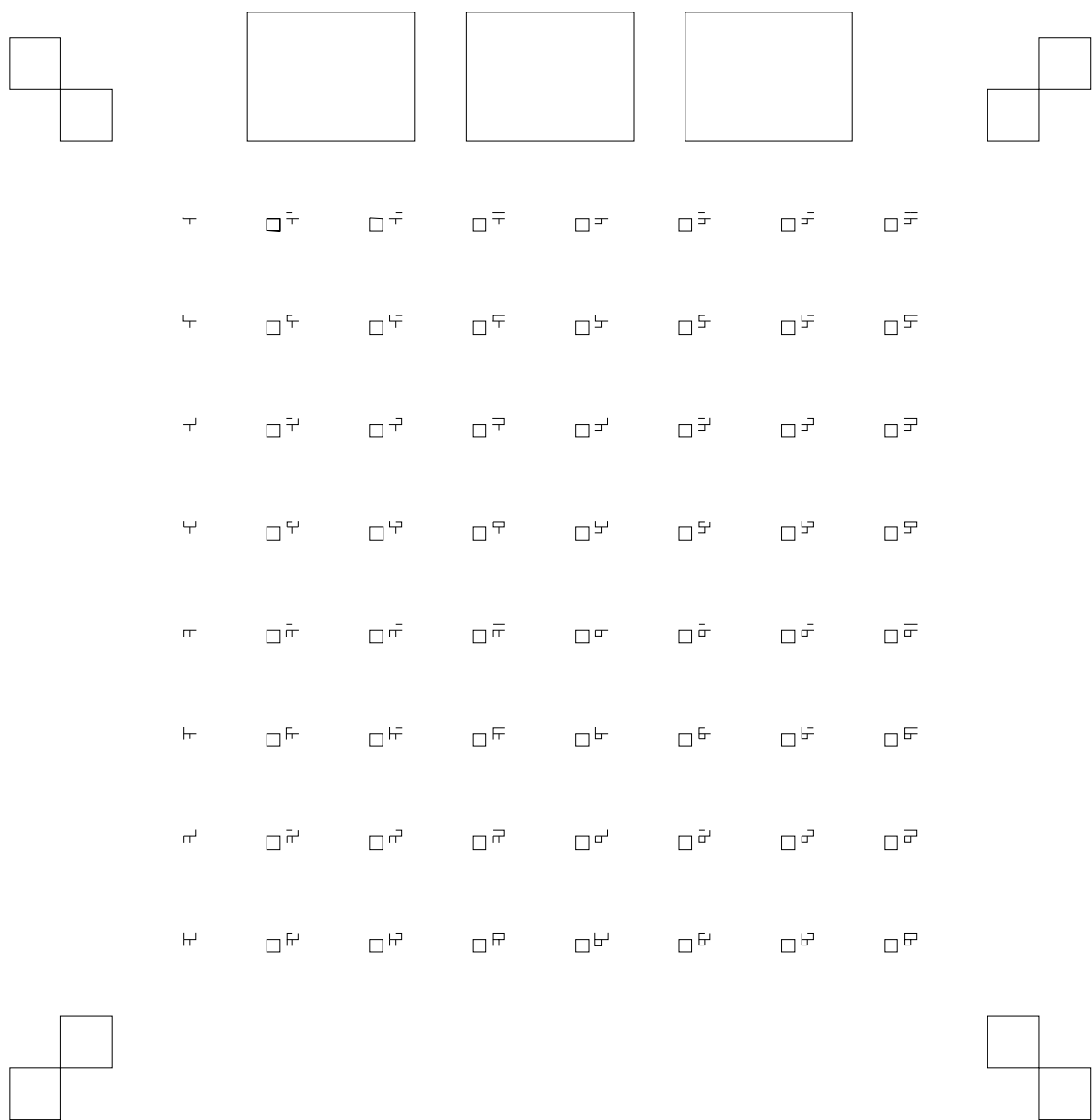
Figure 4.7: Alignment mark pattern. The total size of the pattern shown is $90\,\mu m \times 90\,\mu m$. The group of three large rectangles makes the whole pattern easier to find in subsequent processing steps, the groups of two squares in each of the corners of the pattern allow to align later lithography steps to the pattern with submicron accuracy and the small $(1\,\mu m \times 1\,\mu m)$ squares allow the e-beam to steady itself before writing the small symbols that mark locations throughout the pattern. These small squares are only necessary for the JEOL 5400 SEM, which is not equipped with the beam blanker needed to turn on or off the e-beam quickly.

(a)

(b)

(c)

(d)

(e)

(f)
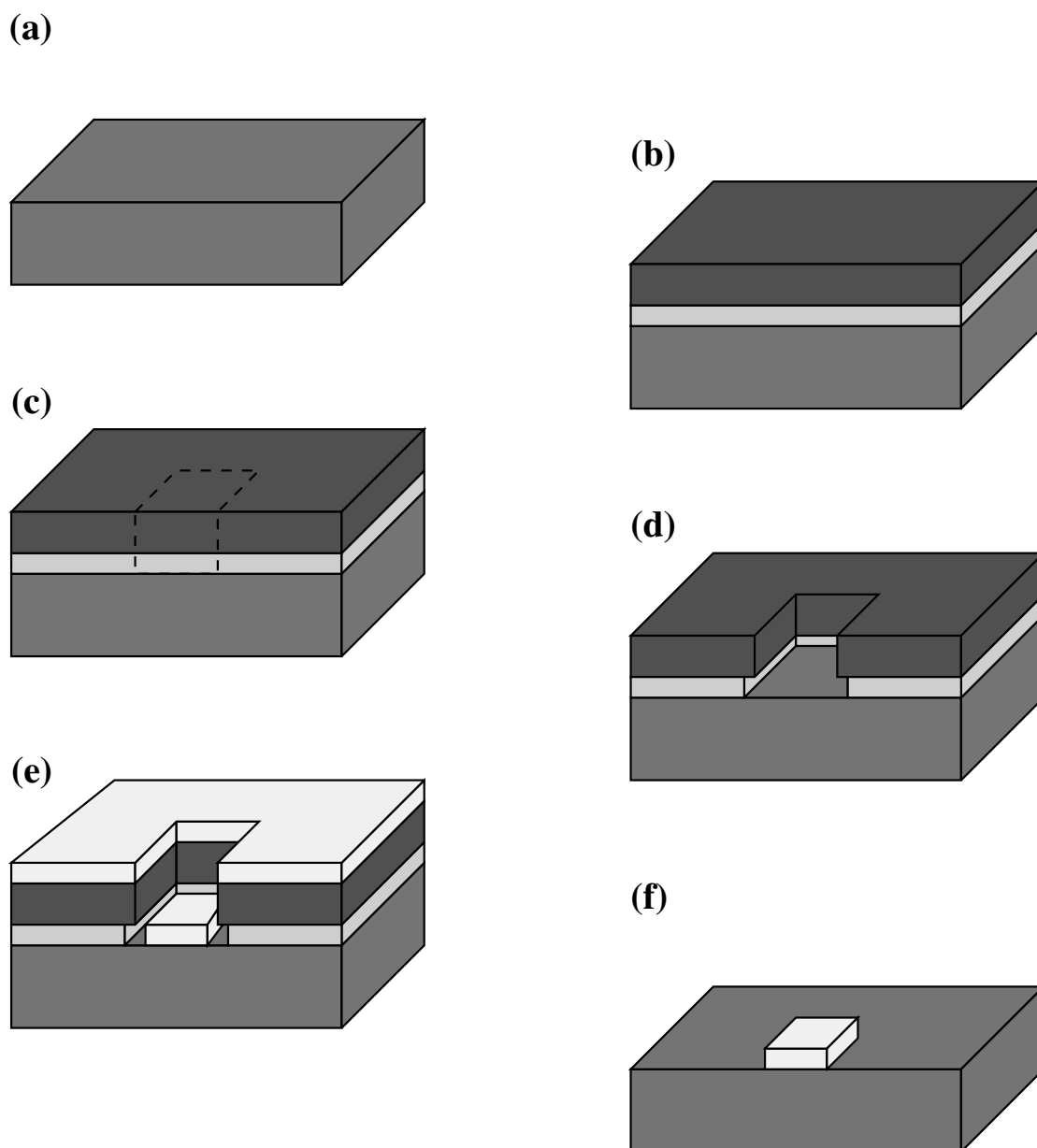
Figure 4.8: Electron beam lithography: (a) Clean sample. (b) Sample with e-beam resist PMMA (dark grey) and copolymer MMA (light grey). (c) Sample after e-beam writing. (d) Developing the sample removes exposed resist. (e) After metal deposition. (f) After liftoff: metal is left only where the resist was exposed.

After this step metal is deposited onto the samples, first a thin (2.5 nm) adhesion layer of Cr followed by 17.5 nm of Au. The remaining resist is dissolved by immersing the sample into acetone for at least 30 min (liftoff). Spraying the sample with more acetone and then rinsing it with methanol and IPA, and drying it with N_2-gas removes the remaining gold except for the portions in the alignment marks. For this procedure to function the first layer of resist (MMA) is vital. It partially dissolves during developing of the sample leaving an undercut around the marks written by e-beam. This undercut prevents the formation of a continuous metal layer during Au-deposition, which otherwise would cause the excess metal to stick to the sample after liftoff. This whole process is illustrated in figure 4.8.

After thus creating the alignment mark pattern as metal islands on the sample it is possible to find positions of nanotubes relative to these alignment marks. We have used two different techniques for this purpose. The first technique uses an AFM. Its advantage is that it immediately provides information about the diameter of a nanotube allowing to be selective about the nanotubes being contacted. Furthermore AFM can be used on conducting and nonconducting surfaces. Figure 4.9 shows a nanotube and some alignment mark.

The disadvantages of this technique for finding nanotubes is its sensitivity to surface roughness. Already the alignment marks, especially if their height is increased due to bad liftoff, make it necessary to perform several image processing steps on the AFM image before it is possible to see nanotubes. Another disadvantage is the time required for taking AFM images. For example a $20\,\mu\text{m} \times 20\,\mu\text{m}$ image takes 15 min, searching a

51
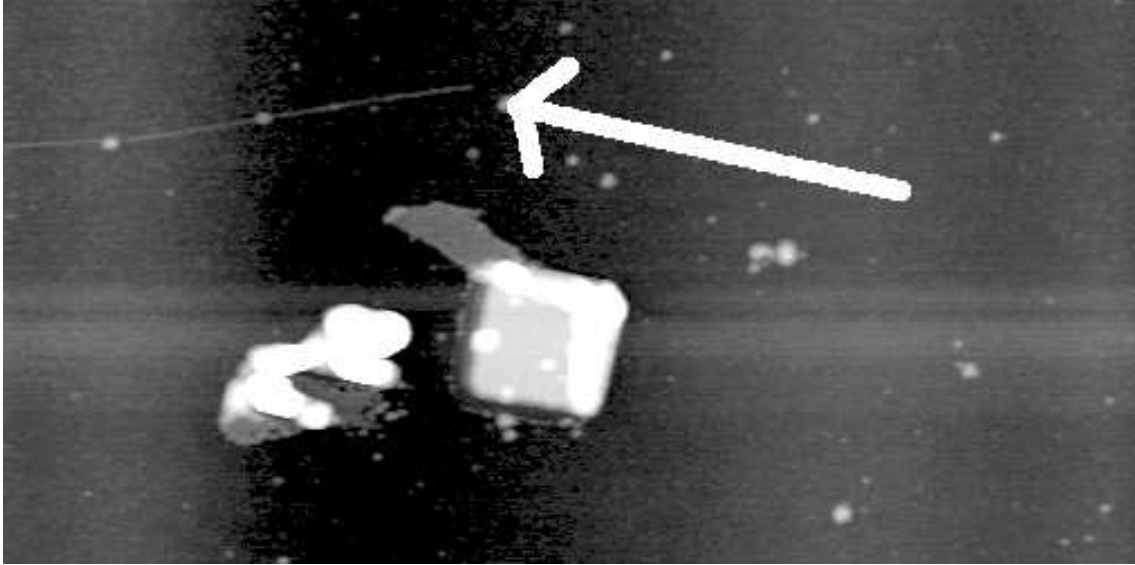
Figure 4.9: AFM-image of a nanotube next to an alignment mark. The white arrow points towards the end of the nanotube. Clearly the comparatively big height of the alignment mark affects the visibility of the surrounding area.

complete pattern like in figure 4.7 can take up to a whole day. Using a field-emission SEM (FESEM) at a low acceleration voltage of 1 kV allows to observe nanotubes due to their difference in conductivity relative to the underlying SiO_2 [107]. With this technique it is possible to search one alignment mark pattern within less than one hour. A disadvantages of this technique is that it is impossible to get direct informations about the diameter of nanotubes since the contrast mechanism that makes nanotubes visible at the same time makes them appear some 100 nm thick. Furthermore, the electron beam of any SEM deposits amorphous carbon on the surface it is scanning. Although in an FESEM the electron source is in ultra-high vacuum, which somewhat lessens the problem, it is still inadvisable to have the beam scan over small areas repeatedly.

After determining the locations of the nanotubes the next step is to manufacture contacts to individual tubes. The technique used here is the same e-beam lithography tech-
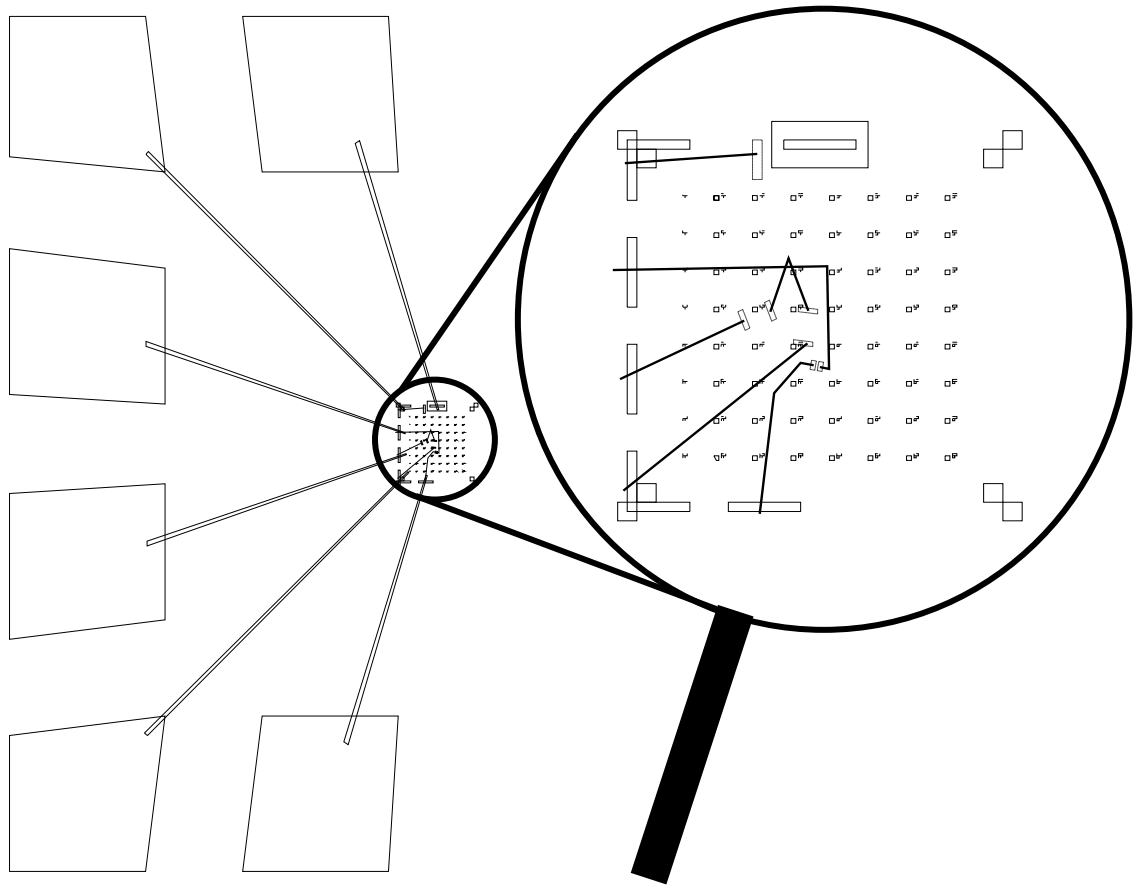
Figure 4.10: Contact design for nanotube devices. The left side shows the large pads used for contacting the sample from the outside, each of which is roughly $150\,\mu\text{m} \times 150\,\mu\text{m}$ in size and the connection to the center area. These bonding pads and the connecting lines are written with the SEM set to a magnification of $100\times$. The right side shows a magnified view of the center area around the alignment mark pattern showing the actual connections to the nanotubes. For this part of the contacts a magnification of $1000\times$ is used during writing.
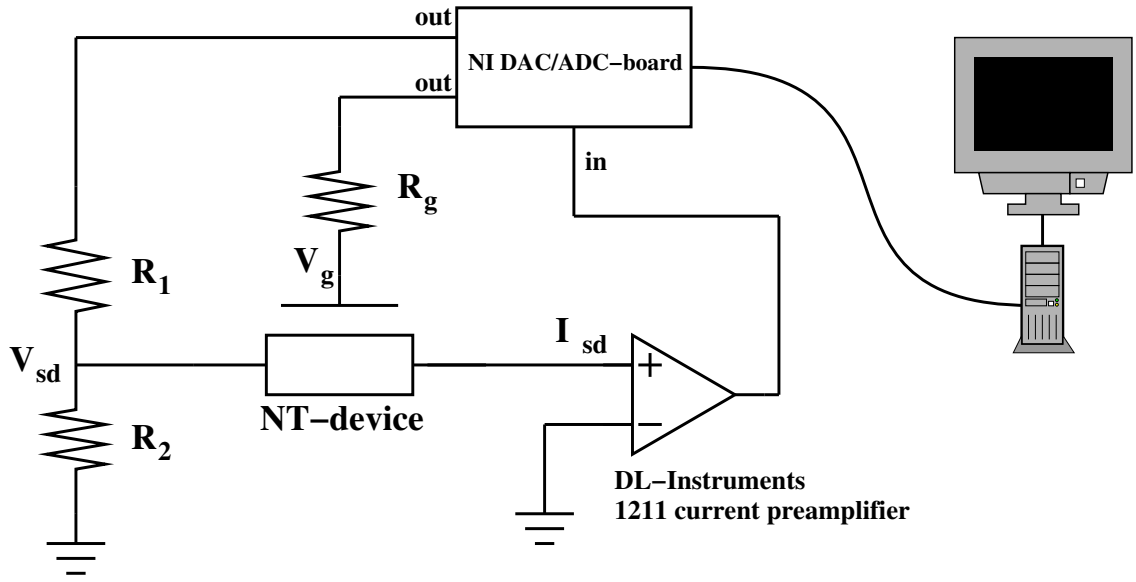
Figure 4.11: DC-measurement of the electronic properties of a nanotube. Typical values for the resistances are $R_1 = 100\,\text{k}\Omega$, $R_2 = 1\,\text{k}\Omega$ and $R_g = 1\,\text{M}\Omega$ making R_1 and R_2 work as a 100:1 voltage divider, while R_g serves to protect the nanotube device from spikes in V_g.

nique used for creating the alignment mark patterns. Figure 4.10 shows an example of a contact design. The metal used for the fabrication of the contacts is 100–150 nm thick gold on an adhesion layer of 2.5 nm of Cr. Examples for such a devices can be seen on page 58 in figure 5.1.

4.3   Electrical Measurements

With the nanotube devices fabricated in the way described above we performed several types of electrical measurements. The simplest form employs a DC measurement scheme as shown in figure 4.11. While R_1 and R_2 form a voltage divider to divide the up to 10 V from the DAC-board, R_g is supposed to protect the devices from spikes in V_g or in case of
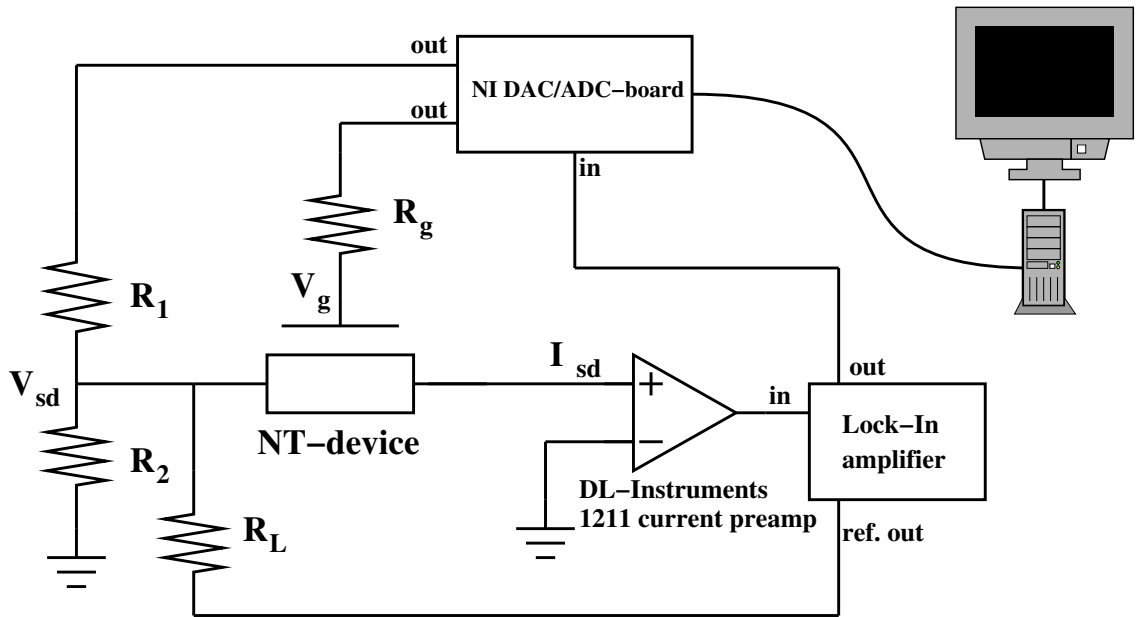
Figure 4.12: AC-measurement of the electronic properties of a nanotube. In contrast to the DC-measurement the reference output of a lock-in amplifier is added to the bias voltage through a $1\,\mathrm{M\Omega}$ resistor R_L at frequencies between $200\,\mathrm{Hz}$ and $2\,\mathrm{kHz}$.

a breakdown of the gate oxide. The quantity that is measured is the current through the device I_{sd}. With a typical device resistance between several $10\,\mathrm{k\Omega}$ to several $10\,\mathrm{M\Omega}$ and a bias voltage V_{sd} of usually between $10\,\mathrm{mV}$ and $500\,\mathrm{mV}$ typically I_{sd} is in the nA-range requiring the use of a current-preamplifier.

A slightly modified technique uses a lock-in amplifier to measure the differential conductance $G_{sd}^* = \mathrm{d}I_{sd}/\mathrm{d}V_{sd}$. This measurement scheme (see figure 4.12) produces data with significantly less noise than DC-measurements making it especially suitable to see transitions between different quantum states [86], which require a much better signal-to-noise ratio than measurements of the Coulomb-blockade (section 3.2) or the FET-characteristics (sections 3.3 and chapter 6). However, the AC-technique cannot be used for measurements of FET-characteristics like the mobility (section 6.1) as the calculation

of the mobility requires knowledge of the actual device current rather than the differential conductance. The only FET-parameter that can be measured by such an AC-technique is the transconductance $g = \mathrm{d}I_{sd}/\mathrm{d}V_g$ [81]. For this type of measurement the reference voltage of the lock-in amplifier is added to V_g, however.

Chapter 5

Single Electron Transistors: Low Temperature Measurements

5.1 Results

5.1.1 Metallic Nanotubes

Measurements on the SET-behavior of metallic carbon nanotubes are not the main focus of this work. However, as they are an important part of testing procedures for device fabrication and allow to measure various nanotube device characteristics that are not easily accessible in semiconducting devices some of the results will be included here.

Of all the devices which exhibited unambiguously metallic behavior, I have performed extensive low temperature measurements on two. The first (sample 58, device EF) is a 3.5 μm long nanotube with a diameter of 3.3 nm. An AFM image of this device is shown in figure 5.1(a). The second device (device FG) is shown in figure 5.1(b). Its length is only 440 nm, and the tube diameter is 2.6 nm.
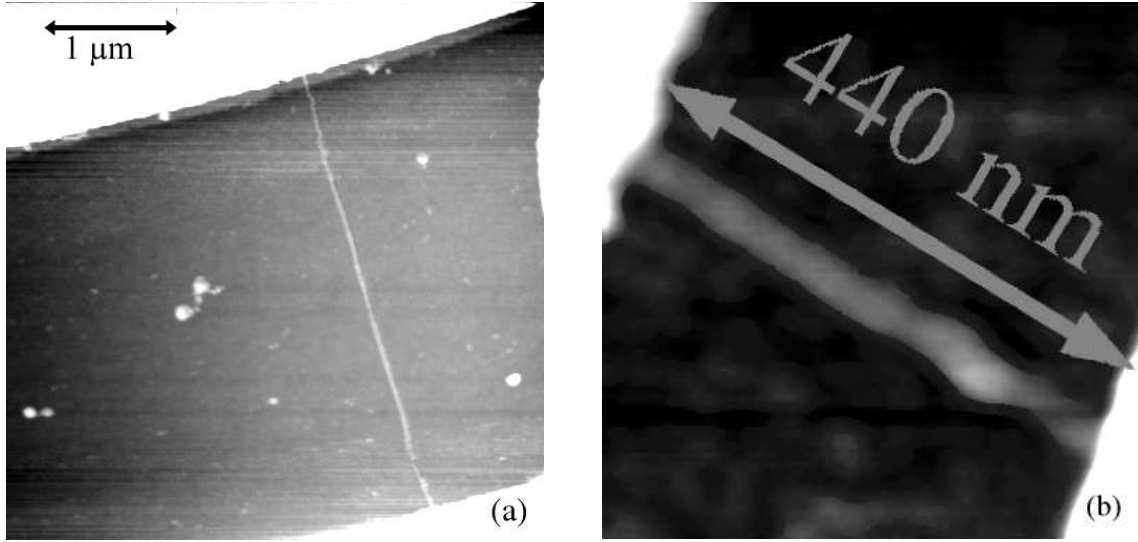
Figure 5.1: AFM micrographs of nanotube SETs. The contacts were fabricated with the technique described in section 4.2 on page 48 using a Cr adhesion layer and Au; the nanotubes themselves were grown with the "doughnut" method (section 4.1.1). (a) Tube EF. The distance between the contacts along the nanotube is 3.5 μm. (b) Tube FG. The device length is 440 nm.

Measured at room temperature using the DC-technique described in section 4.3 (figures 5.2 and 5.3), both devices show ohmic IV-curves, i. e. the device current I_{sd} is proportional to the applied bias voltage V_{sd}. The resistance of device EF as calculated from the data shown in figure 5.2(a) measured at a gate voltage of $V_g = 0$ is 88 kΩ. Device FG has a resistance of 22 kΩ, which is only about 3.5 times the fundamental lower limit of 6.45 kΩ (see section 3.3.1). This device resistance is close to the best values reported for metallic nanotube devices (8 kΩ, [95]). Both devices conduct over the hole gate voltage range of −10 to +10 V, but show a small deviation from ideal metallic behavior. This slight dependence of the device current I_{sd} on the applied gate voltage V_g can be found in many metallic nanotube devices and may be caused by a small band gap opened up by distortion of a nanotube's lattice through interactions with the substrate.

Figure 5.2: Room temperature I_{sd}-V_{sd}-curves at $V_g = 0$ for the two metallic nanotube devices investigated here.

Figure 5.3: I_{sd}-V_g-curves for the devices EF and FG measured at room temperature with a bias voltage of $V_{sd} = 10\,\mathrm{mV}$.

To determine the device parameters, which can be derived from the Coulomb-blockade behavior of the devices we performed transport experiments at low temperatures. For this purpose the sample was permanently mounted on a suitable sampl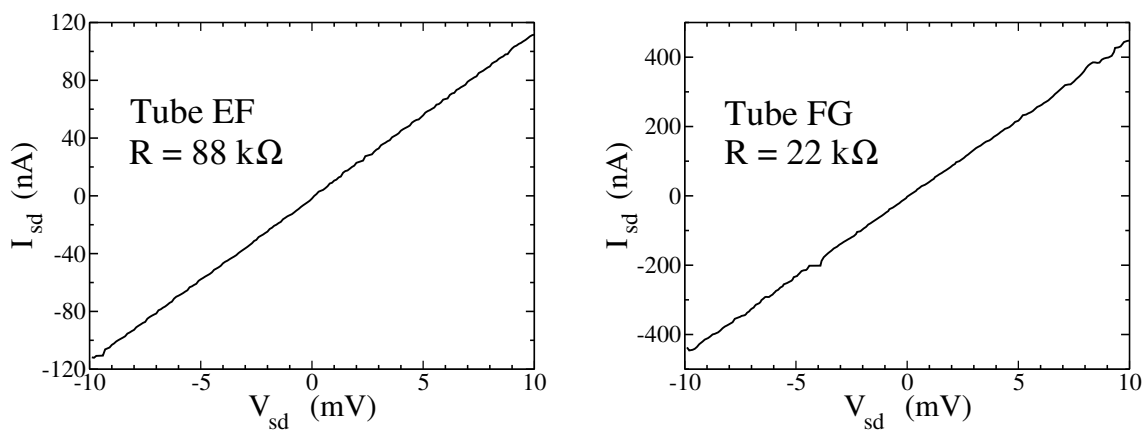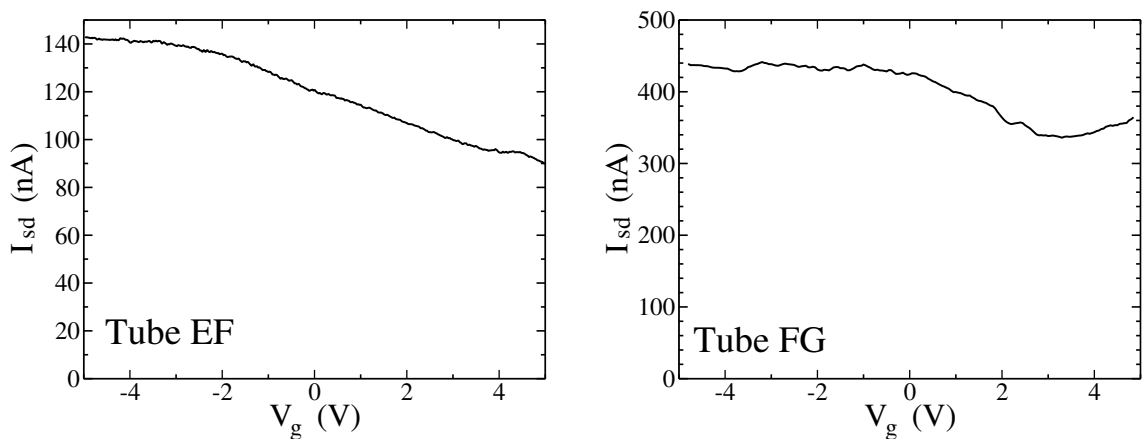e holder, while electrical connections were made using wire bonds. The measurements were carried out in a commercial 3He-cryostat (Desert Cryogenics 3HeIC) with a base temperature of below 300 mK. Figure 5.4 shows the result of one of these measurements. The differential conductance G^* is plotted as a function of V_g. For this measurement the AC-technique (see section 4.3) was used. From the distance in V_g of the conductance peaks (22 peaks per 0.1 V) we get a gate capacitance of $C_g = e \cdot 220 \, \text{V}^{-1} = 35 \, \text{aF}$. Figure 5.5 shows a similar measurement on the same device, but here both the gate voltage and the bias voltage are being varied. Since most of the "Coulomb diamonds" [86] do not have sharply defined boundaries I used a graphical technique as illustrated by the colored lines to extract the charging energy from the plot. The distance in V_{sd} of the two red lines is $2|V_{sd,\text{max}}| = 1.8$ mV, which translates into a charging energy of 0.9 meV. As shown in section 3.2 this is equivalent to a total device capacitance of $C_\Sigma = 90 \, \text{aF}$.

A similar analysis of data measured for device FG was not possible, because this device shows a more complicated behavior than device EF. Only a rough estimate of the gate capacitance was possible yielding $C_g = 4.8 \, \text{aF}$. Figure 5.6 shows a plot of the differential conductance G^* as a function of V_{sd} and V_g. Compared to the simple Coulomb diamonds seen for device EF (figure 5.5) it shows a whole range of additional features marked in the image in different colored ellipses. Black ellipse: Telegraph type switching event [111]; this feature is caused by charge traps or mobile charges near the device that
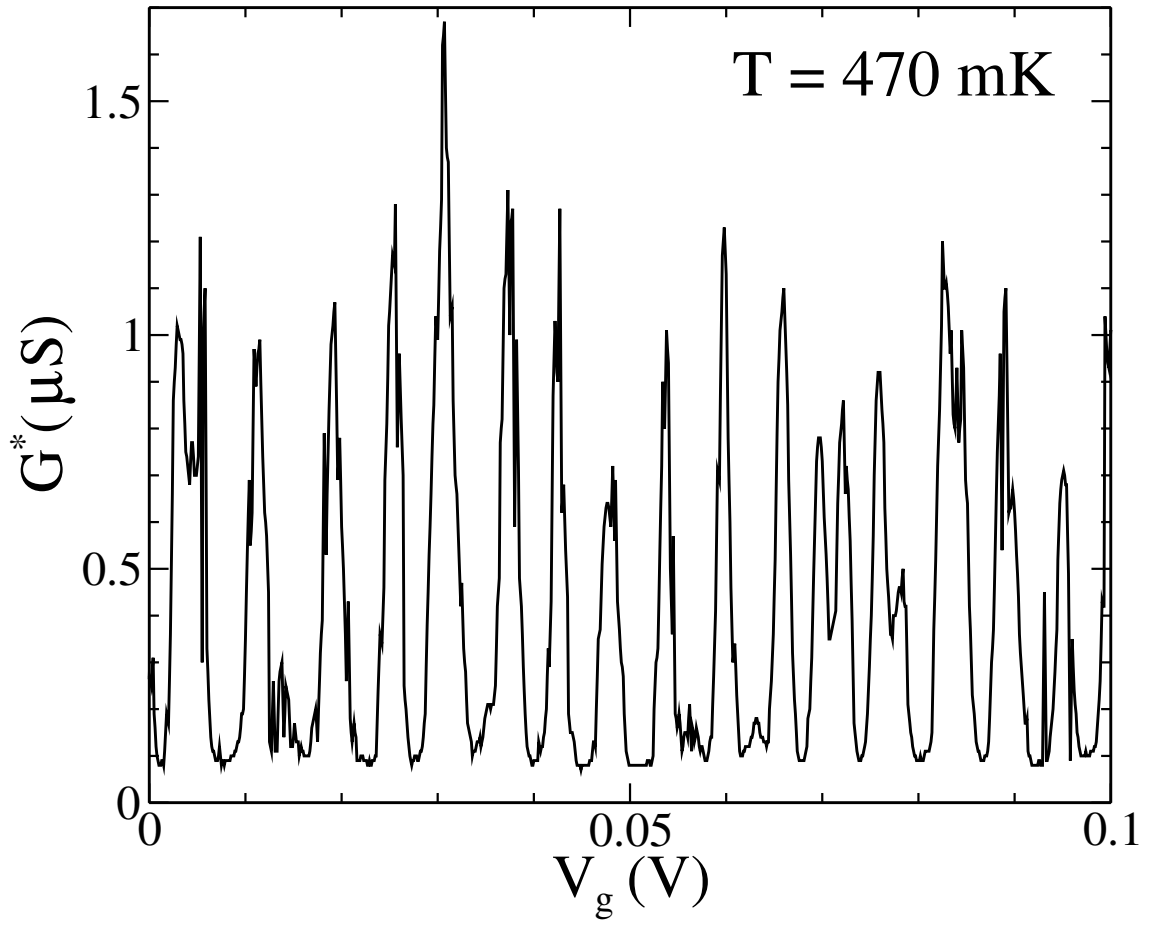
Figure 5.4: Coulomb oscillations of device EF measured at 470 mK for $V_{sd} = 0$. The plot shows the differential conductance G^* as a function of the applied gate voltage V_g measured using the AC-technique described in section 4.3.
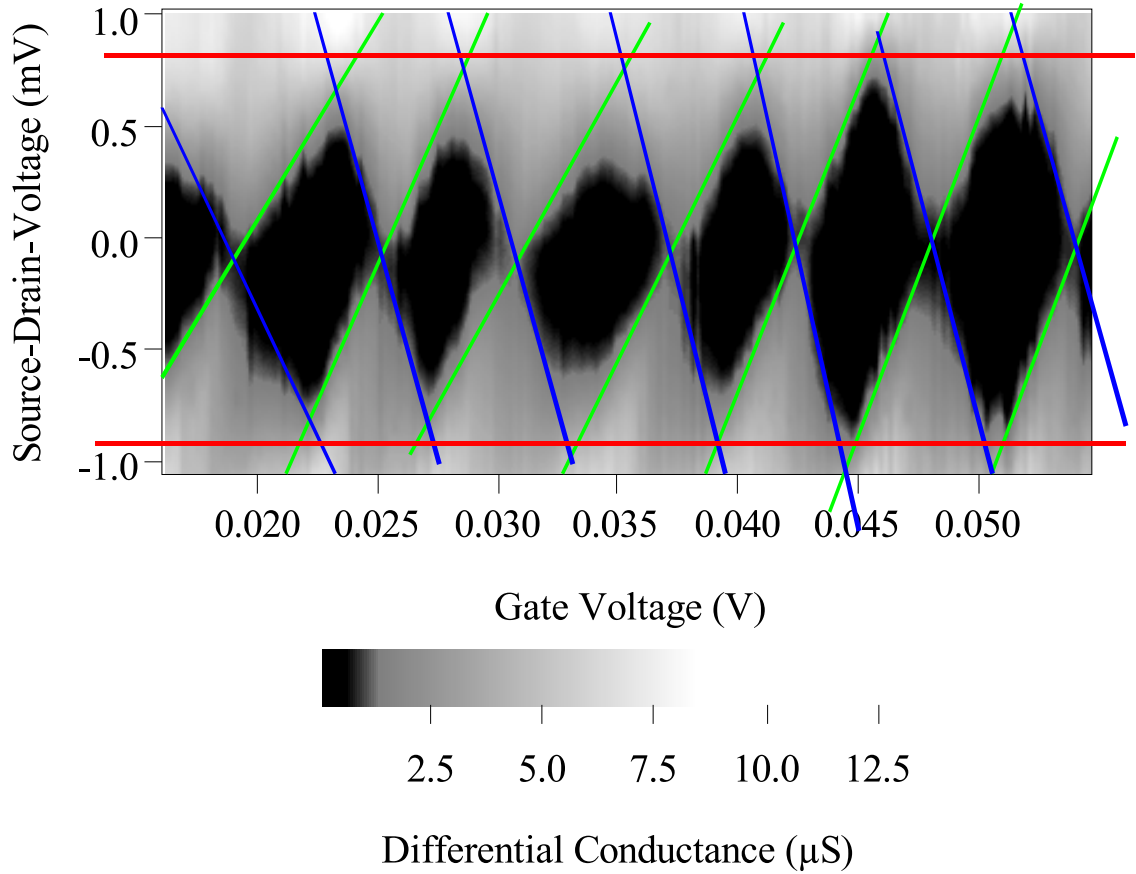
Figure 5.5: Differential conductance as a function of both V_{sd} and V_g of device EF measured at 470 mK. The colcored lines indicate how the charging energy E_C was extracted from this plot.
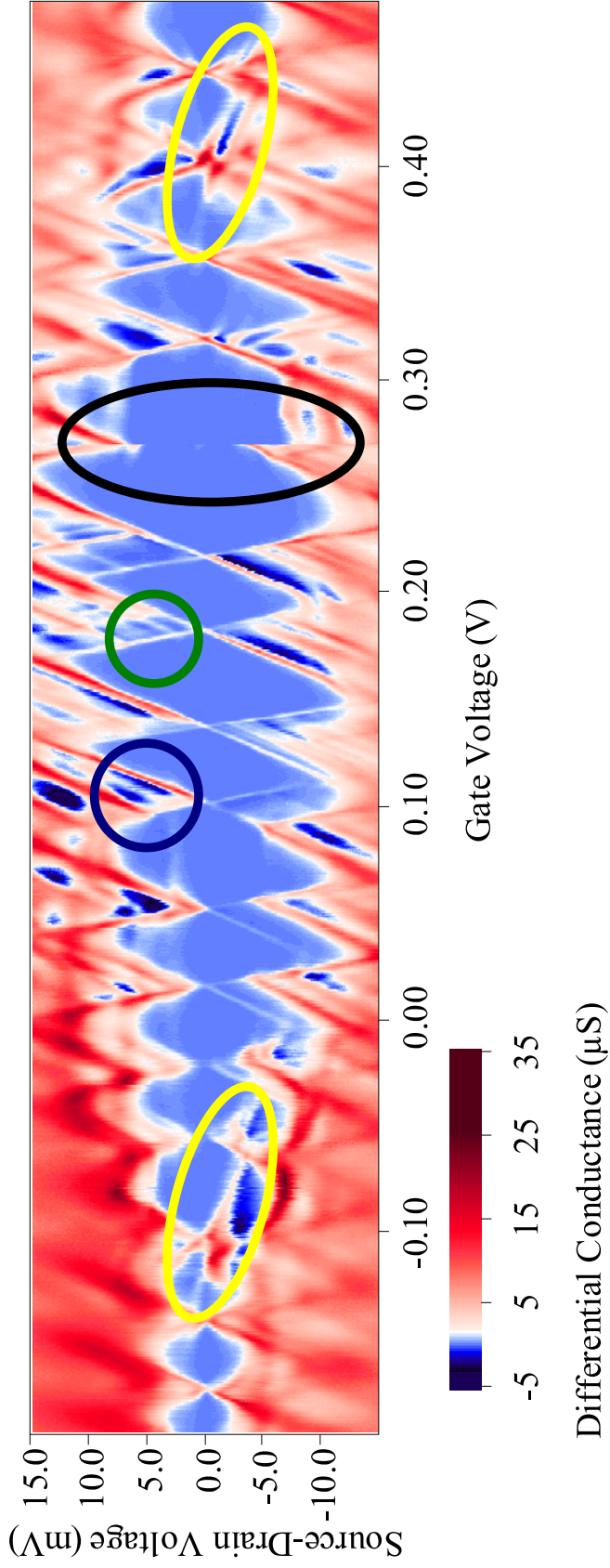
Figure 5.6: Differential conductance as a function of V_{sd} and V_g for device FG at 470 mK. Various features are marked in the plot: Black ellipse: negative differential resistance; blue circle: quantum transitions; green circle: Telegraph type noise; yellow ellipses: unidentified gap features.

can switch between two (or more) different states essentially simulating sudden jumps in V_g. Green circle: transitions involving excited states; the energy difference ΔE between the involved states is larger than the thermal energy making it possible to distinguish the states. Blue circles: a system of two (or more) coupled quantum dots in series [86] exhibits regions of negative differential resistance (compare with color scale). Yellow ellipses: unidentified features inside the Coulomb gap. These features might be related to some kind of resonant tunneling although they do not show the typical characteristics of a Kondo resonance [112], which is a sharp zero bias conductance peak in every other Coulomb diamond.

5.1.2   Semiconducting Nanotubes

While semiconducting nanotubes produced by laser-ablation (see section 2.3.1) often exhibit a gap in the conductance as a function of V_{sd}, interpreted as due to a series of large tunnel barriers approximately 100 nm apart [96] we were able to observe Coulomb blockade in our CVD-grown semiconducting nanotube devices. In this case the FET-behavior (see figure 2.5(b)) of the semiconducting nanotube is superimposed on the Coulomb oscillations. An example of this behavior is given in figure 5.7 (see also [70]). The small amplitude of the oscillations can be attributed to the length of the device resulting in a charging energy not much bigger than the thermal energy.
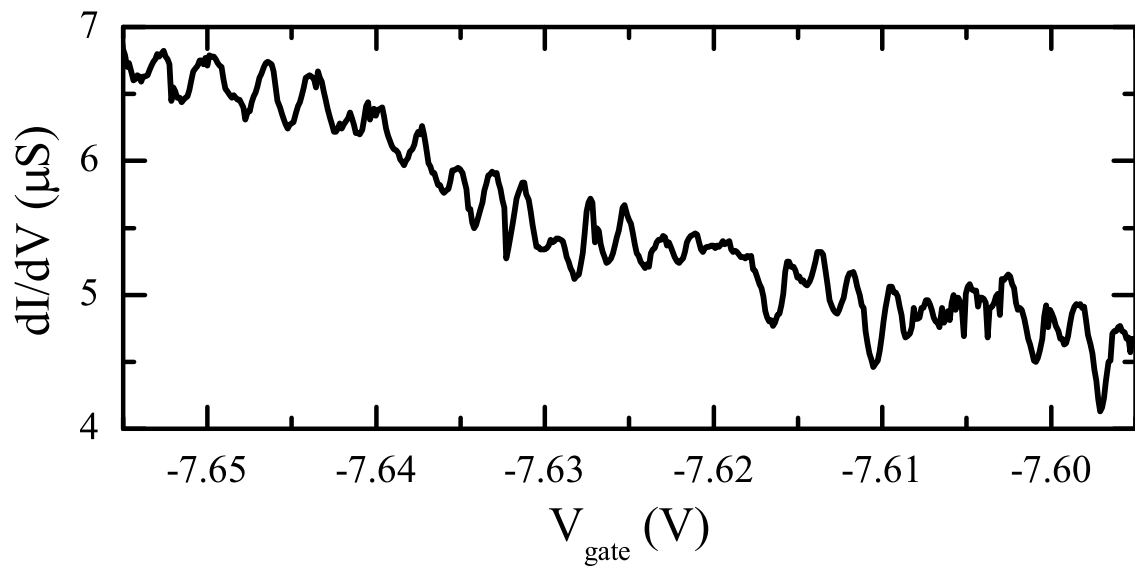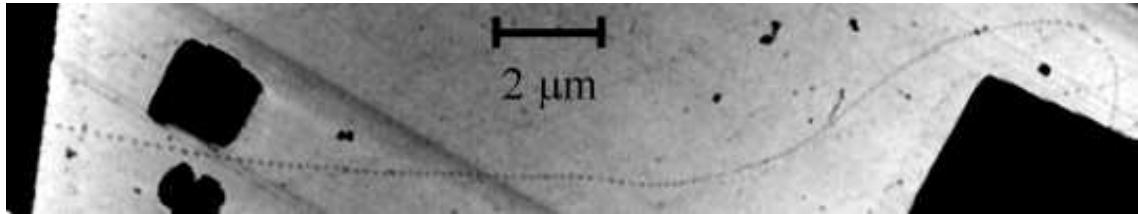
Figure 5.7: AFM micrograph of a 20 µm long semiconducting nanotube (device BF, sample 58 with a diameter $d = 2.2$ nm) and Coulomb oscillations measured on this device at a temperature of 470 mK using the AC-technique described in section 4.3. The DC-component of V_{sd} was set to zero in this measurement.

5.2 Conclusions

From the capacitances measured for the two devices we get the following picture. The total capacitance of device EF is 90 aF, while the gate capacitance is 35 aF leaving a combined capacitance of 55 aF for both contacts. Since the Coulomb diamonds shown in figure 5.5 are fairly symmetric it is fair to assume that both the source and the drain contact have a capacitance of 25–30 aF and assume that to be the typical capacitance for a Cr/Au-nanotube contact. With this the ratio between C_g and C_Σ is about 1:3, in other words the source and drain contacts significantly shield the nanotube from the influence of the gate, which is an important factor in the design of nanotube-FETs.

Since the correction to the gate capacitance due to the different tube diameters is only logarithmic [79] comparison between the two devices (EF: 35 aF, 3.5 µm; FG: 4.8 aF, 440 nm) is allowed and yields a capacitance per length of about 10 aF/µm. Possibly due to the shielding effect from source and drain, this is smaller than values obtained from electrostatic simulations (19 aF/µm, see section 6.2) and the analytical expression [79] which neglects the fact that the SiO_2 dielectric is only between the nanotube and the gate but not above the tube yielding a value of about 40 aF/µm for the 500 nm thick SiO_2 used on our samples.

The appearance of Coulomb blockade in a semiconducting nanotube gives us an interesting insight into the properties of semiconducting nanotubes. Using the same method as for the metallic nanotube devices we can calculate the gate capacitance to be about 90 aF. Using a capacitance per length of 10 aF/µm since it was determined from devices on the same sample under the same experimental conditions used also for this measure-

ment we find 90 aF to correspond to a nanotube length of about 9 μm, which is about half of the actual device length. This suggests that the Coulomb blockade is not governed by the device length but the localization length [92], which is twice the mean free path for the charge carriers. Thus, in this nanotube the mean free path l is about 4.5 μm. If we add the capacitance of the contacts (55 aF) to C_g as determined from the periodicity of the Coulomb oscillations in order to estimate the charging energy we get $E_C \approx 500\,\mu\text{eV}$, i. e. in this device a possible Peierls gap opening up around the Fermi energy would have to be smaller than $E_G = 500\,\mu\text{eV}$. Therefore, a Peierls transition, which takes place at $T_C \approx 0.28 E_G/k_B$, is suppressed above at least 100 mK, much lower than the temperature predicted for a (5,5)-nanotube (9 K [113] or 15 K [114]).

Chapter 6

Field-Effect Transistors

6.1 Mobility

Field-effect transistors are extremely important for electronics applications in general and digital electronics in particular. One of the factors determining their high-frequency performance is the carrier mobility in the FET channel. A high mobility also results in reduced resistive losses inside the transistor lowering its power consumption.

6.1.1 Fundamentals

Due to the debate about the Schottky barrier at nanotube-metal contacts the amount of research done on mobility in nanotubes has been limited. Since mobility and especially its temperature dependence can give information about the type of scattering processes taking place in a material knowledge about mobility and its dependence on e. g. temperature is important in understanding the physics of a material. Furthermore, mobility is an important factor in determining the frequency response and the switching speed of a

transistor. For most semiconductor materials the simple picture given in section 3.3.1 is not sufficient, because current is not only carried by electrons but also by holes. For such a case we have to amend the relation for the conductivity σ given by the Drude model to obtain

$$\sigma = ne \cdot \mu_e + pe \cdot \mu_h. \tag{6.1}$$

Here n is the number density of electrons and p the number density of holes. Accordingly, μ_e is the electron mobility and μ_h the hole mobility. Generally the two are not equal. The carrier densities n and p depend on the levels of chemical doping as well as field doping. It is often possible in an FET geometry to reach a level of field doping sufficient to ignore one type of carrier completely. In addition the shift of band edges caused by the field doping also creates large barriers for the minority carriers. As-fabricated nanotubes usually show p-type conductance and require either large positive gate voltages or additional fabrication steps (potassium doping or annealing in H_2) to switch to n-type behavior [67, 115, 100, 79]. The different methods for determining the mobility presented in the following sections all rely on the dominance of just one type of charge carriers. Since we used as-grown nanotubes for our devices all mobilities presented here are hole-mobilities.

McEuen et al. [96] have made arguments that interband backscattering, which is forbidden in metallic nanotubes, limits the conductivity at low doping levels i. e. at low applied gate voltages, while at higher levels of field doping the conductivity should approach values for metallic tubes. Based on this assumption we can make an attempt at obtaining a rough estimate for the mobility in a semiconducting CNT.

Assuming that applying a V_g that pushes the Fermi level E_F to the beginning of the

second subband at 2Δ (see also figure 2.4 on page 10 and section 2.2.2) is sufficient to make a semiconducting tube achieve a conductivity similar to a metallic tube we can use the Fermi velocity of metallic nanotubes ($v_F = 8.1 \times 10^5$ m/s [25]) to estimate the mobility of a semiconducting tube in the following way:

First we need to calculate the charge density n in the tube from the Fermi velocity. Following the derivation in 3D (see e. g. [116]) we get for a 1D system $n = k_F/\pi$. With two spins and two equivalent bands this becomes

$$n = 4\frac{k_F}{\pi} \tag{6.2}$$

for an SWNT, where k_F is the magnitude of the Fermi wave vector. Using equation 2.2 with $E = E_F = 2\Delta$ and $k = k_F$ and we can write for the first subband

$$2\Delta = \sqrt{\left(\frac{\hbar k_F v_F}{2}\right)^2 + \Delta^2}. \tag{6.3}$$

With equation 6.2 this yields

$$n = \frac{8\sqrt{3}\Delta}{hv_F}. \tag{6.4}$$

Now we use the expression from [28] that relates Δ to the diameter d of the nanotube $E_g = 2\Delta = 0.7/d$ [eV/nm] obtaining $n \cdot d = 2.9$. Using the arguments from section 3.3.1 especially equation 3.8 relating length L and conductance G of a 1D conductor to the mean free path l and the fundamental conductance limit G_{max} we get for the mobility

$$\mu = \frac{\sigma}{ne} = \frac{GL}{ne} = \frac{G_{max}l}{ne}. \tag{6.5}$$

Using the mean free path of metallic nanotubes $l \approx 3\,\mu\text{m}$ [25] we can now estimate the mobility to be $\mu = 10{,}000\text{–}50{,}000\,\text{cm}^2/\text{Vs}$ for the commonly observed tube diameters

between 1 and 5 nm. These numbers, while high compared to most semiconductors, are in the same range as the mobilities within the sheets measured in graphite, which are 15,000 cm^2/Vs for holes and 20,000 cm^2/Vs for electrons [2].

A more thorough approach to calculating mobility in semiconducting nanotubes has been used by Pennington and Goldsman [117]. They have employed a semiclassical model to investigate electron-phonon coupling in semiconducting nanotubes. From this model, which ignores impurity scattering, they derive the electron drift velocity v_d for various diameters of zigzag nanotubes, which then allows one to calculate the mobility as the ratio between v_d and the electric field E applied along the nanotube. For a (59,0)-nanotube they obtain a maximal mobility of 120,000 cm^2/Vs. The second result of their model is the fact that v_d decreases in the case of high applied fields. This is in good agreement with experimental results for metallic nanotubes by Yao et al. [118] who explain the effect with the emission of zone boundary phonons if the kinetic energy of the electrons is sufficient, thus, limiting the mean free path at high fields.

Another result of their study was a strong dependence of mobility on the nanotube diameter. They found the time τ between scattering events to be roughly proportional to the tube diameter: $\tau \propto d$. Since the electron effective mass at the band bottom is inversely proportional to the diameter $m^* \propto d^{-1}$ the mobility calculated from this model depends on d like $\mu = e\tau/m^* \propto d^2$. Although this relationship is likely to fail for larger d where Δ becomes too small this model suggests that larger diameter tubes should exhibit higher mobilities making them more desirable for electronics applications then thinner nanotubes. In this respect our simple model agrees with Pennington and Goldsman's

model.

6.1.2 Intrinsic Mobility

The standard method of measuring mobility in semiconductor materials is to measure the Hall coefficient and Hall resistance of the material and use these parameters to determine the so called Hall-mobility [89]. This method, however, cannot be used in 1D materials like SWNTs. In nanotube films [119, 120] and mats [121] it is possible to carry out Hall effect measurements but those measurements do not allow the determination of mobility within the individual tubes as they measure only the collective behavior of many nanotubes.

In order to measure the mobility μ intrinsic to a nanotube one must use the characteristics of a nanotube FET and try to deduce μ from them. Generally, this is harder to do and more ambiguous than the fairly direct measurements using the Hall effect. To understand this we first revert to one of the definitions of μ. According to this definition given within the Drude model [91] μ is the ratio between conductance σ and charge density q: $\mu = \sigma/q$. In a 1D system like a SWNT the charge density can be calculated as $q = c_g(V_g - V_{th})$ where c_g is the gate capacitance per length and V_{th} is the threshold voltage at which the FET starts to turn on. This assumption is valid only for $V_g > V_{th}$, i. e. when the device is actually turned on. Furthermore, it requires the bias voltage V_{sd} to be small enough for the device to be in the linear response regime. We also assume that the gate capacitance is much smaller (Capacitances in series add inversely!) than the quantum capacitance of the nanotube [122, 72], such that the quantum capacitance

may be neglected. For our devices grown on $500\,\mathrm{nm}$ SiO_2 this is certainly the case. The relationship ignores thermally activated carriers, which may be significant for small values of $V_g - V_{th}$ and high temperatures. Most importantly, this relationship assumes that c_g and V_{th} do not vary appreciably along the length of the channel, which requires the length of the nanotube L to be much greater than t, the dielectric thickness of the gate oxide. Few nanotube devices studied in the literature satisfy this last criterion. For a p-type device (like most as-fabricated nanotube transistors) this relationship reverses its sign to $q = c_g(V_{th} - V_g)$. Using $\sigma = G \cdot L$ from section 3.3.1 we get

$$\mu = \frac{L}{c_g} \frac{G}{V_{th} - V_g}. \tag{6.6}$$

Besides the above requirements regarding the validity of the simple expression used to calculate the charge density, this relation also depends sensitively on the threshold voltage V_{th}, which cannot always be determined unambiguously. Finally G has to be the actual nanotube conductance. Only if the device conductance is dominated by the nanotube conductance and not the contact resistances is it meaningful to use the device conductance as G. For a Schottky barrier transistor this formula is meaningless. If this formula is applicable, however, it provides the value closest to the intrinsic mobility in a nanotube. In the following we will therefore denote the mobility computed from this formula as μ and for brevity call it intrinsic mobility. It is analogous to the so-called "effective mobility" in conventional MOSFETs [90].

6.1.3 Field-Effect Mobility

In many cases it is impossible to determine the threshold voltage V_{th} with sufficient precision. To be able to compare the performance of FETs in such cases it is common to use a slightly different way of calculating the mobility [90]:

$$\mu_{FE} = \frac{L}{c_g} \left| \frac{\partial G}{\partial V_g} \right|. \tag{6.7}$$

The mobility μ_{FE} obtained in this way is called field-effect mobility and is a device specific quantity not a material specific parameter. It is useful in order to compare the performance of different devices. In most cases the $G(V_g)$-curve of an FET has negative curvature beyond the subthreshold region, such that we get $\mu_{FE} < \mu$, i. e. the field-effect mobility underestimates the mobility.

6.1.4 Saturation Mobility

At high bias voltages the device resistance of an FET is no longer constant. Instead the device current $I_{sd}(V_{sd})$ saturates at a value dependent on the applied gate voltage. This behavior can be used as an alternate method for calculating a mobility called saturation mobility μ_{sat}. Although not as reliable as the previously introduced techniques, the advantage of this method is that it probes different aspects of the device characteristics, making it suitable to independently verify results obtained for μ and μ_{FE}. Adapted for the 1D geometry of our devices the saturation mobility can be calculated as follows:

$$\mu_{sat} = \frac{2L}{Bc_g} \frac{I_{sd,sat}}{(V_g - V_{th})^2}. \tag{6.8}$$
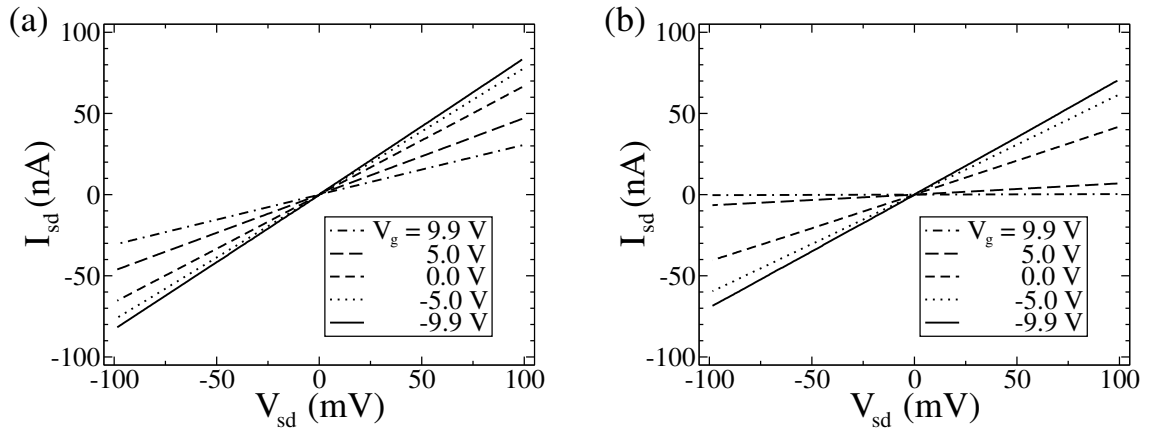
Figure 6.1: *I-V*-curves for both ultralong nanotube devices. Clearly for all gate voltages the curves are Ohmic (i. e. the devices have constant resistance) in this bias voltage range. The total device resistance has increased compared to the data shown in figure 6.3 since these curves were measured several months later. (a) Tube AD. (b) Tube BC.

In this formula B is the so-called body factor, which accounts for the dependence of V_{th} on the position along the device caused by a nonlinear variation of the charge density along the device in the saturation regime [87, 90]. Even for conventional MOSFETs B is not well understood, much less so for nanotube transistors. For this reason we set $B = 1$ in the following. In addition any dependence of μ on the charge density will cause a deviation from the ideal $V_g{}^2$-dependence in this equation. We use μ_{sat} only as a way of verifying data obtained from equations 6.6 and 6.7.

6.2   Results from FETs

Using the growth method for ultralong nanotubes described in section 4.1.3 we were able to fabricate several devices with lengths of several hundred micrometers between the contacts. Figure 6.2 shows two devices fabricated on sample UL7 (degenerately doped Si with 500 nm thermally grown SiO_2). These devices showed clear FET-behavior and were
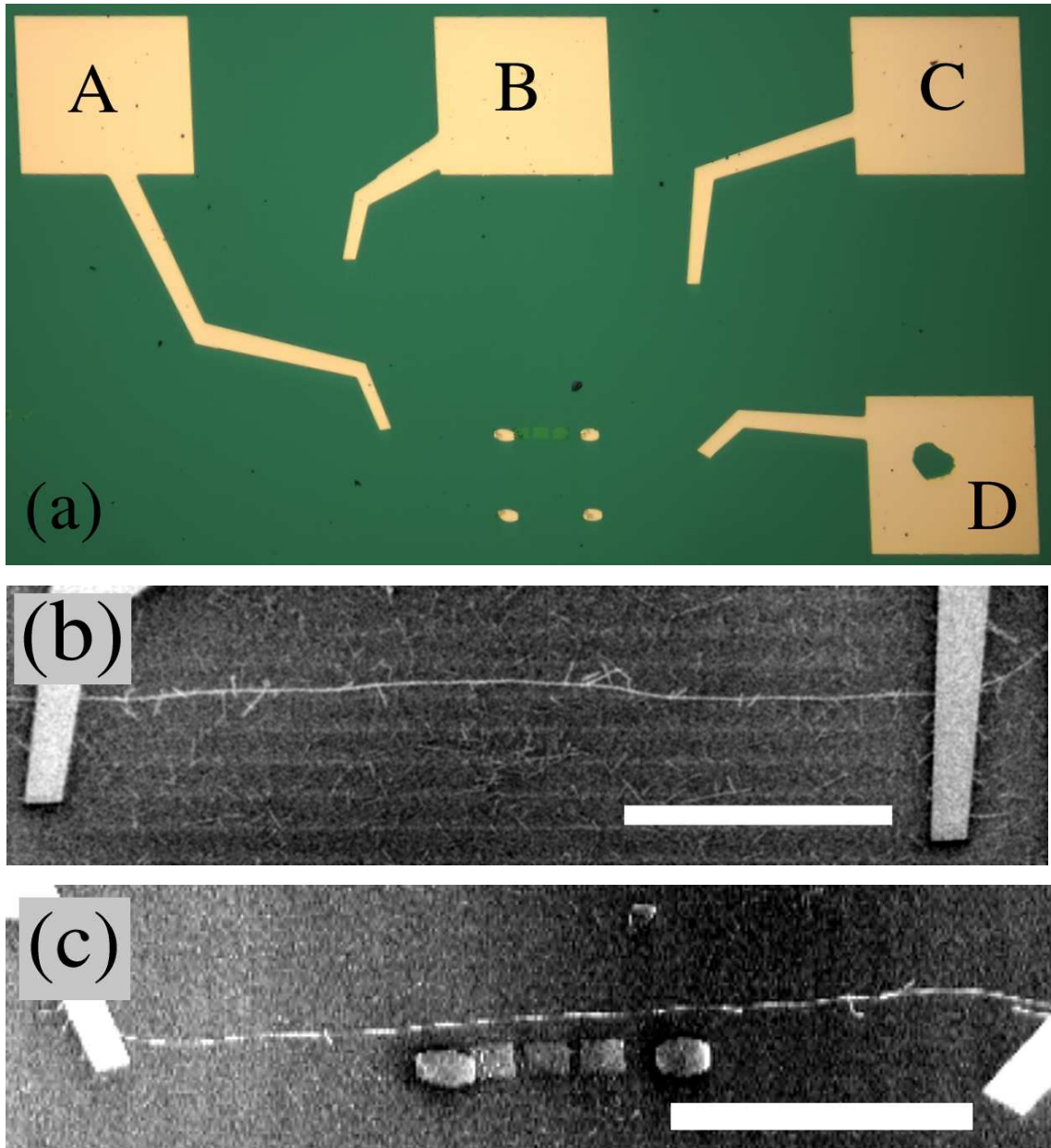
Figure 6.2: Devices made from ultralong nanotubes. (a) Optical microscope image of two devices on sample UL7. There are two devices on this sample, the first between bonding pads A and D and the second between B and C. The gold bonding pads are approximately $150\,\mu m \times 150\,\mu m$ in size. The additional gold patches in the center of the bottom half of the images are residues from the alignment procedure marking the corners of an alignment marker pattern like in figure 4.7. (b) Device AD imaged with a Zeiss DSM982 field-emission SEM. The scale bar is $100\,\mu m$. (c) FESEM image of device AD. ($100\,\mu m$ scale bar)
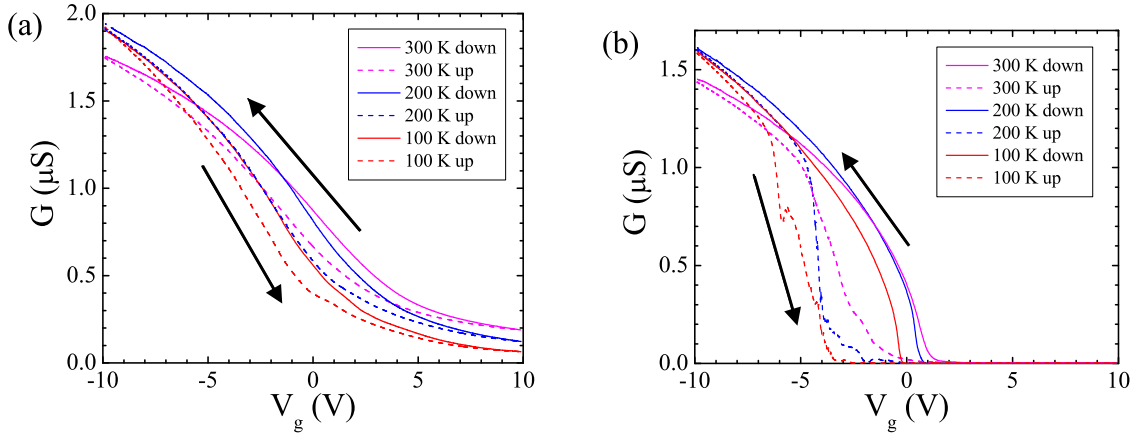
Figure 6.3: G-V_g-curves for the ultralong nanotube devices at 100, 200 and 300 K measured with a bias voltage of 50 mV. The arrows indicate the direction, in which the current is being swept on each branch of the hysteresis loop. (a) Tube AD. (b) Tube BC.

Figure 6.4: G^2-V_g-curves for the ultralong nanotube devices at 100, 200 and 300 K. (a) The plot for tube AD shows $(G - G_{min})^2$ rather than G^2 as a function of V_g. G_{min} is the conductance at $V_g = 10$ V, assumed to be the "metallic background". (b) Tube BC.

chosen for further analysis. Device AD has a length of 345 μm and a diameter of 5.3 nm; device BC is 325 μm by 3.9 nm. The device length were extracted from FESEM images (see also [107]) while the diameters were measured by AFM.

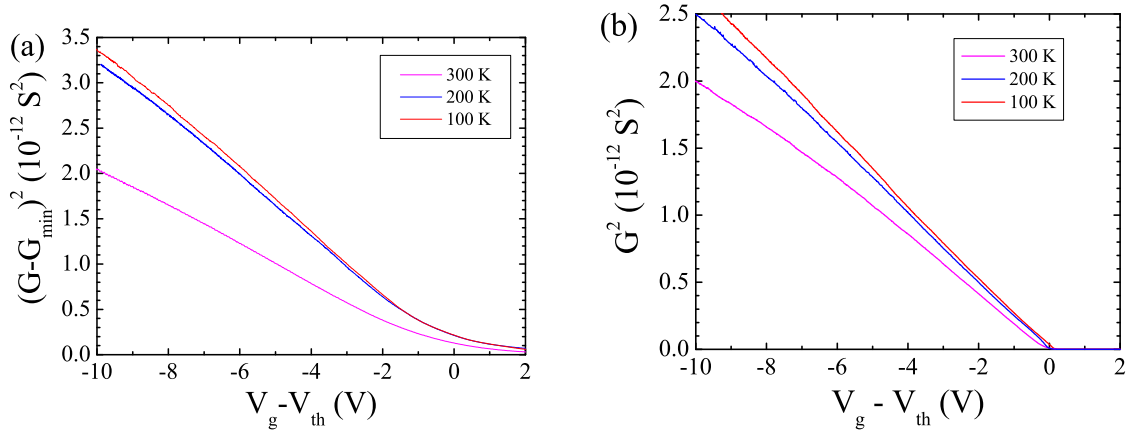On these devices we performed electrical measurements utilizing the DC-technique described in section 4.3 inside a commercial low temperature probe station[1]. Some of these measurements are shown in figures 6.3 and 6.1. Figure 6.1 shows I-V-curves of the devices demonstrating constant resistance, i. e. Ohmic behavior for all gate voltages in a bias voltage range of up to 100 mV. Figure 6.3 shows the dependence of the device conductance $G = I_{sd}/V_{sd}$ on the gate voltage v_g. The curves were measured at different temperatures at a bias voltage of $V_{sd} = 50$ mV. The hysteretic behavior of both devices, similar to what is described in [64], is clearly visible. Comparing the two branches of the hysteresis loop the downward sweep is much smoother and more reproducible than the upward sweep. This hints that the trapped charges responsible for the hysteresis are positive (holes), with only few trapped holes on the downward sweep, and many trapped holes in irreproducible configurations on the upward sweep. We therefore use the downward sweep in V_g for further analysis.

When analyzing the device behavior we noted that the conductance of device BC followed the empirical relationship $G \propto \sqrt{V_{th} - V_g}$ remarkably well at temperatures from 50 K up to 300 K. Figure 6.4(b) illustrates this by showing a plot of G^2 as a function of applied gate voltage measured during the downward sweep. Since device AD does not turn off completely we assume the nanotube in this device is a semiconducting nanotube

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[1]Desert Cryogenics TT-probe station with a temperature range from 1.5 K to 400 K.

with a metallic tube inside, electrically in parallel with the semiconducting tube. Subtracting the conductance $G_{min} = G(V_g = 10\,\mathrm{V})$ as the metallic background (see figure 6.4(a)) this device shows the same $G^{1/2}$-behavior as device BC. This $G^{1/2}$-behavior allows to perform simple fits to the G-V_g-curves to determine V_{th} and subsequently to calculate the intrinsic mobility μ.

6.3   Conclusions

Since the behavior of device AD as well as its diameter of 5.9 nm suggest it to consist of a multi-walled nanotube with at least one semiconducting nanotube on the outside and one or more metallic tubes on the inside we will focus on device BC in analyzing the device characteristics. Before starting to extract information about nanotube mobility we need to ascertain that the methods presented in section 6.1 are in fact applicable. Figure 6.5 shows the subthreshold behavior of device BC at various temperatures and the subthreshold swing S for this device. As figure 6.5 demonstrates S is temperature dependent in contradiction to the behavior expected for a Schottky barrier transistor [71]. Furthermore with about 100 mV/decade the value of S is much lower than expected for a Schottky barrier transistor with the same oxide thickness (1500 mV/decade [71]). Finally the device length of $L = 325\,\mu\mathrm{m}$ is clearly larger than the dielectric thickness t of the SiO_2 gate oxide as required in section 6.1.2.

To calculate the mobility it is necessary to know the capacitance C_g between the nanotube and the gate. Since previously accessible values for the capacitance per length c_g vary significantly (10 aF/µm from SET-behavior, see chapter 5 to about 40 aF/µm for a
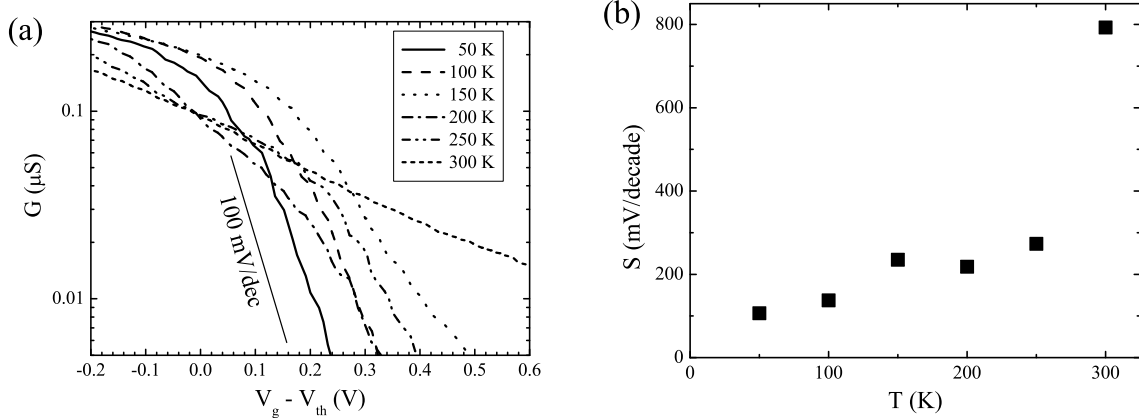
Figure 6.5: (a) Conductance G as a function of $V_g - V_{th}$ in the subthreshold regime for temperatures from 50 to 300 K. For comparison a subthreshold swing of 100 mV/decade is shown. (b) Subthreshold swing S as a function of temperature. S shows a clear temperature dependence for all temperatures. The jump in temperature dependence at 300 K coincides with a slight increase of total device resistance at 300 K. This behavior cannot be understood in terms of the models presented here and requires further study.

nanotube completely surrounded by SiO_2 [79]) we decided to calculate c_g with a commercial computer simulation solving Poisson's equation [123]. This yielded a value of 19 ± 3 aF/µm. Using this number we could calculate the mobility for device BC. Figure 6.6(a) shows the intrinsic mobility μ for temperatures between 50 and 300 K; figure 6.6(b) shows the field-effect mobility as calculated from the same data sets. As expected from the $G^{1/2}$-dependence of the device conductance the intrinsic mobility shows a power law behavior itself. Remarkably, for low $V_{th} - V_g$ the mobility exceeds 77,000 cm^2/Vs, which is the electron-mobility in high-quality InSb at room temperature [124]. It also exceed the highest known hole mobility, which is 4,000 cm^2/Vs in PbTe [87]. To our knowledge this makes our nanotubes the material with the highest mobility measured at room temperature. On the other hand the field-effect mobility (figure 6.6(b)) being a device specific parameter allows direct comparison with other types of transistors.
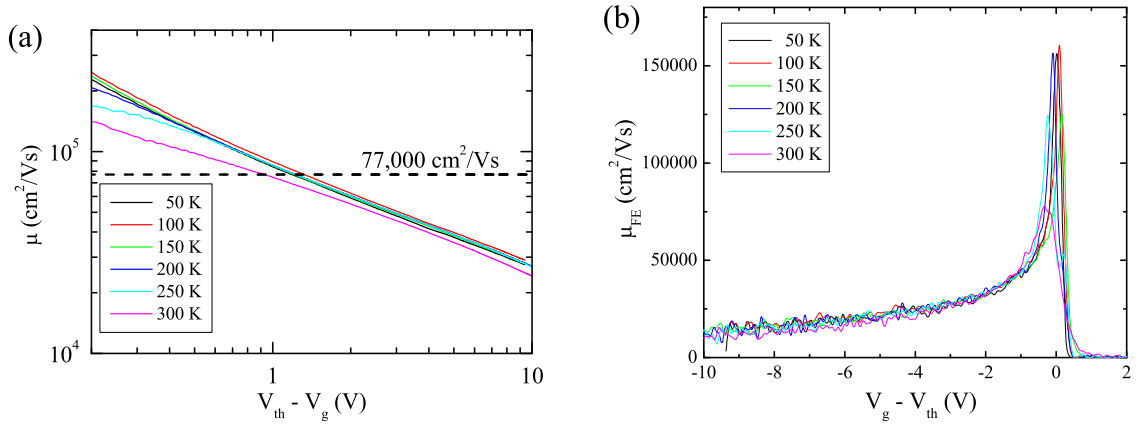
Figure 6.6: (a) Intrinsic mobility as a function of $V_{th} - V_g$. The horizontal line indicates the electron-(Hall)-mobility of the InSb which to date is the highest mobility at room temperature known for any semiconductor. (b) Field-effect mobility as a function of $V_{th} - V_g$.
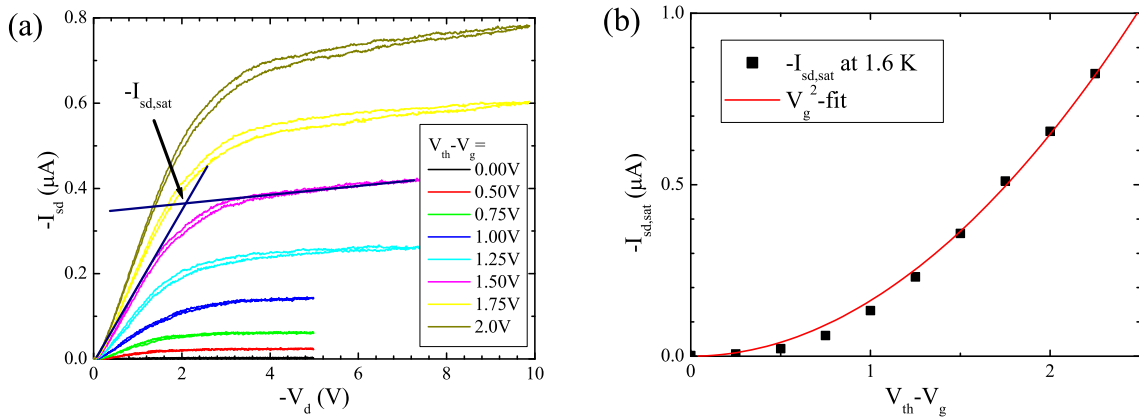
Figure 6.7: Determining the saturation mobility. (a) $I_{sd} - V_{sd}$ curves in saturation for different V_g. The dark blue lines illustrate the graphical method used for determining the respective saturation current I_{sdsat}. (b) Saturation current as a function of V_g and V_g^2-fit to calculate μ_{sat}. (Measurement courtesy of S. Getty.)

Although not commonly used this comparison is even possible in the case of Schottky barrier transistors, for which the calculation of the intrinsic mobility does not make sense physically. As shown in figure 6.6(b) the field-effect mobility μ_{FE} at room temperature peaks at 79,000 cm^2/Vs. This number compares favorably to values measured for typical Si-devices: $\sim 1,000$ cm^2/Vs [125] or state-of-the-art high-electron mobility transistors (HEMTs) [126]. One problem in utilizing the high mobility in nanotubes could be the fundamental limitation on the field-effect mobility due to finite dwell time of the carriers in transistors with short channel length [127].

In order to verify the mobility values we also conducted measurements to determine the saturation mobility in device BC. For much shorter nanotubes Javey et al. [65] have used this method to determine the hole mobility in their Pd-contacted nanotubes, which yielded a value of 4,000 cm^2/Vs. The result of our measurements is shown in figure 6.7. Figure 6.7(a) shows the I_{sd}-V_{sd}-curves used to determine the saturation current $I_{sd,sat}$, while (b) shows its V_g^2-dependence and the fit used to determine the mobility. The value derived from this V_g^2-fit is $\mu_{sat} = 55,000$ cm^2/Vs. This confirms the results of the calculations for μ and μ_{FE}. Because of the length of this device, even a comparatively large V_{sd} of 10 V results in a field of only 300 V/cm, about 10 times lower than the field at which the mobility starts to decrease due to saturation of carrier velocity [117].

With the knowledge that the device resistance is dominated by the intrinsic nanotube resistance we can apply equation 3.8 and obtain a fair estimate of the mean free path in our semiconducting nanotube. A non-zero contact resistance would imply a longer mean free path. Using the maximum conductance of 1.4 μS observed at room temperature (see fig-

ure 6.3(b) and assuming that the nanotube is either single-walled or multi-walled with the current carried only by the outer shell [128, 129] we get a mean free path of $l = 2.9\,\mu$m. This is in good agreement with the mean free path ($l = 4.5\,\mu$m) determined in chapter 5 for a different nanotube device using a fundamentally different method (Coulomb oscillations). The validity of our calculations is further corroborated by the observation that at around $3\,\mu$m length a nanotube in an FET no longer behaves ballistic [65]. Finally the mean free path is very similar to values found in metallic nanotubes (see also section 3.3.1 on page 30).

Chapter 7

Hysteretic behavior

7.1 Hysteresis in Nanotube-FETs

The high mobility of carbon nanotubes suggests high sensitivity in applications where charge detection is required, for example in a memory cell, in which the charge on a floating gate is detected by a transistor; or a chemical sensor, in which chemisorption of a target species produces a charge detected by a transistor. Unfortunately the high sensitivity also makes a nanotube device susceptible to hysteresis effects and fluctuations caused by charges moving near the nanotube. While present in many if not all nanotube devices these hysteresis effects have been the subject of only a few publications.

Figure 7.1 shows an example of such a hysteretic behavior. The nanotube was grown with the "doughnut" method described in section 4.1.1 on a degenerately doped Si-substrate with 500 nm of thermally grown SiO_2. Obviously the hysteresis loop increases in size between 200 K and room temperature.

The direction in which the device goes through the hysteresis loop (see arrows in
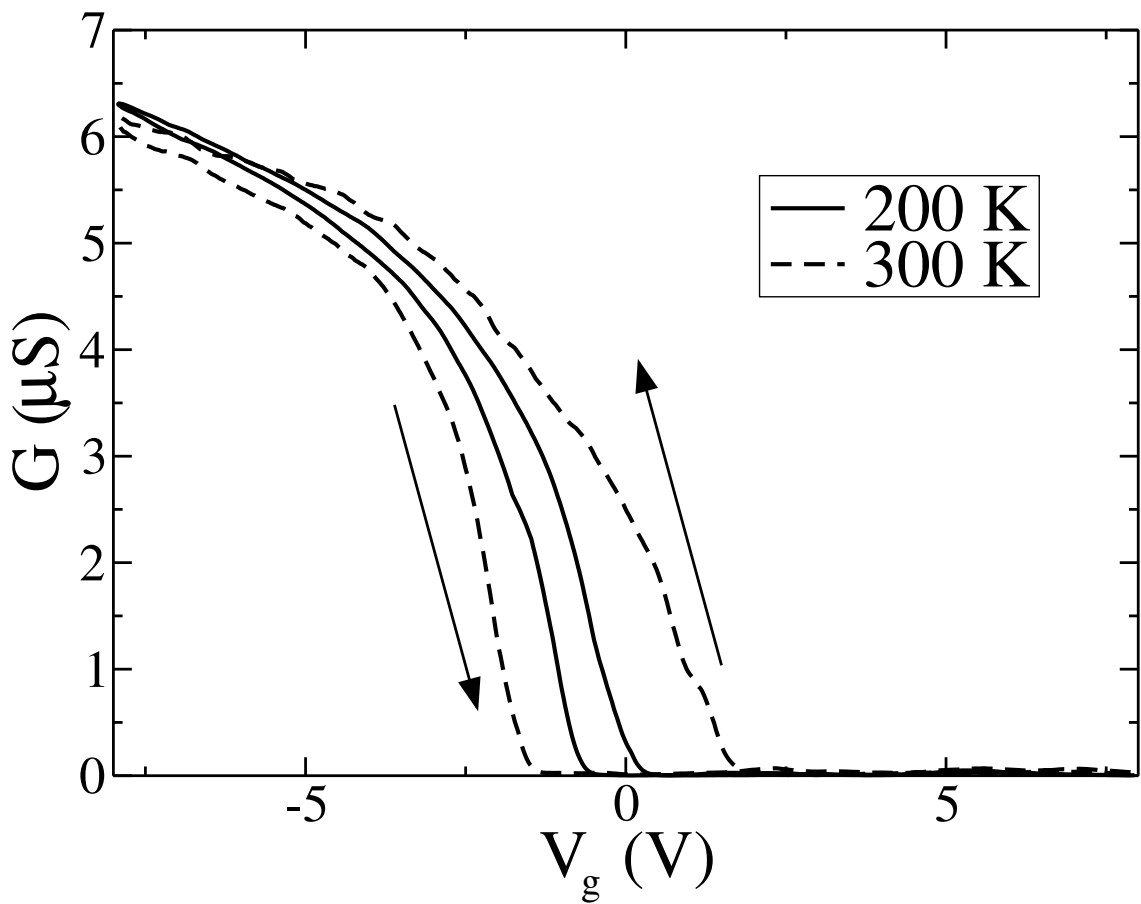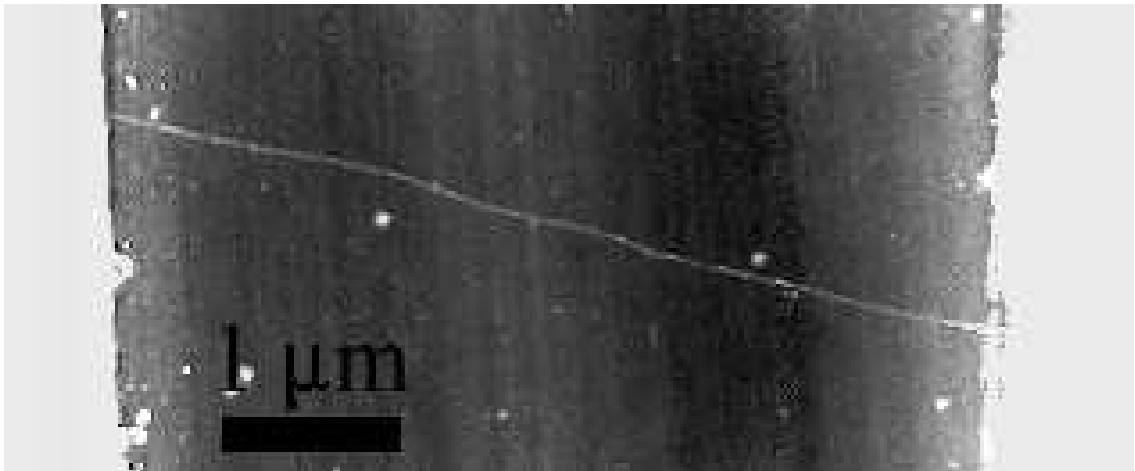
Figure 7.1: 4.8 µm long semiconducting nanotube with a diameter of 2.7 nm, device AB on sample 58: AFM-micrograph of the device and hysteresis loops in the $G(V_g)$-curve of the device at 200 K and 300 K. The data was measured with a bias voltage of 500 mV. The arrows indicate the direction in which V_g was being swept on each branch of the hysteresis. (Measurement courtesy of M. Fuhrer.)
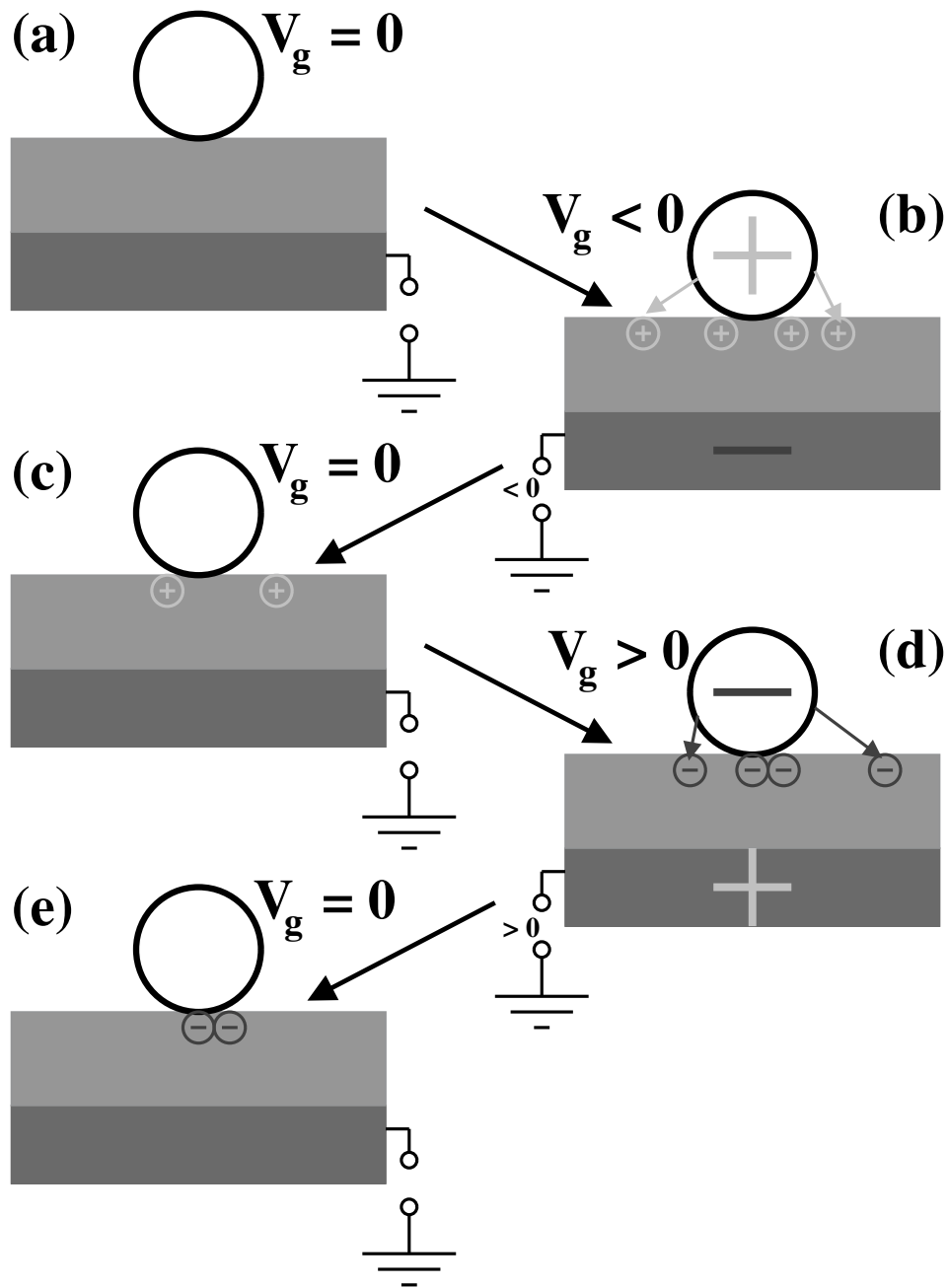
Figure 7.2: Hysteresis caused by charge injection. (a) Initial state: $V_g = 0$. (b) $V_g < 0$ applied: Positive charges from tube fill charge traps near surfaces. (c) $V_g = 0$ applied, but some of the charges remain in the traps. The tube sees an effective positive V_g. (d) $V_g > 0$: reversed situation compared to (b). Negative charges near tube at the SiO_2-surface. (e) Back to $V_g = 0$: some of the charges remain. Now the tube sees an effective negative V_g.

figure 7.1) allows conclusions to be drawn about the mechanism causing the hysteresis. Mobile charges or dipoles in the oxide would result in a hysteresis opposite to what is observed in nanotube FETs, while charge traps into which charges jump from the nanotube are consistent with the measured effects. These traps presumably are located in the gate oxide or on the surface near the nanotube [64]. Figure 7.2 illustrates this idea. Most important in this figure are parts (c) and (e). Due to the charge remaining in the charge traps the nanotube experiences an effective gate voltage that is opposite to the previously applied voltage. Although this primitive illustration assumes an equality between positive and negative trapped charges the results presented in chapter 6 suggest there to be a majority of positive charges taking effect mainly on the upward sweep of the loop.

One explanation for this behavior follows from the observations published by Kim et al. [130]. This publication investigates the hysteretic behavior of nanotube FETs and concludes that the charge traps mainly consist of water adsorbed on the SiO_2-surface partly weakly adsorbed such that it can be removed by simply putting a sample into vacuum for an extended period and partly strongly adsorbed. This strongly adsorbed water can only be removed by heating the sample in vacuum to temperatures over 200°C, which mostly removes the hysteresis.
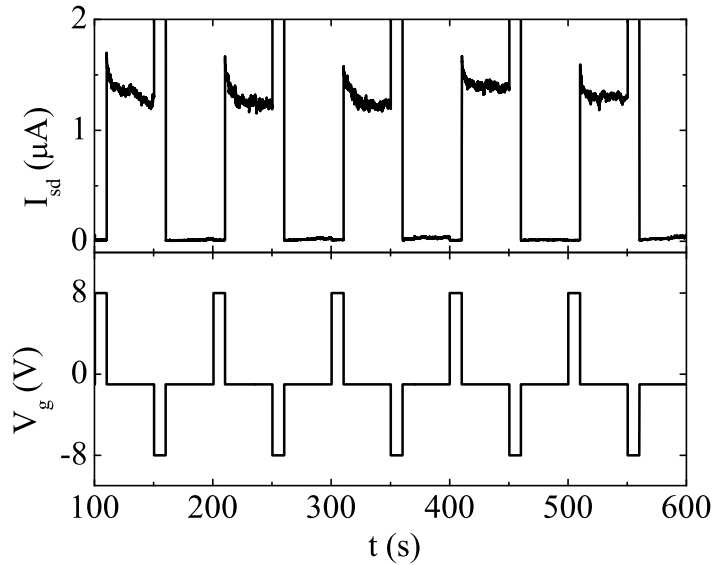
Figure 7.3: Nanotube memory at room temperature based on the hysteresis shown in figure 7.2. By applying short gate voltage pulses of ten seconds duration (bottom graph) the device can be put into the on-or off-state. While the applied bias voltage of 500 mV is constant the device current is switched on and off (top graph) depending on the sign of the preceeding pulse. (Measurement courtesy of M. Fuhrer.)

7.2   Memory Devices

7.2.1   Room-Temperature Behavior

While unwanted in most amplifier applications or in digital logic devices the hysteresis effect can be useful in memory applications. Fuhrer et al. [64] and Radosavljević et al. [69] give examples of for this kind of application. Figure 7.3 (see also figure 1 in [64]) shows such a memory application. This example uses device AB on sample 58 (see section 7.1) at room temperature. While a constant bias voltage of $V_{sd} = 500$ mV is applied across the device the gate voltage is kept at -1 V to keep the device in the center of the hysteresis loop. By applying a 10 s gate voltage pulse of $+8$ V the device can be

pushed to the upper branch of the loop (on-state), while the opposite pulse (-8 V for 10 s)

switches it to lower branch, i. e. the off-state. While an initial decay with a time constant

of several ten seconds is visible in figure 7.3 the on-and off-states remain stable for hours.

The idea of using some kind of charge trap for storage in a memory device has been used

for floating gate memory for a long time [131] with traditional FETs. The case of our

nanotube memory is particularly elegant because the memory effect is created during the

normal device fabrication.

7.2.2   Single Electron Memory

The physical concept of single-electron memory as the memory device with the smallest

possible amount of charge used has been demonstrated in several systems either with

deliberately created charge traps [132, 133, 134] or charge traps created by chance [135].

The nanotube device presented in the previous section exhibits single-electron memory

effects in a similar way. Unlike at room temperature the hysteresis loop shows discrete

and reproducible steps. Figure 7.4(a) gives an example of this behavior measured at 20 K.

While the room temperature hysteresis is caused by the reaction of the hole nanotube

to charge traps in its environment, these discrete steps are caused by the reaction of a

single defect in the nanotube to a single charge trap in its neighborhood [136]. As shown

in figure 7.4(b) this can be utilized as single-electron memory. Again a constant bias

voltage of 500 mV is applied to the device. Applying a constant V_g of -2.25 V keeps the

device between two of the steps such that short pulses in V_g (-1.5 or -3 V) can be used

to switch the device on either the upper or the lower branch corresponding to pushing a
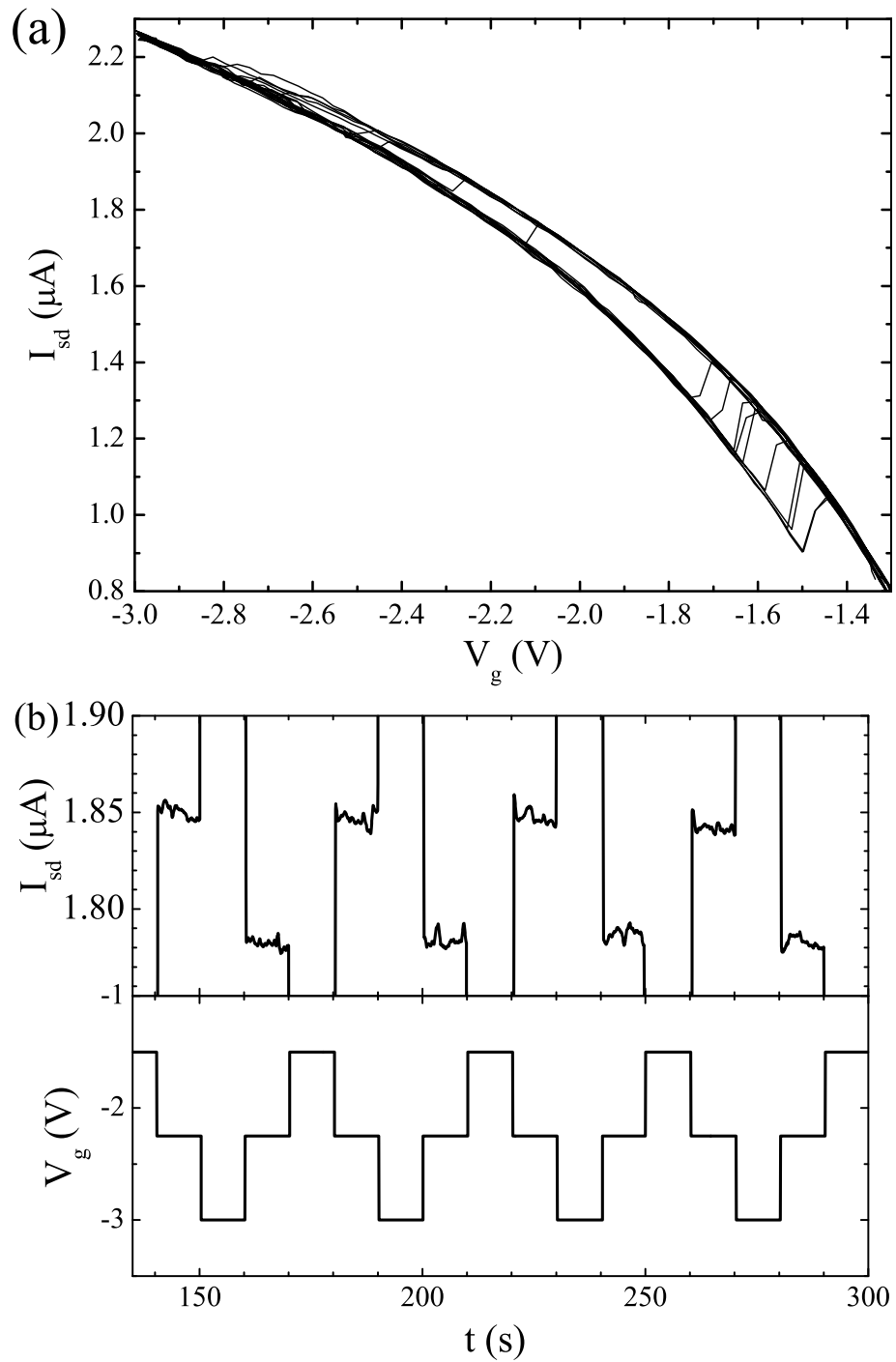
Figure 7.4: (a) Device current I_{sd} at $V_{sd} = 500\,\text{mV}$ for sample 58, device AB (see figure 7.1) measured at 20 K while sweeping V_g between $-1.3\,\text{V}$ and $-3\,\text{V}$ repeatedly. (b) Single-electron memory based on this discrete hysteresis. (Measurement courtesy of M. Fuhrer.)
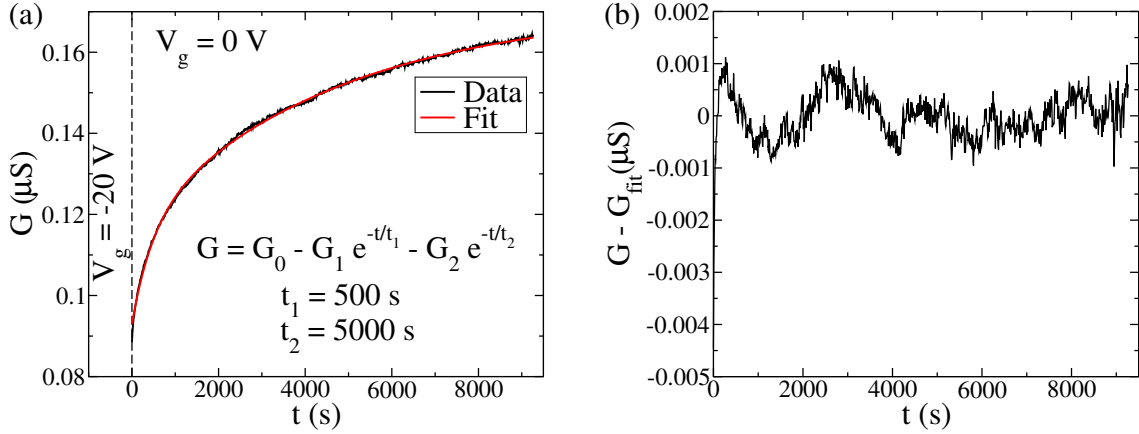
Figure 7.5: (a) Time dependence of the hysteresis at $T = 400$ K starting at negative V_g. With a bias voltage of 50 mV applied the gate voltage V_g was kept at -20 V for 5 min and then at $t = 0$ s turned off. The curve shows the slow decay of the hysteresis following an double-exponential decay with time constants of 500 s and 5000 s. Measurements with $V_g = -10$ V and $V_{sd} = 500$ mV confirm only the magnitude of these time constants. (b) Difference between fit and data. This plot does not show a systematic deviation of the fit from the data except for the initial minute of the data.

single charge into the charge trap or emptying it.

7.2.3 Time Dependence Measurements

In order to test the long term stability of a memory device we conducted measurements trying to determine the decay time for the hysteresis effect. To test whether carrying out such measurements with the available equipment was feasible we decided to investigate the decay of the hysteresis at an elevated temperature of 400 K. The measurements were carried out in our commercial low temperature probe station[1] at a pressure of better than 10^{-6} torr using sample UL7, device BC (see figure 6.2(b)). During the measurement, which used the DC-measurement scheme shown in figure 4.11, a constant bias voltage

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[1]Desert Cryogenics TT-probe station with a temperature range from 1.5 K to 400 K.
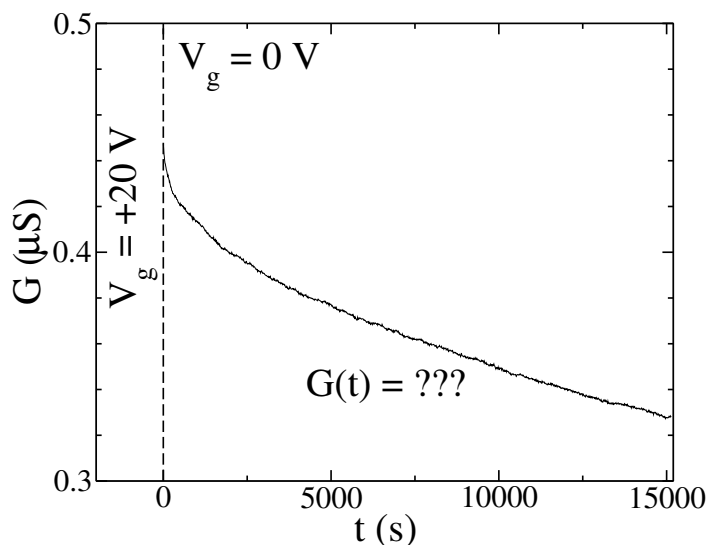
Figure 7.6: Time dependence of the hysteresis starting at positive V_g. This is the same measurement as shown in figure 7.5 but beginning at $V_g = +20\,\text{V}$. For this type of experiment we could not find a simple formula to describe the time dependence.

V_{sd} was applied across the device. A high ($\pm 10\,\text{V}$ or $\pm 20\,\text{V}$) gate voltage would then be applied for 5 min and then turned off. After turning off V_g we monitored the device current for several hours. Typical results are shown in figures 7.5 and 7.6. The decay after switching from negative V_g reproducibly followed a double-exponential decay as shown in figure 7.5. The time constants of this decay could not be reproduced well. While the smaller time constant ($t_1 = 500\,\text{s}$) was not visible in all measurements the larger constant t_2 varied from $3000\,\text{s}$ to $10{,}000\,\text{s}$. Possibly this effect critically depends on what kind of measurements were performed with the device immediately before the long term measurement was taken. The existence of two different time constants might be related to the two different ways in which water molecules are bound to the surface [130]. In the case of switching from positive V_g to $V_g = 0$ we were unable to find a simple formula to describe the decay of the hysteresis in a satisfactory manner.
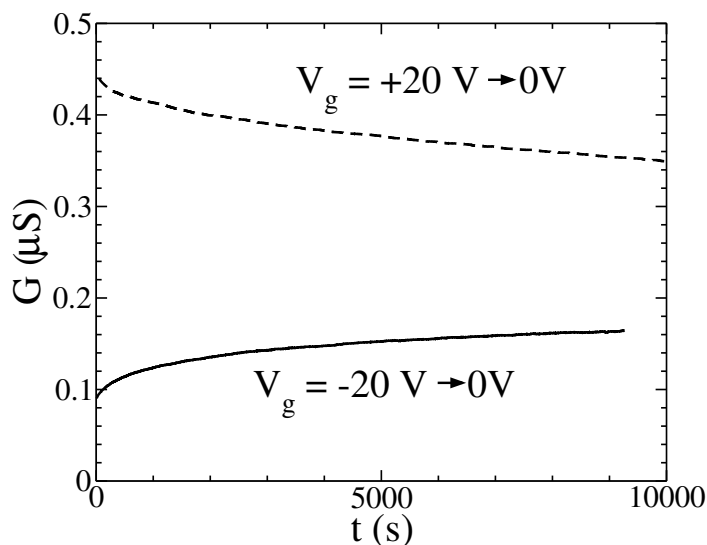
Figure 7.7: Comparison of the measurements shown in figures 7.5 and 7.6. Even after 9000 s the hysteresis effect does not decay completely, even at a temperature of 400 K. This comparison suggests a decay time for the hysteresis effect that could easily be orders of magnitude larger than the time scale investigated here.

A comparison of both types of measurements is given in figure 7.7. It is obvious that at 400 K, which is the highest temperature accessible in our probe station, the hysteresis will not decay within several 10,000 s. (One day has 86,400 s!) Considering this and the fact that there does not seem to be one simple process causing the hysteresis we did not pursue these experiments further. However, in a system that can reach temperatures high enough to remove water adsorbed on the surface this type of experiment might be more promising.

Concerning the application of nanotubes as memory elements these long term experiments show that even at elevated temperatures the lifetime of the content of such a nanotube memory element would be hours if not days making them suitable as at least semi-permanent storage devices.

Chapter 8

Conclusions

This work reviews the synthesis of nanotubes with lengths from a few hundred nanometer to several hundreds of micrometers using CVD-techniques. With these nanotubes we were able to fabricate devices. For the first time these devices allow for measuring the carrier mobility in a nanotube on Ohmically contacted devices long enough to be clearly in the regime of diffusive conductance.

Low temperature measurements of Coulomb blockade effects as well as room temperature conductance measurements on nanotube devices longer than $300\,\mu m$ agree in showing a mean free path of several micrometers in semiconducting nanotubes.

The conductance measurements on these long devices show outstanding mobilities that exceed those of all other semiconductors at room temperature in good agreements with theoretical predictions. While largely independent of the temperature the mobility shows a power law dependence on the gate voltage and hence on the carrier density in the nanotube. These two findings call for further studies to verify them and ultimately determine the dominant scattering mechanisms in nanotubes.

In the last chapter I present measurements on the temperature and time dependence of hysteresis effects in nanotube FETs. While these measurements are clearly not complete they show an interesting picture suggesting that the hysteresis in nanotube devices is governed by several different types of charge traps with different time constants that, even at elevated temperatures of 400 K, reach up to hours. Just as there has been a significant amount of research on hysteresis effects in silicon devices there will have to be more research about these hysteresis effects in nanotubes, in order for them to be useful for digital electronics applications.

Appendix A

Abbreviations

AFM **A**tomic **F**orce **M**icroscope *or* **A**tomic **F**orce **M**icroscopy

CNT **C**arbon **N**ano**t**ube

CVD **C**hemical **V**apor **D**eposition

DCE **Di**chloro**e**thane

DOS **D**ensity **O**f **S**tates

FESEM **F**ield-**E**mission **SEM**

FET **F**ield-**E**ffect **T**ransistor

IPA **I**so-**P**rop**a**nol or 2-Propanol

MIBK **M**ethyl **I**so **B**utyl **K**etone

MMA **M**ethyl **M**eth**a**crylate)

MOSFET **M**etal **O**xide **S**emiconductor **FET**

MWNT **M**ulti-**W**alled **N**ano**t**ube

PMMA **P**oly(**M**ethyl **M**eth**a**crylate)

SEM **S**canning **E**lectron **M**icroscopy

SET **S**ingle **E**lectron **T**ransistor

STM **S**canning **T**unneling **M**icroscopy

STS **S**canning **T**unneling **S**pectroscopy

SWNT **S**ingle-**W**alled **N**ano**t**ube

TEM **T**ransmission **E**lectron **M**icroscopy

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