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Comparative Analysis of Two Novel Passive Harmonic Suppression Circuits for Industrial Applications

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ABSTRACT

The 12-pulse diode rectifier (12-PDR) fails to comply with the limits of total harmonic distortion (THD) of supply current to be less than 5% specified in the IEEE Standard 519. Increasing the number of pulses further improves various power-quality indexes while imposing an additional cost of adding different converters and growing system complexity. Passive harmonic suppression circuits (PHSCs) have been observed to be a viable and cost-effective solution to improve the THD of AC-mains current at a reduced cost. PHSCs increase the number of rectification pulses without leading to significant changes in the installations and yield harmonic reduction in both AC and DC sides. This paper presents a comparative analysis of two novel PHSCs connected at the DC-bus of 12-PDR. One is PHSC-I based on four tapped reactors (FTRs) and four auxiliary diodes; the other is PHSC-II, with two tapped reactors (TTRs) and two auxiliary diodes. The operation modes and optimal parameters of both PHSCs are analyzed with similar inputs (AC side) and outputs (DC side). Both 12-PDR are connected to the same AC source as input, and both PHSCs supplied similar DC loads at their outputs, thus leading to an accurate and fair comparison between the two PHSCs. The results show that the input current THD of a 12-PDR with PHSC-II is lower than that of a PHSC-I and lower than existing passive harmonic suppression circuits. In addition, PHSC-II leads to lower connection losses, current stress, and cost than PHSC-I, so in industrial applications that require low input current THD, low connection losses/current stress, and low cost, PHSC-II is highly recommended.

I. Introduction

The application of rectification systems in the high-power industry is increasing, such as in DC-arc furnaces, plasma power supplies, graphite electrolysis plants, and electric aircraft [1]. Multi-pulse rectifiers (MPRs) have received more attention thanks to their straightforward configuration and high reliability and efficiency compared to DC generators. MPRs convert the alternative to direct voltage with a negligible ripple on a rectifier bridge and a phase-shifting transformer. Extensive research has been conducted to suppress input current harmonic distortion using MPR in industrial applications [1-2]. The current THD in the buck-boost PFC rectifier [3] and six-pulse rectifier [4] are 5.5% and 3.3%, respectively. The theory of 12-pulse rectification was developed long ago and played an irreplaceable role in multi-pulse basic research [5]. The first method is to adopt multi-phase transformers with multi-pulse diode bridges. Theoretically, this operation increases the number of MPRs and thus reduces the input current harmonic distortion [6-7]. Yet, the complex structure of multi-phase transformers and the high number of diodes employed are some of the disadvantages of this method [8-9]. The second method to reduce the input harmonic distortion is utilizing the multi-tapped interphase reactor (IPR) [10]. If the IPR existing in the

conventional 12-pulse rectifier is replaced with a two-tapped IPR and two auxiliary diodes, the performance of the rectifier will be upgraded to 24 pulses [11]. It should be noted that the current flow through these two auxiliary diodes is equal to the load current, increasing the diodes' conduction losses. The third method proposed recently is adding passive harmonic suppression circuits (PHSC) [12]. This method has two windings, the primary winding, including unconventional IPR (UIPR), is similar to the multi-tapped IPR and is connected to diode bridges, and the secondary winding is connected to a passive harmonic suppression circuit [13].

PHRCs are generally classified into two categories, single and dual PHRCs, as shown in Fig. 1. Basically, the main difference between various PHRCs is the configuration of the interphase transformer and the number of auxiliary diodes. In single PHRCs (tapped IPT [11], single-phase full-wave rectifier [12], single-phase diode-bridge rectifier [13]), auxiliary diodes are connected only to the secondary side of the interphase transformer. Auxiliary diodes are connected to both the primary and secondary sides of the interphase transformer in the following structures: double PHRCs (two single-phase full-wave rectifiers) [14], single-phase diode-bridge rectifiers and single-phase full-wave rectifiers [15], two-tapped IPT and single-phase full-wave rectifier [16], and two-tapped IPT and single-phase diode-bridge rectifier [17]. In [18], the classification of PHSC types is presented, and in [19], PHSC types are compared in terms of technical indicators, such as the ability to reduce input current harmonic distortion, efficiency, and economic indicators, such as weight, kVA rating, and cost.

This paper presents two novel harmonic suppression circuits (PHSC-I and PHSC-II) in 24-PDR and compares them in terms of technical and economic indicators. The PHSC-I consists of one FTR and four auxiliary diodes, and the PHSC-II includes two TTRs and two auxiliary diodes. Each of PHSC-I and PHSC-II can optimally operate in different applications in high-power rectification systems. The paper's primary purpose is to present two novel PHSCs and describe the performance and comparative analysis of these two circuits from technical and economic aspects. The performance of PHSC-I and PHSC-II in the DC-link of 12-PDR is described in Sections 2 and 3, respectively. Then the technical and economic comparison of PHSC-I and

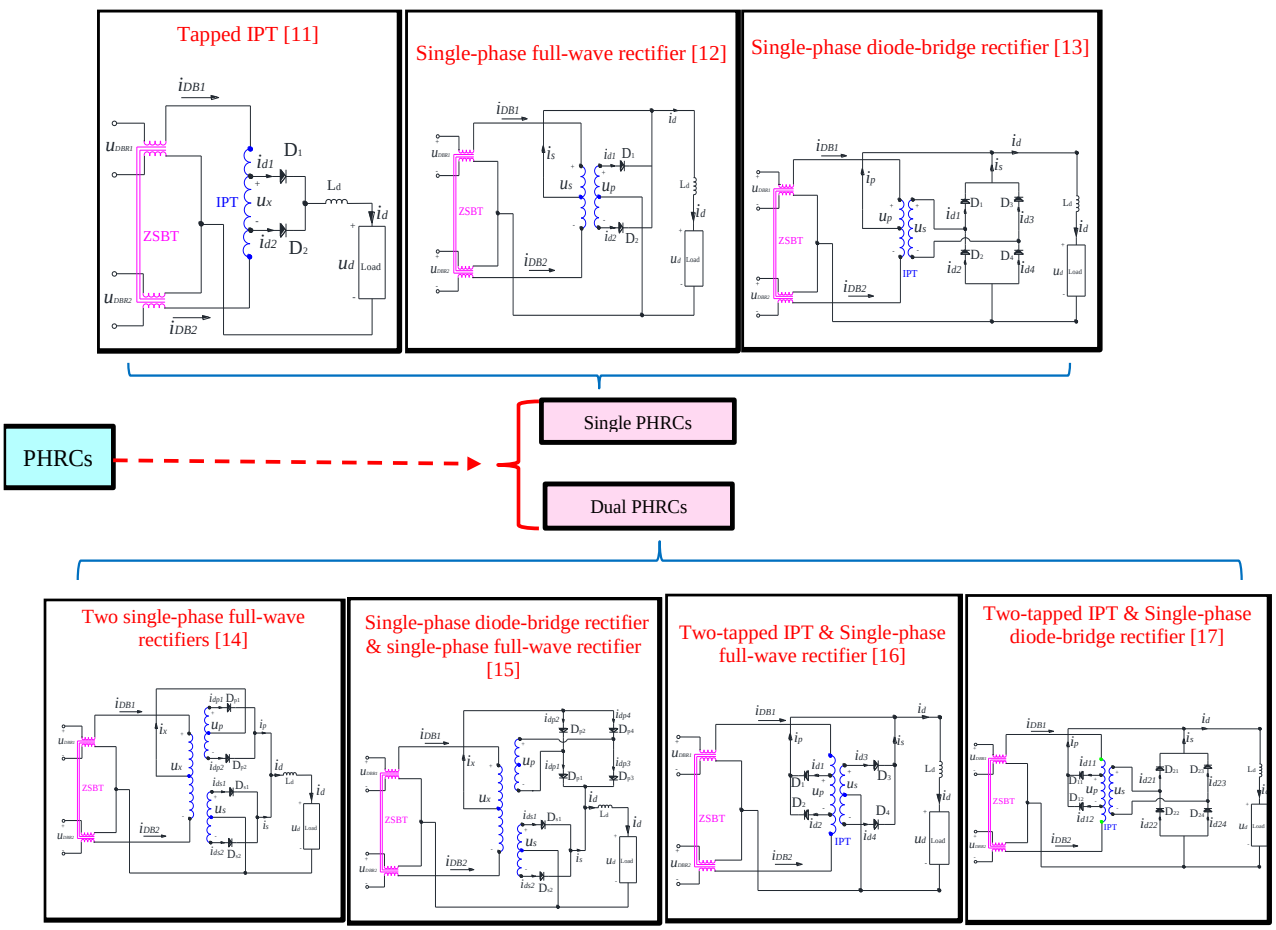

Fig. 1. Conventional PHSCs classification.

PHSC-II is presented in Section 4. Some conclusions are given in Section 5.

II. 12-PDR with PHSCs

As shown in Fig. 2, the 12-PDR with PHSCs consists of two main parts:

- A conventional 12-PDR
- Two novel PHSCs (PHSC-I or PHCS-II)

The 12-PDR comprises a tapped star-connected 6-phase autotransformer to produce two sets of 3-phase voltages (v_{a1} to v_{d1} and v_{a2} to v_{d2}) with a 30˚ phase shift. These two sets of the 3-phase voltage are converted to a 12-pulse waveform bypassed through two 6-pulse DBRs. To increase the 12-pulse waveform to the 24-pulse waveform, the PHSC is connected to the DC bus of these two 6-pulse DBRs. The 12-PDR with PHSC-I consists of two 6-pulse DBRs, and zero-sequence blocking transformer (ZSBT), an FTR, and two auxiliary diodes. But, the 12-PDR with PHSC-II consists of two 6-pulse DBRs, two TTRs, and two auxiliary diodes. ZSBT ensures the independent operation of DBRs, but 12-PDR with PHSC-II does not require ZSBT.

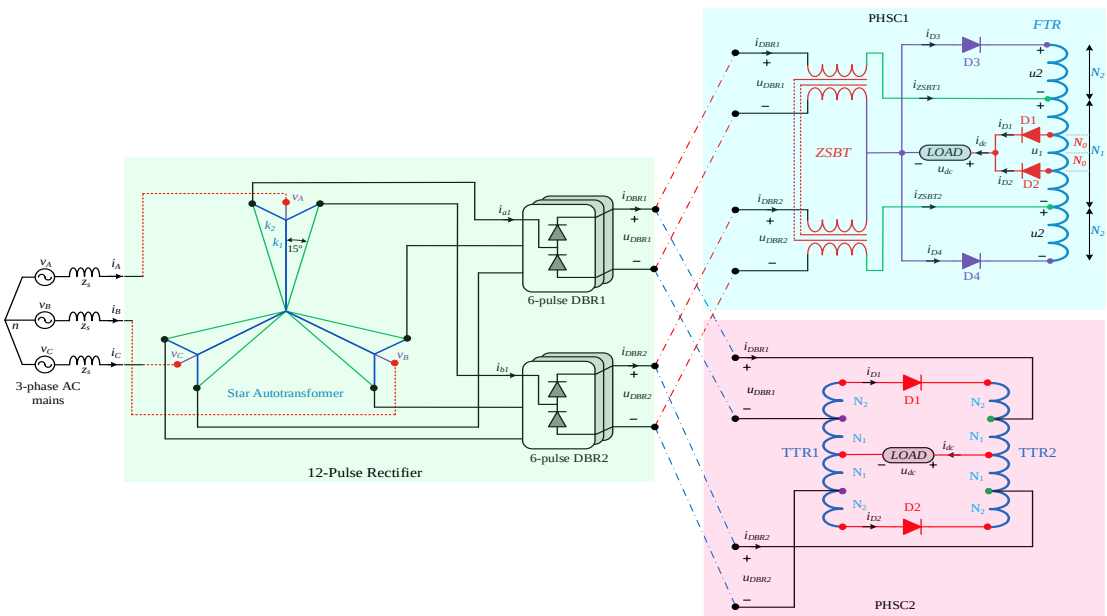

Fig. 2. 12-DBR with two novel PHSCs

A. Circuit Configuration and Working Principle of the PHSC-I

As indicated in Fig. 2, the 24-PDR comprises a conventional 12-PDR and PHSC-I. The PHSC-I is connected to the DC bus of the conventional 12-PDR, two 6-pulse DBRs, to generate a 24-pulse waveform. According to Fig. 3, the PHSC-I contains a ZSBT and a Four Tapped Reactor (FTR) with four auxiliary diodes. Output terminals of DBR1 and DBR2 are connected to ZSBT. Diodes D1 and D2 are connected to FTR1 with the N_1 turn on the winding. The diodes D3 and D4 are connected to the FTR2 with N_2 turn on the winding.

The following equations describe tap ratios m and k for this FTR:

$$k = \frac{N_0}{N_1} \quad (1)$$

$$m = \frac{N_2}{N_1} \quad (2)$$

The operation of the 24-PDR depends on the relation between the voltages across the windings (N_1 and N_2) of the FTR (u_1 and u_2) and output voltage (u_{dc}). According to the relation between u_{dc}, u_1, and u_2, the 24-PDR has four operation modes. Table 1 describes the operating principle of the PHSC-I indicated in Fig. 3 in four modes based on the relationship between load voltage u_{dc} and voltages u_1 and $(u_2 + (k+0.5)u_1)$. These four modes are described in Table 1 through KirchhOFF's Voltage Law (KCL) and KirchhOFF's Current Law (KCL) based on the status of diodes and DBRs. In this table, the ON and OFF status of diodes means forward bias (conducting) and reverse bias (not conducting); ON for DBRs means being active, and OFF means being in the reverse bias.

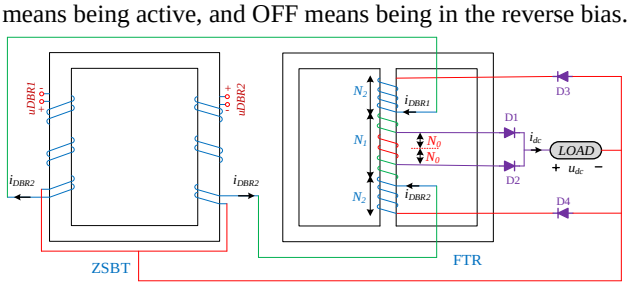

Fig. 3. Structure of the PHSC-I

In mode 1, D3 and D4 are OFF, so both u_2 are zero. The load is supplied by DBR1 (iDBR1) and DBR2 (iDBR2) output currents through D1. By applying KCL

$$i_{dc} = i_{DBR1} + i_{DBR2} \quad (3)$$

The FTR equation for MMF is expressed as

$$i_{DBR1}(0.5N_1 - kN_1) = i_{DBR2}(0.5N_1 + kN_1) \quad (4)$$

Using (3) and (4), the currents i_{DBR1} and i_{DBR2} are determined by the following equations:

$$\begin{cases} i_{DBR1} = (0.5 + k)i_{dc} \\ i_{DBR2} = (0.5 - k)i_{dc} \end{cases} \quad (5)$$

And also, applying KVL gives:

$$u_{dc} = u_{DBR1} - (0.5 - k)u_1 \quad (6)$$

$$u_{dc} = u_{DBR2} + (0.5 + k)u_1 \quad (7)$$

$$u_1 = u_{DBR2} - u_{DBR1} \quad (8)$$

In mode 2, the DBR2 is OFF since u_2 is higher than (v_{a2} to v_{d2}), so DBR1 supplies the load through D1. In this mode, D4 adds N_2 to N_1 to keep voltage and current in the fixed range. Here, applying KCL gives:

$$i_{dc} = i_{DBR1} + i_{D4} \quad (9)$$

The MMF equation of the FTR is presented as follows:

$$i_{DBR1}(0.5N_1 - kN_1) = i_{D4}(N_2 + 0.5N_1 + kN_1) \quad (10)$$

Using (8) and (9), the currents i_{DBR1} and i_{D4} are written as below:

$$i_{DBR1} = \frac{k+m+0.5}{m+1} i_{dc} \quad (11)$$

$$i_{D4} = \frac{0.5-k}{m+1} i_{dc} \quad (12)$$

The relations among u_{DBR1}, u_{DBR2}, u_{dc}, and u_1 are summarized as follows:

$$u_{dc} = \frac{k+m+0.5}{m+1} u_{DBR1} \quad (13)$$

$$u_{DBR2} = \frac{m}{m+1} u_{DBR1} \quad (14)$$

$$u_{FTR1} = \frac{1}{m+1} u_{DBR1} \quad (15)$$

In mode 3, similar to mode 1, D3 and D4 are OFF, so both u_2 are zero, and the load is supplied by DBR1 (i_{DBR1}) and DBR2 (i_{DBR2}) output currents through D2. Applying KCL gives:

$$i_{dc} = i_{DBR1} + i_{DBR2} \quad (16)$$

The MMF equation in N_1 is written as follows:

$$i_{DBR1}(0.5N_1 + kN_1) = i_{DBR21}(0.5N_1 - kN_1) \quad (17)$$

Using (15) and (16), i_{DBR1} and i_{DBR2} can be written as

$$i_{DBR1} = (0.5 - k)i_{dc} \quad (18)$$

$$i_{DBR2} = (0.5 + k)i_{dc} \quad (19)$$

The following relationship is established between u_{DBR1}, u_{DBR2}, u_{dc}, and u_1:

$$u_{dc} = u_{DBR1} - (0.5 + k)u_1 \quad (20)$$

$$u_{dc} = u_{DBR2} + (0.5 - k)u_1 \quad (21)$$

$$u_1 = u_{DBR1} - u_{DBR2} \quad (22)$$

In mode 4, the DBR1 is OFF because -u_2 is higher than (v_{a1} to v_{d1}), so just DBR2 supplies the load through D2. In this mode, D3 adds N_2 to N_1 to keep voltage and current in the fixed range. Here, applying KCL gives:

$$i_{dc} = i_{DBR2} + i_{D3} \quad (23)$$

The following equation expresses the MMF equation of the FTR:

$$i_{DBR2}(0.5N_1 - kN_1) = i_{D3}(N_2 + 0.5N_1 + kN_1) \quad (24)$$

Using (23) and (24), the currents i_{DBR2} and i_{D3} are determined as below:

$$i_{DBR2} = \frac{k+m+0.5}{m+1} i_{dc} \quad (25)$$

TABLE 1
WORKIND MODEs OF THE PHSC-I

#	KVL	KCL	Diode1	Diode2	Diode3	Diode4	DBR1	DBR2
1	$u_1>0$ & $u_2+(k+0.5)\,u_1<u_{dc}$	$i_{DBR1} + i_{DBR2} = i_{dc}$	ON, $i_{D1} > 0$	OFF, $i_{D2} = 0$	OFF, $i_{D3} = 0$	OFF, $i_{D4}= 0$	ON, $i_{D1}>0$	ON, $i_{D1} > 0$
2	$u_1>0$ & $u_2+(k+0.5)\,u_1>u_{dc}$	$i_{DBR1} + i_{D4} = i_{dc}$	ON, $i_{D1} > 0$	OFF, $i_{D2} > 0$	OFF, $i_{D3} = 0$	ON, $i_{D4} > 0$	ON,$i_{D1} > 0$	OFF, $i_{D1} = 0$
3	$u_1<0$ & $-u_2-(k+0.5)\,u_1<u_{dc}$	$i_{DBR1} + i_{DBR2} = i_{dc}$	OFF, $i_{D1} < 0$	ON, $i_{D2} < 0$	OFF, $i_{D3} = 0$	OFF, $i_{D4}= 0$	ON,$i_{D1} > 0$	ON, $i_{D1} > 0$
4	$u_1<0$ & $-u_2-(k+0.5)\,u_1>u_{dc}$	$i_{D3} + i_{DBR2} = i_{dc}$	OFF, $i_{D1} < 0$	ON, $i_{D2} < 0$	ON, $i_{D3} < 0$	OFF, $i_{D4}= 0$	OFF,$i_{D1} = 0$	ON, $i_{D1} > 0$

$$i_{D3} = \frac{0.5-k}{m+1} i_{dc} \quad (26)$$

The relations among u_{DBR1}, u_{DBR2}, u_{dc}, and u_1 are determined as follows:

$$u_{dc} = \frac{k+m+0.5}{m+1} u_{DBR2} \quad (27)$$

$$u_{DBR2} = \frac{m}{m+1} u_{DBR2} \quad (28)$$

$$u_{FTR1} = -\frac{1}{m+1} u_{DBR2} \quad (29)$$

The optimal tap ratios of the FTR (i.e., m and k) are obtained subject to minimizing the input current %THD. Therefore, the critical point of designing the PHSC-I is determining the optimal FTR turns ratio, significantly decreasing the input current %THD. These values could be determined based on the try-and-error method using MATLAB simulation, which is set (k=0.25 and m=6.5), resulting in an input current THD of 1.72%. The designed PHSC-I has been evaluated using MATLAB simulation in situations where the load voltage is 380V (50Hz) and the full load power is 10kW. Fig. 4 and Fig. 5 indicate the simulation

results, the waveform of the primary voltage, and the current of the 12-PDR with PHSC-I, respectively. The 12-PDR with PHSC-I output voltage waveform is shown in Fig. 4(a), and the FTR1 and FTR2 voltage waveforms are shown in Fig. 4(b) and Fig. 4(c), respectively. As mentioned before, the relationship between these voltages determines the operating modes of the PHSC-I. The ZSBT voltage waveform is also shown in Fig. 4(d).

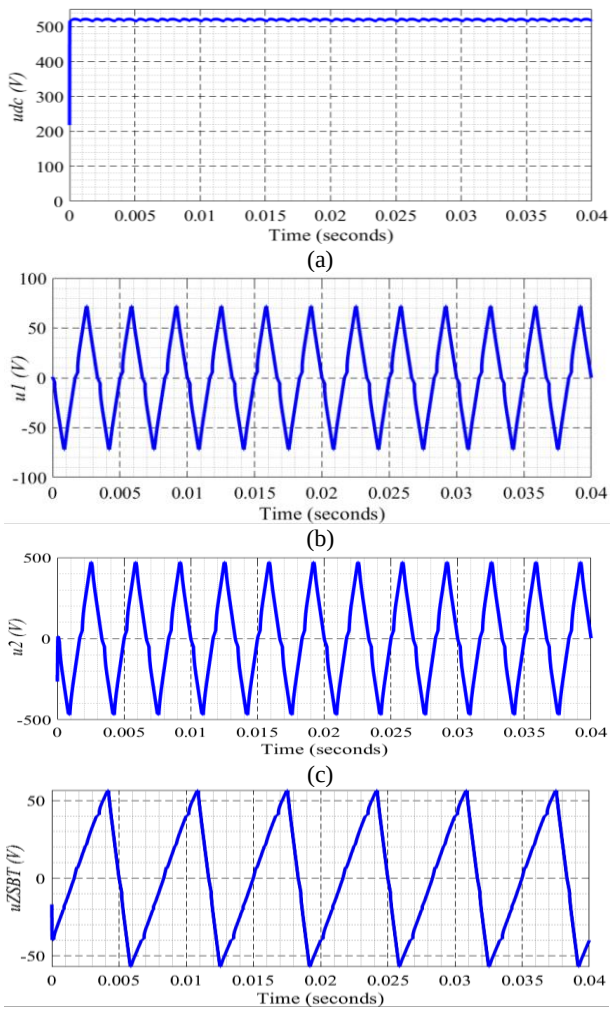

Fig. 4. Main voltage waveforms of the 12-PDR with PHSC-I. (a) u_{dc}, (b) u_1, (c) u_2, (d) u_{ZSBT}

The 12-PDR with PHSC-I output current waveform is shown in Fig. 5(a). The currents flowing through the auxiliary diodes (i_{D1} and i_{D2}) are shown in Fig. 5(b), and the currents flowing through the auxiliary diodes (i_{D3} and i_{D4}) are shown in Fig. 5(c). As can be seen, a significant part of the load current passes through the D1 and D1, and the current passing through the auxiliary diodes D3 and D4 are minimal compared to the load current, which leads to a reduction in conduction losses and the current stress of the auxiliary diodes D3 and D4.

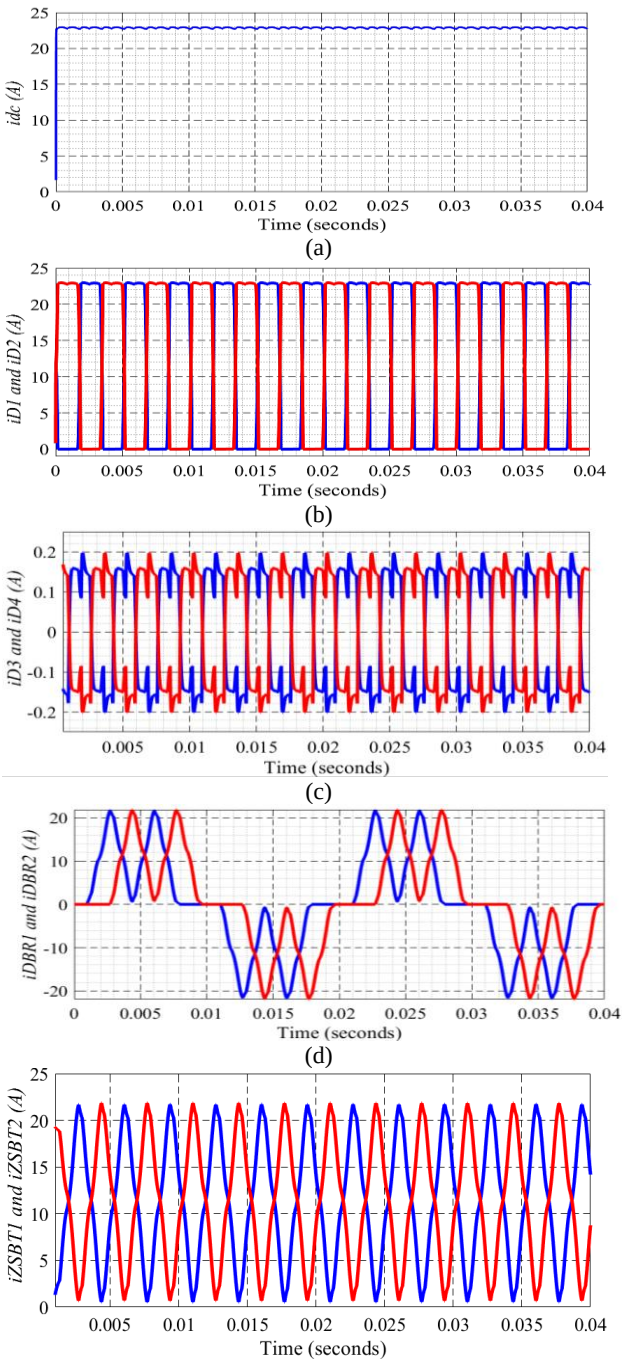

Fig. 5. Main current waveforms of the 12-PDR with PHSC-I. (a) i_{dc}, (b) i_{D1} and i_{D2}, (c) i_{D3} and i_{D4}, (d) i_{DBR1} and i_{DBR2}, (e) i_{ZSBT}

The input currents of these two 6-pulse DBRs are shown in Fig. 5(d), and the ZSBT current of the 12-PDR with PHSC-I is demonstrated in Fig. 5(e). These figures confirm the high performance of the 12-PDR with PHSC-I in reducing the harmonic distortions of the input current, thus providing a fully sinusoidal current.

B. CIRCUIT CONFIGURATION AND WORKING PRINCIPLE OF THE PHSC- II

According to Fig. 6, The PHSC-II consists of two TTRs and two auxiliary diodes. Each TTR is hooked up in the positive and negative polarity of 6-pulse DBRs. Then, the two TTRs are connected through two auxiliary diodes. Finally, the two TTRs are connected to the load. Table 2 describes the working principle of the PHSC-II, indicated in Fig. 6, in three modes based on the relationship between load voltage u_{dc} and voltage (u_{TTR1}+u_{TTR2}). These three modes could be described based on the status of diodes and DBRs through KCL and KVL.

In mode 1, D_1 and D_2 are OFF, and the 24-PDR behaves as a conventional 12-PDR. From the KCL and Magnetic Motive Force (MMF) balance of the windings in the two TTRs, the relationship among the output current of DBR1, the output current of DBR2, and the load current are given as follows:

$$i_{DBR1} = i_{DBR2} = \frac{1}{2} i_{dc} \quad (30)$$

In mode 2, D_2 and DBR1 are ON. Meanwhile, the DBR2 is turned OFF.

TABLE 2
WORKIND MODEs OF THE PHSC-II

#	KVL	KCL	Diode 1	Diode 2	DBR 1	DBR 2
1	$\lvert u_{TTR1} + u_{TTR2}\rvert < u_{dc}$	$i_{DBR1} + i_{DBR2} = i_{dc}$	OFF, $i_{D1} = 0$	OFF, $i_{D2} = 0$	On, $i_{DBR1} > 0$	On, $i_{DBR2} > 0$
2	$u_{TTR1} + u_{TTR2} > u_{dc}$	$i_{DBR1} + i_{D2} = i_{dc}$	OFF, $i_{D1} = 0$	On, $i_{D2} > 0$	On, $i_{DBR1} > 0$	OFF, $i_{DBR2} = 0$
3	$-(u_{TTR1} + u_{TTR2}) > u_{dc}$	$i_{D1} + i_{DBR2} = i_{dc}$	On, $i_{D1} > 0$	OFF, $i_{D2} = 0$	OFF, $i_{DBR1} = 0$	On, $i_{DBR2} > 0$

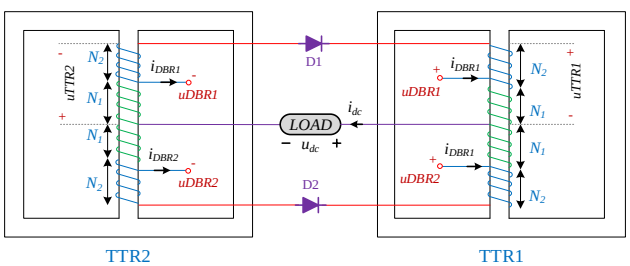

Fig. 6. Structure of the PHSC-II

$$\begin{cases} i_{DBR1} = \frac{2m}{2m+1} i_d \\ i_{D2} = \frac{1}{2m+1} i_d \end{cases} \quad (31)$$

In mode 3, the diodes that were ON in mode 2 now turn OFF, and vice versa. In terms of KCL and the MMF of the two TTRs, the currents i_{DBR2} and i_{D1} are given as follows:

$$\begin{cases} i_{DBR2} = \frac{2m}{2m+1} i_d \\ i_{D1} = \frac{1}{2m+1} i_d \end{cases} \quad (32)$$

where m is the turns ratio of the TTR and equals to $(N_1+N_2)/2N_1$ (as shown in Fig. 6). The optimal turns ratio of the TIPR (i.e., m) is determined using the try and error method subject to minimize %THD of the input current. The TTR turns ratio of 7.90 results in an input current THD of 0.67%.

Figs. 7 and 8 show the primary voltage and current of the 12-PDR with the PHSC-II. The rectifier output voltage waveform is shown in Fig. 7(a), and the TTR voltage waveform is shown in Fig. 7(b). As mentioned before, the relationship between these voltages determines the operating modes of the PHSC-II. The 6-pulse DBRs output voltage is shown in Fig. 7(c). According to this figure, by using PHSC-II in 12-PDR, the operational independence of these two DBRs is confirmed without needing ZSBT. Fig. 7(d) shows the output waveform of a 6-phase autotransformer, which consists of two series of 3-phase voltages with 30-degree displacement. These two series of 3-phase voltages supply two 6-pulse diode bridges (DBR1 and DBR2) to achieve a 12-PAR. The rectifier output current waveform is shown in Fig. 8(a). The currents flowing through the auxiliary diodes (i_{D1} and i_{D2}) are shown in Fig. 8(b), and the current flowing through the DBRs (i_{DBR1} and i_{DBR2}) is shown in Fig. 8(c). Based on Fig. 8(b), a significant part of the load current passes through the TTR, and the current passing through the auxiliary diodes (i_{D1} and i_{D2}) is minimal compared to the load current, which leads to a reduction in conduction losses and the current stress of the auxiliary diodes.

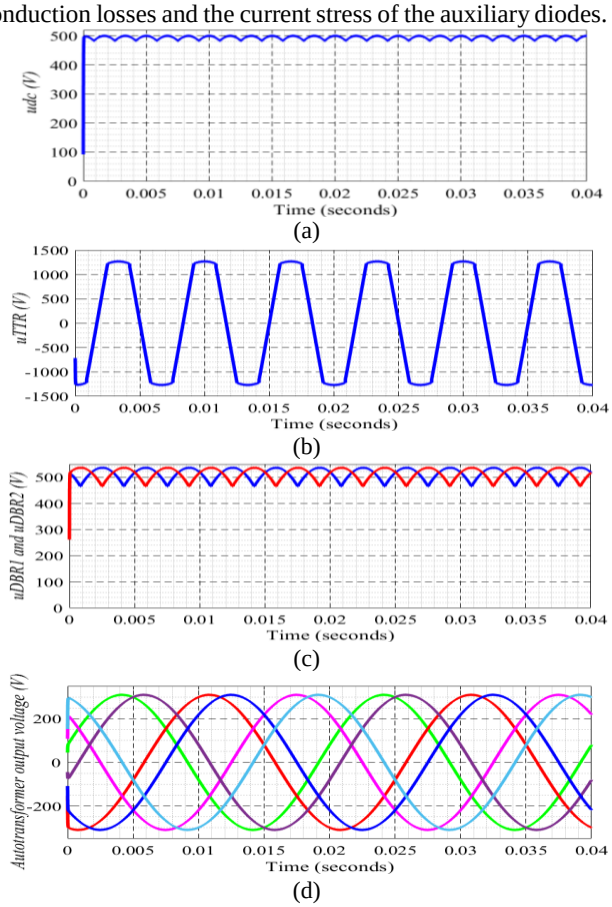

Fig. 7. Main voltage waveforms of the 12-PDR with the PHSC-II. (a) u_{dc}, (b) u_{TTR}, (c) u_{DBR1} and u_{DBR2}, (d) autotransformer voltage

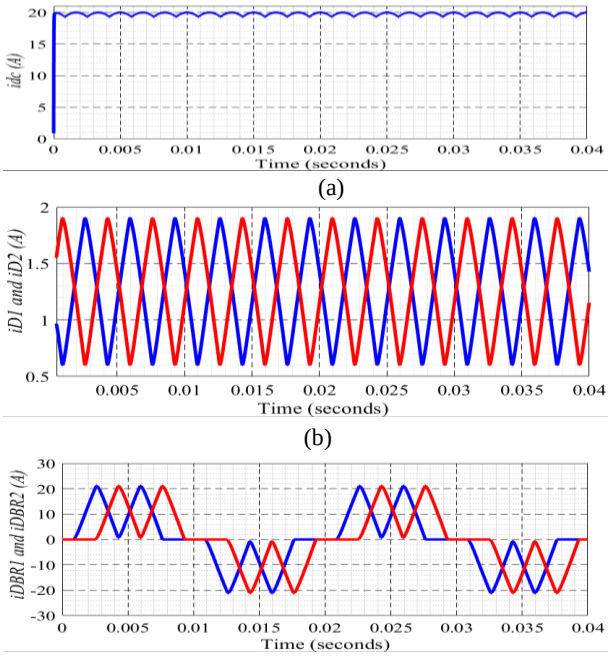

Fig. 8. Main current waveforms of the 12-PDR with the PHSC-II. (a) i_{dc}, (b) i_{D1} and i_{D2}, (c) iDBR1 and i_{DBR2}

III. Comparison of PHSC-I with PHSC-II

Ref. [20] presents an electrical and magnetic comparison between two structures of 10-phase autotransformers. With this approach to clarifying the main characteristics of the two novel PHSCs, a technical and economic comparison is performed between the PHSC-I and the PHSC-II. Comparison of technical indicators includes calculating %THD input current of 12-PDR with PHSCs under different load conditions, according to standard requirements IEEE-519. Fig. 9 shows the input current/voltage and their harmonic spectrums of the 12-PDR with (a) PHSC-I and (b) PHSC-II. The input current THD is calculated under 380V line-to-line voltage and 50Hz frequency, and a source reactance of 3mH and considering a load resistance of 10kW. After using the PHSC-I in the 12-PDR, the simulated THD of the current and voltage are about 1.72% and 0.57%, respectively.

Also, using the PHSC-II in the 12-PDR, the simulated THD of the current and voltage are about 0.67% and 0.31%, respectively. Therefore, the harmonic reduction ability of the PHSC- II is significant. Although the input current THD in both 12-PDR structures with PHSC-I and PHSC-II is less than 5%, considering the harmonic components according to Fig. 10, the harmonic components are slightly more than the requirements of IEEE-519 in 12-PDR with PHSC-I in the range of 23-35 and 35-50 [21]. Instead, 12-PDR with PHSC-II fully complies with the requirements of the IEEE-519 standard for both input current THD and amplitude of harmonic components.

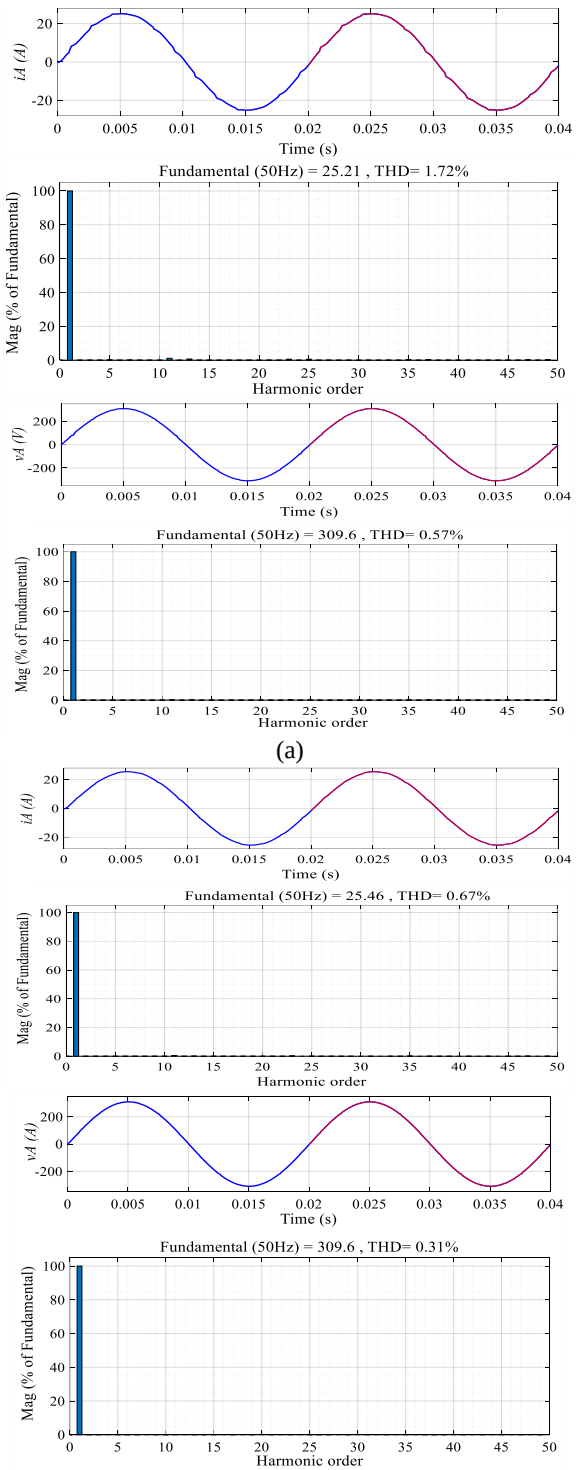

Fig. 9. Input current/ voltage waveform and their harmonic spectrums of the 12-PDR with (a) PHSC-I and (b) PHSC-II

TABLE 3
THE VOLTAGE/CURRENT OF WINDINGS AND RATING OF TWO NOVEL PHSCs UNDER 10 KVA

Topologies	C	RMS values	W_1	W_2	W_3	W_4	W_5	VA rating	Total VA rating
PHSC-I	ZSBT	V_{rms} (V)	34.44	34.44	34.44	34.44		442.55	697.58
		I_{rms} (A)	12.85	12.85	12.85	12.85			
	FTR	V_{rms} (V)	291.2	11.18	21.94	11.18	291.2	255.03	
		I_{rms} (A)	0.17	12.85	5.64	12.85	0.17		
PHSC-II	TTR1	V_{rms} (V)	540.7	34.96	34.96	540.7		563.46	1126.92
		I_{rms} (A)	1.34	11.51	11.51	1.34			
	TTR2	V_{rms} (V)	540.7	34.96	34.96	540.7		563.46	
		I_{rms} (A)	1.34	11.51	11.51	1.34			

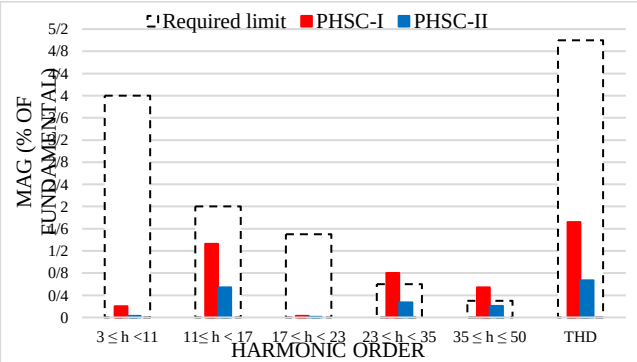

Fig. 10. Harmonic current limits of the 12-PDR with PHSC-I and PHSC-II in % of fundamental.

It should be noted that the passive harmonic suppression circuit similar to the structure of PHSC1 is presented in an 18-pulse rectifier [22], but it should be noted that firstly, in this 18-pulse rectifier, the optimal turns ratio is k=0.15 and m=1.87. Secondly, for this optimum turns ratio, the minimum of the input current THD is 5.44%, while in the proposed 24-pulse rectifier, for the optimal turn ratio PHSC1, k=0.25 and m=6.5 and the minimum of The input current THD is 1.72%. Also, a 40-pulse rectifier based on a passive harmonic suppression circuit similar to the structure of PHSC2 is proposed with an optimal turns ratio of m=14.17 [23], while the optimal value of the winding turns ratio of PHSC2 in the proposed 24-pulse rectifier is m=7.90. In other words, in this paper, the turns ratio of PHSC1 and PHSC2 is optimized according to the 24-pulse rectifier.

For the economic evaluation, first, the kVA rating of improved PHSCs is calculated, and then the cost is estimated according to the approach outlined in [24], where the cost of the transformer is estimated to be 4.5 times the kVA rating, and a diode price is considered as 2.25$. The kVA rating of the components of the PHSCs is calculated based on the following equation [25]:

$$S = 0.5 \sum V_{winding} I_{winding} \quad (33)$$

where $V_{winding}$ and $I_{winding}$ are the rms voltage and current of the windings of the PHSC components obtained from simulations under a 10 kVA load. As can be seen in Table 3, it can be seen that the kVA ratings of the PHSC-I and PHSC-II are 697.58 VA and 1126.92 VA, respectively. Therefore, the rating of PHSC-I and PHSC-II is 6.97% and 11.27% of the load power, respectively. It should be noted that the kVA rating of PHSC-I is 40% lower than the rank of PHSC-II.

Considering the diode's voltage drop of 0.7 V and the internal resistance of the diode of 1 mΩ, the connection losses of the diodes are determined as follows.

$$P_{Diode} = \frac{1}{\pi}\int_0^{\pi}(V_f i_d + i_d^2 R_d)d\theta = V_f I_d + I_d^2 R_d \quad (34)$$

Considering the current of the diodes in PHSC-I (I_{D1} = I_{D2} =15.7 A and I_{D3} = I_{D4} = 0.17 A) and PHSC-II (I_{D1} = I_{D2} =1.34 A), the connection losses are 22.71 W and 1.87 W, respectively. Also, due to the low current passing through the diodes of PHSC-II, it can be concluded that the current stress of circuit PHSC-II is much less than that of PHSC-I. Therefore, the connection losses and current stress of PHSC-II are much less than those of PHSC-I.

The iron and winding losses of the transformer are calculated as follows:

$$P_{core} = m_c k_c B_m^{\alpha} f_T^{\beta} \quad (35)$$

The copper losses can be determined by:

$$P_{copper} = \sum J \rho_{cu} (MLT_i) K_i N_i I_i \quad (36)$$

where, the mean length per turn (MLT_i), the number of turns (N_i), and the RMS current of the i^{th} winding (I_i) have been given in [26]. The total losses of the PHSCs have been calculated based on simulations using equations (34)-(36) and the parameters listed in Table 4. Therefore, the total losses in PHSC-I and PHSC-II are 104.36 W and 153.49 W, respectively.

To present the advantages of each of the PHSCs, Table 5 presents a technical and economic comparative analysis of the two novel PHSCs. According to this table, the THD of the input current of a 12-PDR with PHSC-II is less than PHSC-I.

TABLE 4
PARAMETERs USED IN THE CALCULATION OF LOSSEs [26]

Parameter	Symbol	Value
Material Coefficient	k_c	6.754×10^{-4}
AC/DC Resistance Factor	K_i	1.05
Maximum Flux Density	B_m	1.2 T
Current Density	J	2.3 A/mm^2
Electrical Resistivity of Cu	ρ_{cu}	2.3×10^{-8} Ωm
Exponent of Frequency	β	1.651
Exponent of Flux Density	α	1.559

Also, the connection losses and current stress of PHSC-II are less than those of PHSC-I. The total losses of PHSC-I are less than those of OHSC-II, and, as a result, its efficiency is higher. The kVA rating of PHSC-I is smaller, so its weight and size are lower. The PHSC-I consists of 4 diodes, and the PHSC-II consists of two diodes. Considering the kVA rating and the number of diodes, the cost of PHSC-II is less than that of PHSC-I, which is more economical. With these specifications, the PHSC-I is recommended for applications where weight, size, and efficiency are required. Also, in industrial applications with low input current THD, low connection loss, low current stress, and low cost, PHSC-II is recommended.

TABLE 5
COMPARISON OF TWO NOVEL PHSCs FOR 10 KW LOAD

Topologies	%THD of input current	Core Losses [W]	Copper Losses [W]	Connection Losses [W]	Total Power Losses [W]	kVA-Rating [VA]	Number of	Approximate Cost
PHSC-I	1.72	18.33	63.32	22.71	104.36	697.58	4	12.14
PHSC-II	0.67	26.64	125.18	1.87	153.69	1126.92	2	9.57

A comparison of the input current THD of a 12-pulse rectifier using existing PHSCs compared to PHSC-I and PHSC-II is shown in Fig. 11. As can be seen in this figure, the THD of the input current of 12 pulses with PHSC-II is much lower compared to other different PHSCs, which shows the high ability of PHSC-II in suppressing the harmonic distortion of the input current.

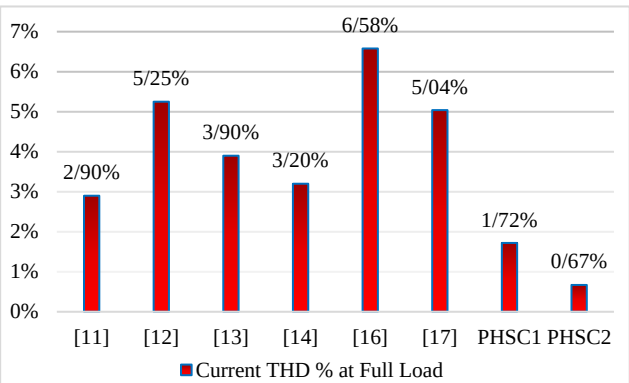

Fig. 11. Comparison of input current THD of 12-pulse rectifier with different PHSCs

IV. Conclusion

In the last few years, utilizing the PHSC in the DC-link of the multi-pulse rectifier has been considered an efficient solution to reducing the harmonic distortion of the input current. With this approach, two novel PHSCs are presented in this paper, and their performance is described, then are technically and economically compared under the same input source and output load conditions. The results demonstrate that the input current THD of a 12-PDR with PHSC-II is lower than that of PHSC-I and lower than existing passive harmonic suppression circuits, which verifies the high performance of PHSC-II to suppress the harmonic distortion of the input current. Furthermore, PHSC-II has lower connection losses, current stress, and cost than PHSC-I, so PHSC-II is recommended in industrial applications that require low input current THD, low connection losses/current stress, and low cost.

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