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Enhancing Microcomputer Edge Computing for Autonomous IoT Motion Control

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Abstract— Devices microprocessors, microcontrollers, and Field Programmable Gate Arrays (FPGA) play the core rule at the IoT edge level and it should be right provisioned. For proper controller performance, control algorithms should be implemented near the actuator eliminating the delay effects. In the IoT domain, this means to implement the mentioned algorithm at the edge level and prior data transmitting. The efficient IoT-enabled motion control can be obtained by considering two main factors; the first factor is from the actuator design point of view and the second factor is from the controller performance point of view. Therefore, in this article, the two mentioned factors are treated concerning the microprocessor rule and importance as a core for proper prototype design and as the main platform to implement the control algorithms. A comparison of controller performance indices for both prototypes is done using previously distributed motion control schemes and newly developed schemes after tuning the respective schemes gains in an optimal manner. The scheme with better behavior of both prototypes are selected for the IoT integration process, this scheme ensures optimal edge computing for the distributed motion control, making the implementation of all control computation take place at the IoT-edge level. As a result, the dynamic pipeline stages (DPS) based prototype gives better controller performance indices for most strategies, less power consumption, and optimally utilized resources encouraging the use of the microprocessors with reconfigurable components at the IoT-edge level.

Keywords- Controller, Internet of Things, Edge Computing, Pipeline, Dynamic pipeline stages, Embedded system and Motor.

I. INTRODUCTION

This article highlights the importance of decentralized motion control as one of the main industrial uses of the rising state-of-the-art Internet of Everything. IoT basics and IoT definitions are introduced. A broad overview of the problem is presented, and the objectives of this paper are outlined. From cloud level the operator can specify individual channels for individual motors and individual channels for n-motors working together [1]. IoT enables the researchers to develop new systems which can be observed, analyzed and controlled remotely. With IoT enabled distributed motion control, both data visualization and data analysis for n-motors working in the industry can be carried out and abnormal cases can be detected early [2]. Microprocessors, microcontrollers, and field-programmable gate arrays (FPGAs) have evolved to the point where they constitute the backbone of Internet of Things (IoT) systems, beginning with nodes and progressing to gateways and servers [3]. Edge computing reduces delays, energy costs, and communication bottlenecks. Researchers in the Internet of Things sector have identified edge-level exploitation of reconfigurable microarchitecture as a potential research topic [4]. Taking into consideration the fact of using the microprocessors, microcontrollers, DSPs and FPGAs for control algorithms implementations, the emerging of IoT with the industry will require new modifications in the platforms architecture in order to be more suitable for the integration

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process and to insure optimal behavior in real-time working conditions. Existing meanings of the term "Internet of Things" (IoT) vary. Many of these definitions have advanced as a result of the evolution of prior technologies and the effects of more recent ones [5]. The primary IoT techniques should be understood before working on the IoT architecture. In 1998, Ashton coined the phrase "Internet of Things" (IoT) to describe a network in which everyday things are linked by RFID and their data is utilised in online supply chains. Communication range, memory, and computing power are the constraints. Many requirements are reflected through those constraints and are needed to connect the internet to constrained devices by using TCP/IP protocols. However, a lot of meanings are missed through this definition. In 2009, CASAGRAS definition [6] is introduced. We were inspired to take on the task of transferring our focus from the home automation area, where most IoT research has been conducted, to the industrial control domain, where it has received much less attention.

Even IoT is considered as a new name of recent developed embedded systems, the device microprocessor which considered as brine for any embedded system has got less attention with respect to the research in the new technology IoT and more attention is given to the connectivity and protocol aspects [7]. The device microprocessor is intensively used at edge level with both sensors and actuators enabling them to be intelligent. However, the current fixed architecture of the device microprocessor is found to be unsuitable for utilization with IoT applications. Reconfigurable architecture makes the microprocessor more flexible with less power consumption and resource utilization as per application requirements. The focus of this work is to illustrate the suitability of using microarchitecture with reconfigurable (dynamic) pipeline stages against a one with fixed pipeline stages by using them as cores in developing two actuators for one of the important industrial control applications. That is a distributed motion control. The developed Distributed motion control scheme is to be enabled through the new technology IoT using the microprocessors in an optimal manner at edge level i.e. to have optimal performance indices through Edge Computing [7]. For this purpose, two different systems have been developed. The first system is a microprocessor (with fixed pipeline stages (FPS)) based PMDC Motor prototype, and the second system is a reconfigurable microarchitecture (with dynamic pipeline stages (DPS)) based PMDC Motor prototype. The aim of such developments is to show the possibility of overcoming the drawbacks with the current available fixed microprocessor architectures and obtaining the flexibility of avoiding the data loss in an optimal manner when high frequency measurement is required. The idea behind proposing the reconfigurable microarchitecture is due to expectation of having high speed machines in the industry and when high speed devices are connected with slow devices it is very important to see not to lose any data in transmission. If the input device speed is high then the pulses frequency coming from its sensor will be higher than the receiving element in processor, it is very difficult in synchronizing the data rate between them, so it is very important in considering some handshaking device between fast and slow devices [8]. For instance, a buffer or some delay system can be inserted between processor element and measurement system. But simple buffer and delay elements may increase the design complexity, slow down the process and shows impact on accuracy. The main reason of data loss caused when high-speed machines connected with low-speed devices is due to the frequency difference between them, and when the processor receiving element enters into its NRS status due to the processor “clear” signal effect, the coming pulses from the data source i.e. the high-speed machine will not be counted and therefore it will be lost [9]. The accuracy loss will occur only if a large number of delay elements are inserted without proper clocking protocol; however, the value of accuracy loss depends on the frequency value to be measured and the number of utilized delay elements and buffers. In the proposed micro architecture, dynamic pipeline is integrated to overcome these problems and its suitability for the industrial IoT utilization is confirmed.

II. LITERATURE REVIEW

The more current embedded systems are now referred to by their new term, Internet of Things (IoT). On the other hand, a fixed architectural design is seen as a disadvantage in the context of the internet of things, particularly in light of the growing number of things that are linked to the internet.

The device microprocessor acts as the brain of any embedded system. This section illustrate the previous research work related to the device microprocessor in the IoT domain [10]. In another hand and as per current work requirements, the distributed motion control application is selected as an important industrial topic for IoT integration process, so the research work related to both frequency measurement and distributed motion control is reviewed within current article, as proper frequency measurement results in proper motion control, along with illustrating the role of the computational hardware in PMDC motor control applications. Several application domains are offered computing potential by the IoT. The application domains include healthcare, logistics and transportation, smart environments, social and personal domains. Sensing includes data collection about case or event. The data can be temperature, motion or pressure, etc. The data acquired from the sensors should be manipulated to a more meaningful form. For example: in sensor fusion [11], the

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sensed data using different sensors are merged to produce a more robust and accurate quantitatively/qualitatively data. The algorithms that used for sensor fusion can occupy different levels of memory/compute intensity. Many nodes are connected together and the data travels through them. Wi-Fi and Bluetooth are examples of the communication technologies. Software defined ratio (SDR) is a communication system where filters, modems and other physical layer functions that are presented in hardware are implemented in software [12]. The most important characteristics of SDR are the flexibility in which the system enhancements do not require hardware updates. With SDR, both instruction memory and data footprints are small. However, its applications are compute intensive. Signal processing is the major function in image processing. The parameters of an input video stream or image are to be extracted or converted to a more meaningful form [13]. Face recognition, traffic sign recognition and automatic license plate recognition are IoT applications which use image processing. More computation capabilities are required with image processing as it includes matrix multiplications. In addition to that, large amount of data is to be stored either as input, intermediate or output, so this raise the memory size requirements. Compression ensures that the data is transmitted fastly, analyzed or/and retrieved by reducing the communication requirements. If the storage on the edge level is required then compression reduces the amount of required storage thus reducing memory size, and this will meet with fact of resource-constrained of the IoT devices [14]. There are two types of compression and those are lossy and lossless compression. With first type, i.e. lossy compression, the perceptibility of data in question is exploited, but the unnecessary data is removed. With second type, i.e. lossless compression, the redundant data are removed statistically for the aim to concisely represent the data. Second type is more memory intensive and more compute [15]. In order to keep the integrity of both the data and the device, security applications are required; those applications prevent unauthorized access to sensitive data. Malicious attacks affect the IoT devices which functioning in open environments. Data encryption ensures data confidentiality [16]. With data encryption, the encryption algorithm is utilized to create encrypted data which require decryption in order to be read / utilized. Encryption speed is related to the memory access latency for storage and data retrieval, so this is again forms both memory and compute intensively. When the IoT devices are utilized in unattended environments, the system should be capable to function properly if a failure of some their component accrues [17]. This is referred to as fault tolerance and it is important for quality of service (QoS) insurance. There are two types of fault tolerance and they are hardware-based and software based. First type i.e., hardware-based fault tolerance are a storage devices and use redundancy. Second type includes algorithms and applications that make operations like error detection and correction, cyclic-redundancy checks and memory scrubbing. However, in our work, we focus on configurable pipeline stages due to their effect on area and power consumption and thereby on performance. With configurable pipeline stages, both not ready sequence (NOT) and data propagation delay are avoided. We observe how the controller performance indexes values are enhanced when using configurable (dynamic) pipeline stages for speed measurements by comparing with their values in the case of non-configurable (fixed) pipeline stages. Even after linking the controller with IoT technology, the published data shows the enhanced performance of the controller behavior with configurable pipeline stages. With heterogeneous architectures, the same instruction set can be executed with different cores, but the cores have different performance and capabilities. The software of the concern application will determine the core that best ensures the optimization behavior based on evaluating the resources requirements [18]. There will be several cores with the heterogeneous architectures and those cores may be GPUs, CPUs, DSPs, etc Heterogeneous architectures provide a much reduced design space, but this requires more design time and efforts. However, if the number of applications is increased, then heterogeneous architectures may provide less optimization potential than adaptable architectures. The number and choice of the cores is a major challenge and scheduling of applications to the best core is another major challenge in designing the heterogeneous architectures for the IoT. The distributed heterogeneous architectures in the form of a network are an alternative to heterogeneous cores on one device. In this case, many research challenges are to be addressed in order to use distributed heterogeneous architectures. IoT devices are under more number of attacks due to their pervasiveness, mobility and connectedness [19]. IoT devices resources constraints make security a challenging as they will not have hardware support for enhance security features. In addition to resources constraints, IoT devices may generate sensitive information. Most of hardware security techniques that proposed for embedded systems can be used in IoT devices with runtime configurable security policies which adaptable to the requirements. Several control and instrumentation applications require accurate measurement of frequency in digital form. The device microprocessor plays the main rule in frequency digital measurement and there are several methods in which the microprocessor can be programmed to perform the task of frequency measurement [20]. The latency requirements at computational stages should be given significant importance to insure proper and trusted control algorithm implementation via

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a specified hardware target. However, those requirements are greatly depended on the processor working frequency while performing the control algorithm program cycling and the operator should ensure a complete program scale on each cycle before every controller necessary action to satisfy the desired output. This goal can be achieved by suitably selecting the sampling time period in such a manner to allow the smooth and accurate controller algorithm implementation using specified hardware boards. This section presents the relevant work related to the device microprocessor in the IoT context and its optimization for the utilization with IoT especially at edge level. Reconfigurable microarchitecture is recommended for the components that can be configured within the run-time[21]. A review of the velocity measurement methods based on the device microprocessor is introduced within this article considering the fact of obtaining proper motion control through proper velocity measurement. The DMA method is found to be the best for frequency measurement but it has the problems of NRS and propagation delay which can be solved via pipeline system, but with fixed processor architecture the pipeline stages number is fixed which a drawback, and therefore this can be solved via dynamic (reconfigurable) microarchitecture.

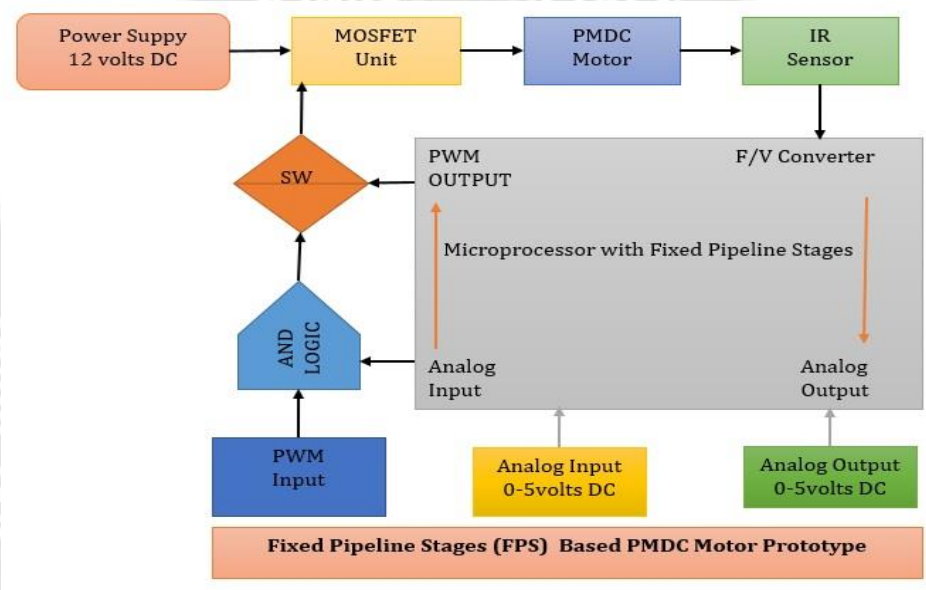

Figure1: Block schematic for the proposed PMDC motor prototype

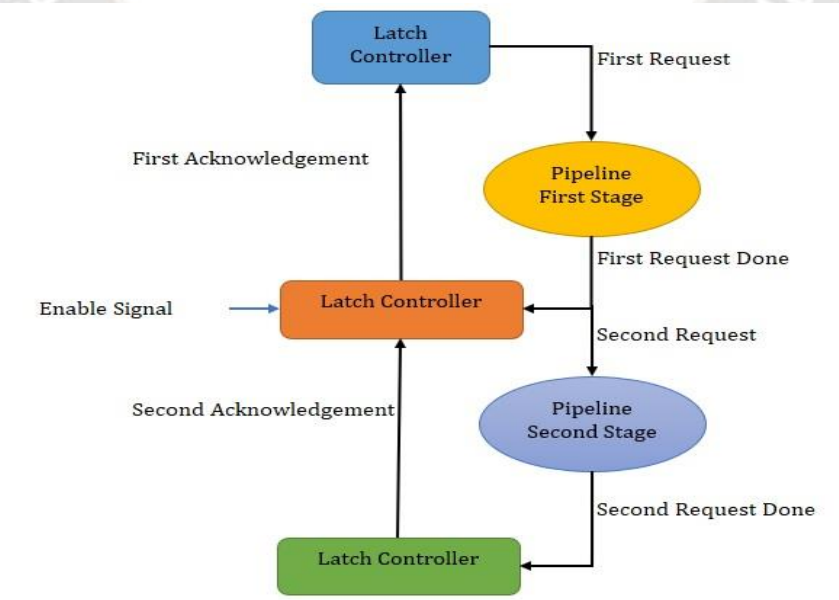

Figure.2: Two pipeline stages

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III. Proposed System

Digital electronic devices become much faster, smaller and cheaper due to two main reasons, first reason is the massive progress in semiconductor technology paced by planer processing and the second one is the Very-Large-Scale Integration (VLSI) process [22]. The applications of the microprocessors are extended to the industry due to the spectacular development semiconductor memory such as ROMs, PROMs and EPROMs [23]. In many industrial applications, microprocessors are presented [24]. One important industrial application is motor speed control with the ability of changing the speed within wide ranges.

The block diagram of the prototype PMDC motor design is shown in Figure.1. The front panel is the interface for the PMDC motor, via which the user may send commands and get feedback. A switch on the actual front panel lets the user choose between an analogue input with a range of 0-4.5 or a pulse width modulation (PWM) input. If the user chooses analogue input, a potentiometer on the physical front panel may be used to adjust the input voltage within the aforementioned range. Selecting an analogue input working scenario provides the microcontroller with the input voltage it needs to transform the analogue input into a pulse width modulation signal.

Dynamic pipeline stages are used to create a PMDC prototype based on reconfigurable microarchitecture. The Reconfigurable Microarchitecture is designed to be used for edge computing in the IoT. This microarchitecture is built utilising an FPGA board and a reconfigurable computer system. The PMDC motor's feedback circuit is utilised with reconfigurable microarchitecture to create a speed control prototype that can be successfully integrated with IoT technology [25]. The goal of designing a reconfigurable microarchitecture with the aid of a reprogrammable computing system based PMDC motor speed control prototype was to address the shortcomings of the fixed architecture (fixed pipeline stages as per our aim) microprocessor that are encountered in the previous designed PMDC motor speed control prototype. Both Not Ready Sequence (NRS) and data propagation latency of the DMA controller are eliminated with this produced prototype. To determine the best speed measuring technique at the IoT edge level, many approaches are explored utilising various pipeline architectures.

IV. Edge level technology for IoT

Some of the costs of using cloud computing include higher energy use, longer reaction times, and more demands on available communication bandwidth. Edge computing (carrying out the calculations near the data source) is favoured for the purpose of reducing these overheads, decreasing latency, preventing bottlenecks, and boosting performance. Because of the heterogeneity of IoT edge node platforms, it is challenging to create a common application based on the edge computing paradigm. Fog computing is presented as a virtual platform that offers networking services, computation, and memory between edge nodes and cloud-based data centres and is also known as mobile edge computing (MEC). The high throughput is a result of the pipeline layout's design. Like a factory line, a pipeline allows for the processing of fresh data even before the previous data has completed. In today's high-tech computers, the pipelining method is indispensable. It's put to use in a variety of contexts, including but not limited to parallel processing, cutting-edge computer design, high-velocity ALUs, and instantaneous I/O data retrieval. When the bulk of data processing is sequential, pipelines may increase system throughput. Power consumption rises proportionally with pipeline depth and falls with pipeline diameter. Transparent or opaque latches/registers allow pipeline stages to be merged or divided at runtime, resulting in dynamic pipeline stages. Think about the pipeline's first two phases, as seen in Figure 2.

In order to achieve precise signals, it is very important to get non-overlapping timing signals. The input signals are activated either at falling or rising edge of the clock signal. In this case, the clock edges imply that the main reason of inaccuracy is the timing jitter. For the aim of further suppressing the charge injection errors, the rising edge of pre-phase would be placed slightly before than that of past phases. It occurs when a pulse is readily available at Direct Memory Access Request (DRQ) of the Direct Memory Access (DMA) controller in Not Ready Sequence (NRS). NRS occurs in two cases: first case when the DMA is executing the past pulse and second case when the DMA is in inactive state. In this situation, second pulse should wait for DMA permission to enter into DRQ. Maximum efficient operation of the pipeline system cannot be obtained because of the internal propagation delay. Wave and mesochronous pipeline systems are used to manage the propagation delay [16]. However, it is difficult to estimate the required delay element. The clock pulses, in most digital systems, are used to control the execution of sequential functions. Non-overlapping clock pulses are difficult to be avoided, especially in two phase systems. Higher performance digital gates are achieved by minimizing the clock period. This population-based strategy finds the optimal answer by generating a swarm of particles that then flies about the study area. Each particle in the research space uses its own experience (Pbest) and the experiences of other particles in the swarm (Gbest) to update its flying direction and location using its fitness value and velocity. This process is carried out at the start of each iteration and continues until the termination requirements are fulfilled. Nonetheless, the PSO algorithm flowchart is shown in figure.3. The idea of developing the

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new prototype comes to make the designed prototype more suitable for using with Internet of Things (IoT) technology as it is based on a processor with reconfigurable pipeline stages and this is recommended for the new generation of IoT microprocessors. A procedure of both System Identification and Optimal Speed Controller Design is performed for the dynamic pipeline stages (DPS) based PMDC motor. The merits of the new proposed PMDC motor, i.e. DPS_based one are its dynamic power consumption and better performance indexes, but the dis-merit is: it has less data matching percentage in comparison with FPS based PMDC in system identification procedure.

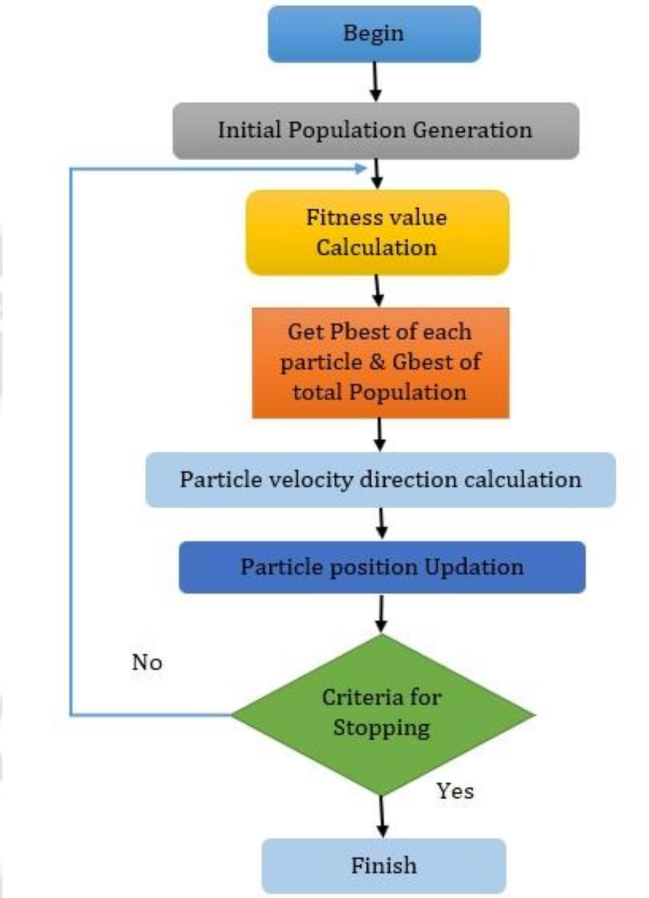

Figure.3: Schematic representation of the PSO algorithm

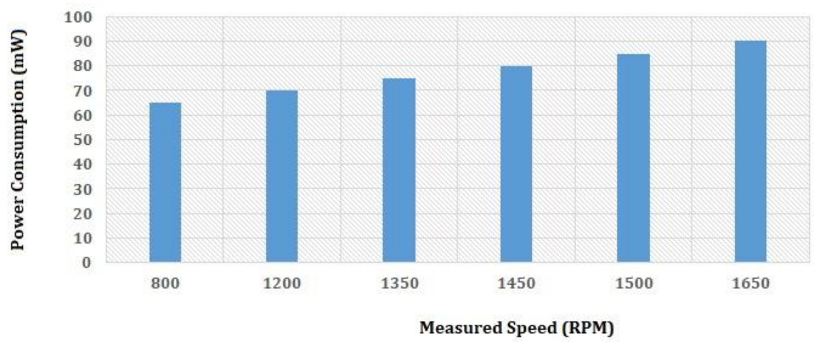

Figure.4: Examination of the prototype power consumption based on fixed microarchitecture

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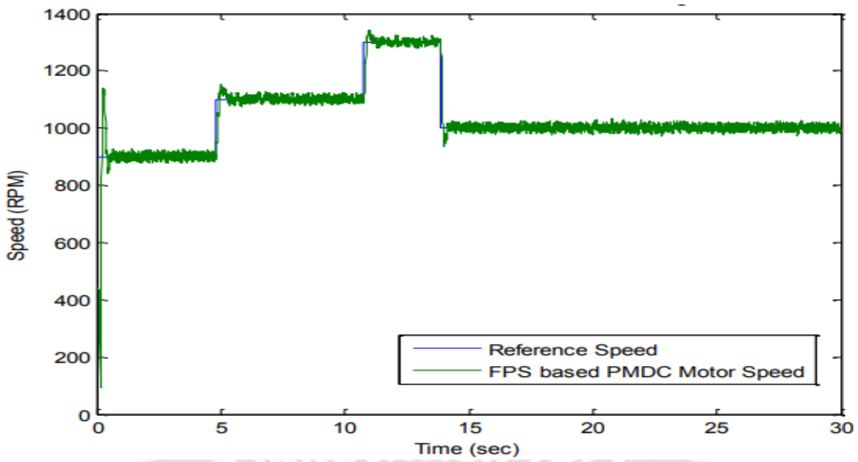

Figure.5: Set point tracking work Real Time test

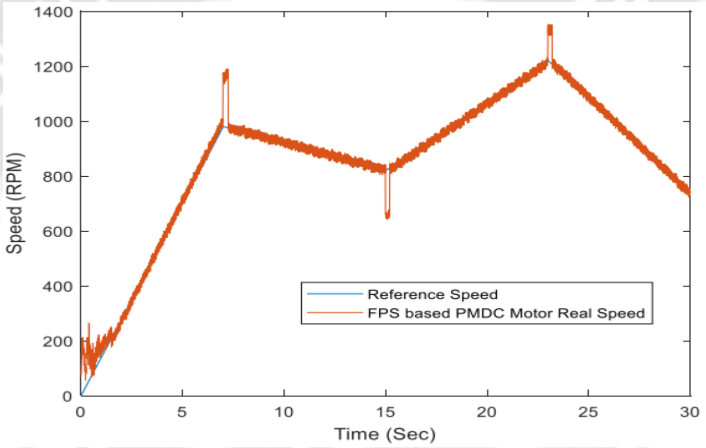

Figure.6: Prototype real time response for variable ramp input sequence

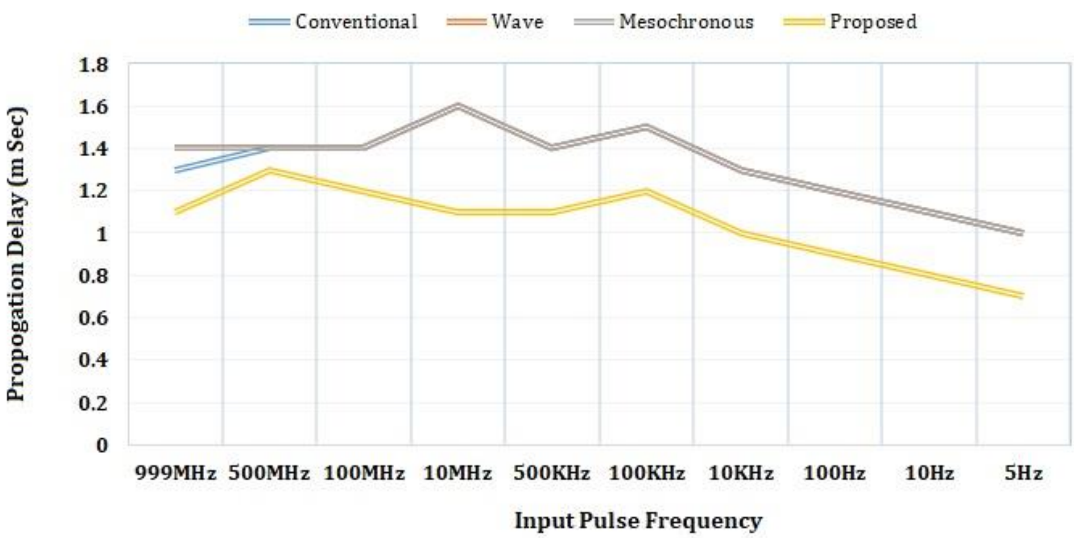

Figure.7: Three- Pipeline Stages

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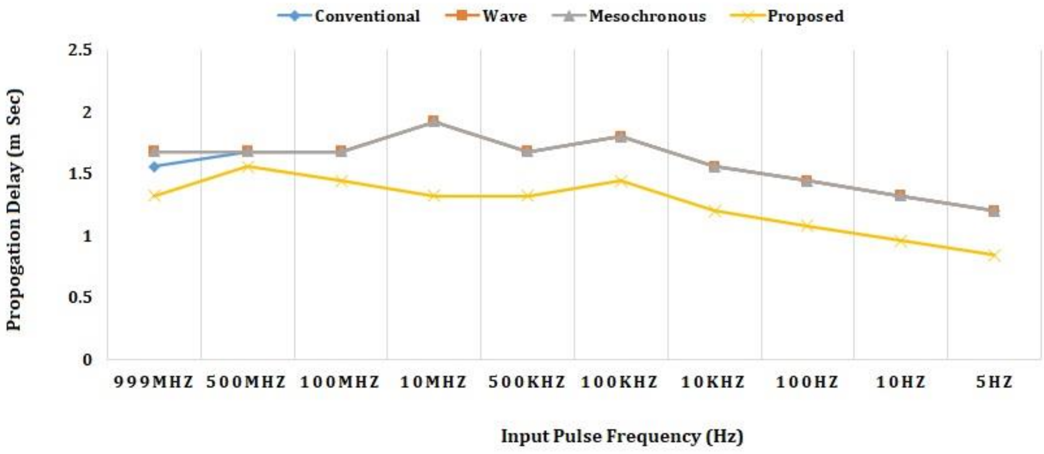

Figure.8: Four Pipeline Stages

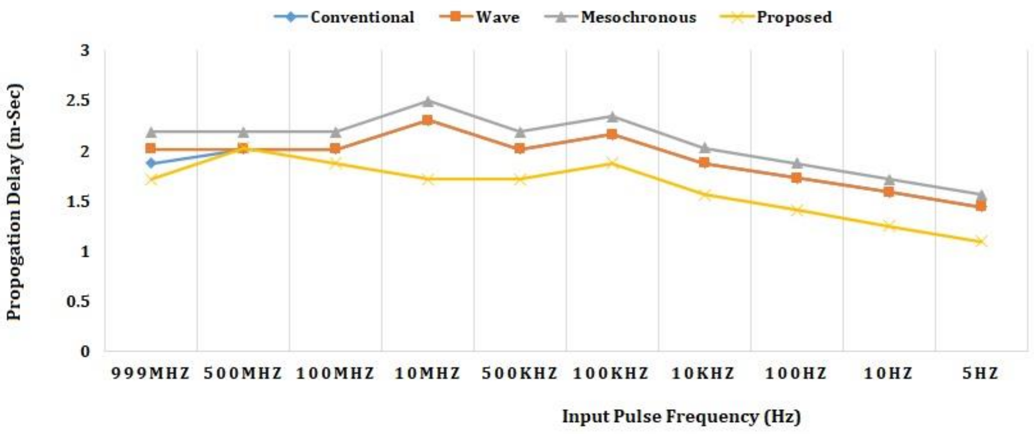

Figure.9: Five Pipeline Stages

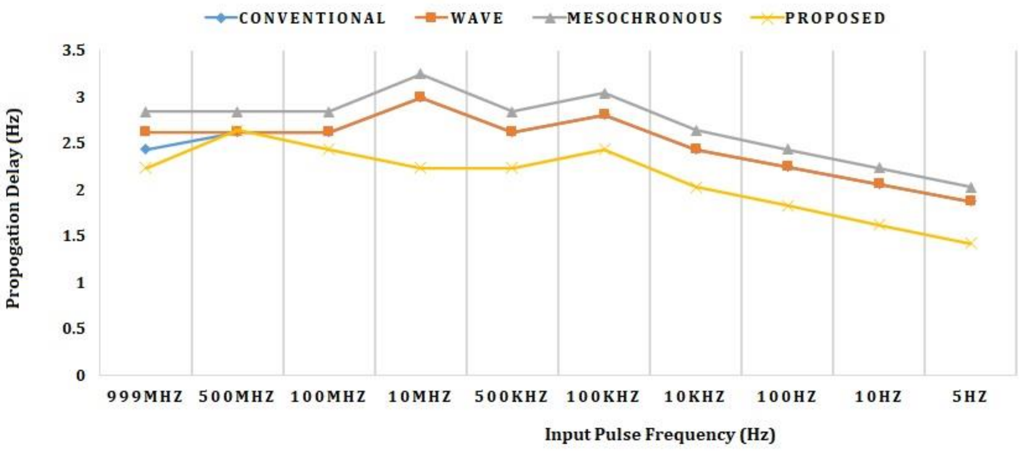

Figure.10: Six Pipeline Stages

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V. Results and Discussion

As it is mentioned and tested, current development makes the procedures of both system identification and controller design straightforward and easy due to its single input single output (SISO) configuration, but the fixed microarchitecture based microprocessor as a core for such development is considered as a drawback for its utilization with the-state-of-the-art IoT technology. When the user is going to use the prototype at the IoT edge-level as an actuator, the same amount of power consumption is required regardless the application speed requirements. However, the INA 219 current sensor is linked in contact with the feedback circuit of this fixed microarchitecture based developed prototype, and its output is collected by means of an Arduino mega board in order to examine the developed's power consumption. Power consumption is calculated by multiplying the computed current by the voltage difference between the power supply and the load, and a consistent value of 54 mW is recorded over a range of observed speeds (figure 4). In addition to that, only two pins i.e. the PWM input pin and the Analog output pin have been utilized from whole the microcontroller pins and the others are left idle which is considered as resources waste utilization. The fixed operating frequency of such fixed microarchitecture design limits its utilization when high frequency measurements are required due to the fixed number of its pipeline stages (FPS) and, in such case, the problems of the not ready sequence (NRS) due to the clear signal and the data propagation delay will take place. The reconfigurable microarchitecture-based prototype will ensure dynamic power consumption, proper resources utilization and overcome the NRS and data propagation delay problems by means of its dynamic pipeline stages (DPS) structure. In order to carry out the PMDC motor set point tracking job, the simulation test is being carried out. Figure 5 shows the response. In this particular illustration, the different paces is established at 900 revolutions per minute (RPM), and the flow rate conforms to this trajectory. Following that, at a real time interval of five seconds, a fresh trajectory consisting of 1100 RPM is implemented, and the controller makes it such that the motor speed follows this trajectory. After that, after ten seconds of real time, a fresh trajectory of 1,300 RPM is given, and the controller makes it such that the motor speed follows this trajectory. In the last step, which occurs after 15 seconds of actual time has passed, a new trajectory consisting of 1000 RPM is provided. In addition to that, the real-time reaction to a varied ramp input sequence was evaluated, and the results are shown in the figure.6. by carrying out a series of steps that are similar to those described in the section on simulation tests. The following statistics (Figure.7 to Figure.10) provide a graphical comparison of the propagation delays between the existing pipeline systems and the proposed pipeline system. A logical analysis is performed. When the logic is added, the suggested pipeline system has the lowest latency in propagation among the systems.

VI. Conclusion

The fundamental benefits of integrating the-state-of-the-art IoT with distributed motion control as an important industrial application along with IoT definitions, problem statements and article objectives are discussed in the first article. Literature review for enabling right-provisioned microprocessors and their optimizations for IoT along with microprocessor-based speed measurement and distributed motion control are discussed in article two. From the review, it is observed that: the microprocessors utilizations with IoT domain and especially for edge computing task should be designed in an optimal manner which can be obtained through several aspects and the reconfigurable architecture is one of them, in other side, the DMA method is found to be the best for speed measurement but it has the problems of NRS and data propagation delay which can be solved via pipeline system, so the fixed processor architecture is a drawback and therefore the selection of dynamic (reconfigurable) microarchitecture took place. The idea of developing the new prototype comes to make the designed prototype more suitable for using with Internet of Things (IoT) technology as it is based on a processor with reconfigurable pipeline stages and this is recommended for the new generation of IoT microprocessors. The merits of the new proposed PMDC motor, i.e. DPS based one are its dynamic power consumption and better performance indexes, but the demerit is: it has less data matching percentage in comparison with FPS based PMDC in system identification procedure.

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