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Space Vector Modulation for Induction Motor on ARM-based Microcontroller

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ABSTRACT

This article presents the review and the implementation of Space Vector Modulation (SVM) in a low-cost microcontroller-based motor drive system. The output three-phase voltages are obtained from a reference voltage vector in the polar coordinate system using the PWM technique; these voltages can reach up to the level of the DC voltage source (experimentally 16 VDC or practically 237 V with an inverter module). The article also provides a detailed presentation of the pre-calculations and the computations required for SVM on a STM32F1 ARM-based microcontroller. For achieving high frequency precision, a novel method for vector rotation based on the fixed-point arithmetic is proposed and tested. The experimental results highlight that the presented implementation including vector rotation can reach 1 Hz without significant error and it requires only 0.684 MIPS at 5 kHz computation rate for a 72 MIPS 32-bit microcontroller with single-cycle multiplication. The maximum instantaneous output phase-to-phase voltages could be as high as the DC voltage source.

1. INTRODUCTION

At present, along with the development of renewable energy, the market of the converters for these energy resources is becoming more and more diverse. Converter systems are becoming increasingly compact and cheaper due to the continuous research and development of advanced technology such as resonance techniques that reduce the size of magnetic components or the techniques that optimize the output voltage, simplifying the gate driving circuitry and DC link capacitor requirement.

In modern domestic electronic appliances such as inverter-powered refrigerators or air conditioners, the intelligent power module (IPM) involving a three-phase inverter bridge and its driver circuitry is frequently utilized. These IPMs mitigate significant efforts in the PCB (Printed Circuit Board) design process and make cost-sensitive drive systems become less stressful to be dealt with. A typical IPM does not support an absolute maximum DC voltage rating more than 500 VDC. However, a passive rectifier gives approximately 320 VDC under a grid voltage condition of 220 VAC while yielding nearly 540 VDC with a 380 VAC grid. Therefore, an IPM is commonly used for a 220 VAC grid. For a popular industrial motor, the rated output power should be achieved with rated input voltage. Thus, attempts to recover the magnitude of the rectified grid voltage have been carried out to optimize the motor power rating. Many pulse width modulation (PWM) techniques have been developed for generating three-phase voltages in order to drive an induction or a permanent magnet synchronous motor. Space Vector PWM (SVPWM or SVM for short) is one of

the most preferred techniques in the condition of balanced load.

In previous studies (Basera & Vora, 2018; Datta et al., 2016; Duong et al., 2020; Erfidan et al., 2008; Minas et al., 1999; Muangjai & Premrudeepreechacharn, 2009; Rony et al., 2018; STMicroelectronics, 2007), the method to obtain pulse width modulation duty cycles based on the reference voltage vector was described thoroughly. The key advantages of SVM over the Sine PWM technique have been explained by Mansuri et al. (2020) and Parekh (2015). Nevertheless, the frequency precision (resolution) plays a significant role in a closed loop control system, where the control signal (referred as the frequency input in V/f control scheme) should be guaranteed to be as smooth as possible. STMicroelectronics (2007) demonstrated the results of the high precision vector rotation method. Unfortunately, these studies have neither clarified the vector rotating algorithm for V/f control nor proposed a method that can achieve adequate frequency precision in the near-zero region.

The main contribution of this study is clarifying the detailed vector rotating algorithm for overcoming near-zero frequency glitches from a new interesting perspective. Furthermore, a brief overview of the SVM implementation on a typical Cortex-M3 core microcontroller-powered motor drive system is presented. The frequency precision has been exemplified and compared in cases with and without applying the proposed method on the custom-made hardware (the PCB). To demonstrate the output currents of the implementation, an induction motor mounted on a floating paddle-wheel aerator was utilized. The measurements are obtained with a digital signal oscilloscope.

2. MATERIALS AND METHOD

2.1. Space Vector Modulation Technique

Space Vector Modulation (or Space Vector Pulse Width Modulation) is a pulse width modulation technique that converts a reference voltage vector in the αβ or the polar coordinate system into PWM signals that generate average phase-to-phase voltages. The key advantage of SVM over Sine PWM is that the phase-to-phase voltages can potentially reach 100% of the DC source in case of no deadtime inserted. This is a great advantage that leads to many benefits:

− Less motor current for the same horsepower, this contributes to the reduction of heat dissipation on both motor side and converter side, as well as the reduction of cost for motor windings.

− Reduce motor insulation requirement, inverter bridge absolute rating of voltage and system stresses by decreasing DC voltage source (and thus maximum voltage on motor windings) by nearly 15% for same output AC voltage.

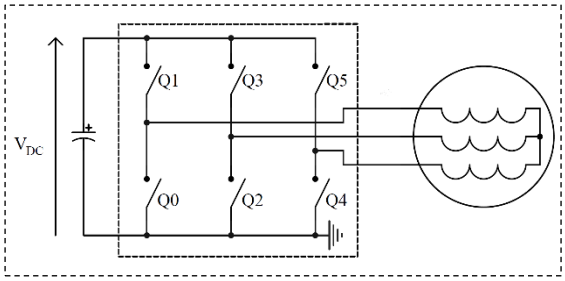

Figure 1. Induction motor connection

Due to its advantages, especially in small systems, such as home appliances, small industrial motor control, and speed control feature modification for popular motor systems, SVM is preferred over Sine PWM. The SVM will be briefly described as follows:

With a three-phase two-level inverter bridge, the connection of an induction motor is shown in Figure 1, where V_{DC} is the DC voltage source. The ON-OFF switches represent the semiconductor switching devices. There are 6 switches (Q1 to Q6) composing into 3 groups (3 legs of the inverter: Q1 and Q0 on the same leg and so on).

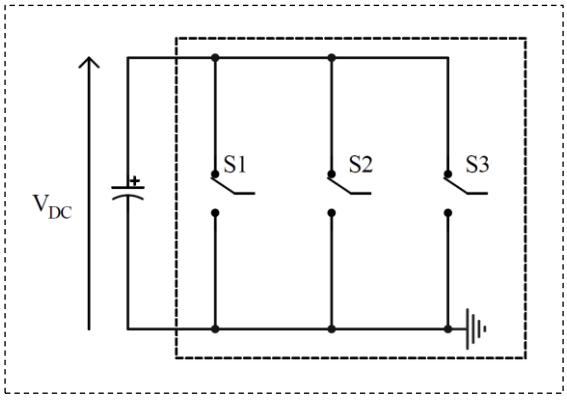

Figure 2. Inverter bridge presented by bi-state switches

The inverter bridge can be redrawn in Figure 2 and its output is presented by 8 states as in Table 1 where: S1, S2, S3 stand for bi-state switches; state 1 and 0 of each switch stand for its output value (1:

V_{DD}, 0: GND); $\overrightarrow{V0}$, $\overrightarrow{V1}$, $\overrightarrow{V2}$, $\overrightarrow{V3}$, $\overrightarrow{V4}$, $\overrightarrow{V5}$, $\overrightarrow{V6}$, $\overrightarrow{V7}$ are output state vectors that are named Space Vectors.

Table 1. Inverter output states

State	S1	S2	S3	V_{an} (times V_{DC})	V_{bn} (times V_{DC})	V_{cn} (times V_{DC})	Space Vector
0	0	0	0	0	0	0	$\overrightarrow{V0}$
1	1	0	0	$\frac{2}{3}$	$\frac{-1}{3}$	$\frac{-1}{3}$	$\overrightarrow{V1}$
2	1	1	0	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{-2}{3}$	$\overrightarrow{V2}$
3	0	1	0	$\frac{-1}{3}$	$\frac{2}{3}$	$\frac{-1}{3}$	$\overrightarrow{V3}$
4	0	1	1	$\frac{-2}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	$\overrightarrow{V4}$
5	0	0	1	$\frac{-1}{3}$	$\frac{-1}{3}$	$\frac{2}{3}$	$\overrightarrow{V5}$
6	1	0	1	$\frac{1}{3}$	$\frac{-2}{3}$	$\frac{1}{3}$	$\overrightarrow{V6}$
7	1	1	1	0	0	0	$\overrightarrow{V7}$

Because of the output voltage states and input DC voltage sourcing method (capacitor decoupling), this type of converter is termed a two-level voltage source inverter (two-level VSI). The voltages seen by motor windings in Figure 1 result in a vector diagram plotted in αβ reference frame shown in Figure 3, where the windings are supposed to be identical and dimensionally $2\pi/3$ displaced to each other. As in balanced load condition, the resultant magnetic field vector produced by these voltages is a fixed-length vector that rotates at the synchronous frequency, therefore it is only one reference vector $\overrightarrow{V_{ref}}$ required to represent them. In fact, the relationship between the resultant magnetic field magnitude φ_r and the magnitude of each component phase magnetic field φ_m is:

$$\varphi_r = \frac{3}{2}\varphi_m \tag{1}$$

Therefore, the reference voltage vector modulus can be considered:

$$\left|\overrightarrow{V_{ref}}\right| = \frac{3}{2}\left|\overrightarrow{V_{phase-neutral}}\right| \tag{2}$$

The hexagon formed by the active vectors from $\overrightarrow{V1}$ to $\overrightarrow{V6}$ at which there is non-zero voltage applied to motor windings is divided into 6 sectors: from I to VI, each occupies an angle of $\pi/3$ in the plane without overlap. $\overrightarrow{V0}$ and $\overrightarrow{V7}$ are zero vectors at which all motor windings are considered to be shorted together, these two are located in the center of the hexagon.

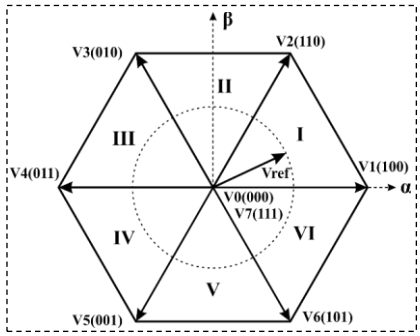

Figure 3. Voltage vector diagram of inverter output states

The moduli of the Space Vectors are given:

$$\begin{cases} \left|\overrightarrow{V\langle n\rangle}\right| = V_{DC}, & n \in \{1,2,3,4,5,6\} \\ \left|\overrightarrow{V\langle n\rangle}\right| = 0, & n \in \{0,7\} \end{cases} \tag{3}$$

Taking a closer look, assuming that $\overrightarrow{V_{ref}}$ is in sector I, the projections of $\overrightarrow{V_{ref}}$ to $\overrightarrow{V1}$ and $\overrightarrow{V2}$ yield $\overrightarrow{V_{cw}}$ and $\overrightarrow{V_{ccw}}$, respectively. This projection is depicted in Figure 4. With the Conventional SVM switching rule (Parekh, 2015), the time computation for $\overrightarrow{V_{ref}}$ implementation is shown in (4) where T_S the switching cycle in theory.

$$\overrightarrow{V_{ref}} = \frac{T_{cw}}{T_S}\overrightarrow{V1} + \frac{T_{ccw}}{T_S}\overrightarrow{V2} + \frac{T_0}{T_S}\overrightarrow{V0} + \frac{T_7}{T_S}\overrightarrow{V7} \tag{4}$$

This means that the inverter output state remains in the state $\overrightarrow{V1}$ of for T_{cw}, in the state of $\overrightarrow{V2}$ for T_{ccw} and the rest in the states of zero vector(s) ($\overrightarrow{V0}$, $\overrightarrow{V7}$ or both) within a single switching cycle, yielding (5).

$$T_S = T_{cw} + T_{ccw} + T_0 + T_7 \tag{5}$$

T_{cw} and T_{ccw} must be computed in the αβ reference frame such that the generated output voltages are exactly represented by $\overrightarrow{V_{ref}}$.

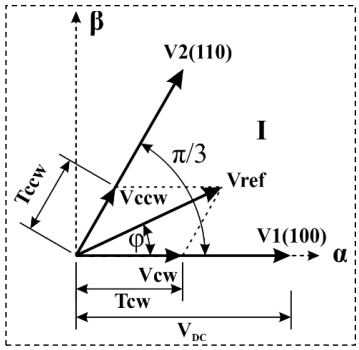

Figure 4. An instance of $\overrightarrow{V_{ref}}$ in sector I

The projections of $\overrightarrow{V_{ref}}$ along α and β axes are given by (6).

$$\begin{cases} V_{DC}\dfrac{T_{cw}+T_{ccw}cos(\pi/3)}{T_S} = |\overrightarrow{V_{ref}}|cos(\varphi) \\ V_{DC}\dfrac{T_{ccw}sin(\pi/3)}{T_S} = |\overrightarrow{V_{ref}}|sin(\varphi) \end{cases} \quad (6)$$

By solving (6), T_{cw} and T_{ccw} are obtained in (7), where $m = |\overrightarrow{V_{ref}}|/V_{DC}$ is defined as the modulation index that is also known as the amplitude ratio.

$$\begin{cases} \dfrac{T_{cw}}{T_S} = \dfrac{2}{\sqrt{3}}m \cdot sin(\pi/3-\varphi) \\ \dfrac{T_{ccw}}{T_S} = \dfrac{2}{\sqrt{3}}m \cdot sin(\varphi) \end{cases} \quad (7)$$

For minimizing switching loss, T_0 and T_7 (known as the active time of $\overrightarrow{V0}$ and $\overrightarrow{V7}$) are split into two equal parts and distributed into the beginning and the end of T_S as shown in Figure 5. This leads to a PWM aligning method named center-aligned PWM. It can be seen that the actual PWM frequency is reduced by twice as there is no transition between two single consecutive switching cycles.

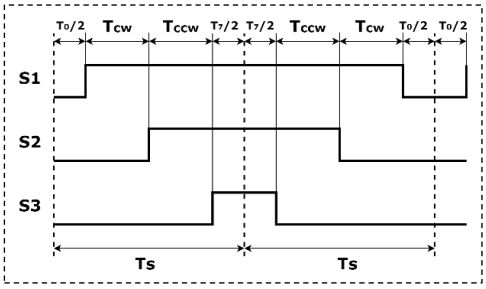

Figure 5. Conventional SVM switching waveforms

Figure 3 has pointed out that the maximum modulation index that could be utilized for sinusoidal modulation times DC source equals the radius of the inscribed circle of the hexagon formed by six active Space Vectors. From the hexagon, the maximum modulation so that the modulus of the reference vector remains unchanged is calculated in (8). This limit ensures there is no harmonic distortion caused by reference vector modulus fluctuation.

$$\max(m) = \frac{V_{DC}\cdot cos(\pi/6)}{V_{DC}} = \frac{\sqrt{3}}{2} \quad (8)$$

From (2) and (8), it can be easily stated:

$$\max\left(|\overrightarrow{V_{phase-neutral}}|\right) = \frac{\sqrt{3}}{3}V_{DC} \quad (9)$$

Then the possible maximum line voltages is:

$$\max(\overrightarrow{V_{phase-phase}}) = \frac{\sqrt{3}}{3}V_{DC}\cdot\sqrt{3} = V_{DC} \quad (10)$$

From (10), the utilization of the DC voltage source of SVM is proved. For the same modulated phase-to-phase voltages, the DC voltage level could be decreased by nearly 13.4% than Sine PWM. The vector length relationships are demonstrated in Figure 7.

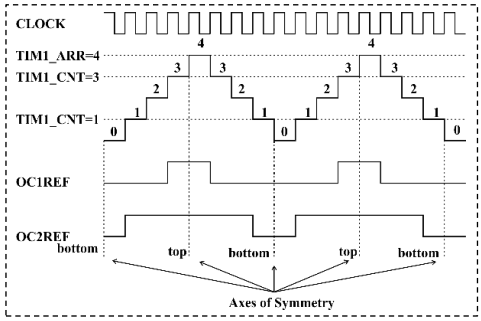

Figure 6. TIM1 center-aligned PWM mode 1

If the deadtime is negligible during the switching cycle, the line voltages will be perfectly recovered in case the VSI is combined with a full three-phase diode rectifier bridge in a drive system. This gives the systems operating with general AC motors the ability to be easily upgraded to be speed-controllable by eliminating the source voltage boosting stage.

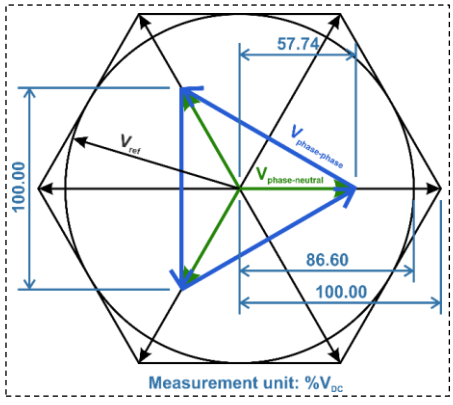

Figure 7. Demonstration of voltage vector length relationships

2.2. Implementation of Space Vector Modulation on STM32F1 microcontroller

2.2.1. Space Vector Modulation from phase and modulus of reference voltage vector

A low-cost high-performance STM32F103 microcontroller (MCU) was utilized in this study.

This MCU is powered by a 72 MHz Cortex M3 CPU and equipped with many powerful peripherals (STMicroelectronics, 2021). The timer chosen for pulse generation was the advanced-control timer TIM1, this timer provides four powerful channels of PWM, capture or compare for various general and special applications. In the center-aligned mode, the value of the counter register $TIM1\_CNT$ is increased from 0 towards the auto-reload value ($TIM1\_ARR$) and then decreased towards 0 by one per rising edge of the input clock and the cycle keeps repeating. The rate of increment and decrement is equal and determined by input clock frequency of the timer (can be divided by a pre-scaler ratio which is configured via $TIM1\_PSC$).

Due to the symmetry of counting operation, the resolution and the output frequency of TIM1 have decreased by twice, this coincidentally matches with the consequence of the Conventional SVM switching rule, resulting in:

$$T_{PWM,actual} = 2T_S \quad (11)$$

It could be seen from Figure 5 that there is no special requirement for the timer except the center-aligned PWM mode 1 and all three output channels are configured to work in PWM Mode 1. Thus, CMS bits in $TIM1\_CR1$ are assigned to a value of 01_2. Figure 6 describes the behavior of $OC\langle x\rangle REF$ signals in center-aligned PWM Mode 1 by default settings, where x denotes the channel number. Without deadtime insertion and extra settings specified, the level of the positive output pin $OC\langle x\rangle$ on Channel $\langle x\rangle$ coincides with $OC\langle x\rangle REF$ signal. This behavior is suitable for the Conventional SVM switching rule that is presented in Figure 5.

$$T_{PWM,actual} = 2 \cdot TIM1\_ARR/F_{CLOCK} \quad (12)$$

In Figure 6, the timer auto-reload register $TIM1\_ARR$ equals 4 for example, $TIM1\_CCR1$ and $TIM1\_CCR2$ and are assigned to 3 and 1, respectively. $OC\langle x\rangle REF$ output signal remains high if $TIM1\_CNT \geq TIM1\_CCR\langle x\rangle$ or low if $TIM1\_CNT < TIM1\_CCR\langle x\rangle$. If a channel is working in PWM Mode 2, its $OC\langle x\rangle REF$ output signal will be inverted (Zhu, 2017). The period of the timer and the output duty cycle of a specific channel is given in (12) and (13), respectively.

$$D\langle x\rangle = 1 - OC\langle x\rangle REF/TIM1\_ARR \quad (13)$$

The actual switching frequency F_{PWM} was chosen to be 5 kHz, this frequency is suitable for most of the common motor speed control applications. At 5 kHz, the VSI generates a moderate amount of audible noise. The designed system in this paper utilizes an intelligent power module (IPM) whose model is FNA41560. The IPM supports integrated IGBT drivers allowing them to be directly connected to the PWM output channels of the MCU. The chosen PWM frequency is recommended by the IPM manufacturer; it also yields a wider safe operating area. For the given PWM frequency, assuming that the MCU system clocks run at the highest available frequency (72 MHz), $TIM1\_ARR$ is obtained using the following formula:

$$TIM1\_\text{ARR} = 72 \cdot 10^6/(2T_{PWM}) = 7200 \quad (14)$$

The STM32F1 advanced-control timer TIM1 module contains a post-scaled counter named Repetition counter ($TIM1\_RCR$), this counter is increased every time $TIM1\_CNT$ reaches $TIM1\_ARR$ or 0. The Timer Update Event occurs and $TIM1\_RCR$ is reset to 0 every $TIM1\_RCR + 1$ time. When a Timer Update Event occurs, all of the counting or timing registers in TIM1 are updated and the update flag is set (STMicroelectronics, 2021). TIM1 has been configured to update the generated SVM duty cycles to $TIM1\_CCR\langle x\rangle$ every time the timer counter reaches 0 (at the "bottom" axis of symmetry), for best stability and symmetry maintenance. The drawback of this interrupt configuration is that the response time of the whole SVM routine including SVM duty cycle value calculation and output pulse generation is slowed down. The update is performed within TIM1 Update Interrupt Service Routine.

The SVM duty cycle is obtained from (7). To deal with sine trigonometric function, a look-up table ($s\_lookup[]$) has been utilized. This table contains 1024 entries fitting into a sector of $\pi/3$, giving an angle resolution of 0.0586°. The values of these entries are pre-calculated using MS Excel and upscaled by a factor of $8 \cdot 7200 = 57600$ to be compatible with unsigned 16-bit fixed-point arithmetic. The values will later be downscaled by 8 before being passed to $TIM1\_CCR\langle x\rangle$, where 7200 is the period register $TIM1\_ARR$ of TIM1. Formula (15) represents the values of the array entries and has been manipulated for generating the entries in the look-up table, where i represents the entry index within a specific sector and ranges between [0; 1023] corresponding to the angle between $\overrightarrow{V_{ref}}$ and its clockwise adjacent Space Vector.

$$s\_lookup[i] = 57600sin(i\pi/3069) \quad (15)$$

Since there is only the commutation of the Space Vectors between sectors, this look-up table can be

utilized for all sectors by considering the adjacent Space Vectors of $\overrightarrow{V_{ref}}$. From (16) and (17), the duty cycle values for generating $\overrightarrow{V_{ref}}$ in each sector passed to $TIM1\_CCR\langle x\rangle$ are given in the following table where Phase a control signal is implicitly connected to PWM Channel 1 positive output, Phase b control signal is connected to PWM Channel 2 positive output and so on for Phase c control signal:

Table 2. Duty cycle in each sector for PWM channels

Sector	Channel 1	Channel 2	Channel 3
I	T_z	$T_z + T_{cw}$	$T_{PWM} - T_z$
II	$T_z + T_{ccw}$	T_z	$T_{PWM} - T_z$
III	$T_{PWM} - T_z$	T_z	$T_z + T_{cw}$
IV	$T_{PWM} - T_z$	$T_z + T_{ccw}$	T_z
V	$T_z + T_{cw}$	$T_{PWM} - T_z$	T_z
VI	T_z	$T_{PWM} - T_z$	$T_z + T_{ccw}$

In Table 2, T_z is the total time of inactive vectors. They are computed as follows:

$$T_z = (T_{PWM} - T_{cw} - T_{ccw})/2 \quad (16)$$

Thanks to fixed-point arithmetic, a real number can be processed in the processors that do not support floating-point instructions with fewer instructions compared to software-implemented floating point operations. The idea behind this arithmetic is that the value of a number will be first upscaled, passed to computations and finally downscaled into the desired range. The larger upscaling factor is, the better precision will be achieved.

The m_i modulation index on the MCU system has been mapped to the range of [0; 65535] which can be expressed by the unsigned 16-bit integer type. Thus, T_{cw} and T_{ccw} can be computed as:

$$\begin{cases} T_{cw} = \dfrac{m\_i}{65536} \cdot \dfrac{s\_lookup[i]}{8} \\ T_{ccw} = \dfrac{m\_i}{65536} \cdot \dfrac{s\_lookup[1023 - i]}{8} \end{cases}$$
$$\Rightarrow \begin{cases} T_{cw} = \dfrac{m\_i \cdot s\_lookup[i]}{524288} \\ T_{ccw} = \dfrac{m\_i \cdot s\_lookup[1023 - i]}{524288} \end{cases} \quad (17)$$

2.2.2. Reference voltage vector rotating algorithm for V/f open-loop control scheme

For the V/f control scheme, the reference voltage vector in the αβ or polar reference frame should rotate at a certain speed and hold a suitable value in modulus. A method to rotate the vector was proposed by Parekh (2015). It was stated that the index of the look-up table must be increased by a computed amount based on the rotating speed. This speed is corresponding to AC output voltage frequency. At high output frequency, this method works fine by shifting a large amount of the array index, but it shows a major drawback when working in near-zero frequency region. By shifting a non-zero amount of index, the modulated output voltage cannot maintain a very long period and hence, a near zero-frequency is unachievable. Because the shifting amount is an integer number, at the high frequency region, the frequency precision is poor as well. In this study, a novel method for achieving near-zero frequency has been developed. This method is presented as follows:

As mentioned, each sector contains a fixed amount of 1024 entries and thus, 6 sectors contain a total amount of 6144 entries. The method proposed in this article is based on the idea of using coaxial gears, assuming the following points:

– Two variables representing two gears are utilized for entry index shifting. These gears are coupled together on a common shaft fixed to the hexagon formed by Space Vectors and have the same module.

– Imagining that $\overrightarrow{V_{ref}}$ is static, then the hexagon and the gears rotate around at the same speed and in reverse to the inherent direction of $\overrightarrow{V_{ref}}$.

– The bigger gear has 2^n teeth on it. The smaller one has 6144 teeth which is the number of entries in the whole 6 sectors.

The coupling and the rotation of these coaxial gears are demonstrated in Figure 8. In case the coaxial gear system has not been utilized, there is no bigger gear and the shifting operation (the act of rotation) will be undertaken by the teeth of the small gear.

$$k = \frac{6144}{2^n} j \quad (18)$$

With a bigger gear attached to this system, the same number of teeth will be taken into account for the rotation. The difference is that the rotation is done indirectly on the bigger gear. This means the bigger gear will be rotated by j teeth every TIM1 Update Interrupt Service Routine is served. This results in the shifted teeth on the smaller gear k, which is given by (18). If n is chosen to be sufficiently large, k will be far smaller than j, which leads to a near-zero AC frequency. k will get the result of an integer division since it must be an integer number.

Therefore, the shifting amount of the reference vector can be whether zero or non-zero for every duty cycle update event, depending on the result of the integer division. The denominator is chosen to be 2^n because the division by 2^n is performed with a bit shifting operation. Such bitwise operations are widely supported by almost all ranges of MCU and the required CPU instruction cycles are inherently low. This is the main idea of how the upscaling and downscaling factor of fixed-point implementation is chosen. In this work, n is chosen to be 30.

Without a big gear, the integer variable representing the smaller gear will have to be increased by approximately $6144f$ in a second for f Hz AC output. In other words, it will be continuously increased by $6144f/5000$ every time TIM1 Update Interrupt Service Routine is served. Thus, the frequency precision $p_{f,small}$ at f Hz of this method is given:

$$p_{f,small} = \frac{5000}{6144f} = \frac{625}{768f} \quad (19)$$

Similarly, the precision $p_{f,big}$ at f Hz of the proposed method with coaxial gear system is given:

$$p_{f,big} = \frac{5000}{2^{30} \cdot f} = \frac{625}{134217728f} \quad (20)$$

From (19) and (20), it can be seen that the frequency precision of the proposed method is improved by approximately 175000 times. The precision at 1 Hz of the proposed method is $4.6566 \cdot 10^{-6}$ Hz in comparison with 0.8138 Hz and 0.003 Hz of the methods presented by Minas et al. (1999) and Parekh (2015). This advantage of frequency precision gets the implementation well compatible with the control systems requiring high resolution of control signals.

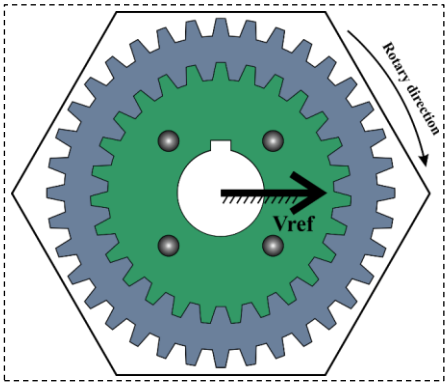

Figure 8. The rotating coaxial gear system

The MCU coding is based on the flowchart depicted in Figure 10. Where, j is obtained by considering the desired output AC frequency; T_{cw}, T_{ccw}, T_z are computed using (16) and (17); the duty cycle registers are loaded with corresponding values as shown in Table 2. For proper sector determination, the gear variable is checked every time the SVM computation is executed.

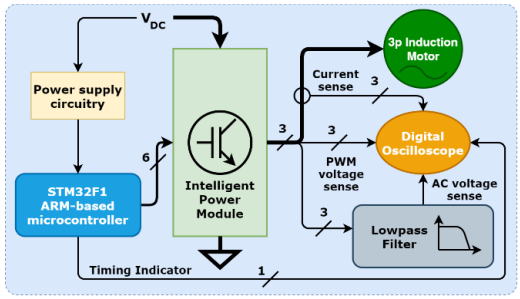

Figure 9. System block diagram

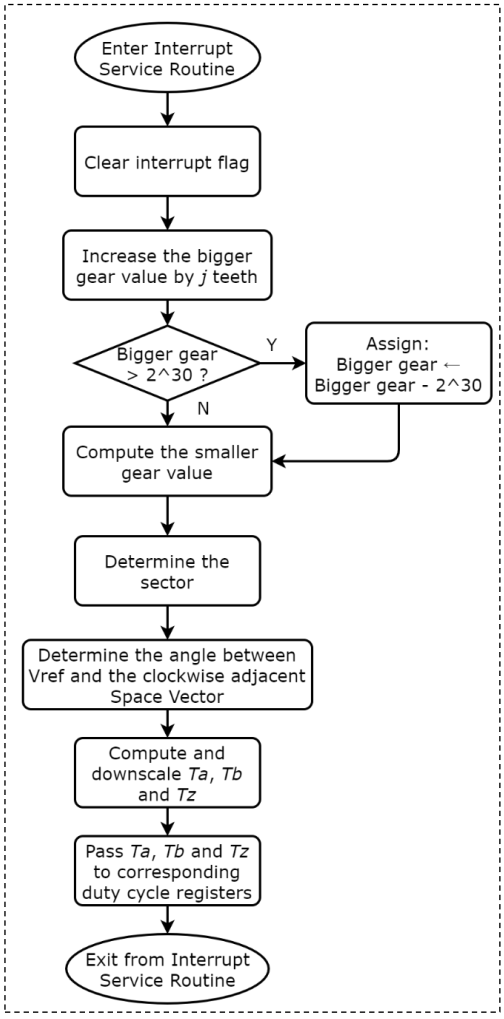

Figure 10. Flowchart of SVM computation

2.3. Experimental Set-up

The set-up of the conducted experiment in this article is presented in Figure 11, the measurements are depicted in the diagram shown in Figure 9.

Figure 11. Experimental set-up

The waveforms of motor line currents, the output AC voltages and the output PWM signals are captured and analyzed by a digital oscilloscope. The synthesized frequency is configured to increase from 0 Hz to 50 Hz within 3.277 seconds along with current measurement. At the same time, the modulation index increases from 0 to the maximum allowed value (65535). The PWM frequency is fixed at 5 kHz. For motor currents measurement, the utilized induction motor is the one that has been installed into a paddle-wheel aerator which is usually utilized for shrimp farming. Figure 12 presents a paddle-wheel working with the voltages supplied from the inverter. The ratings of this aerator are: (line voltage: 380/220 VAC; frequency: 50 Hz; power: 1.5 kW at 380 VAC; paddle count: 4; speed: 105 RPM).

Figure 12. Working paddle-wheel aerator connected to the inverter

3. RESULTS AND DISCUSSION

The frequency precision before and after applying the proposed method is demonstrated in Figure 13, Figure 14 and Figure 15. Since the digital oscilloscope has a limited degree of measuring low frequency, the experiment was conducted in simulation on PSIM. Supposing 1 Hz output is demanded, it is whether only 0.8 Hz or 1.6 Hz can be achieved without applying the proposed method. This is shown in Figure 13 and Figure 14. Nonetheless, it is possible to obtain an 1 Hz output with the proposed vector rotation method, which is displayed in Figure 15. The frequency error is about 0.004%, which is partly from the simulating operations.

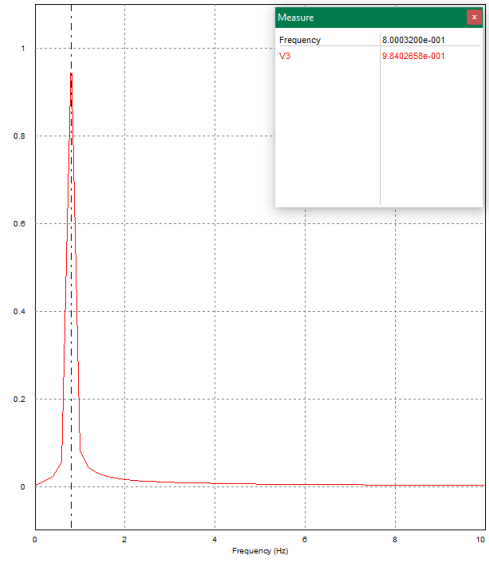

Figure 13. Lowest non-zero output frequency without applying the proposed method

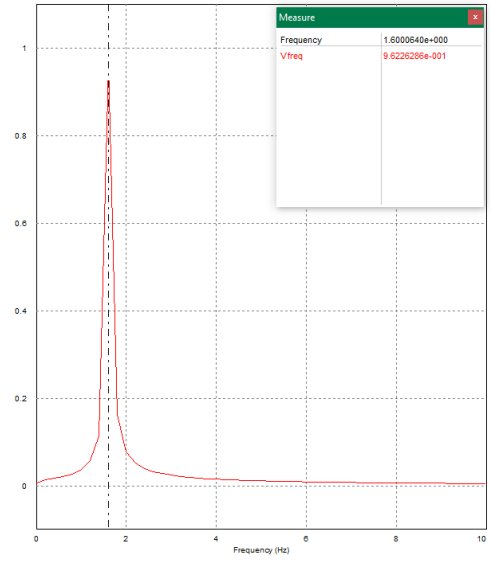

Figure 14. Next-to-lowest non-zero output frequency without applying the proposed method

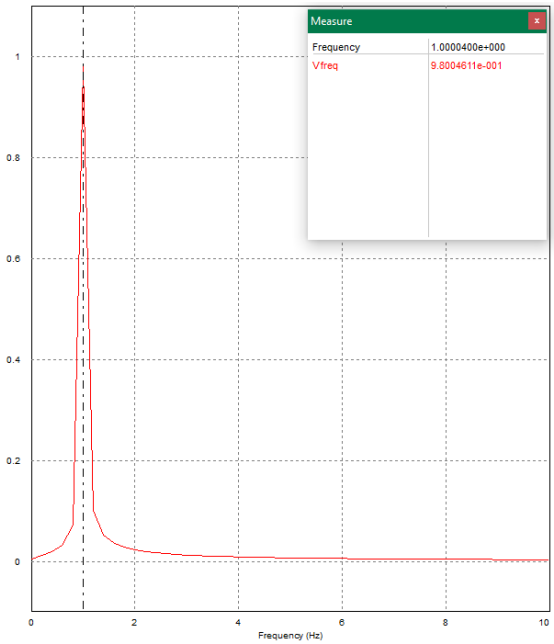

Figure 15. Precise output frequency with applying the proposed method

Figure 16 shows the filtered ramping-up phase voltages with respect to the internal virtual neutral point in the low pass filter. These voltages are the actual voltages being seen by motor windings. The ramp-up occurring within 1.635 seconds involves the frequency ramp between [0; 50 Hz] and the amplitude ramp between [0; 1] by modifying the modulation index and the AC frequency simultaneously. In all voltage measuring experiments, V_{DC} equals 16 VDC and being sourced from an external power supply, the filter bandwidth for voltage measurement was 234.05 Hz.

Figure 17 shows the filtered AC phase to pseudo-neutral voltages in steady-state. The resultant phase shift is $2\pi/3$. This matches the conventions of the induction motor winding specifications. The amplitude of phase-to-phase voltage was approximately 15 VDC, which can be observed in Figure 18. These voltages were sequentially measured using the oscilloscope Ref Channel feature.

The drop of AC output voltages can be explained by Figure 19. Due to the high- and low-side IGBT saturation voltages, which are specified as top and base levels of PWM output in the Figure, the drop is understandable. The effective output PWM range is calculated in (21). This demonstrates that the implementation could utilize the whole DC supply.

$$V_{out,effective} = Top - Base = 14.962 \quad (21)$$

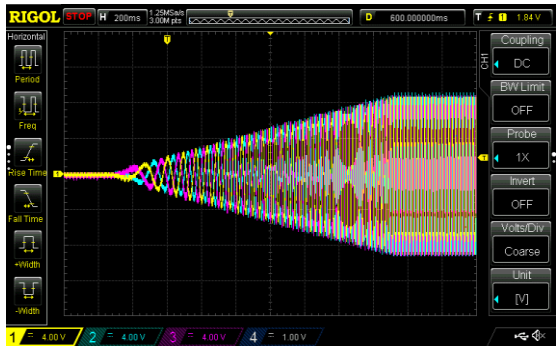

Figure 16. Ramp-up phase voltages

The results of current measurement are shown in Figure 20, Figure 21 and Figure 22. In this experiment, the DC voltage source is obtained from the utility grid using a passive diode bridge rectifier. In the steady state, the grid and its rectified voltages are 202 VAC and 237 VDC, respectively. The ramp-up time is now set to 3.277 seconds in order to avoid the motor inrush current. It can be seen that the transition in current frequency from zero to more than 10 Hz is very smooth. This has proved the effectiveness of the novel vector rotating algorithm.

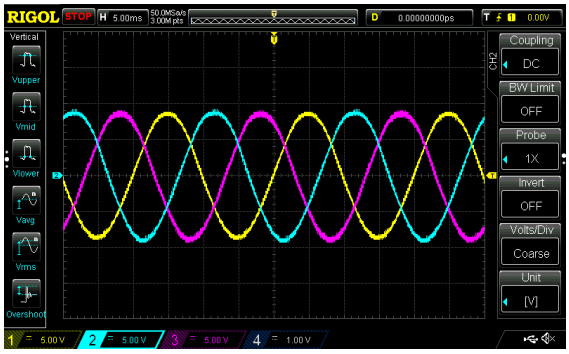

Figure 17. Steady-state phase voltages

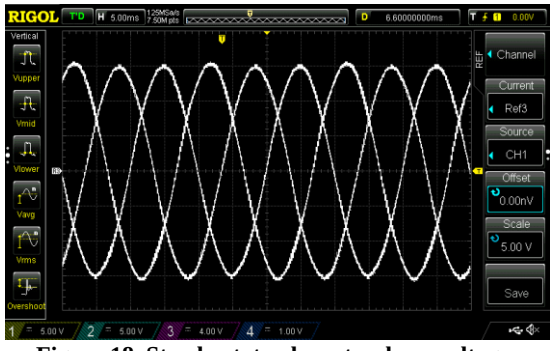

Figure 18. Steady-state phase-to-phase voltages

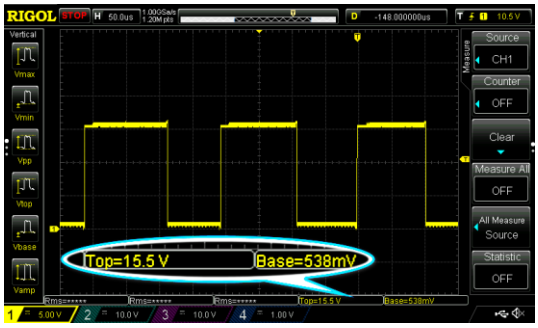

Figure 19. A closer look to PWM output signal

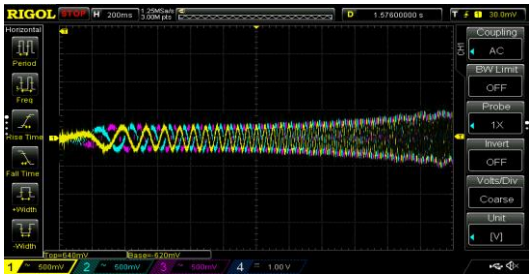

Figure 20. Ramp-up current with the aerator

Figure 21. A closer look to motor current in ramp-up state

As the motor windings are connected in star configuration, Figure 22 shows the steady-state phase-to-neutral currents of the motor. These currents were observed through isolated current sensors with 146 mV/A transfer ratio. The difference in amplitudes between them was due to the difference in motor winding parameters.

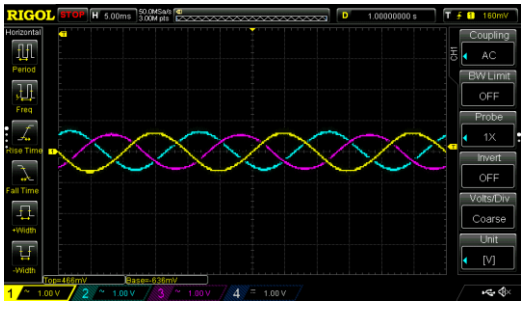

Figure 22. Steady-state motor currents

The frequency of TIM1 Update Interrupt Service Routine was measured and is shown in Figure 23. An indicator IO pin was utilized for the measurement. The pin was set to high right before TIM1 Update Interrupt Service Routine executed the SVM computation and cleared to low right after the SVM computation finished.

Figure 24 and Figure 25 show the time required for the SVM computation with and without vector rotation algorithm execution, respectively, using the same technique as the interrupting frequency measurement.

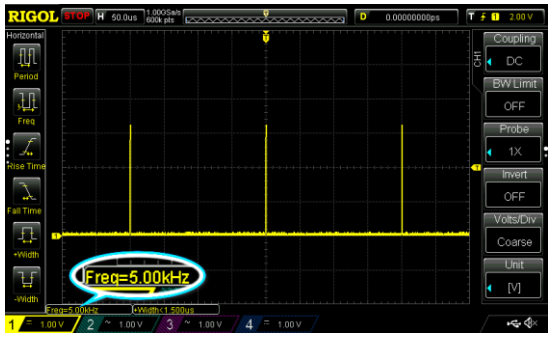

Figure 23. Frequency of TIM1 Update Interrupt Service Routine

The corresponding execution times were 1.72 µs and 1.9 µs per 5000^{-1} s. At 72 MIPS CPU instruction frequency, the CPU usages were 0.684 MIPS (0.95%) for the whole SVM computation including vector rotation algorithm execution and 0.6192 MIPS (0.86%), not including vector rotation algorithm execution. The mentioned instruction frequency was the CPU clock frequency as well. This measurement highlighted that the proposed implementation was both effective and suitable for MCUs with modest computation power.

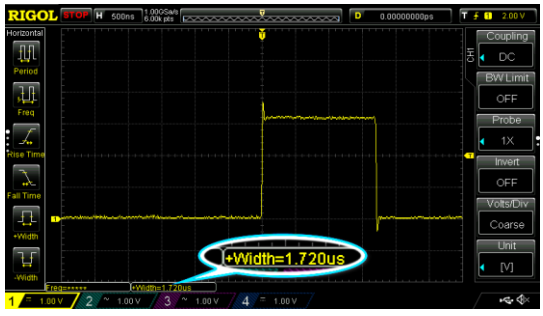

Figure 24. Maximum execution time of the SVM duty cycle computation without vector rotation

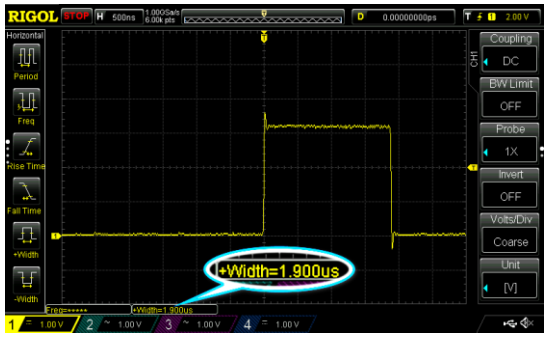

Figure 25. Maximum execution time of the SVM duty cycle computation with vector rotation

4. CONCLUSION

This paper has thoroughly outlined the implementation of the Space Vector Modulation for an induction motor using a low-cost ARM-based microcontroller with a novel method for reference voltage vector rotation. The results highlight that this technique can successfully utilize approximately 100% of the DC voltage source, which is an unignorable optimization when an IPM is chosen to be the motor driver instead of an inverter bridge constructed from discrete components. The required MIPS is very low and suitable for low-cost microcontrollers that support at least three channels of PWM. Furthermore, the novel vector rotating algorithm for overcoming near-zero frequency glitches has been proposed under a new perspective and tested. This algorithm is the significant basis for deploying further vector control strategies in the future, where the torque control at 0 Hz is an important feature.

The implementation presented in this article can be utilized for further work, such as small solar powered systems where the ratio between the DC source for the inverter and the array voltage might be relatively low with a conventional boost converter stage. The power control structures of such solar-powered systems can also take advantage of the mentioned output frequency precision.

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