Trabajo Fin de Grado Grado en Ingeniería Aeroespacial

Reliability analysis and optimization of the LISA Phasemeter Frequency Distribution System

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> Dpto. Ingeniería Aeroespacial y Mecánica de Fluidos Escuela Técnica Superior de Ingeniería Universidad de Sevilla

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El tribunal nombrado para juzgar el trabajo arriba indicado, compuesto por los siguientes profesores:

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Resumen Global

Título: Análisis de fiabilidad y optimización del Sistema de Distribución de Frecuencia del Fasómetro de LISA.

Resumen del trabajo: Tras introducir la misión espacial LISA y sus objetivos, se expone la metodología empleada para el análisis de fiabilidad del módulo electrónico objeto de este trabajo, así como el modelo térmico asumido para el mismo. Como punto de partida para su optimización, se obtiene un resultado de fiabilidad preliminar del módulo, cuyos resultados se buscan mejorar respaldados por los análisis térmicos realizados con distintos parámetros. Además, se propone una modificación estructural del módulo. Finalmente se extraen conclusiones de los resultados obtenidos y se propone una línea de trabajo futuro.

Palabras clave: Fiabilidad, redundancia, diagrama de bloques de fiabilidad, tasa de fallo, temperatura de operación, modelo térmico.

Conclusiones: El resultado final de fiabilidad arrojado por los cálculos es muy favorable, lo que sugiere no implementar el módulo redundante propuesto, ahorrando así masa y coste. Por otro lado, la mejora de fiabilidad tras la optimización ha sido muy reducida dada la baja tasa de fallo de los componentes de partida. A pesar de ello se ha conseguido una reducción de peso del módulo de un 17.84%.

Resumen

A escala astronómica, el principal motor de muchos de los procesos del Universo es la gravedad. El objetivo de la misión LISA es la detección de ondas gravitacionales de baja frecuencia desde del espacio. Dada la imposibilidad de sustituir o reparar el equipo de las misiones espaciales no tripuladas, uno de los factores fundamentales es la fiabilidad de la instrumentación a bordo.

El objetivo de este proyecto es estudiar la fiabilidad de uno de los módulos electrónicos que componen el fasómetro de la misión LISA, así como la optimización de la misma. El análisis de la fiabilidad se basa en la arquitectura interna de las placas electrónicas y en la interacción entre los componentes. El proceso de optimización se centra en la búsqueda de un aumento de la fiabilidad mediante una mejora del rendimiento térmico de los componentes. Otro de los objetivos desarrollados en este documento es establecer una disposición de los componentes en la placa, de forma que se cumplan los requisitos necesarios de cada uno para su correcto funcionamiento. Por último, se proponen modificaciones en la estructura del módulo para reducir el peso total.

Abstract

On an astronomical scale, the main driver of many of the processes in the Universe is gravity. The goal of the LISA mission is to detect low-frequency gravitational waves from space. Given the impossibility of replacing or repairing the equipment of unmanned space missions, one key factor is the reliability of the on-board instrumentation.

The objective of this project is to study the reliability of one of the electronic modules that make up the Phasemeter of the LISA mission, as well as its optimisation. The reliability analysis is based on the internal architecture of the electronic boards and the interaction between components. The process focuses on the search for an increase in reliability based on an improvement in the thermal performance of the components. Another of the objectives developed in this document is to establish a layout of the electronic devices on the board so that the necessary requirements of each one are met in order for them to operate correctly. Finally, modifications to the module structure are proposed in order to reduce the overall weight.

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Notation

| Δ | Increment |
|--------------|---------------------------------------|
| Ea | Activation energy |
| $	heta_{JC}$ | Junction to case thermal resistance |
| ΔT | Temperature increment |
| h | Layer conductance |
| q | Heat flux by conduction |
| u | Velocity vector of translation motion |
| | |

Constants

| Notation | Description | Value | SI-Unit |
|-------------------------------------|--|-----------------------|-------------------------|
| ${ m M}_{\odot}$ | Mass of the Sun | $1.988 \cdot 10^{30}$ | kg |
| С | Speed of light | 299792458 | $m \cdot s^{-1}$ |
| k _B | Boltzmann's constant | $0.862 \cdot 10^{-4}$ | $eV \cdot K^{-1}$ |
| $ ho_{Al}$ | Density of Aluminium | 2700 | $kg \cdot m^{-3}$ |
| $ ho_{CHO}$ | Density of CHOTHERM | 1550 | $kg \cdot m^{-3}$ |
| $ ho_{Cu}$ | Density of Copper | 8930 | $kg \cdot m^{-3}$ |
| $ ho_{FR4}$ | Density of FR4 | 1850 | $kg \cdot m^{-3}$ |
| k_{Al} | Thermal conductivity of Aluminium | $1.67 \cdot 10^{2}$ | $W \cdot m^{-1} K^{-1}$ |
| k _{CHO} | Thermal conductivity of CHOTHERM | 2.6 | $W \cdot m^{-1} K^{-1}$ |
| k_{Cu} | Thermal conductivity of Copper | $3.98 \cdot 10^{2}$ | $W \cdot m^{-1} K^{-1}$ |
| k_{Al} | Thermal conductivity of Aluminium | $1.67 \cdot 10^{2}$ | $W \cdot m^{-1} K^{-1}$ |
| k_{FR4x} | Thermal conductivity of FR4 in \hat{x} | $9.35 \cdot 10^{-1}$ | $W \cdot m^{-1} K^{-1}$ |
| k_{FR4v} | Thermal conductivity of FR4 in \hat{y} | $9.35 \cdot 10^{-1}$ | $W \cdot m^{-1} K^{-1}$ |
| k_{FR4z} | Thermal conductivity of FR4 in \hat{z} | $3.17 \cdot 10^{-1}$ | $W \cdot m^{-1}K^{-1}$ |
| $C_{p_{Al}}$ | Specific heat of Aluminium | $8.96 \cdot 10^{2}$ | $J \cdot kg^{-1}K^{-1}$ |
| $C_{p_{CHO}}$ | Specific heat of CHOTHERM | 1000 | $J \cdot kg^{-1}K^{-1}$ |
| $C_{p_{Cu}}$ | Specific heat of Copper | $3.85 \cdot 10^{2}$ | $J \cdot kg^{-1}K^{-1}$ |
| | Specific heat of FR4 | $7.95 \cdot 10^{2}$ | $J \cdot kg^{-1}K^{-1}$ |
| $C_{p_{FR4}} \ \sigma_{Al}^{yield}$ | Yield strength of Aluminium | $276 \cdot 10^{6}$ | Pa |
| $\sigma_{Al}^{ultimate}$ | Ultimate tensile strength of Aluminium | $310\cdot 10^6$ | Pa |

Acronyms

| AEI | Albert Einstein Institute |
|------|---|
| ADC | Analog to Digital Converter |
| BEE | Back-End Electronics |
| CAD | Computer Aided Design |
| CFDS | Clock side bands Frequency Distribution System |
| СТМ | Compact Thermal Model |
| DHLC | Data Handling and Laser Control |
| ESCC | European Space Components Coordination |
| EOM | Electro-Optic Modulator |
| ESA | European Space Agency |
| FBD | Functional Block Diagram |
| FDS | Frequency Distribution System |
| FIT | Failure In Time |
| GW | Gravitational Wave |
| IFO | Interferometer |
| LIGO | Laser Interferemeter Gravitational Wave Observatory |
| LISA | Laser Interferometer Space Antenna |
| MTTF | Mean Time To Failure |
| NASA | National Aeronautic and Space Administration |
| PCB | Printed Circuit Board |
| PMS | Phase Measurement Subsystem |
| PSM | Power Supply Module |
| PT | Pilot Tone |
| REF | Reference |
| RF | Radio frequency |
| SPF | Single Point Failure |
| TM | Test Mass |
| TFP | Temperature Reference Points |
| USO | Ultra-Stable oscillator |
| VFDS | VCXO Frequency Distribution System |
| | |

1 Introduction

The detection of the first gravitational wave in 2015 was a revolution for the scientific world, opening a whole new window to explore the Universe. This occurrence, GW150914, was observed by the onground gravitational waves detectors LIGO (Laser Interferometer Gravitational-Wave Observatory). These waves were caused over a billion light years away by the merger of a pair of black holes around $36M_{\odot}$ and $29M_{\odot}$. The resulting black hole had a mass of $62M_{\odot}$, leaving $3.0M_{\odot}$ of energy radiated away as gravitational waves [1]. The obtained frequency of the signal rises, ranging from 40 to 250 Hz, as shown in Figure 1.1. Nevertheless, the frequency of gravitational waves that can be sensed from Earth is limited to a specific range of 40-7000 Hz [2], owing to the effects of seismic noise, such as the atmosphere or the Earth's own gravity. In addition, the size of the detectors is limited due to the planet's curvature, which also limits the bandwidth.

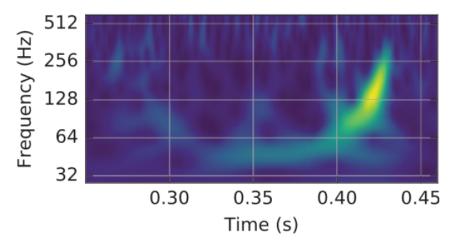


Figure 1.1 Frequency data from the event GW150914 at the Washington and Louisiana observatories on 14 September 2015 [1].

This limitation in the frequency range was the motivation for the mission LISA (Laser Interferometry Space Antenna), on which this work is focused, becoming the first space-based observatory for gravitational waves. LISA will allow access to a band of gravitational waves from about 0.1 mHz to 100 mHz. This low-frequency range will provide information about how binary stars formed in our Milky Way, the formation of the first seed black hole or even the cosmic background gravitational radiation [3]. LISA will provide information from a part of the Universe that will forever remain undetectable with light. By 'listening' to gravity, it will be possible to see further than ever before.

1.1 Nature and detection of Gravitational waves

General Relativity replaces the Newtonian conception of gravitation as instantaneous action at a distance with a geometric one, relating that space and time do not have an independent existence but are in intense interaction with the physical world. The essence of this theory is that matter and energy create a curve four-dimensional in the fabric of space-time, and this curvature influences the movement of matter. Gravitational waves are a consequence of this basis. If a mass distribution has a changing asymmetric movement (like acceleration spinning), then gravitational waves appear as space-time indenta-

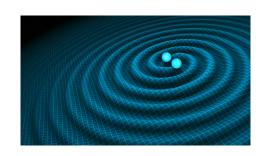


Figure 1.2 GWs generated by binary neutron stars [4].

tions travelling outwards as ripples in space-time [5]. This concept is illustrated in Figure 1.2

For a better understanding of this idea, they are compared to the well-known electromagnetic waves, from which almost all information about the Universe has been obtained so far. Gravitational waves are the solution for Einstein's field equations, that determine the interaction between mass and curvature of space-time, in the same way as electromagnetic waves are the Maxwell's equations solution that relates the relationship between electric charges and electromagnetic fields.

Nevertheless, gravitational waves are fundamentally different. Electromagnetic waves propagate in space and time, but gravitational waves are waves of the space-time fabric itself. They stretch and squeeze any distribution of matter or energy by which they go through, acting transverse to the direction of wave propagation. The propagation of GWs in the two polarizations is presented in Figures 1.3 and 1.4. In particular, the graph in Figure 1.4 presents the travelled distance by the gravitational wave, described by a strain amplitude h, while the rest shows the four phases of one particle deformation cycle: the strain design contracts space in the transverse dimension, whereas it expands along the orthogonal direction within the transverse plane.

Furthermore, they have a different nature. On one side, electromagnetic waves are created by the acceleration of electric charges. As charge only exists in two polarities, electromagnetic radiation is caused by a dipole moment of the charge distribution. On the other side, gravitational waves are generated by accelerated masses. Due to mass and momentum conservation, gravitational waves can only be created by a variable mass *quadrupole*.

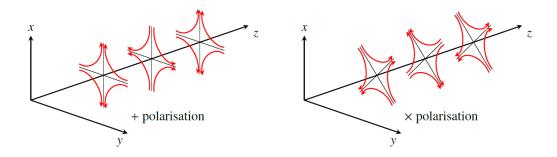


Figure 1.3 GWs propagating along the z axis in the two different polarisations ("+"and "x") [3].

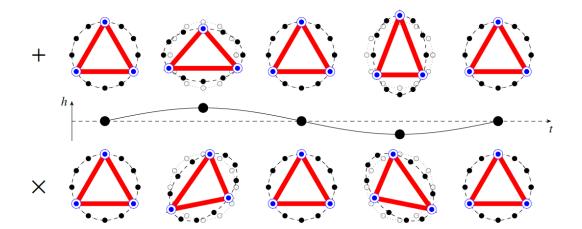


Figure 1.4 Passage of a GW through a ring of masses [3].

Therefore, it can be said that the nature of gravitational waves is a change in the quadrupole moment of the mass distribution. This is why spherically symmetrical gravitational effects do not generate gravitational radiation. An example of this is a perfectly symmetric collapse of a supernova, while a binary system will always emit GWs [5].

Gravitational waves' effects are apparent. They bend space-time, changing the distance between macroscopic free objects. When a gravitational wave passes through the Solar System it induces a time-varying strain in space that periodically changes the distances between all bodies in the Solar System in a direction perpendicular to the direction of wave propagation. The main problem is that the relative change in length due to the passage of a gravitational wave is exceedingly tiny.

In order to detect gravitational waves, it is necessary to measure these variations in the distance between objects with extremely high precision (pm to nm). The measurement process used is laser interferometry. For that, a laser beam pulse is established between a free-floating source and a free-floating reflecting mirror. The basis of interferometry is to constantly measure the time it takes the laser beam to return after being reflected in the mirror. When a gravitational wave crosses the laser path, it will stretch space and alter the distance between the source and the mirror. As a result, the laser light will return at a different time. LISA's measurement system is explained in section 1.2.

1.2 LISA

The principal aim of the Laser Interferometry Space Antenna (LISA) is the detection of gravitational waves in a frequency range from 0.1 mHz to 100 mHz, which is impossible to measure in ground-based experiments. LISA project is based on the success of LISA Pathfinder, whose goal was to pave the way for LISA mission. More precisely, its main objective was to test the core assumption of gravitational wave detection and general relativity: that free particles follow the waves of space-time curvature, as well as demonstrate the new technologies in a space environment that will be used in LISA, such as inertial sensors or high precision laser interferometry to free-floating mirrors [6].

The LISA mission will be made up of three spacecraft flying in a triangular formation, (one 'mother' at the vertex and two 'daughters' at the ends) with a nominal separation distance of 2.5 million km, which follow an Earth-trailing heliocentric orbit between 50 and 65 million km from Earth. The distance between the spacecraft, the interferometer arm length, determines the frequency

range in which LISA is able to make observations; it was carefully chosen to allow the observation of most of the interesting sources of gravitational radiation. The centre of the triangular formation is located in the ecliptic plane, more precisely, 1 AU from the Sun and $19^{\circ}-23^{\circ}$ behind the Earth. Furthermore, the plane of the triangle is inclined at 60° with respect to the ecliptic.[5]

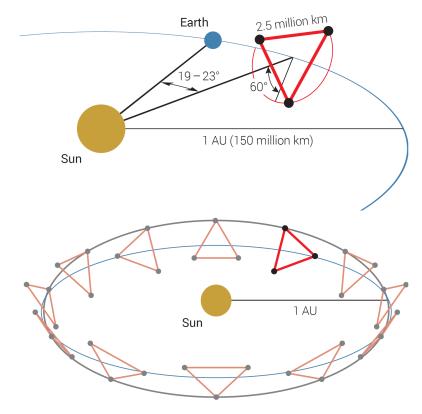


Figure 1.5 Depiction of the LISA Orbit [7].

The LISA orbital configuration mentioned above is depicted in Figure 1.5. Due to the laws of celestial mechanics, the triangle rotates almost rigidly about its centre while orbiting around the Sun, with variations of arm length and opening angle around the per cent level [8]. The launch and transfer for LISA will be carried by a dedicated Ariane 64 vehicle [9].

LISA will detect gravitational waves using laser interferometry technology due to the minuscule distance variation caused. The spacecraft are connected using optical links over the 2.5 million km long arms. This path length distance is continuously measured by heterodyne laser interferometers in both directions along each arm. This methodology will ensure to measure at all times the distance along the three free-falling test masses, which are contained inside co-orbiting drag-free spacecraft without having any contact, in order to detect variations caused by a passing gravitational wave. LISA can measure displacements on the order of fractions of a picometer [7]. The distance variation between the test masses due to the gravitational waves are minute (nm to pm) compared with the alteration caused by solar system celestial dynamics (around 10000 km), but can be clearly distinguished since the former have frequencies about mHz, whereas the latter have periods of many months and are unnoticeable at mHz frequencies.

LISA can provide unique new information as it constitutes the very first mission that will study the whole Universe based on low frequencies gravitational waves. The science objectives expected of the mission are the following [7]:

- · Research the formation and evolution of compact binary stars in the Milky Way Galaxy
- Track the history, growth and origin of massive black holes throughout cosmic ages
- Understand the astrophysics of stellar origin black holes
- · Examine the fundamental nature of gravity and black holes
- Detection of a stochastic GWs background of cosmological origin for the first time and probe the rate of expansion of the Universe

Gravitational waves coming from well known galactic binaries, like the X-ray binary 4U1820-30, will also be detected. The intensity and polarisation of these waves has already been predicted by General Relativity. This means that LISA will also be able to test General Relativity by comparing the experimental results with the already predicted ones, checking the accuracy foundations of gravitational physics.

The duration of the mission has great relevance for the reliability study to be carried out, so the proposed nominal mission lifetime of seven years is considered in this work [7].

1.3 Phase Measurement System

The Phase Measurement System (PMS) is part of the spacecraft payload, and it constitutes the core digital signal processing of the Optical Bench. The physical structure of the PMS is presented in Figure 1.6, composed of seven assembled modules that execute distinct functions [10]:



Figure 1.6 PMS physical assembly [10].

- Back-End Electronics (BEE). It constitutes four of the modules that make up the PMS. Their main goal is to set up the incoming signals from the photo receivers, digitize them and obtain their phases. The specific operation differences are detailed below:
 - Long-Arm Back-End-Electronics (LARM-BEE). The LARM-BEE measures the variations in the path length displacements between the optical benches of a LISA arm. Accordingly to this, two of these modules will be required, as each spacecraft is connected with the other two by the Long-Arm path length.

- Test-Mass Back-End-Electronics (TM-BEE). In this case, the Test-Mass Interferometer measures the longitudinal and angular pathlength displacements between the local optical bench and Test Mass.
- Reference Back-End-Electronics (Ref-BEE). The Ref-BEE aim is to procure a phase reference between interferometric measurements, thus establishing a connection between the two local optical benches.
- Power Supply Module (PSM). This module is responsible for conducting the necessary conversions to the primary power received from the platform input and distributing it internally to the rest of the modules and the photo-receivers. Due to the criticality of the power supply of modules for its correct functioning, each of them will have a dedicated supply bus.
- Frequency Distribution System (FDS). The Frequency Distribution System is in charge of generating and distributing all the different frequencies supplying to the rest of the modules of the PMS, necessary for the proper functioning of the whole PMS. In particular, the generated Pilot Tone calibration signal and clock sidebands modulation output, which are explained in Section 1.3.1, have critical performance implications in the complete LISA system.
- Data handling and Laser Control (DHLC). This module houses the primary control of the PMS. It constitutes a control interface for both external and internal functions. The internal functions involve the data interface to the Test Mass-BEE, Ref-BEE and FDS modules. In contrast, the external are those related to the communication with the platform of Laser Assembly or the on/off switching of the photo-receivers.

The PMS is anchored to the satellite at the base, which corresponds to the back surface of the physical assembly shown in Figure 1.6. This anchor point will be of great relevance for the thermal study of the PMS, as it is a thermal reference point (TRP) by design. It is qualified a constant temperature of 20 degrees with a tolerance of $\pm 5^{\circ}C$ degrees [10].

In the following, PMS1 and PMS2 will refer to the two PMS located on each spacecraft. Both are functionally the same. They differ in the configuration of the FDS, which will be configurable either by hardwiring or by command [10].

1.3.1 Frequency Distribution System

For a better understanding of the functioning of this module, it is necessary to mention another of the instruments that make up the LISA payload, the Central Timing Unit (CTU). The current design assumes a single common master ultra-stable oscillator (USO) for each spacecraft. The function of the CTU is to distribute the USO and PPS signal to all subsystems that require timing synchronisation. Synchronisation refers to the need for the events recorded in different modules to happen at the same time with the same timestamp. It is also essential to explain the term clock locking, which means the need to utilise one stable and general source for obtaining all the signal frequencies used in the PMS.

The Frequency Distribution System has the crucial function of getting the USO clock and the PPS signal from the CTU and generating all the frequencies required for the functioning of the Phasemeter. The expected functions of this module are [11]:

- Provide internal distribution of the 10MHz reference clock and PPS signals to the 4 BEE modules and DHLC.
- Synthesis of the Pilot Tone. This signal is one of the most critical signals in the PMS, due to the fact that it constitutes a calibration signal for ADC timing jitter correction, used for

the readout of every ADC channel from the BEE module. The phase fidelity of the Pilot Tone signal limits the ultimate performance of the instrument, as therefore quite sensitive to thermal gradients due to coupling of thermal noise into phase readout performance [12]

• Synthesis and distribution of the clock sidebands modulation signals (either 2.4 GHz or 2.401GHz) locked from the USO external frequency input. The electro-optic modulators (EOM) modulate the outgoing laser beams with reference to this 2.4 GHz oscillator frequency. EOMs transfer their phase noise in sidebands to the other spacecraft where it is compared to the local oscillators' noise. The phase noise of the oscillators is down-converted in the dividers, producing the sampling clock and a pilot tone.[12]. This modulation and transfer of the pilot tone is represented in Figure 1.7

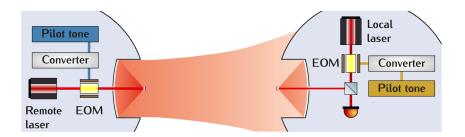


Figure 1.7 Pilot tone phase modulation by electro-optic modulators (EOM) [12].

- Procurement of the 1 MHz signal by frequency mixing process between clock sideband modulation signals.
- Synthesis and distribution of an 80 MHz signal also locked to the USO reference. The obtaining of this signal is crucial because without it, the FPGA of the DHLC module can not work, losing the signal processing of the entire PMS.

The FDS module is divided into two PCBs where all the functions are achieved. One of them is the VCXO Frequency Distribution System (VFDS) electronics, and the other is the Clock Frequency Distribution System (CFDS) electronics. The detailed internal functioning of each board is explained in Sections 3.1.1 and 3.1.2, to carry out the reliability diagram. Since they are be mentioned quite frequently, the abbreviations VFDS and CFDS for each board are be assumed hereinafter.

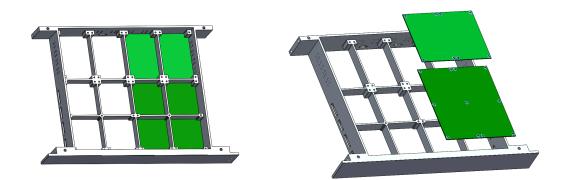


Figure 1.8 Frequency Distribution System disposition.

Figure 1.8 illustrates the structural appearance of the module. The enclosure is the part that confers structural integrity to the PMS, and is common to all the modules to build a regular structure, as presented in Figure 1.6. Inside the enclosure, the VFDS and CFDS boards are proposed to be

8 Chapter 1. Introduction

arranged so that they only occupy half of the module. This is due to the need for a possible redundant FDS architecture, which would be implemented in the same module if the reliability is not high enough.

1.4 Objectives of this work

Given the stringent timing and synchronisation requirements for the correct functioning of the whole mission, the timing and synchronisation architecture in the FDS that provides the locked signal plays a critical role. If any of the devices that make up this module fails, it could lead to a degradation of the performance or a complete failure of the mission. As mentioned in the previous Section 1.3.1, some examples of mission failure related with FDS critical functions are the correct readout of the income signals of the PMS or the functioning of the FPGA from the DHLC.

The focus of this work is not only an internal reliability study of this module's functioning but the possible improvement of these results. As it is explained in section 2.1, the reliability of an electronic component is strongly dependent on the temperature at which it operates. The higher the operating temperature, the higher the probability of failure. The search for a decrease in operating temperature implies an improvement in reliability. To achieve this reduction, different resources will be used such as changing the distribution of the components on the PCB, modifying the parameters that make up the PCB or modifying the enclosure to which they are attached. Finally, one of the objectives of optimisation is the possible reduction of weight while maintaining the performance characteristics of the module.

Furthermore, there is a need to ensure that each electronic component meets the necessary requirements for its proper performance. This is especially critical for the quartz crystals, which are responsible for the locked signals that are distributed to the rest of the system. In order for them to function correctly, they must remain at the lowest possible temperature. There is also a critical need to contemplate the Pilot Tone signal generated in the CFDS. Contrary to the robustness that characterises the differential signal in terms of transmission, this signal is single-ended and therefore extremely sensitive to temperature gradients. High exposure to temperature gradients can lead to a degradation of the signal itself. This means that, as a result of this project, a justified accommodation of the materials on the plates is also obtained, which will be useful for their physical implementation in the future.

In brief, the purpose of this project is to make the necessary modifications to improve the module's reliability, to propose a layout of the components according to the needs of each one for their correct performance, as well as to serve as a future guide for the analyses of the rest of the PMS modules.

1.5 Structure

This project is structured in the following way:

Chapter 1: The context of LISA mission is presented, starting with an explanation of the nature of gravitational waves and its detection, followed by a general description of the mission, Phasemeter and the FDS module. The objectives and the structure of the project are exposed at the end.

Chapter 2: The basic concepts related with reliability are explained, just as the used methodology and the equations. Following that, the assumed thermal model for the module is explained and its

implementation in COMSOL Multhiphysics, as well as the the structural model.

Chapter 3: Firstly, a preliminary reliability study is done. Afterwards, several thermal analyses are carried out to improve these results by modifying different features of the module. In addition, a structural analysis is presented to validate the changes in the structure. Finally, the reliability study based on the influence of the temperature is carried out.

Chapter 4: The final conclusions are exposed and a future line of work is proposed.

2 Theoretical background

This section establishes a theoretical basis that will serve as support for the development of this document and the achievement of its objectives.

2.1 Reliability methodology

Given the enormous scientific importance and amount of money invested in space missions, reliability prediction significantly impacts the design of any space-applicable electronic architecture.

Reliability is understood as the probability that equipment can perform continuously, without failure, for a specified interval of time when operating under stated conditions. For a better understanding of the process to be carried out, some key concepts for conducting reliability analysis are also introduced:

- Failure: an event when equipment is not available to produce parts at specified conditions when scheduled or is not capable of producing parts or performing scheduled operations. For every failure, an action is required.
- MTTF (Mean Time To failure): measures the mean time a component functions before failing, an essential basic measure of system reliability for non-repairable items [hours/failure].
- Failure rate: number of failures per unit of gross operating period in terms of time, events, cycles, or number of parts.
- Single Point Failure (SPF): Failure that can stop the entire system from working.
- Redundancy: is a commonly applied reliability improvement technique to enhance the system reliability and availability of safety-critical systems, or operational impact systems in the railroad and mass transit industry.
- Hot Redundancy: redundant components are continuously energized and operate simultaneously.
- Cold Redundancy: some or all of the redundant items are not operating continuously but are activated only upon failure of the primary item performing the function.
- Cross-strapping: two identical units that are interconnected with the remaining system in such a way that either unit can provide the required functionality.

2.1.1 Requirements

One of the main aspects sought in this thesis is to achieve the requirements imposed by the mission. In particular, the requirements associated with reliability exposed in [13] are,

- The overall reliability of the PMS shall be above 97% over the in-orbit operational lifetime.
- An equipment failure shall not propagate to another unit or subsystem.
- No single hardware or software failure of the PMS shall lead to irreversible degradation in performance or loss of mission.

2.1.2 Reliability analysis

As mentioned in the Space Standards ECSS-Q-ST-30C, this analysis will be used to predict the system's life service, identify the criticalities of the baseline architecture and optimise the design to meet the reliability requirements while considering limitations such as mass and cost [14].

The variables that have a major influence on the system reliability are given below:

- Duration of use of the electronics, which in LISA's case can be translated in a lifetime of seven years.
- Reliability block diagram based on the system's operation, establishing the redundancy architecture in terms of serial or parallel blocks.
- Failure rates of every electronic device and the number of them that make up the system.
- Working temperature value.

In terms of obtaining the failure rate, there are three types of reliability prediction methods [15]:

• Bottom–up statistical methods. This method is built on the assumption that the failure rate of a device is a consequence of the failure rates of its internal components, which are supposed to be independent of each other. The failure of the component as a whole is not studied but built as a result of applying different mathematical models to the prediction.

This type of method uses mainly two models of reliability prediction. These methods vary in the degree of information needed to apply them.

- Part count method: requires less information, generally part quantities, quality level and the application environment. The Parts Count Methods usually results in a more conservative estimate of system reliability than the Parts Stress Method.
- Part Stress Analysis Methods: needs a greater amount of detailed information, including the schematics.

An example of this method is the widely used military standards MIL-HDBK-217F [16].

- Top-down similarity analysis methods. Based on proprietary databases where failures are recorded of the whole systems or subsystems.
- Bottom-up physics-of-failure methods. This method utilises the devices' reliability results from the physical accelerated test such as temperature cycling, highly accelerated stress test or temperature humidity bias. This data builds the failure rate by using statistical laws, commonly Weibull, using a confidence level of 60% or 90%. The final failure rate of the device is formed with the obtained failure rates from each accelerated test.

In this process of reliability prediction analysis to be done, the primary reference for the FDS equipment is the manufacturer data, manufacturer calculation tools and the communication with manufacturers. The methods used by manufacturers varies between them, although most provide failure rates based on bottom-up physics-of-failure methods, commonly expressed in the form of FITs for a better understanding of them. Detailed reliability data of each device is provided in the Annex A.1.

2.1.3 Reliability equations

Reliability calculations are ruled by the following equations [17]:

• Failure rate:

$$\lambda_{hours} = \frac{1}{MTTF_{hours}} \tag{2.1}$$

• Failures in Time:

$$FIT = \lambda_{hours} \cdot 10^9 \tag{2.2}$$

• Reliability of one element:

$$R_i = e^{-\lambda_{hours}t} \tag{2.3}$$

where t is the mission lifetime in hours.

• Reliability of n elements in series:

$$R_{n_s} = \prod_{i=1}^n R_i \tag{2.4}$$

• Reliability of n identical elements in hot redundancy:

$$R_{n_{br}} = 1 - (1 - R_i)^n \tag{2.5}$$

• Reliability of n identical elements in cold redundancy for non-repairable systems as demonstrated in [18]:

$$R_{n_{cr}} = 1 - (1 - e^{-\lambda_{hours}\frac{t}{2}})^n = 1 - (1 - \sqrt{R_i})^n$$
(2.6)

• Reliability of "m" out of "n" identical elements to survive:

$$R_{m/n} = \sum_{k=m}^{n} \frac{n!}{k!(n-k)!} R_i^k (1 - R_i^{n-k})$$
(2.7)

It is important to consider that reliability is highly influenced by other agents apart from time of use and redundancy. Electronic parts are exposed to varied stresses such as electrical, thermal or ambient throughout the operation. However, temperature is the most influential factor in electronic failures. It has a significant impact on its reliability, as it causes slow progressive deterioration of the materials of which the part is made [19]. Equipment which works adequately at one temperature level will be less reliable or inoperable as temperatures increase.

Hence is crucial to be aware of the effect of the temperature on the reliability of the device. Given the reliability value (or total FIT) of a device at a specific temperature, one can determine what the reliability would be at a different temperature by introducing an acceleration factor [20]:

$$R_i(T_n) = [R_i(T_i)]^{1/AF}$$
(2.8)

Where AF is the acceleration factor given by the Arrhenius equation:

$$AF = e^{\frac{-E_a}{k_B}(\frac{1}{T_i} - \frac{1}{T_i})}$$
(2.9)

Where k_B is the Boltzmann's constant and Ea is the activation energy of the failure mechanism. In Table 2.1 are shown the activation energy values for some typical failure mechanism [20].

| Failure Mechanism | Ea |
|------------------------|-------------|
| Corrosion | 0.45 eV |
| Electromigration of Al | 0.6 eV |
| Contamination | 1.0 eV |
| Oxide defects | 0.3-0.5 eV |
| Charge inj ection | 1.3 eV |
| Mask defects | 0.7 eV |
| Assembly defects | 0.5 -0.7 eV |

 Table 2.1
 Activation energy for failure mechanisms.

The activation energy for each component is detailed in Annex A A.1.

Consider an assembly that is comprised of the PCB and the electronic devices, both active and passive. High power values consumed by an electronic component entail a source of heat. Heat transfer can imply the heat flux from one hot device to another through different heat transfer mechanisms. If the component receiving the heat is a device sensitive to temperature and the internal heat reaches a high value, the device reliability will decrease consequently.

As electrical and thermal stresses are closely interrelated with reliability, it is crucial to study the accurate working temperature of each device in order to have realistic reliability results. This temperature is obtained by simulation in COMSOL Multiphysics, explained in detail in Section 2.2, considering all the effects of heat transmission between the power consumed by each device and how this heat is transmitted to the PCB, the enclosure and the CHOTHERM.

2.2 Thermal model

Three different mechanisms can occur in the process of heat transfer between two bodies:

• Conduction: this process arises from the molecular vibration of the solids, where the heat is exchanged from the solid with more energy to the solid with less energy. Conduction is

commonly the primary heat transfer mechanism in solids.

- Convection: this form of heat dissipation is caused by the movement of a fluid. Due to the vacuum environment operation, convection will not be studied.
- Radiation: as radiated heat is transferred by electromagnetic waves, it does not require a physical medium to occur. Consequently, thermal radiation may become considerably relevant in space applications, up to 30% of the heat dissipation of an electronic device to the surrounding environment.

As exposed in [21], thermal conduction problems are solved using an electrical analogy. In these models, known as compact thermal models (CTMs), the thermal contact between the solids of the system is characterized by a thermal conductance h, simulating the electrical equivalent of an electrical resistor, and the heat flow is modelled as the circuit current flow.

In order to model the heat transfer by conduction of the whole Frequency Distribution System, the electrical analogy presented in Figure 2.1 has been assumed. This outline shows all the solids involved in dissipating heat from the component to outwards the PMS, whose detailed heat transfer behaviour is explained below in Section 2.2.1. The starting point is the heat 'applied' to the electronic component. This heat is transferred directly to the PCB, followed by the enclosure. Moreover, a conductive elastomer insulators has been placed at the base of the enclosure, CHOTHERM, whose utility consists in ensuring efficient heat dissipation and preventing local temperature overloads, moreover it must also be considered for the thermal study.

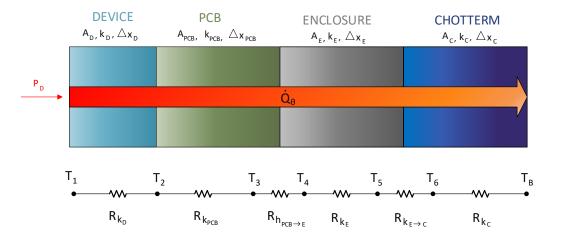


Figure 2.1 Electrical analogy for the FDS.

2.2.1 Implementation of the thermal model in COMSOL Multiphysics

This section aims to explain the creation of the electrical analogy shown in Figure 2.1 in the COMSOL Multiphysics simulation program, explaining in detail the assumptions considered, boundary conditions applied, and meshing of the geometry.

2.2.2 Geometry and materials

The first step for the implementation of this model is the creation of the geometry to work with. The CAD software used for this purpose is SolidWorks, where an assembly has been created with all the

aforementioned solids: PCBs, enclosure, CHOTHERM and every particular device geometry.

For the thermal modelling of each electronic component, several simplifying hypotheses have been considered :

- The whole device has been assumed as a unique resistance, simplifying the composition of die, package and finish.
- Heat transmission from the device to the PCB will be considered perfect [21]. Thermal transfer between two solids is dependent on the on the surface's roughness and the pressure applied between them. In the current design state, it is impossible to know these variables with precision, and experimentation would be needed for each of the component. Given the enormous number of components, and the differences between them, it seems reasonable to model the heat transfer based on the junction-to-case value θ_{JC} , provided in the datasheet. Its implementation is detailed explained in this Section.
- Radiated heat from every device will not be considered. Despite the fact that radiation in space applications plays a very important role, radiated heat from electrical components depends on many variables that are still unknown at this stage of the design, such as the ambient temperature of the module or the disposition of the different modules along the PMS, as some of them will generate more heat than others and heat that will be conducted within the modules. Therefore, internal heat radiation is not considered for the analysis to be carried out, assuming in that sense a worst-case scenario, where all the heat dissipated by the component will be presupposed to source from conduction.
- As the operation of each component generates internal heating which must be dissipated to the PCB, the heat transmission is modelled as a heat flux from the top surface of the device as shown in Figure 2.2. This heat rate is the power consumed by every device, whose value is calculated in the power budget in Annex A.3.

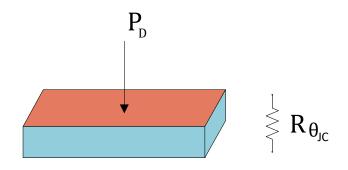


Figure 2.2 Electronic device thermal model.

These considerations have a great impact the model's material definition, as each of the solids in the model must have an associated material. When defining materials in COMSOL Multiphysics, three parameters must be designated: density ρ , heat capacity at constant pressure C_p and thermal conductivity k.

In order to simulate the behaviour of each device as closely as possible to reality, the material constituting the component package has been taken as the reference material for the density and heat capacity values, as it constitutes the central part of the entire component. The package generally used for space devices is ceramics, as it performs better against the internal heating of the component. In some cases, the devices' datasheet are insufficient to know the package materials specifications accurately. Hence, a generic ceramic material for space upgrade has been used for density and heat capacity values, and their properties were also obtained from the material database *Matweb* [22]. This simplification is reinforced later with the approach of the heat transfer equations solved in COMSOL in Section 2.2.2.

Regarding the thermal conductivity k, it is calculated based on each devices' characteristics. This property is related to how well the material can conduct heat. Subsequent to consider the perfect heat transmission hypothesis already mentioned, the thermal conductivity of each device has been modelled by its junction-to-case data $\theta_{JC} = K/W$, obtained in the datasheet. The process reflected in the Equation 2.10 leads to the derivation of the thermal conductivity:

$$k = \frac{W}{m \cdot K} = \frac{S}{\theta_{JC} \cdot V} \tag{2.10}$$

Where S is the contact surface of the device and V the volume. All the thermal data employed is attached in Annex A.2.

Following the diagram in Figure 2.1, the next item is the PCB. To define the whole material that constitutes the PCB, several assumptions have been considered. First, the PCB is formed by several layers of different material superposes (copper and dielectric, generally FR4), as shown in Figure 2.3.

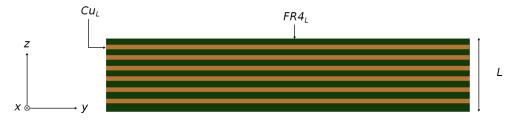


Figure 2.3 PCB layers [23].

This implies that the material that makes up the PCB is a composite material. Consequently, their parameters depend on the properties of the constituent materials and the quantity of each one. In a first approximation, a thickness of 1.65 mm and six layers of copper have been assumed. Since the objective of this study is the thermal optimisation of the FDS, it is helpful to introduce in COMSOL these quantities in the form of parameters to facilitate future extraction of results as follows:

$$n = 6$$

$$Th_{Cu} = 35 \cdot 10^{-6} mm$$

$$L_{PCB} = 1.65 mm$$

$$L_{Cu} = n \cdot Th_{Cu}$$

$$L_{FR4} = L_{PCB} - L_{Cu}$$

Where L_{FR4} is the remaining thickness of the PCB, *n* is the number of used copper layers and Th_{Cu} is the used copper thickness, whose values will be 6 layers and 35 microns in principle. On

this basis, the density $\rho[kg/m^3]$ and the heat capacity at constant pressure of the PCB material C_p $[J/(kg \cdot K)]$ have been obtained with the following approach:

$$C_{p_{pcb}} = \frac{L_{Cu} \cdot C_{p_{Cu}} + L_{FR4} \cdot C_{p_{FR4}}}{L}$$
(2.11)

$$\rho_{pcb} = \frac{L_{Cu} \cdot \rho_{Cu} + L_{FR4} \cdot \rho_{FR4}}{L}$$
(2.12)

Nevertheless, for the whole thermal conductivity, it must be considered that the FR4 has lower thermal conductivity in the plane perpendicular to the PCB, and consequently, the board cannot be treated as an isotropic material. To implement this in COMSOL, the thermal conductivity of the material defining PCB has been modelled with a diagonal matrix of its values in each direction

$$k = k_{i,i} = \begin{pmatrix} k_x & 0 & 0\\ 0 & k_y & 0\\ 0 & 0 & k_z \end{pmatrix}$$
(2.13)

Basing this calculation on the same logic as the previous ones:

$$k_{i} = \frac{L_{Cu} \cdot k_{Cu} + FR4_{L}L_{FR4}}{L} \quad for \quad i = x, y, z.$$
(2.14)

This question is simplified in the case of the other solids parameters in the scheme, which are the enclosure and the CHOTHERM. The density, heat capacity and thermal conductivity for these materials had been directly obtained from the database [24] [25].

Boundary conditions

One of the main boundary conditions for a thermal study is the definition of the thermal contact areas between the solids.

Heat transfer between the enclosure and the PCB is defined by the layer conductance value, though it depends on many unknown variables. Not all the contact between the PCB and the enclosure will be the same throughout the module, as there are areas with higher pressure between the two solids. The example that best illustrates this situation is the screw joint area. In these, the contact area will be larger; therefore, the heat transfer will also be higher than the rest of the interface.

In consequence, a good approximation of the thermal contact area is crucial to carry out a realistic thermal study. In the following analysis, the thermal contact is limited to a circular region as presented in Figure 2.4 around the union screws as studied in [23].



Figure 2.4 Thermal contact area. Inner diameter is 4mm and outer 8mm.

The implementation of the thermal boundary conditions in COMSOL looks as displayed in Figure 2.5. The Figure in the left shows the internal surface of the CHOTHERM as a thermal contact boundary condition with the enclosure, where all the surface has been selected as heat transfer interface. Additionally, each screw junction area has been established as a thermal contact between the enclosure and the PCBs, characterised by the contact layer conductance discussed below. Nevertheless, as the thermal contact between these solids is supposed to be limited exclusively to this circular area, the rest of the contact area between the enclosure and the PCB must be set as a thermally isolated area, as displayed in the right-hand Figure. Setting this condition is necessary because COMSOL would default set it as a zone where the thermal contact is perfect between these solids, obtaining very optimistic results far from reality.

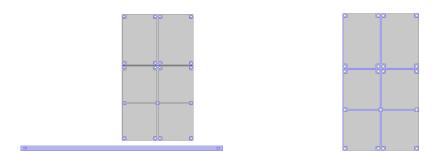


Figure 2.5 Thermal contact boundaries conditions.

In order to get the unknown value of the layer conductance of this circular area, a comparison between experiments and simulations was carried out in the AEI [23]. By sweeping the values for this layer conductance in the simulations, and then comparing the results with the experimental data, it has been concluded that the appropriate layer conductance value for this area is

$$h_{PCB\to E} = 1650 \left[\frac{W}{m^2 \cdot K}\right]$$

A similar study has been carried out to calculate the layer conductance value between the enclosure and the CHOTHERM. In this case, the contact area has been assumed to be the entire junction area between the two, obtaining the following result

$$h_{E\to C} = 293 \left[\frac{W}{m^2 \cdot K}\right]$$

Additionally, boundary conditions from the outer part of the enclosure had also been defined. On the one hand, the enclosure base is supposed to remain at 20°C by design, with a tolerance of $\pm 5^{\circ}C$. With the aim of parameterise this temperature and its possible variations, a variable called T_{table} was generated. This temperature condition has been imposed on the outer face of the CHOTHERM, as seen in the left image of Figure 2.6. On the other hand, the right image shows a boundary condition associated with the heat transmitted by radiation. This has been assumed because, although the effects of radiated heat have not been considered at any time given the influence of many unknown internal variables, this surface shown is the only surface not influenced by other factors, and can radiate heat freely inwards the satellite. To implement the radiation condition in COMSOL the study of surface-to-surface radiation has been explicitly used, making it necessary to establish the refractive index of the medium, whose value for vacuum is 1 by definition:

$$n = \frac{c}{v} \tag{2.15}$$

As *c* is the speed of light in vacuum and *v* is the speed of light in the medium, which coincides in this case.

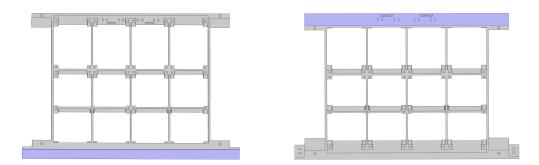


Figure 2.6 Boundary conditions.

The last boundary condition to be imposed on the model is the heat generated by every device. As mentioned in the assumed assumptions for the thermal modelling of the electronic devices 2.2.2, the generated heat is modelled as a heat flux from the top surface of the device, whose heat rate value is the power consumed by the device. This makes clear the need for a power budget for each component's consumption.

In terms of domain meshing, COMSOL builds a mesh appropriate to the imported geometry. Specifically, a mesh of tetrahedral elements has been used. In COMSOL, there is the possibility of adjusting the size of the mesh elements and refining the mesh in any of the x, y or z directions. For this analysis, a 'Finer' refinement has been used motivated by the complexity of the assembly. Additionally, the mesh has been refined ten times in the perpendicular direction of both solids PCBs and CHOTHERM. The indicated decision is due to the importance of heat transmission in the critical dimension of the solids, and the fact that the PCBs are not isotropic materials. The resulting mesh is presented in Figure 2.7.

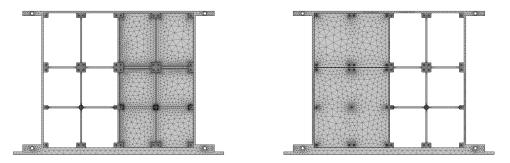


Figure 2.7 Frequency Distribution System mesh.

Stationary analysis

Heat conduction is ruled by Fourier's law, establishing a link between the heat flux and the temperature gradient:

$$\mathbf{q}(\mathbf{r},t) = -k \cdot \nabla T(\mathbf{r},t) \tag{2.16}$$

From Equation 2.16, the thermal conductivity k is proportional to the temperature gradient, and the heat flows in the direction opposite to the temperature gradient. This equation is involved in the solved equations in COMSOL for a stationary study, which is the following:

$$\rho c_p \mathbf{u} \cdot \nabla T + \nabla \cdot (\mathbf{q} + \mathbf{q_r}) = Q + Q_{ted}$$
(2.17)

Where *u* is the velocity vector of translation motion, *q* the conduction heat flux defined in Equation 2.16 and q_r is the radiated heat. Additionally, c_p is the Specific heat and ρ is the density, material

parameters already defined.

Stationary results aim to obtain the working temperature of each device and the temperature gradient map of the PCBs. These temperatures will allow performing a study to lower the working temperature as much as possible by making modifications in the distribution of the components, the PCBs internal parameters and modifying the geometry of the enclosure. Knowing the operating temperature will conjointly make it possible to test its effect on every device's reliability. Furthermore, the gradient map will be necessary to ensure that the Pilot Tone is exposed to the minimum temperature gradient, as is exposed in Section 3.2.1.

Time dependent analysis

The time dependent studies in COMSOL will make it possible to verify the $\pm 5^{\circ}C$ offset effect in this module. This uncertain temporary change becomes influential in terms of the correct functioning of the PCB. Particularly, it will be decisive to study the effect that it has on the Pilot Tone signal since, as mentioned several times, it is very susceptible to temperature gradients. It is also crucial to examine the temperature evolution of the crystals under this change, as it could reach unsuitable temperatures.

The dependence on time in the equations to be solved in this analysis is reflected in the first term of the following equation, which constitutes the only difference regarding the stationary study Equation 2.17.

$$\rho c_p \frac{\partial T}{\partial t} + \rho c_p \mathbf{u} \cdot \nabla T + \nabla \cdot \mathbf{q} = Q + Q_{ted}$$
(2.18)

This term represents a partial time derivative of the temperature, which is proportional to the parameters of the material conducting the heat, density and specific heat. The influence of these parameters on the analysis is tested here. However, as the intended results are primarily about the PCBs temperature, the materials of the individual electronic components do not play a relevant role, except for the crystals. Although attempts have been made to obtain the particular material properties of the crystal package for this specific study, this has not been possible at this design stage. The specific crystals selected for the mission will be designed on an as-needed basis due to their criticality, customising the packaging for their space applications, which is not yet defined. So it is assumed for them the generic ceramic material forehead mentioned.

The offset case from 20 to 25 degrees is studied, as it is the most restrictive situation reaching higher temperatures. To model this temperature change in COMSOL, experimental data has been used to simulate a realistic thermal behaviour. These experiments where carried out in the AEI, with the aim of measuring the evolution of the temperature set at the base of the enclosure in vacuum conditions, when a change of 5° C is applied.

From these experiments, the thermal time evolution of the enclosure base vs. time from Figure 2.8 is obtained.

It should be mentioned that the data in this experiment is measured every second. As the number of points that are given by this experiment is too large to introduce them in COMSOL, information has been extracted from this function every 60 seconds, obtaining a new function that reproduces in an approximate but sufficiently accurate way the behaviour of the temperature under this change. The new function data has been collected in a text file to be used as the input sweep parameter for the study. Setting a step of 60 seconds, COMSOL changes the temperature of the base every 60 seconds following the data from the input function. In this way it is possible to obtain a transient response in a reasonable real analysis time, thanks to the reduction of input points.

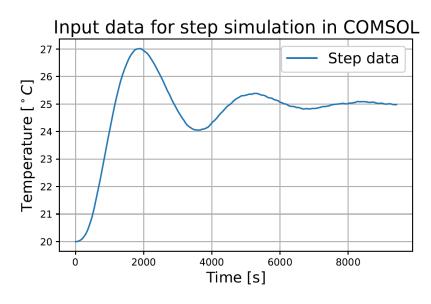


Figure 2.8 Input data for simulation in COMSOL.

2.3 Structural model

Weight has always been a determining factor for space missions. Therefore, one of the module's optimisations process proposed in this thesis is the modification of the enclosure, which is the structural part that houses the PCBs. Based on the obtained results, it will be possible to check whether adding more aluminium in some areas is necessary to improve the heat dissipation of certain components, or if, on the contrary, it is possible to reduce the mass of the structure.

However, any changes in the enclosure must be validated to ensure that the structural integrity of the PMS is not compromised at any time. The PMS will be subjected to high loads at launch. Specifically, it will be launched with the Arianne 64 [9] and it has been deemed sufficient that the PMS can bear the load of 5G for this early analysis.

To test whether these modifications are structurally valid to meet this load requirement, a solid mechanics study is necessary to study the possible effects of this force on the assembly. No indepth structural analysis is carried out in this section, so it is subject to much improvement. The purpose of this analysis is to ensure that the modifications made to the enclosure are valid to withstand these loads, thus allowing further work on the new structure to be carried out on a reliable basis for future studies. The obtained data will allow to examine if the yield strength σ_{Al}^{yield} is exceeded in any area, and if it is happens, that it is not greater than the ultimate tensile strength $\sigma_{Al}^{ultimate}$.

In order to solve any elastic problem, it is necessary to establish the boundary conditions applied to the solid:

- Load boundary condition: As mentioned above, the PMS will be subjected to a force of up to 5G at launch. To model this force, it is necessary to know the direction in which it will be applied, however, the direction in the real case can be completely arbitrary. Therefore, an study is carried out for a load of 5G in each of the axes, x,y and z.
- Boundary conditions in displacements: The PMS is anchored to the satellite at the base As explained in Section 1.3. Therefore, one of the conditions to be imposed is that the displacement of that surface in its perpendicular axis is prevented. However, the displacement

in the other axes is not limited and the solid can deform freely. Another area that is limited in displacements is the area of the screws, as these will be assumed to be fixed.

. The detailed implementation of this analysis is exposed in Section 3.2.3, based on the architecture determined in the optimisation process.

3 Results

3.1 Preliminary reliability analysis

A preliminary reliability analysis is carried out as a starting point, where the failure rate data has been obtained for an operating temperature of 55° C, as this is the typical value provided by the manufacturers.

To develop this reliability analysis, it will be of great importance to understand the functioning and the design architecture of each PCB in terms of involved devices and intern redundancy. For that reason, in the coming sections the functioning of the PCBs that make up the FDS will be explained, followed by its reliability diagram and the corresponding reliability results.

3.1.1 VCXO

Functional diagram

The primary purpose of this PCB is to lock the system clock running at 80MHz to the external USO input. Moreover, the VFDS board implements the distribution electronics and clock buffering of the USO, System Clock (PPS) and distributes the required signals to the rest of the BEE modules for its correct functioning. These are the 80 MHz, USO, and PPS signals. Figure 3.1 presents the detailed functional diagram of the VFDS, whose operational mode is explained based on this outline.

The signal entry point is located in the upper left-hand corner connector. This input receives USO and PPS signals, both nominal and redundant. As mentioned in Section 1.2, the USO (Ultra Stable Oscillator) signal comes from the spacecraft master clock. Both PPS and USO signal pass through a buffer that divides this signal into 10, to be distributed to all modules (USO OUT and PPS OUT in the diagram), both nominal and redundant (4xBEE nominal, 2xBEE redundant, 1xDHLC nominal, 1xDHLC redundant, 1xPSM nominal, 1xPSM redundant).

One of the main complexity of this PCB is the necessity for the 80 MHz signal to be locked with the input USO signal. For that reason, an external control loop with the FPGA is needed. In this loop, the output signal of the USO buffer is constantly compared in FPGA-logic with the 80 MHz output signal with a phase/frequency detector. If the signal suffers a variation concerning the master signal at any time, the FPGA responds with a modification in the feedback signal to correct this variation. A PI controller adapts the error signal into a voltage level, tuning the frequency of the 80MHz quartz crystal to follow the USO input frequency. After quartz crystal actuation, the signal is converted into a square signal to be compared in FPGA logic. Later, both clock chains are combined in a junction point, establishing a slip-less switching point. This point is motivated by

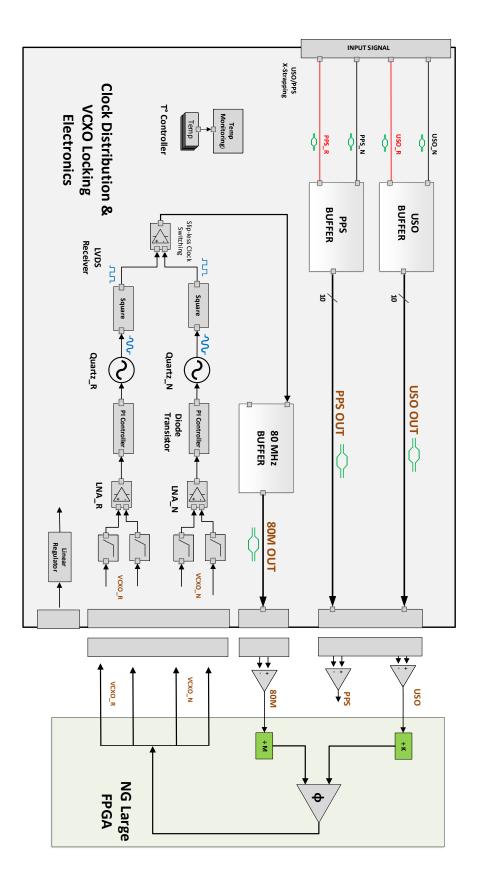


Figure 3.1 VFDS functional diagram.

the fact that switching from one clock to another requires a transition time in which cycles are lost. Given the criticality of the 80 MHz signal, this slip-less switching point ensures that the 80 MHz signal is constantly being provided to the PMS.

This external loop is represented in the right part of Figure 3.1. The green rectangle includes the logical control operator of the FPGA from the DHLC, whose inputs are the USO OUT and the 80 MHz OUT.

Regarding the electrical aspects, this board receives 5 volts from the Power Supply Module. However, a linear regulator must convert these five volts to 3.3 volts, as some devices require this specific voltage for their correct operation. Additional functions, such as temperature reading, are also performed in this board.

Reliability diagram

Based on the functional diagram shown in Figure 3.1 and the reliability methodology explained, the reliability diagram of this PCB is built.

In terms of reliability, it is necessary to establish the 'success' to be achieved. For this PCB, the success will be the correct functioning of the whole PCB, including all the functions it has to perform (PPS, USO and 80 MHz signal distribution, voltage regulation, temperature control). To represent this objective, each component should be considered as a functional unit, as this is where the failure rate is known. Before building this diagram, it is necessary to identify the redundant parts or if, on the contrary, the devices form a serial chain. In the VFDS, it can be found a redundant architecture in the clock chain. This is justified by the fact that the quartz crystal has the highest failure rate on this board. It is also supported due to the criticality of getting the 80 MHz signal. In addition, the LVDS Receiver is a quad-gate device that must perform three functions: convert the sinusoidal signal to square from the nominal string, from the redundant string and establish a junction point where the two strings are combined. However, it can be clearly seen that this junction point is an SPF. If this LVDS receiver fails, the 80 MHz signal is completely lost. For this reason implementing a second cold redundant LVDS receiver was proposed, thus avoiding this problem.

Focusing on the reliability of this board, the following Figure 3.2 is presented as a function of the devices that compose the VFDS. The figure shows how the linear regulator and buffers, USO and PPS, are in a series arrangement, followed by the redundant clock chains, whose constituent devices differ. This architecture is justified in an intern design document [11]. After that, it can be found LVDS driver and receiver again in series.

It should also be mentioned that the operation of this board involves the functioning of the modules DHLC (external control loop with the FPGA) and PSM (power supply to the board), marked in red in the diagram. If any of these modules fail, the VFDS will also fail. However, this dependency is not studied in this project since that corresponds to a complete reliability study of all the PMS modules.

Reliability data

Based on the reliability diagram exposed in Figure 3.2 previously developed and the methodology explained in Section 2.1, the achieved result is:

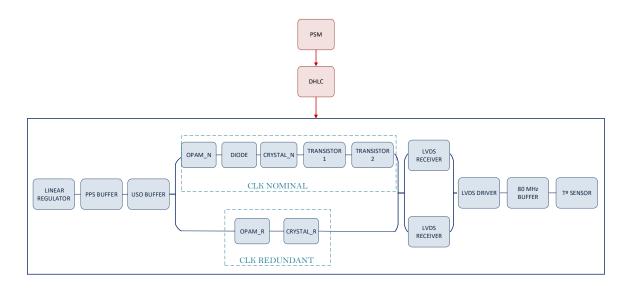


Figure 3.2 VFDS Reliability diagram.

TOTAL VFDS RELIABILITY 99.85 %

Whose calculations are shown in Table 3.1. Detailed reliability data for each component can be found in Appendix A.1.

| BLOCK | DEVICE | FIT | RELIABILITY | BLOCK RELIABILITY | | |
|-----------------------|------------------|--------|-------------|-------------------|------------|--|
| USO BUFFER | USO Buffer | 2.8 | 0.999828319 | 0.999828319 | | |
| PPS BUFFER | PPS Buffer | 2.8 | 0.999828319 | 0.999828319 | | |
| | OPAM N | 1.17 | 0.999928258 | | | |
| | Diode | 0.5938 | 0.999963592 | | 0.99999695 | |
| VCXO NOMINAL | Crystal N | 18 | 0.998896849 | 0.998788515 | | |
| | Transistor 1 | 0.0025 | 0.999999847 | | | |
| | Transistor 2 | 0.0025 | 0.999999847 | | | |
| | OPAM R | 1.17 | 0.999928258 | 0.00545064 | | |
| VCXO REDUNDANT | Crystal R | 40 | 0.997550206 | 0.99747864 | 1 | |
| RECEIVER | LVDS Receiver | 5.4 | 0.999668927 | 0.999668927 | 0.99999989 | |
| | LVDS Driver | 2.9 | 0.999822188 | | | |
| 80MHz BUFFER | 80 MHz Buffer | 2.8 | 0.999828319 | 0.999650537 | | |
| REGULATOR | Linear regulator | 4.29 | 0.999736972 | 0.999736972 | | |
| T ^o SENSOR | T Sensor | 2.8 | 0.999828319 | 0.9998 | 28319 | |

Table 3.1VFDS Reliability calculations.

3.1.2 Clock Sidebands

Functional diagram

In this section, the internal functioning of the Clock Sidebands board is explained based on the diagram shown in Figure 3.3.

Similar to the VFDS, this board essentially fulfils two functions. The main one is to distribute the Pilot Tone signal to the rest of the modules (LARM-BEE 1, LARM-BEE 2, TM-BEE and REF-BEE), while the second one is the procurement of a 1 MHz signal, which can be added or not to the output of the REF-BEE, in the convenience of operation.

PILOT TONE SIGNAL DISTRIBUTION

The main input of this PCB is the 80 MHz signal coming from the VFDS, already locked with the Ultra Stable Oscillator master signal. This input connector is shown on the upper right side in the Figure 3.3.

The first device involved after the input is the frequency up-converter, generating the clock sidebands modulation signals. This component can generate two different frequencies using its internal oscillator and different intern dividers or multipliers. These frequencies can be seen on the two different output ports of the controller A and B. Port A is set at a frequency of 2.4 GHz or 2.401 GHz, depending on operating requirements, while port B is set at Pilot Tone. In Figure 3.3, the case where the exact 2.4 GHz signal is generated at PMS 1 has been depicted as an example.

The purpose of this frequency difference is to secure two different strings to obtain the Pilot Tone. From port A, 2.4 or 2.401 GHz are output in differential form to suppress the high-frequency harmonics at the output of the frequency up-converter, acting as a shaping filter to convert from a square signal to a sinusoidal output. After this, the signal arrives at power splitter 1, where it is distributed to other parts of the satellite, in addition to the interconnection with the other PMS. This interconnection is shown in Figure 3.3 as the PMS2_Mixer_out and PMS2_PT_out outputs, both marked in blue. It should be noted that these outputs go to a board completely identical to this one, which means that we find these same signals as input also on this PCB, marked in red. The PMS2_PT_in input is found on the next component, switch 1. This device allows the module to choose between 2.4 GHz generated on PMS 1 or PMS 2. After this choice, a chain of dividers converts the 2.4 GHz into Pilot Tone in two steps.

From port B, the Pilot Tone signal comes directly out of this port without any transformations up to switch 2, clearly constituting a redundant path for the Pilot Tone signal. However, this chain has an undesired signal degradation, so that the nominal chain will be the one from port A.

Both chains converge at switch 2, where the chosen path is programmed from the FPGA. After that, the signal is amplified (LNA 1) due to possible losses that the signal may have experienced, passing then through a filter (LPF 2). Finally, the signal is split in the power splitter 2 to distribute it to all the modules, represented in Figure 3.3 as LARM_BEE 1, LARM_BEE 2, TM_BEE, REF_BEE outputs in green. For clarity, the redundant modules have not been included in the diagram, but the two redundant modules of the BEE have been taken into account in the design.

1 MHz SIGNAL PROCUREMENT

The interaction between the two PMS is also involved in acquiring the 1 MHz signal. The signal is extracted in the mixer, located at the mid-bottom part of the Figure 3.3. As it is represented, one

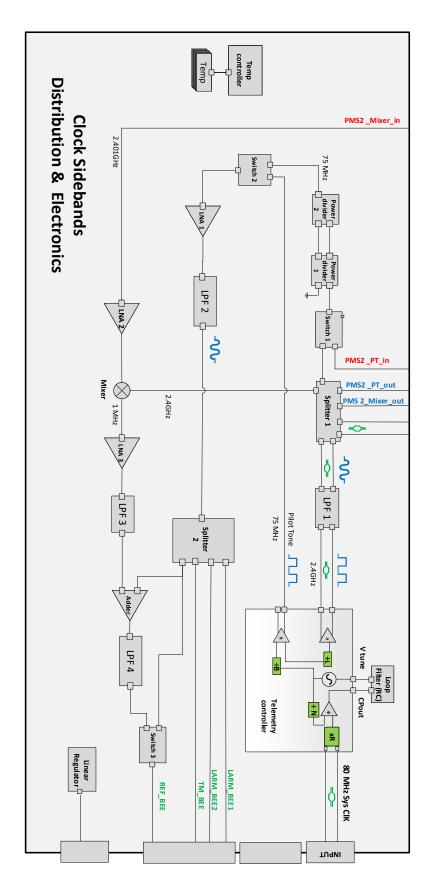


Figure 3.3 CFDS functional diagram.

of the inputs comes from this same board, specifically the 2.4 GHz of splitter 1, while the second input comes from PMS 2, with a frequency of 2.401 GHz. The mixer gets the difference of both signals as the output, obtaining the required 1 MHz signal. This signal is amplified (LNA 2) before entering the mixer due to the possible power losses it may have experienced. Hereafter the mixer, the signal is again amplified (LNA 3) and passes through a low frequency filter (LPF 3) to remove noise.

This 1 MHz signal can be added or not to the REE_BEE output from splitter 2, decision implemented by the switch 2.

Reliability diagram

It is important to note that the reliability diagram represents the probability of success of the entire operation of the board (both Pilot Tone and 1 MHz signal, T control and 3.3V power supply). As explained above, these functions require direct intervention by the similar board on the PMS 2. The PMS interconnection can make the reliability diagram complex to set up. This is why the reliability diagrams of the PCB functionalities explained previously are made independently, and then the diagram of the whole PCB will be constructed.

On the one hand, several devices are involved in obtaining the Pilot Tone signal. Depending on the position of Switch 1, the signal will come from either PMS 1 or PMS 2 as shown in Figure 3.4. It is important to stress that one of them will be set up at 2.4 GHz and the other at 2.401 GHz, so this can not be considered a redundant path, as it would not be possible to get the Pilot Tone signal from the port set to 2.401 GHz. However, port B of both phasemeters shall be set to exactly Pilot Tone. Therefore, although this is not a desired path due to the signal degradation, port B is a redundant path on both boards from a reliability point of view. The reliability diagram to get the Pilot Tone signal is represented in Figure 3.4. As in both options the signal is obtained with the same component configuration due to the similarity of the boards, this functionality is studied as if the switch were activated to get the signal from PMS 1.

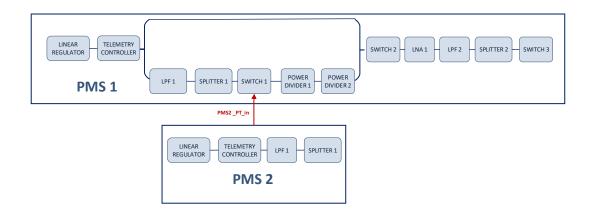


Figure 3.4 CFDS Pilot Tone reliability diagram.

Note that the interaction of the PMS 2 is displayed in the diagram just to show the same components that would be involved if the signal comes from PMS 2, but they are not considered in the reliability diagram of this function.

On the other hand, for procuring the 1 MHz signal in the mixer, two incoming signals are involved, one from PMS 1 and other from PMS 2. As both signals are necessary to get the desired output

in the mixer, all the implicated elements are arranged in series in the reliability diagram. The components that perform after the mixer to get the 1 MHz signal have also been included building the reliability block diagram in Figure 3.5 of this function.

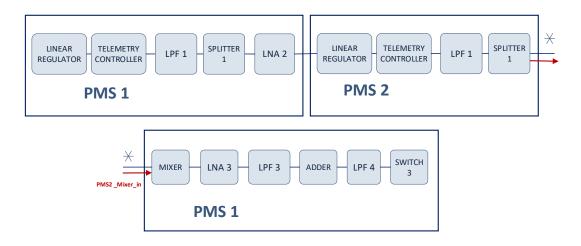


Figure 3.5 CFDS 1 MHz reliability diagram.

Where the symbol * represents the serial continuation of the reliability diagram. Based on this fragmented study, the reliability diagram of the whole CFDS is presented in Figure 3.6

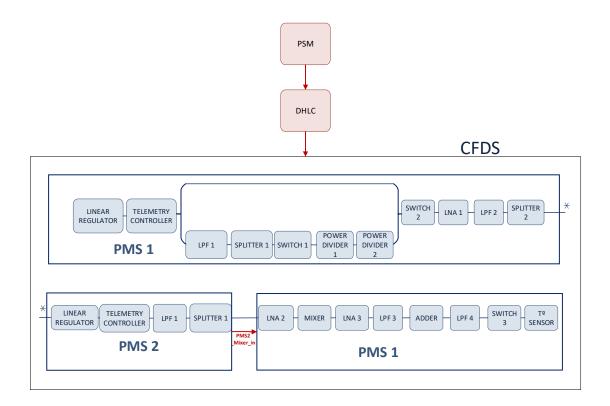


Figure 3.6 CFDS reliability diagram.

Reliability data

The reliability results for the basis diagram presented in Figure 3.6 are detailed in Table 3.2.

| BLOCK | DEVICE | FIT | RELIABILITY | BLOCK REI | LIABILITY |
|---------------|---|--|---|-------------|-----------|
| | Linear regulator Telemetry controller | 4.29 1.4 | 0.999736972 0.999914156 | 0.9996 | 5115 |
| 75 MHz OPTION | LPF 1 Splitter 1 Switch 1 Power divider 1 Power divider 2 | 85.216 96.572 26.7 0 0 | 0.994788184 0.994095704 0.998364096 1 1 | 0.98729689 | 1 |
| | - | 0 | 1 | 1 | |
| DISTRIBUTION | Switch 2 LPF 2 LNA 1 Splitter 2 | 26.7 10.68 0.25 40 | 0.998364096 0.999345317 0.99998467 0.997550206 | 0.995251041 | |
| PMS 2 CHAIN | Linear regulator Telemetry controller LPF 1 Splitter 1 | 4.29 1.4 85.216 96.572 | 0.999736972 0.999914156 0.994788184 0.994095704 | 0.988569677 | |
| 1 MHz CHAIN | LNA 2 Mixer LNA 3 LPF 3 Adder LPF 4 Switch 3 | 1.269 3.953 0.25 23.01 0.25 10.68 26.7 | 0.999922188 0.999757631 0.99998467 0.998590022 0.99998467 0.999345317 0.998364096 | 0.9959 | 54218 |
| T° SENSOR | T Sensor | 2.8 | 0.999828319 | 0.99982 | 28319 |

 Table 3.2 CFDS Reliability calculations.

Yielding a preliminary reliability result for this board of

TOTAL CFDS RELIABILITY 97.93 %

3.2 Thermal results

As mentioned in Section 2.2, every electronic device is modelled as Figure 2.2, where the internal heat is characterized by its power consumption. For that reason, the first step to carry out the thermal analysis is to make a power budget for every device's consumption. The obtained values are listed in Annex A.3.

3.2.1 Stationary results

This section focuses on performing stationary analysis to find the temperature of the components and the associated heat maps. Most of the module optimisation process will take place here, modifying parameters such as components layout in the board and PCB features. In addition, the process of constructing the geometry used for the analysis is detailed, as well as the decisions made to place each component in a specific location.

Firstly, it is necessary to make an assembly consisting of the PCB and each particular electronic component. For this purpose, a part was created for each device according to the dimensions of its package provided in each of the datasheets, simplifying the physical component details and

constructing a prism by taking the outermost dimensions of the devices. Regarding the PCB, its size is imposed by the enclosure dimensions, and a preliminary thickness of 1.65 mm has been assumed as it is a standard value in PCB manufacturing. Note that only the active devices have been considered for this model.

Regarding the devices distribution on the PCB, the driving factor of the CFDS layout is the sensitivity of the Pilot Tone signal to temperature gradients. Since there is no information about this at first, a preliminary arrangement very similar to that associated with the functional diagram in Figure 3.3 is adopted, whose result of which can be seen in the Figure 3.7. This will also help in the identification of each component and the Pilot Tone signal path, marked in yellow in the figure. At all times, an approximate spacing has been considered for the remaining electronic components which are not included in this analysis.

The starting layout of the devices in the VFDS was done considering the needs of each device. One of the main priorities is the correct functioning of the crystals due to their criticality, and for this reason they must be at the lowest possible temperature. The results from the thermal studies of the enclosure developed at the AEI [23], yields the conclusion that the base of the enclosure is proved to be the coldest area. That is why the crystals are placed as close as possible to the base of the enclosure. On the other hand, the regulator has a high power consumption, so it was also placed near the base to dissipate more heat and near the power supply input connector. Finally, several aspects have been considered for the arrangement of the buffers. Firstly, the signal path in the PCB and the distribution of the connectors. Secondly, as they are elements that also heat up considerably, they should be located as far apart as possible from each other and close to areas with a greater amount of metal. This distribution is shown in Figure 3.8.

| VFDS Devices Ter | nperature [°C] | CFDS Devices Temperature [°C] | | |
|------------------|----------------|-------------------------------|-------|--|
| USO BUFFER | 48.29 | Telemetry controller | 59.49 | |
| PPS BUFFER | 51.49 | Switch 1 | 55.09 | |
| Driver | 42.66 | Power divider 1 | 60.07 | |
| 80 MHz Buffer | 50.65 | Power divider 2 | 60.92 | |
| T° controller | 42.49 | Switch2 | 55.65 | |
| Linear regulator | 50.14 | Linear regulator | 58.71 | |
| LVDS receiver N | 39.67 | LNA 1 | 57.83 | |
| OPAM N | 40.05 | T°controller | 51.80 | |
| Crystal 1 | 39.212 | LNA 2 | 56.52 | |
| LVDS receiver R | 39.37 | Mixer | 54.47 | |
| Crystal 2 | 38.61 | LNA 3 | 55.94 | |
| OPAM R | 41.35 | Adder | 58.31 | |
| - | - | Switch 3 | 57.34 | |

 Table 3.3 FDS Devices Temperature.

After an initial analysis, Table 3.3 lists the temperature results for the Baseline distribution, and Figure 3.9 depicts its thermal map, where the isotherms lines have been included. The temperature of the VFDS components is in a reasonable range, especially that of the crystals, and no additional considerations are necessary. However, CFDS is clearly subject to improvement, primarily seeking that the line that follows the signal crosses the minimum possible temperature gradients, the effect can be minimized simply by changing the distribution of the components.

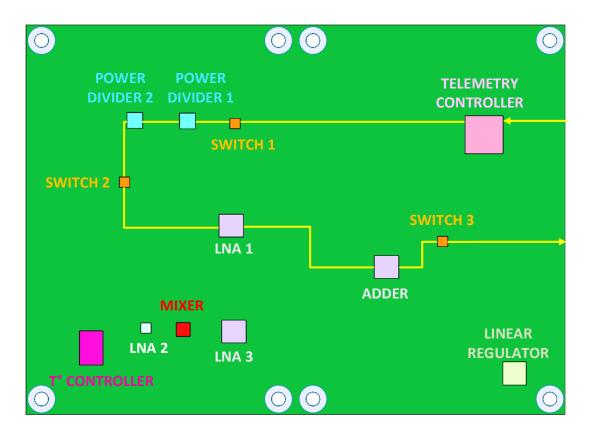


Figure 3.7 CFDS Device layout.

With this aim, different layouts are studied with the purpose of finding one that can minimize this effect as much as possible. It should be noted that this will not be searched for the 1 MHz chain, as this signal is not as sensitive.

In the first modification, the aim was to approximate the components of the Pilot Tone chain, seeking to form a more uniform area where the temperature is more regular. The thermal map is depicted in Figure 3.10. To check if there is any improvement due to the influence of the components of the 1 MHz chain on the isotherms of this PCB, these components have been separated in the second optimisation shown in Figure 3.11, maintaining the position of those of the Pilot Tone chain.

For the third optimisation, a different arrangement is tested. In this layout, the 80 MHz signal will enter from the bottom right of the CFDS, running across the PCB in the opposite direction to that shown in the baseline 3.7. In addition, the regulator has now been positioned in the top left corner of the PCB. This means that the elements that consume the most power and therefore dissipate the most heat are now as far from each other as possible and close to the areas with the most aluminium. This result can be found in Figure 3.12.

Finally, in optimisations four and five, the Pilot Tone signal path is approximated to each other to see if, in this case, a smaller temperature gradient is generated in the area. The thermal distributions of each distribution are presented in 3.13 and 3.14 respectively.

It is also possible to detect the hottest spots from every analysis, being them placed in the power dividers. This is mainly caused by the elevated value of power consumed by them as well as a high θ_{JC} value.

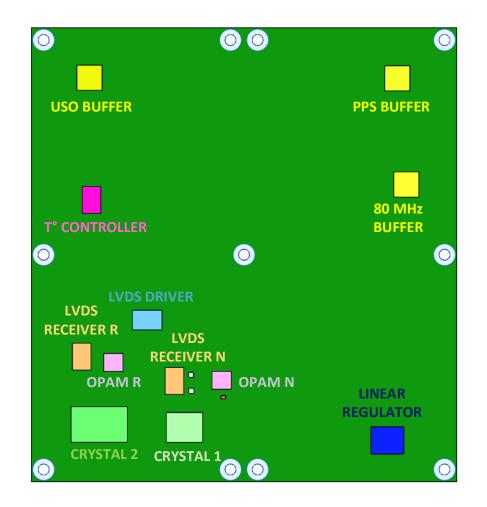


Figure 3.8 VFDS Device layout.

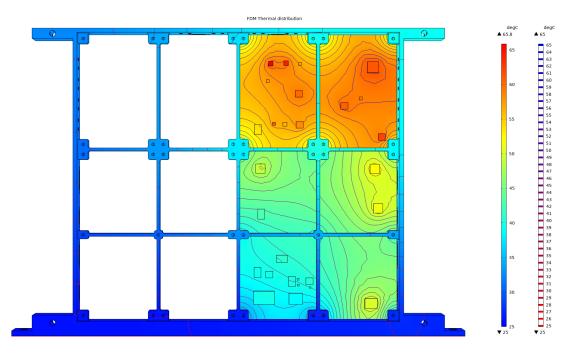


Figure 3.9 Thermal distribution: Baseline.

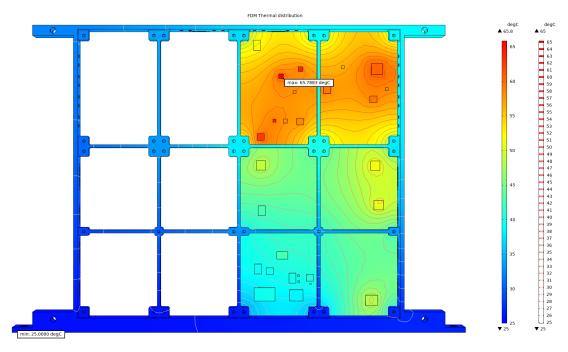


Figure 3.10 Thermal distribution: Optimisation 1.



Figure 3.11 Thermal distribution: Optimisation 2.

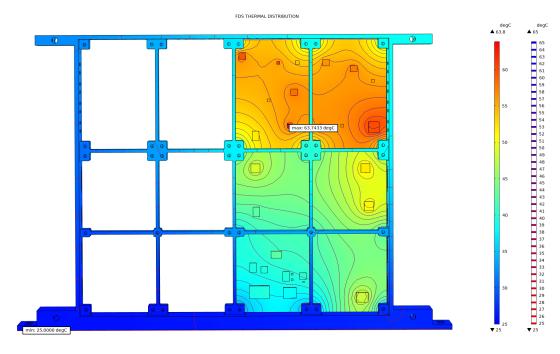


Figure 3.12 Thermal distribution: Optimisation 3.

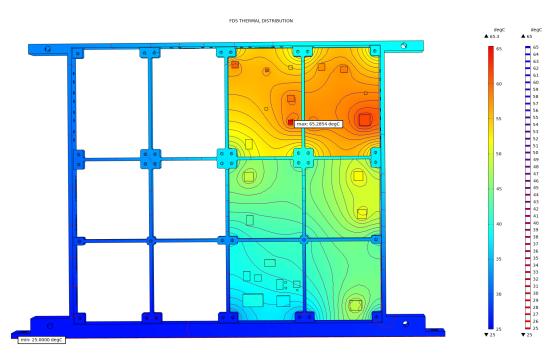


Figure 3.13 Thermal distribution: Optimisation 4.

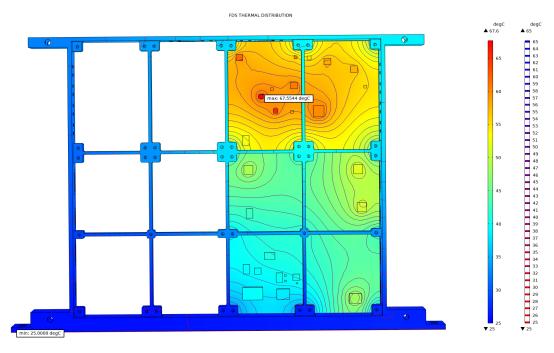


Figure 3.14 Thermal distribution: Optimisation 5.

Far from obtaining a negligible temperature gradient, the case that best represents a lower exposure to great temperature changes is the Optimisation 3, depicted in 3.12.

All the information about the devices working temperature are gathered in Table 3.4 for each of the modifications conducted. Comparing the obtained results, it can be confirmed that the best option is the third distribution, as the devices generally get less working temperature, with particular attention to the power dividers 1 and 2.

| (| CFDS Devices temperature [°C] | | | | | | | | |
|---------------------|-------------------------------|-------|-------|-------|-------|-------|--|--|--|
| Device | Baseline | Opt 1 | Opt 2 | Opt 3 | Opt 4 | Opt 5 | | | |
| Linear regulator | 58.71 | 61.07 | 60.71 | 57.86 | 58.34 | 60.15 | | | |
| Frequency converter | 59.49 | 60.43 | 60.74 | 59.96 | 61.47 | 59.90 | | | |
| Switch1 | 55.09 | 56.55 | 56.49 | 56.56 | 57.66 | 57.98 | | | |
| Power divider 1 | 60.07 | 61.15 | 61.48 | 59.68 | 61.31 | 62.70 | | | |
| Power divider 2 | 60.92 | 62.69 | 63.43 | 60.66 | 62.16 | 64.52 | | | |
| Switch2 | 55.65 | 58.01 | 57.97 | 54.87 | 55.49 | 59.27 | | | |
| LNA 1 | 57.83 | 58.91 | 58.84 | 57.64 | 58.75 | 60.09 | | | |
| T° controller | 51.80 | 52.04 | 52.17 | 51.75 | 51.42 | 52.89 | | | |
| LNA 2 | 56.52 | 61.46 | 61.16 | 58.23 | 58.92 | 57.98 | | | |
| Mixer | 54.47 | 58.01 | 57.68 | 53.73 | 53.99 | 54.47 | | | |
| LNA 3 | 55.94 | 58.08 | 57.03 | 55.86 | 57.12 | 57.49 | | | |
| Adder | 58.31 | 58.92 | 59.17 | 56.95 | 58.18 | 57.06 | | | |
| Switch 3 | 57.34 | 58.49 | 58.37 | 55.62 | 58.09 | 55.13 | | | |

Table 3.4 Devices Temperature.

For all these reasons, the adopted distribution from now on for further optimisation is the one

shown in Figure 3.12.

Layers and thickness optimisation

One of the aspects which can be influenced to improve thermal transmission is to modify both the number of copper layers on the PCB and the thickness of the PCB. Up to now, a 1.65 mm board and six copper layers have been considered.

It is clear that the more copper layers used, the better the heat dissipation of the components will be. However, it is necessary to contemplate the limits imposed by the ESCC space regulations for this. As quoted in Chapter 12.4 from ECSS-Q-ST-70-12C Design of Print Circuited Boards (Reproduced verbatim from [26]):

- **1.** *"The thickness of RF PCB as-designed should be* $\leq 3 mm$."
- **2.** The number of layers for RF PCBs should be ≤ 8 .
- **3.** The number of layers for RF PCBs may be > 8 in case the following conditions are met:
 - **a**) the number of layers is ≤ 14 , and
 - b) it is recorded as a Review Item in the PCB definition dossier."

These limits lead to study the different configurations in order to find the option that entails the best results. This means a sweep from the optimised baseline configuration (1.65 mm and 6 copper layers) up to the ESCC accepted maximum (3 mm and 14 copper layers).

Moreover, the thickness of the copper layers is also of great relevance. As mentioned in Chapter 7.1.2 from ECSS-Q-ST-70-12C: "the external and internal layers shall use basic copper thickness 70 μ m, 35 μ m or 17 μ m" However, it is also mentioned that "High layer count in combination with thick copper layers can have significant impact on manufacturability and long-term reliability". In order not to decrease the reliability of the board while maintaining a good heat transfer capacity, the commonly used thickness of 35 microns is assumed.

In the following, the operating temperatures of each component are studied for thicknesses of 1.65, 2.4 and 3 millimetres, all for 6, 10 and 14 layers of copper. The resulting data is reported in Table 3.5. The next conclusions can be extracted from the reported data:

- Increasing the thickness of the PCB does not improve the results. This makes perfect sense due to how the thickness of the PCB has been defined. As shown in Equation 2.11, the total thickness is implemented as the volume occupied by the copper layers plus the volume occupied by the FR4, assuming the copper layer thickness to be of $35\mu m$. If the total thickness is increased with the same number of copper layers, what it is being done is increasing the amount of FR4, which will not improve the thermal dissipation properties of the PCB. Nevertheless, this total thickness increase can be a determining factor in terms of manufacturing simplicity or electrical issues such as insulation for RF boards, but these aspects are also not addressed in this work.
- As previously predicted, the results improve with increasing copper layers. However, it can be observed that the improvement is not entirely linear. There is a greater thermal decrease from 6 to 10 layers of copper than from 10 to 14 layers of copper.

It is clear that the option that yields the best results is the 1.65 thickness, a typical thickness value in the industry. On top of that, high PCB thickness makes the drilling process, lamination and

| | | PCB CONFIGURATION | | | | | | | | |
|------------|----------------------|-------------------|-----------|-----------|----------|-----------|-----------|----------|-----------|-----------|
| | | | 1.65 mm | | 2.4 mm | | | 3 mm | | |
| | DEVICE | 6 layers | 10 layers | 14 layers | 6 layers | 10 layers | 14 layers | 6 layers | 10 layers | 14 layers |
| | Linear regulator | 57.87 | 54.83 | 53.43 | 58.37 | 55.17 | 53.71 | 58.6 | 55.33 | 53.83 |
| | Telemetry controller | 59.96 | 55.53 | 53.5 | 60.52 | 55.93 | 53.82 | 60.74 | 56.04 | 53.91 |
| | Switch 1 | 56.56 | 53.36 | 51.89 | 56.93 | 53.63 | 52.11 | 57.03 | 53.65 | 52.11 |
| | Power divider 1 | 59.59 | 56.24 | 54.7 | 60.08 | 56.58 | 54.99 | 60.34 | 56.73 | 55.09 |
| | Power divider 2 | 60.53 | 56.9 | 55.27 | 61.02 | 57.25 | 55.55 | 61.35 | 57.43 | 55.69 |
| S | Switch 2 | 54.91 | 52.25 | 51.05 | 55.19 | 52.44 | 51.2 | 55.3 | 52.49 | 51.23 |
| CFDS | LNA 1 | 57.62 | 54.13 | 52.57 | 57.98 | 54.41 | 52.79 | 58.1 | 54.44 | 52.81 |
| | T° Controller | 51.77 | 50.27 | 49.6 | 51.94 | 50.38 | 49.68 | 52.18 | 50.57 | 49.83 |
| | LNA 2 | 58.2 | 55.21 | 53.85 | 58.64 | 55.51 | 54.1 | 58.9 | 55.66 | 54.2 |
| | Mixer | 53.73 | 51.56 | 50.57 | 54.04 | 51.79 | 50.76 | 54.17 | 51.86 | 50.81 |
| | LNA 3 | 55.87 | 53.1 | 51.84 | 56.19 | 53.32 | 52.01 | 56.34 | 53.4 | 52.07 |
| | Adder | 56.9 | 53.72 | 52.28 | 57.25 | 53.95 | 52.46 | 57.39 | 54.02 | 52.51 |
| | Switch 3 | 55.57 | 52.71 | 51.4 | 55.91 | 52.92 | 51.56 | 56.05 | 52.98 | 51.6 |
| | USO Buffer | 48.29 | 45.43 | 44.05 | 48.59 | 45.64 | 44.21 | 48.68 | 45.73 | 44.29 |
| | PPS Buffer | 51.41 | 47.5 | 45.6 | 51.71 | 47.72 | 45.79 | 51.91 | 47.85 | 45.89 |
| | LVDS Driver | 41.63 | 40.93 | 40.67 | 41.79 | 41.04 | 40.75 | 41.91 | 41.14 | 40.84 |
| | 80 MHz Buffer | 50.49 | 46.68 | 44.89 | 50.83 | 46.93 | 45.1 | 51.06 | 47.09 | 45.23 |
| | T° Controller | 42.47 | 41.41 | 40.91 | 42.62 | 41.51 | 40.98 | 42.7 | 41.59 | 41.05 |
| VFDS | Linear regulator | 47.82 | 44.44 | 43.01 | 48.22 | 44.76 | 43.28 | 48.41 | 44.83 | 43.32 |
| V F | LVDS Receiver N | 39.62 | 39.22 | 39.13 | 39.8 | 39.34 | 39.22 | 39.9 | 39.4 | 39.27 |
| | OPAM N | 40.01 | 39.48 | 39.33 | 40.19 | 39.61 | 39.42 | 40.29 | 39.67 | 39.47 |
| | Crystal 1 | 38.15 | 38.19 | 38.33 | 38.3 | 38.28 | 38.37 | 38.4 | 38.32 | 38.42 |
| | LVDS Receiver R | 39.34 | 39.06 | 39.02 | 39.5 | 39.16 | 39.1 | 39.61 | 39.21 | 39.14 |
| | Crystal 2 | 38.57 | 38.69 | 38.89 | 38.72 | 38.78 | 38.94 | 38.82 | 38.82 | 38.97 |
| | OPAM R | 39.5 | 39.15 | 39.08 | 39.67 | 39.26 | 39.16 | 39.78 | 39.32 | 39.21 |

 Table 3.5
 Devices Temperature.
 Different PCBs configuration.

handling in automated equipment more difficult. Lower thicknesses have not been studied due to manufacturing and structural features, which are the responsibility of the manufacturer.

For further study, the configuration of 1.65 mm thickness and 14 copper layers is examined, as this thesis focuses on maximising the reliability improvement. However, the use of 10 layers in the case of simplifying the design would be more than justified given the obtained results.

3.2.2 Transient results

In order to consolidate that the proposed layout complies with the requirements of each PCB, this section carries out transitional analyses to the configuration presented above. As explained in Section 2.2, the transient results are obtained from the STELLA input function. This kind of analysis are very useful to check the behaviour of the quartz crystals and the Pilot Tone to a change of 5 degrees in the base of the enclosure.

In order to study the response of the Pilot Tone single-ended signal, the measurement points shown in Figure 3.15 have been established in CFDS, simulating the approximate path the signal would follow.

The thermal response of these selected points to the input function (marked in red) can be found in Figure 3.16. As it is described, the response to these points is smoother than the input function, in consequence of the distance between the point of application of the temperature change (base) and the Pilot Tone signal. This outcome shows an adequate result for this area and confirms the correct arrangement of the PCBs inside the enclosure.

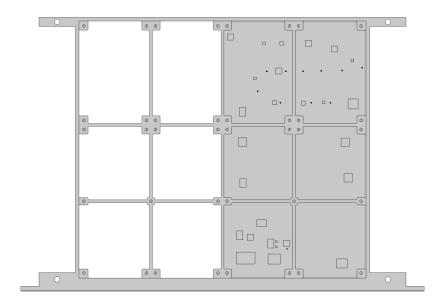


Figure 3.15 Pilot Tone measurement points.

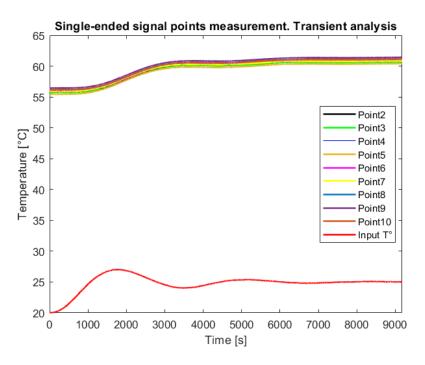


Figure 3.16 Pilot Tone measurement points transient response.

In the crystals behaviour Figure 3.17, it can be noticed the second-order response similarity to the input function due to the fact that it is very close to the base, where the change of temperature is applied. As it was mentioned previously, the proper functioning of quartz crystals is determined by the operating temperature, which should remain as cold as possible. The highest temperatures for this device could be reached then at the peak of this second-order function. Nevertheless, the graph shows that the response of the crystals is even softer than the input signal, so the peak is not as pronounced. Furthermore, it is proven in this graph that the maximum temperature to which it can be exposed is still low.

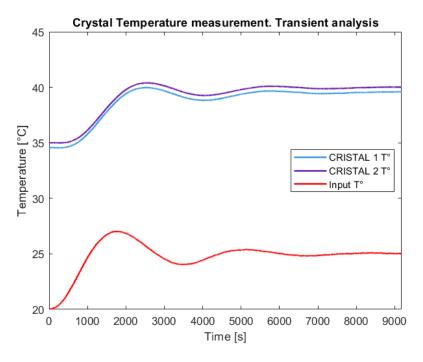


Figure 3.17 Crystals transient response.

It should be remembered that this input function is the experimental function used in this laboratory, which has been obtained by applying a change of five degrees using a vacuum chamber. However, in reality, the evolution of this five-degree temperature tolerance may be completely different.

For additional information, the transient response of the surface of each PCB has been included in Figure 3.18, proving again how the areas furthest from the base have a generally less pronounced result, and then confirming that the layout of both PCBs is appropriate.

3.2.3 Structural optimisation

In order to further optimise the module, an adjustment of the enclosure's shape is carried out. The enclosure can be modified by adding or removing aluminium or even changing its shape to improve the heat dissipation in some areas. However, the thermal improvement is meagre in relation to the weight added.

In pursuit of an overall improvement of the PMS, aluminium mass is removed to reduce the weight of the mission. For this purpose, mainly part of the internal ribs of the module have been removed, as the outer part of the module is exposed to more structural stresses and needs to be studied in depth to make significant changes to it. However, it is true that when placing the components, there is some excess space in the direction perpendicular to the plate. For this reason, the height of the module has also been reduced by five millimetres, from 50 mm to 45 mm in the outer area and from 20 mm to 15 mm in the area of the internal ribs. The final shape of the enclosure can be found in Figure 3.19.

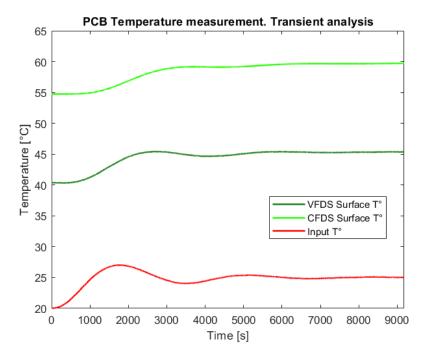


Figure 3.18 PCBs transient response.

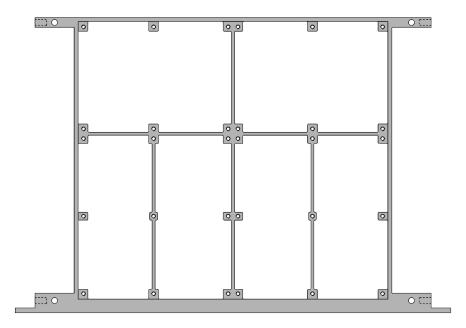


Figure 3.19 Optimised enclosure design.

The volume decrease from an initial value of $6.5707 \cdot 10^{-4}m^3$ to a final volume of $5.3984 \cdot 10^{-4}m^3$. These changes lead to a volume reduction of 17.84%, which can be translated into an aluminium mass saving of 316.521 grams.

Structural analysis

In the optimisation of the enclosure, it has been proposed to remove internal ribs and base volume to reduce weight. This motivates a structural analysis, as introduced in section 2.3. For the study of the new architecture a new COMSOL physics module was used, Structural Mechanics, in particular

the Solid Mechanics option.

The first step for the implementation in COMSOL has been to build the assembly. To get the structural response of this module, the complete assembly of the PMS has been built with the optimised module shown in Figure 3.19, superimposing seven units simulating the rest of the modules. The result of this assembly is illustrated in Figure 3.20. Although the rest of the modules may not have the same internal structure given the needs and geometry of each module, seven identical FDS design units have been arranged. The other modules are more complex and hotter, and therefore generally have a more robust internal structure. The safety factor is being increased by studying the worst case by doing the study only with the module with the lower internal reinforcement. In this assembly, a 2.5mm top and bottom cover and 2.5mm thick triangular stiffeners have also been added to the structure to achieve greater structural integrity. The final appearance of the structure is shown in Figure 3.20.

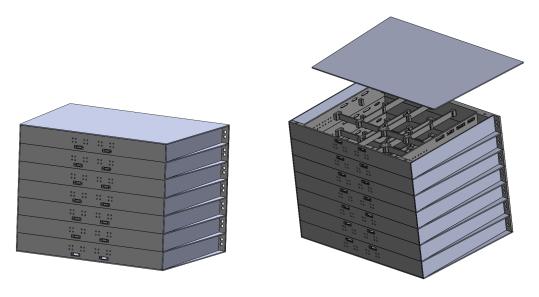


Figure 3.20 PMS assembly structure.

Neither the CHOTHERM nor the PCBs had been considered for this analysis since they have no structural function, thus having an assembly made of aluminium solids only. Detailed structural analyses of static, shock, thermal and vibration loads will be done in the future when the development is consolidated.

The implementation of the boundary conditions is then considered. Regarding the system's displacements conditions, the shifting in the perpendicular direction to the TRF surface is impeded, as mentioned in Section 2.3. To impose this restriction the 'Prescribed Displacement' option has been used in COMSOL, which allows to limit the movement on a single axis. In the applied case, the displacements of the base surfaces in the z-axis are restricted. In addition, as the screws are presupposed to be attached, the movement of the inner area of the screws is restricted in the assembly. This is implemented in COMSOL with the 'FIXED Constraint' option in the inner cylinder surface of the screw hole. The influenced surfaces by these boundary conditions are illustrated in Figure 3.21.

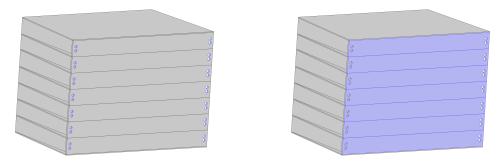
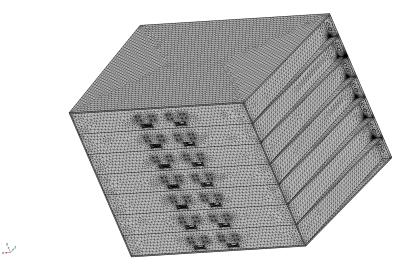
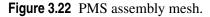


Figure 3.21 Boundary conditions on displacements.

To implement the 5G force in COMSOL, the 'Volumetric forces' option has been used, as it is not a point force or a force that acts on a surface of the solid but on each point of the solid. In particular, the 'Gravity' option has been used, as it allows the force to be written as a function of gravity.

Regarding the meshing, the generic tetrahedral mesh has been used again as shown in Figure 3.22. For the analysis of the assembly, given its more extensive volume, the size of the tetrahedral mesh can be replaced by a normal size by selecting the option 'Normal'. The number of elements generated amounts to 409436 elements, which is a reasonable number for the size of this structure.





The analysis applying the 5G load in the different axes yields the results listed in Table 3.6. These values verify that the assembly's maximum stresses do not exceed the aluminium's yield strength $\sigma_{Al}^{yield} = 276 \cdot 10^6 Pa$ in none of the axes. Therefore, it is demonstrated that the proposed enclosure meets the preliminary structural requirements, allowing the this optimised design to be adopted as the new internal configuration of the module.

| Load direction | Max Stress[N/m^2] | Max displacement [m] |
|----------------|-----------------------|----------------------|
| Х | $2.88 \cdot 10^{6}$ | $1.75 \cdot 10^{-5}$ |
| Y | $1.54 \cdot 10^{6}$ | $4.12 \cdot 10^{-6}$ |
| Ζ | $1.79 \cdot 10^{6}$ | $2.09 \cdot 10^{-6}$ |

3.3 Final results

After replacing the enclosure by the optimised one, a final thermal analysis is carried out. The obtained thermal distribution is presented in Figure 3.23, which clearly confirms that the Pilot Tone signal will not be exposed to a high temperature gradient on its path along the PCB, avoiding the coupling noise effects.

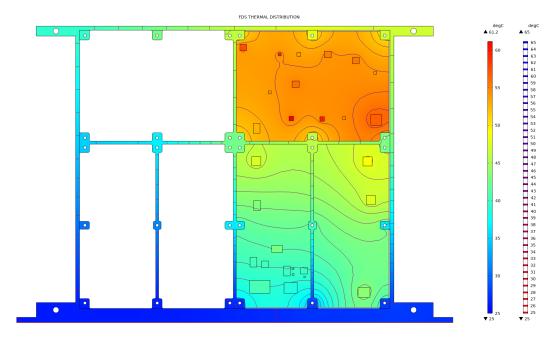


Figure 3.23 Final thermal distribution.

| DEVICES TEMPERATURE [°C] | | | | | |
|--------------------------|-------|------------------|-------|--|--|
| CFDS | | VFDS | | | |
| Linear regulator | 55.59 | USO Buffer | 46.94 | | |
| Telemetry controller | 56.58 | PPS Buffer | 48.45 | | |
| Switch 1 | 54.63 | LVDS Driver | 41.91 | | |
| Power divider 1 | 58.05 | 80 MHz Buffer | 47.14 | | |
| Power divider 2 | 57.23 | T° Controller | 43.14 | | |
| Switch 2 | 53.83 | Linear regulator | 43.5 | | |
| LNA 1 | 55.38 | LVDS Receiver N | 39.85 | | |
| T° Controller | 52.64 | OPAM N | 39.85 | | |
| LNA 2 | 56.6 | Crystal 1 | 38.63 | | |
| Mixer | 53.56 | LVDS Receiver R | 40.2 | | |
| LNA 3 | 54.72 | Crystal 2 | 39.67 | | |
| Adder | 54.99 | OPAM R | 40.15 | | |
| Switch 3 | 54.13 | - | - | | |

| Table 3.7 | Final | working | temperatures. |
|-----------|-------|---------|---------------|
|-----------|-------|---------|---------------|

Moreover, the working temperature data from this analysis is reported in Table 3.7. Comparing these results with the ones obtained in the initial distribution, listed in Table 3.3, it can be checked that the operating temperature of all the devices has been reduced. This is of great importance for devices such as the telemetry controller and linear regulator in the CFDS, which are the ones that

consume more power; in those there has been a decrease of approximately 3 degrees in the operating temperature. In the case of the VFDS linear regulator, this reduction has been almost five degrees.

Lastly, the reliability calculations based on the working temperature of each component are presented for VFDS and CFDS in Tables 3.9 and 3.10 respectively, where the data has been obtained by adjusting the FIT with the acceleration factor caused by the effect of the temperature from Equation 2.9. Table 3.8 summarises the yielded results of the updated model and the ones obtained in the preliminary reliability analysis, showing an improvement in the reliability of 0.03% for the VFDS and 0.05% for the CFDS.

| Table 3.8 | Final | reliability re | sults. |
|-----------|-------|----------------|--------|
|-----------|-------|----------------|--------|

| PCB | Final Reliability % | Preliminary reliability % |
|------|---------------------|---------------------------|
| VFDS | 99.88 | 99.85 |
| CFDS | 97.98 | 97.93 |

| BLOCK | DEVICE | FIT | NEW FIT | RELIABILITY | RELIABILITY BLOC | |
|----------------|------------------|---------|---------|-------------|------------------|-------|
| USO BUFFER | USO Buffer | 2.8 | 1.50175 | 0.999828319 | 0.99982 | 28319 |
| PPS BUFFER | PPS Buffer | 2.8 | 1.69131 | 0.999828319 | 0.99982 | 28319 |
| | OPAM N | 1.17 | 0.35306 | 0.999928258 | | |
| | Diode | 0.59375 | 0.59375 | 0.999963592 | | |
| VCXO NOMINAL | Crystal N | 18 | 4.9072 | 0.998896849 | 0.99878851 | 1 |
| | Transistor 1 | 0.0025 | 0.0025 | 0.999999847 | | |
| | Transistor 2 | 0.0025 | 0.0025 | 0.999999847 | | |
| | OPAM R | 1.17 | 0.3619 | 0.999928258 | 0.00747064 | |
| VCXO REDUNDANT | Crystal R | 40 | 11.8897 | 0.997550206 | 0.99747864 | |
| RECEIVER | LVDS Receiver | 5.4 | 1.62951 | 0.999668927 | 0.99966893 | 1 |
| | LVDS Driver | 2.9 | 1.03679 | 0.999822188 | | |
| 80MHz BUFFER | 80 MHz Buffer | 2.8 | 1.52564 | 0.999828319 | 0.999650537 | |
| REGULATOR | Linear regulator | 4.29 | 1.7463 | 0.999736972 | 0.999736972 | |
| T° SENSOR | T° Sensor | 2.8 | 1.10645 | 0.999828319 | 0.99982 | 28319 |

Table 3.9 VFDS Final reliability calculations.

| BLOCK | DEVICE | FIT | NEW FIT | RELIABILITY | BLOCK | RELIABILITY |
|--------------|----------------------|--------|---------|-------------|-------------|-------------|
| | Linear regulator | 4.29 | 4.48598 | 0.999724958 | 0.999628362 | |
| | Telemetry controller | 1.4 | 1.57578 | 0.999903378 | | |
| | LPF 1 | 85.216 | 85.216 | 0.994788184 | | |
| | Splitter 1 | 96.572 | 96.572 | 0.994095704 | | |
| | Switch 1 | 26.7 | 25.9581 | 0.998409518 | 0.98734 | |
| PT OPTION | Power divider 1 | 0 | 0.01 | 0.999999387 | | 1 |
| | Power divider 2 | 0 | 0.01 | 0.999999387 | | |
| | - | 0 | 0 | 1 | 1 | |
| | Switch 2 | 26.7 | 24.4365 | 0.998502676 | 0.995388752 | |
| DIGTDIDUTION | LPF 2 | 10.68 | 10.68 | 0.999345317 | | |
| DISTRIBUTION | LNA 1 | 0.25 | 0.25717 | 0.999984231 | | |
| | Splitter 2 | 40 | 40 | 0.997550206 | | |
| PMS 2 CHAIN | Linear regulator | 4.29 | 4.48598 | 0.999724958 | | |
| | Telemetry controller | 1.4 | 1.57578 | 0.999903378 | 0.988547142 | |
| | LPF 1 | 85.216 | 85.216 | 0.994788184 | | |
| | Splitter 1 | 96.572 | 96.572 | 0.994095704 | | |
| 1 MHz CHAIN | LNA 2 | 1.269 | 1.43115 | 0.999912246 | | |
| | Mixer | 3.953 | 3.54566 | 0.999782604 | 0.99607329 | |
| | LNA 3 | 0.25 | 0.2447 | 0.999984995 | | |
| | LPF 3 | 23.01 | 23.01 | 0.998590022 | | |
| | Adder | 0.25 | 0.24986 | 0.999984679 | | |
| | LPF 4 | 10.68 | 10.68 | 0.999345317 | | |
| | Switch 3 | 26.7 | 25.001 | 0.998468111 | | |
| T° SENSOR | T° Sensor | 2.8 | 1.10645 | 0.999828319 | 0.99 | 99828319 |

Table 3.10 CFDS Final reliability calculations.

4 Conclusions and future work

4.1 Conclusions

The obtained results yield some clear conclusions. First of all, very favorable reliability results have been obtained for both PCBs, this being a value adjusted to reality by considering the effect of heating on each component. This allows to deduce that a second redundant FDS would not be necessary, proposing to use the enclosure space reserved for it for other functions, thus saving mass and cost.

Besides, the achieved reliability improvement is very low. This is due to the fact that none of the devices had a high failure rate, whose decrease in the working temperature could lead to a significant improve on the reliability of the whole PCB. However, a decrease up to 5 degrees has been achieve for some of the devices. Although it does not have a relevant impact on reliability, it is a minor source of heating that can influence the rest of the components.

Furthermore, an optimal and justified positioning of the quartz crystals, which play a crucial role in the operation of the plate, has been achieved, as well as ensuring that the temperature gradients couples minimally to the Pilot Tone electronic circuitry. This is in addition to a mass reduction of the enclosure of 17.84%, without affecting the performance of both PCBs.

4.2 Future work

Once the analysis developed in this thesis has been presented, the main line of work proposed is to carry out the same process for the rest of the modules that form the PMS: DHLC, PSM and BEE. This would lead to realistic reliability results for the whole PMS, allowing to check whether the PMS complies with the requirements imposed by the mission. Further, the physical architecture of the PMS can be defined based on this result, including redundant modules needed to meet the reliability requirements imposed by design or, on the contrary, eliminating them. Therefore, the PMS reliability result becomes an essential design factor for the mission given the close relationship between module redundancy with a more electrical complexity due to a higher number of connections, increased weight, more money investment or difficulties in programming to activate or deactivate modules that are in cold redundancy.

Another important aspect be to improve is the uniformity in the method of obtaining the failure rate. As a requirement of the mission, these data shall be provided by the manufacturer. However,

there is disparity in the methods and in some cases differences in the confidence levels used. Although reliability is an estimate, it would be desirable to start from a common source method and standardize the studies, so quick changes can be implemented without compromising the whole analysis. Future works considers to move forwards in RAMS analyses, crucial in all space mission to ensure quality standard in the realization of flight hardware.

Appendix A

Data and additional calculations

A.1 Reliability data

| PCB | Device | FIT | Т | CL | Ea | Source |
|------|----------------------|--------|----|----|-----|-------------------------------|
| | Telemetry controller | 1.4 | 55 | 60 | 0.7 | Manufacturer calculation tool |
| | Powe divider 2 | 0 | 55 | 90 | 0.7 | Manufacturer calculation tool |
| | Power divider 1 | 0 | 55 | 90 | 0.7 | Manufacturer calculation tool |
| | T Sensor | 2.8 | 55 | 60 | 0.7 | Manufacturer calculation tool |
| | ADDER | 0.25 | 55 | 90 | 0.7 | Manufacturer calculation tool |
| | LNA* | 0.25 | 55 | 90 | 0.7 | Manufacturer calculation tool |
| S | Switch | 26.7 | 55 | 60 | 0.7 | Manufacturer calculation tool |
| CFDS | Linear regulator | 4.29 | 55 | 90 | 0.7 | Reliability report |
| | LNA 2 | 1.27 | 55 | - | - | MIL-HDBK-217F |
| | Mixer | 3.95 | 55 | - | - | MIL-HDBK-217F |
| | Power splitter 1 | 24.14 | 55 | - | - | MIL-HDBK-217F |
| | Power splitter 2 | 40 | 55 | - | - | MIL-HDBK-217F |
| | LPF1 | 42.61 | 55 | - | - | MIL-HDBK-217F |
| | LPF2 | 10.68 | 55 | - | - | MIL-HDBK-217F |
| | LPF3 | 23.01 | 55 | - | - | MIL-HDBK-217F |
| | Buffer | 2.8 | 55 | 60 | 0.7 | Manufacturer calculation tool |
| | OPAM | 1.14 | 55 | 90 | 0.7 | Manufacturer calculation tool |
| | Crystal N | 18 | 55 | - | - | MIL-HDBK-217F |
| S | LVDS Receiver | 5.4 | 55 | 60 | 0.7 | Manufacturer calculation tool |
| VFDS | Crystal R | 40 | 55 | - | 0.7 | MIL-HDBK-217F |
| | T Sensor | 2.8 | 55 | 60 | 0.7 | Manufacturer calculation tool |
| | Linear regulator | 5 | 55 | 90 | 0.7 | Manufacturer calculation tool |
| | Diode | 0.59 | 55 | - | - | MIL-HDBK-217F |
| | Transistor | 0.0025 | 55 | 90 | 0.7 | Reliability report |

 Table A.1 Devices reliability data.

A.2 Thermal data

| PCB | Device | Surface [m ²] | Volume [m ³] | θ_{JC} [°C/W] | k [W/mK] | Max Temp [°C] |
|------|----------------------|---------------------------|--------------------------|----------------------|----------|---------------|
| | Telemetry controller | 1.22E-04 | 2.81E-07 | 1 | 432.90 | 125 |
| | Power divider 2 | 2.09E-05 | 3.53E-08 | 61 | 9.70 | 85 |
| | Power divider 1 | 2.09E-05 | 3.53E-08 | 74 | 8.00 | 85 |
| | LVDS Driver | 7.91E-05 | 1.60E-07 | 22 | 22.39 | 125 |
| SC | Mixer | 1.63E-05 | 1.70E-08 | 105 | 9.15 | 85 |
| CFDS | LNA | 4.70E-05 | 1.07E-07 | 22 | 19.88 | 125 |
| | Switch | 9.00E-06 | 7.20E-09 | 17 | 73.53 | 125 |
| | Linear regulator | 4.53E-05 | 1.32E-07 | 21 | 16.30 | 125 |
| | LNA 2 | 9.00E-06 | 1.03E-08 | 116 | 7.56 | 125 |
| | ADDER | 4.70E-05 | 1.07E-07 | 22 | 19.88 | 125 |
| | Buffer | 8.61E-05 | 1.91E-07 | 13.4 | 33.56 | 125 |
| | OPAM | 4.69E-05 | 5.40E-08 | 22 | 39.53 | 125 |
| S | Crystal N | 1.47E-04 | 7.37E-07 | - | - | 60 |
| VFDS | LVDS Receiver | 6.80E-05 | 1.38E-07 | 20 | 24.61 | 125 |
| | Crystal R | 2.71E-04 | 2.03E-06 | - | - | 70 |
| | T Sensor | 6.80E-05 | 1.38E-07 | 11.2 | 43.94 | 125 |
| | Linear regulator | 1.21E-04 | 3.75E-07 | 3.3 | 97.75 | 150 |

| | Table A.2 | Devices | thermal | data. |
|--|-----------|---------|---------|-------|
|--|-----------|---------|---------|-------|

* The particular data from this device has been extracted from the military standard MIL-STD-1835D [27].

A.3 Power Budget

Every electronic device will be modelled as Figure 2.2, where the internal heat is characterised by its power consumption. This Annex details the obtained values that have been used in the thermal simulation. Since the design is not mature enough to have accurate and complete electronic simulations of each PCB, this power budget has been developed by different sources:

- The main source of information has been taken from the literature. As the value of the voltage at which each component works is known (either because it is the only one possible, or because it is the one at which it has been programmed by design), the typical value of the current at which each component works is obtained from the datasheet.
- Electronic simulations in LT Spice of specific parts of the design which were more mature at that moment.
- Specialised simulations depending on the function of the component. This is the case of the telemetry controller in the CFDS, whose working current based on the programmed frequencies is higher than the typical value provided in the datasheet. This value had been obtained with the manufacturer's simulation tool.

Note that the power consumed by the regulators is determined by the number of elements it has to supply. For this reason, the following formula has been applied for each case

$$P_{regulator} = (V_{in} - V_{out}) \cdot \sum I_{total}$$
(A.1)

After these clarifications, the power consumption per component is shown in Table A.3 for the VFDS and A.4 for the CFDS. The obtained results induce that the main power consumers are the linear regulators and the telemetry controller. This will lead to special considerations regarding their location on the PCB, in order to avoid the overheating of this components.

| Component | Qty VFDS | Power per unit [W] | Total power [W] |
|------------------|----------|--------------------|-----------------|
| LVDS Driver | 1 | 0.1155 | 0.1155 |
| Buffer | 3 | 1.1022 | 3.3066 |
| Amplifier | 2 | 0.029 | 0.058 |
| Quartz crystal 1 | 1 | 0.001 | 0.001 |
| Transistor | 2 | 0.015 | 0.03 |
| LVDS Receiver | 1 | 0.055 | 0.055 |
| Quartz crystal 2 | 1 | 0.1 | 0.1 |
| T controler | 1 | 0.0107 | 0.0107 |
| Linear regulator | 1 | 1.7629 | 1.7629 |
| | TOTAL | VFDS POWER [W] | 5.4397 |

| | Table A.3 | VFDS Power Budget. |
|--|-----------|--------------------|
|--|-----------|--------------------|

| Table A.4 | CFDS Power Budget. |
|-----------|--------------------|
|-----------|--------------------|

| Component | Qty CFDS Power per unit [W] | | Total power [W] |
|---------------------|-----------------------------|---------|-----------------|
| Frequency converter | 1 | 1.3365 | 1.3365 |
| 4 divider | 1 0.735 | | 0.735 |
| 8 divider | 1 | 0.525 | 0.525 |
| Switch | 3 | 0.0013 | 0.0039 |
| T controller | 1 | 0.0107 | 0.0107 |
| LNA | 3 | 0.45 | 1.118 |
| Linear regulator | 1 | 0.83402 | 0.83402 |
| LNA 2 | 1 0.28248 | | 0.28248 |
| | TOTAL CFDS POWER [W] | | 4.8456 |

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