A detailed study of the gate/drain voltage dependence of RTN in bulk pMOS transistors

P. Saraza-Canflanca[1], J. Martin-Martinez[2], R. Castro-Lopez[1], E. Roca[1], R. Rodriguez[2], M. Nafria[2], F. V. Fernandez[1]

[1]Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla.
Calle Américo Vespucio 28, Isla de la Cartuja, 41092 Sevilla, Spain.
[2]Electronic Engineering Department (REDEC) group, Universitat Autònoma de Barcelona (UAB), Barcelona, Spain
Corresponding author: Francisco V. Fernandez (Francisco.Fermandez@imse-cnm.csic.es)

Abstract

Random Telegraph Noise (RTN) has attracted increasing interest in the last years. This phenomenon introduces variability in the electrical properties of transistors, in particular in deeply-scaled CMOS technologies, which can cause performance degradation in circuits. In this work, the dependence of RTN parameters, namely current jump amplitude and emission and capture time constants, on the bias conditions, both V_G and V_D, has been studied on a set of devices, with a high granularity in a broad voltage range. The results obtained for the V_G dependences corroborate previous works, but suggest a unique trend for all the devices in a V_G range that goes from the near-threshold region up to voltages over the nominal operation bias. However, different trends have been observed in the parameters dependence for the case of V_D. From the experimental data, the probabilities of occupation of the associated defects have been evaluated, pointing out large device-to-device dispersion in the V_D dependences.

Keywords

Random Telegraph Noise, variability, CMOS, transistors, bias dependence

1. Introduction

In the past few years, Random Telegraph Noise (RTN) has become of increasing interest. The reason for this is its role as a source of performance variability in transistors, especially in deeply-scaled CMOS technologies [1]. Significant RTN-induced performance degradation has been reported for circuits such as SRAMs or Ring Oscillators [2]. Furthermore, this impact is expected to increase as technology continues to scale. Therefore, to develop circuits in the nm-range that are resilient to RTN, it is first and foremost necessary to characterize its parameters and their dependence on the bias conditions.

RTN is observed as sudden and random discrete jumps in the drain current (I_D) of the device, which have been associated to changes in the threshold voltage linked to the capture/emission of charge carriers in/from defects in the device. The parameters that characterize the RTN signals are the amplitude of the current jumps, either in absolute or relative terms, and their time constants. These constants are the capture time or τ_c, which is the average time that an RTN defect takes to capture a charge carrier when it is empty, and the emission time or τ_e, which is the average time that a defect takes to emit the charge carrier once it is occupied. The defects that cause RTN can be present in the transistor right after it has been fabricated or can be generated afterwards, during device operation, by degradation mechanisms [3].

Although there are some studies about the dependence of the defect trapping/detrapping parameters on bias conditions, they usually focus on the gate voltage dependence only. In addition, this dependence is usually analyzed by taking only a few bias voltages [4], [5]. In this work, we have thoroughly studied the dependence of the RTN current jump amplitudes and time constants on both drain and gate bias voltages. This exhaustive study of the bias-dependence is especially interesting for the drain voltage (V_D), the effect of which on RTN has not been often analyzed up to this moment.

The rest of this paper is structured as follows. A brief description of the experimental setup and the characterization tests are presented in Section 2. Then, in Section 3, the main experimental results are described and discussed. Finally, conclusions are drawn in Section 4.

2. Experimental framework

In this Section, the main features of the experimental setup and the RTN characterization experiments are briefly summarized. A more detailed description of the complete experimental setup can be found in [6].

2.1 A transistor-array chip for variability characterization

The transistor-array chip in [7], designed for the characterization of time-zero and time-dependent variability, was fabricated in a 1.2-V, 65-nm CMOS technology. The main advantage of this array-based approach with respect to a conventional probe station solution is that it allows the allocation of a high number of transistors in a much smaller area. The characterization chip consists of more than 3,000 transistors, half of which are pMOS and the other half nMOS. Each transistor is embedded into a unit cell that contains the necessary circuitry to allow individual access to its terminals. The chip incorporates a Force & Sense system to avoid undesirable voltage drops, which are not present in a conventional probe station approach but appear in a transistor-array chip such

as the one used in this work. This system enables the application of an accurate voltage to each device terminal. This feature is fundamental for the correct characterization of the dependence of the RTN parameters on the bias conditions.

2.2 Experimental setup

The main components of the experimental setup used for the measurements presented in this work are displayed in Fig. 1. These are:

- A full-custom printed circuit board (PCB) in which the characterization chip is inserted. This PCB is provided with shielded triaxial connectors that allow the access to the analog signal chip paths while minimizing the noise present in the measurements.
- The Keysight Semiconductor Parameter Analyzer, model B1500A, equipped with 4 High Resolution Sense Measurement Units (HRSMU). Each HRSMU contains a Force & Sense triaxial output, which enables accurate voltage application and current measurement.
- An Agilent power supply, model E3631A, which supplies biasing for the PCB and the characterization chip.
- An USB data acquisition system from National Instruments, which is in charge of providing the digital signals needed to perform the tests.
- The IEEE 488.1 GPIB bus, which is used for the interconnection and communication between the personal computer, which serves as a controller, and the rest of the instrumentation.

Apart from the hardware components listed above, another key feature of the measurement system is TARS [8], a software tool designed for the automated generation, execution and control of the characterization tests. This tool, which is provided with a user-friendly graphical interface, generates the thousands of GPIB commands needed for regular RTN experiments, liberating the user from this time-consuming and prone-to-error task.

2.3 RTN characterization tests

For this work, 20 pMOS 80nm x 60nm transistors from the characterization chip were measured. These transistors were selected from a larger set of devices, because they displayed RTN signals where the contribution of individual defects can be clearly distinguished, so that the characteristics of individual defects can be evaluated. Then, the dependence of the RTN transition amplitudes and time constants on both drain and gate bias has been evaluated by monitoring more than 20 defects over a broad range of gate voltages ($0.6V \leq V_G \leq 1.6V$) while keeping $V_D = 0.1V$, and a broad range of drain voltages ($0.1V \leq V_D \leq 1.2V$) while keeping $V_G = 0.8V$. Both gate and drain voltages have been swept with a step of 0.025V within their corresponding range, so that the defects behavior was studied for ~ 40 different voltages. In the case of V_G, this range covered from the near-threshold region up to stress conditions (i.e., voltages over the nominal conditions). For each voltage, RTN signals were recorded during 100 s, with a sampling period of 2 ms. To the best of the authors' knowledge, this is the first work to present such a thorough study of the dependence of the RTN parameters on the bias conditions, especially on V_D.

3. Results and Discussion

For the sake of illustration, typical current traces measured with our experimental setup on two transistors of the characterization chip at $V_G = 0.7V$ and $V_D = 0.1V$ are shown in Fig. 2. In it, the raw measured current is displayed in blue, while the post-processed, background-noise-free trace is displayed in red. The processing of the raw RTN data is performed with an automated Maximum-Likelihood-Estimation-based method.

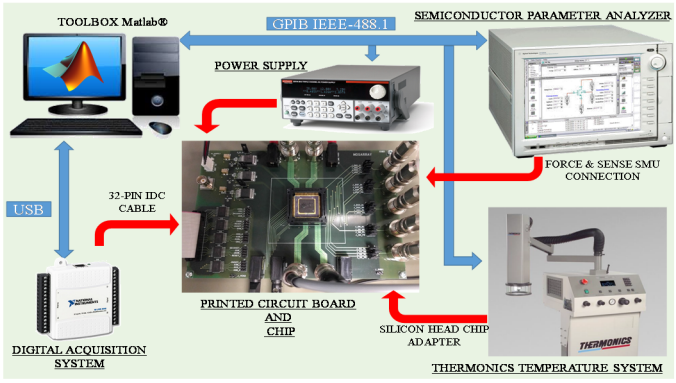

Fig. 1. Schematic representation of the experimental setup used in this work.

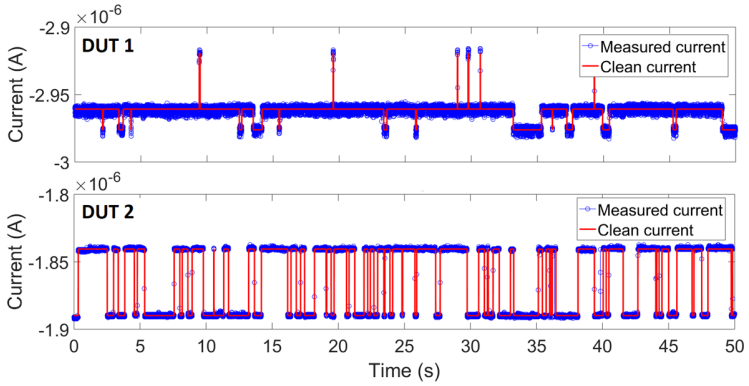

Fig. 2. Current traces measured at V_G = 0.7V and V_D = 0.1V on two transistors of the characterization chip used in this work. In blue, the raw measured current. In red, the "clean" or processed background-noise-free current. The abrupt current jumps seen in both transistors are caused by RTN transitions. In the upper trace, there are two detectable defects causing RTN. In the lower one, there is a single defect causing RTN.

3.1 RTN amplitude dependence on bias conditions

The dependence of the RTN current jump amplitudes on the bias conditions has been first analyzed. As an example, Fig. 3 shows the amplitude of the current jumps, in absolute and relative terms, for 5 of the studied defects, when V_D = 0.1 V and V_G is swept from 0.6 V to 1.6 V, that is, from the near-threshold region to voltages above the nominal power supply voltage. For all the analyzed defects, it has been observed that the absolute amplitude of the RTN transition increases with V_G, until a maximum is reached, and then decreases. The relative amplitude of the current jumps is often used in the literature to characterize RTN [9]. This was found to decrease over the whole measured range, which means that RTN has a larger impact at low or near-threshold gate voltages, a dependence that has been reported in the literature [10]. This must be taken into account in applications that require low power consumption, which often use a low supply voltage, and would be therefore more affected by RTN.

As an example, Fig. 4 displays the current jumps for 4 of the monitored defects, both in absolute and relative terms, when V_G is kept at 0.8 V and V_D is varied. In the case of V_D, two distinct behaviors have been observed. For some defects, the absolute amplitude of the RTN current jumps increases with V_D until it reaches a maximum value, and then decreases from that point on, while the relative amplitude decreases with V_D over the whole measured range. For the other defects, the absolute amplitude increases with V_D over the whole measured range, while the relative amplitude increases with V_D until it reaches a maximum and decreases from that point on.

3.2 RTN time constants dependence on bias conditions

After investigating the dependence of the RTN amplitudes on the bias conditions, the focus was moved to the emission and capture time constants. An example of the dependence of both time constants τ_e and τ_c of one of the monitored defects on the gate bias V_G is displayed in Fig. 5. As expected, τ_e has been found to increase and τ_c to decrease with the gate bias [11]. This

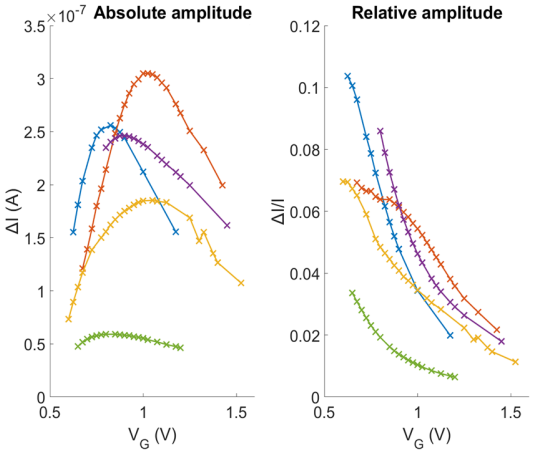

Fig. 3. Dependence on V_G of the absolute (left) and relative (right) RTN amplitude for five defects measured at V_D = 0.1V and V_G ranging from 0.6V to 1.6V. The absolute amplitude increases until reaching a maximum, and then decreases from that point. On the other hand, the relative amplitude of the RTN jumps decreases with V_G across the whole measured range. This trend has been observed for all the defects studied.

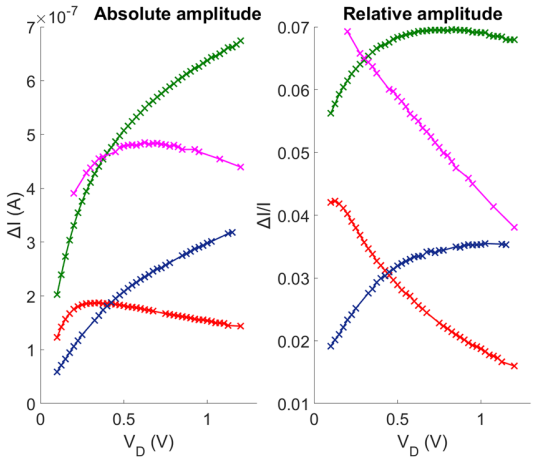

Fig. 4. Dependence on V_D of the absolute (left) and relative (right) RTN amplitude for four defects measured at V_G = 0.8V and V_D from 0.1V to 1.2V. Two different types of defects have been found. For the first type, the relative amplitude of the RTN jumps decreases with V_D over the whole measured range. For the other type, it increases until it reaches a maximum, and decreases from that point.

behavior is observed for all the analyzed defects. The bias dependence of the time constants shows, in general, a linear behavior in a logarithmic time scale, and it is therefore possible to assign them an exponential behavior as the one described by:

$$\tau_i = \tau_{0i,j} 10^{\beta_{i,j} V_j} \quad (1)$$

where *i* corresponds to emission or capture, and *j* to gate or drain. The extracted parameters for these dependences, together with their standard deviations, are listed in Table 1. Although the gate bias dependence of the time constants has been found to follow a general trend for all the defects studied (that of Fig. 5), that is not the case for the drain bias dependence. To show this point, two measured examples, which display a different behavior, are shown in Fig. 6. Note that, although τ_c increases for defect 1, it decreases for defect 2. The dependence of the time constants is stronger on V_G than on V_D, and, on average, opposite tendencies are observed (i.e. τ_e decreases whereas τ_c increases with V_D), as can be seen in Table 1.

V_G				**V_D**			
$<\beta_{e,G}>$	$\sigma(\beta_{e,G})$	$<\beta_{c,G}>$	$\sigma(\beta_{c,G})$	$<\beta_{e,D}>$	$\sigma(\beta_{e,D})$	$<\beta_{c,D}>$	$\sigma(\beta_{c,D})$
2.6	1.6	-3.5	1.1	-1.3	2.0	0.1	0.7

Table 1. Mean value and standard deviation of the parameters of the exponential dependence of the time constants on V_G and V_D, measured in the set of investigated devices. In general, the time constants of the defects show a greater dependence on V_G than on V_D. Standard deviations are not negligible for any of the dependences.

From the time constants at given bias conditions, it is possible to determine the probability of a defect being occupied, known as the occupancy probability (p_{occ}), which is the relevant parameter for the evaluation of the degradation of device performance [12], as:

$$p_{occ} = \frac{\tau_e}{\tau_e + \tau_c} \quad (2)$$

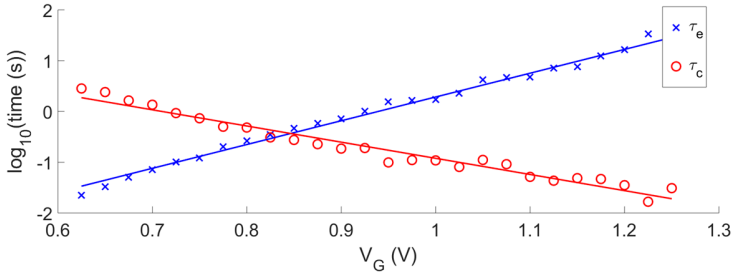

Fig. 5. Experimental dependence of the time constants of a defect on V_G (crosses), together

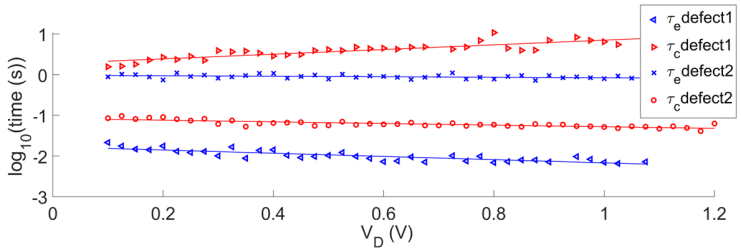

Fig. 6. Experimental dependence of the time constants of two defects on V_D, together with the corresponding linear fitting in a logarithmic time scale. The time constants of different defects have been found to display different behaviors with V_D, which translates into different dependences of their occupancy probabilities, as can be seen in Fig. 7.

Since this probability is based on bias-dependent time constants, it is bias-dependent itself. The dependence of the occupancy probability of the monitored defects on both V_G and V_D is depicted in Fig. 7. In the case of V_G, all the analyzed defects display the same trend, in accordance to the observed dependence of their time constants on V_G. In particular, they feature a sigmoid-type behavior with V_G, so that the defects tend to be occupied when V_G is increased. This corroborates the link between RTN and Bias Temperature Instability (BTI) that has been discussed in previous works [13]. When the gate bias is increased, defects tend to be occupied (BTI behavior), causing a degradation in the transistor operation. At lower gate bias, the impact of the defect will be observed as RTN. Interestingly, for all the defects analyzed in this work, the same kind of dependence for the time constants has been found from the near-threshold region up to voltages over the nominal power supply.

In contrast to the sigmoid behavior with V_G displayed by all the investigated defects, the dependence of the occupancy probability on V_D has been found to be different for different defects, as can be seen in Fig. 7 (right). This is in accordance with the different dependences of the time constants on V_D, which has already been discussed and displayed in Fig. 6. For instance, in Fig. 7, some defects can be occupied at low V_D (circles), while others are partially occupied (crosses). The p_{occ} could decrease (squares) or stay almost constant (diamonds) with V_D. Further analysis is required to explain the different behavior of the defects, but it could be related to the location of the defect along the channel, which has been demonstrated to have a different impact on the device threshold voltage [14]. In any case, the large dispersion in the observed behaviors of defects depending on V_D complicates the modeling of RTN dependence on V_D, which is critical for the evaluation of its impact on circuit performance.

4. Conclusions

In this work, the dependence of the RTN parameters, namely current jump amplitude and time constants, on both V_G and V_D, has been investigated. The results obtained for the V_G dependence corroborate the trends found in previous works and support their validity in a broad range of bias. All the investigated defects show the same type of behavior when V_G is considered. However, this is not the case when analyzing V_D dependences. In this case, two distinct behaviors were found for the current jump amplitudes. For some defects, the relative amplitude of the current jumps decreases over the whole investigated V_D range, while for other defects that amplitude seems to increase until it reaches a maximum, and then decreases from that point on. The

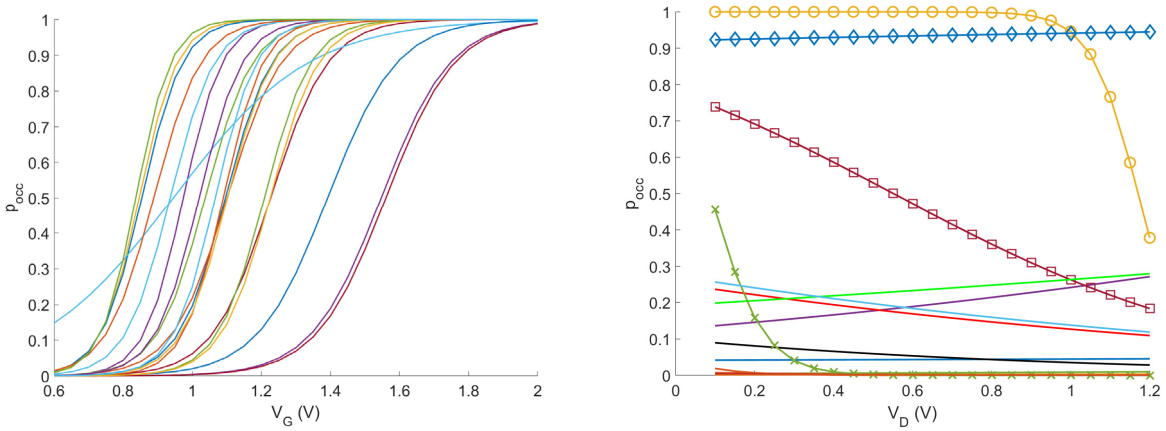

Fig. 7. Calculated dependence of p_{occ} on V_G (left) and V_D (right) of all the studied defects. On the one hand, the dependence of p_{occ} on V_G displays the same general behavior for all the analyzed defects. On the other hand, the p_{occ} of different defects display different dependences on V_D. Interestingly, some defects can be occupied at low V_D, and can be desoccupied at high V_D (circles), while others are partially occupied at low V_D, and are rapidly desoccupied when V_D is slightly increased (crosses). Moreover, p_{occ} could steadily decrease (squares) or stay almost constant (diamonds) when V_D increases.

emission and capture time constants display a linear behavior on V_D in a logarithmic time scale, though increasing and decreasing dependences could be observed. Furthermore, the dependence of the occupancy probability on V_G and V_D has been analyzed. In the case of V_G, all the defects show a sigmoidal-type dependence, being able to identify defects that would display RTN or BTI behavior, depending on V_G. Then, considering the numerical values found for the parameters of the emission/capture times V_G dependences, the device performance degradation could be modeled and predicted, from V_G in the near-threshold region to voltages over the nominal bias conditions. In the case of V_D, very different dependences were found for the occupancy probability in the set of devices. These device-to-device differences will have to be included into the device models, in order to accurately predict the impact of RTN on circuit performance.

Acknowledgements

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