University of Glasgow

Coughlan, C., Mirza, M. M.A. , Kirdoda, J. , Dumas, D., Smith, C., McCarthy, C., Mowbray, H., Watson, S. , Millar, R. and Paul, D. J. (2023) Variation of Sidewall Passivation on Sub-um Selectively Grown Ge-on-Si Devices Towards Single Photon Avalanche Detectors. In: SPIE OPTO 2023, San Francisco, CA, USA, 28 Jan-3 Feb 2023, (doi: 10.1117/12.2665493)

The material cannot be used for any other purpose without further permission of the publisher and is for private use only.

There may be differences between this version and the published version. You are advised to consult the publisher's version if you wish to cite from it.

https://eprints.gla.ac.uk/295043/

Deposited on 24 March 2023

Enlighten – Research publications by members of the University of Glasgow
http://eprints.gla.ac.uk

Variation of sidewall passivation on sub-um selectively grown Ge-on-Si devices towards single photon avalanche detectors

Conor Coughlan[a], Muhammad M.A. Mirza[a], Jaroslaw Kirdoda[a], Derek Dumas[a], Charles Smith[a], Charlie McCarthy[a], Hannah Mowbray[a], Scott Watson[a], Ross Millar[a], and Douglas J. Paul[a]

[a]James Watt School of Engineering, University of Glasgow, Rankine Building, Oakfield Avenue, Glasgow, G12 8LT, United Kingdom

ABSTRACT

Developing single photon avalanche diodes (SPADs) at short-wave infrared (SWIR) wavelengths beyond 1000 nm has attracted interest lately. Numerous quantum technology applications such as light detection and ranging (LIDAR), imaging through obscurants and quantum communications require sensitivity in this region. In quantum communications, operation at the telecoms wavelengths of 1310 nm and 1550 nm is essential. Ge-on-Si SPADs offer potential for lower afterpulsing and higher single photon detection efficiencies in the SWIR in comparison with InGaAs/InP SPADs, at a lower cost due to Si foundry compatibility. In this study, Ge-on-Si devices are fabricated on silicon-on-insulator (SOI) substrates, with a separate absorption, charge and multiplication layer (SACM) geometry and a lateral Si multiplication region. This Si foundry compatible process will allow for future integration with Si waveguides and optical fibres. The Ge is selectively grown inside sub-μm wide SiO_2 trenches, reducing the threading dislocation in comparison with bulk Ge; a typical process for integrated Ge detectors. Here we deliberately exposed Ge sidewalls with an etch-back technique, to allow a passivation comparison not normally carried out in selectively grown devices planarised by chemical-mechanical polishing. Reduced dark currents are demonstrated using thermal GeO_2 passivation in comparison to plasma-enhanced chemical-vapour-deposition SiO_2. The improved passivation performance of GeO_2 is verified by activation energy extraction and density of interface trap (D_{it}) calculations obtained from temperature-dependent capacitance-voltage (CV) and conductance-voltage (GV) measurements. This highlights the benefit of optimal surface passivation on sub-μm wide selectively grown Ge-on-SOI photodetector devices, potentially critical for waveguide integrated SPADs.

Keywords: single photon avalanche detectors, photonics, ge-on-si, selective growth, passivation

1. INTRODUCTION

A single photon avalanche detector (SPAD) allows the detection of light levels, down to that of a single photon. This is a mature technology in the area of visible light detection (from 400 to 1000 nm), due to the ubiquity of Si foundry processing and its bandgap at 1.1eV making it ideal for the absorption of this light. SPAD operation involves the electron-hole pair creation for a single photon, and the subsequent impact ionisation leading to a self-sustaining avalanche and a detectable current pulse. Si SPADs are used in a variety of different fields, including quantum communications, quantum information,[1] imaging through obscurants[2] and time-of-flight LIDAR.[3] However, there are limitations to operation in the visible and near-infrared (NIR), and extension of SPAD absorption to the short-wave infrared (SWIR) above 1000 nm is highly desirable. LIDAR for instance, can be improved by moving to the SWIR because of reduced solar background, higher laser safety thresholds[4] and lower scattering from obscurants.[5] In quantum communications applications crucially, one must also choose specific wavelengths (1550 nm or 1310 nm) that exist within low-loss transmission windows located in the SWIR.

Two classes of devices are used regularly in SWIR single photon detection, InGaAs/InP SPADs[6] and superconducting nanowire single photon detectors (SNSPDs).[7] SNSPDs provide exceptional single photon detection abilities, however these devices are limited by their relatively low operating temperature of approximately 4 K.

Further author information: (Send correspondence to Douglas J. Paul)
E-mail: Douglas.Paul@glasgow.ac.uk

InGaAs/InP SPADs by contrast, typically require temperatures of around 225 K, well within the range of relatively low-cost Peltier coolers. InGaAs/InP SPADs however, can be prohibitively expensive for a number of applications due to high material and fabrication costs. Furthermore, the effect of afterpulsing, the production of additional carriers after a detection event has occurred, limits the maximum count rate and possibility of widespread use. Another option for SPADs is to use Ge as an absorption layer, to extend the absorption of Si technology.[8] Ge has a smaller bandgap than Si and it allows photons of up to $\sim$ 1600 nm to be absorbed.[9] Inclusion of lightly p-doped Si charge layer between the absorption and multiplication region has been used to tailor the electric field in the device, such that photo-generated carriers can be swept into the multiplication region, where avalanche gain can occur. This inclusion creates a device geometry termed the separate absorption, charge sheet and multplication layer (SACM). Ge-on-Si SPADs have the potential to produce single photon detection with higher detection efficiencies and superior afterpulsing than InGaAs/InP SPADs, at higher operating temperatures than SNSPDs,[10] and the lower cost of Si production make these viable for commercial applications in the SWIR.[11][12]

In this work, Ge-on-Si devices with a SACM geometry and with a lateral Si multiplication layer are fabricated on 260 nm silicon-on-insulator (SOI) wafers, in a fully Si foundry compatible process. The possibility for quantum communication applications can be realised via integration with Si waveguides and optical fibres.[13] Reduction of threading dislocation density (TDD) in epitaxially grown Ge is achieved by selectively growing inside SiO_2 trenches.[14] Due to the small device size of waveguide geometry devices, Ge sidewalls have an increased contribution on the devices' performance in comparison to larger devices designed for surface-normal operation. Most selective grown Ge devices are planarised via chemical mechanical polishing (CMP), a process that maintains an interface between the Ge sidewalls and the SiO_2 they are grown in and does not allow optimal passivation of its sidewalls. Thus, understanding of the effects of sidewall passivation is crucial for high performance waveguide geometry devices including APDs and SPADs, and is investigated in this study regarding its dark current performance.

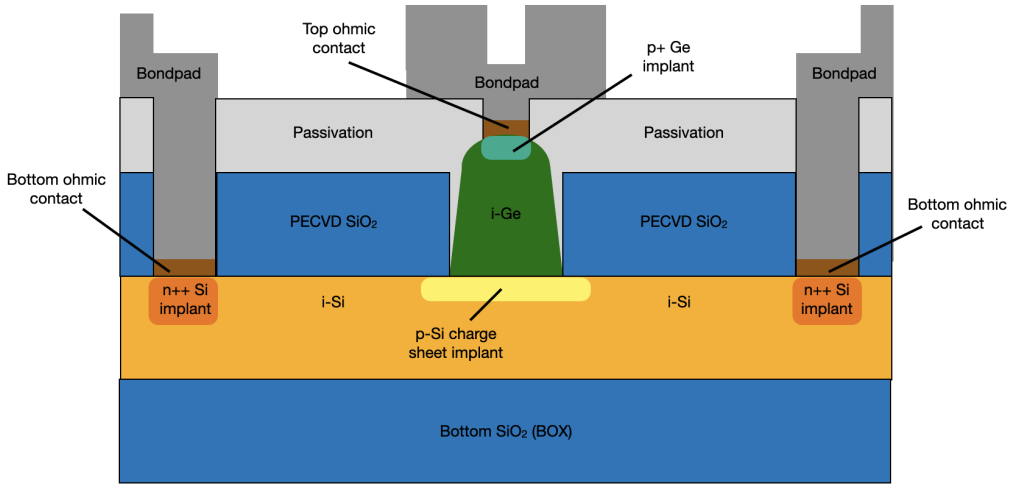

Figure 1. Schematic cross-section of selectively grown Ge-on-Si SPAD

2. DESIGN AND FABRICATION

The devices were fabricated on a 150 mm wafer SOI substrate material, with a 260 nm thick lightly doped p-Si (100) top layer, a 2 μm SiO_2 layer and a lightly doped p-Si substrate. Selective ion implantations were carried out on the top Si using electron-beam lithography to create the n^{++} contacts and charge sheet layer. The n^{++} region was implanted with As at 40 keV and a dose of 1×10^{15} cm^{-2} while the charge sheet was implanted with BF_2 at 20 keV with a dose of 1.8×10^{12} cm^{-2}. 250 nm of SiO_2 was deposited via PECVD and selective

reactive ion etching (RIE) was performed on this layer using CHF_3/Ar chemistry, opening windows in which Ge could be selectively grown. Ge selective growths were conducted after a further solvent and dilute HF clean, and afterwards the wafer was diced into individual chips. The Ge was etched back via another RIE step using flourine-based chemistry (SF_6/O_2) that is highly selective to Ge over SiO_2. The etch was monitored in-situ using a laser interferometer, stopping approximately at the same level as the SiO_2. This approach, in contrast with CMP, would expose the sidewalls of the Ge in doing so, and allow for optimal passivation to be used.

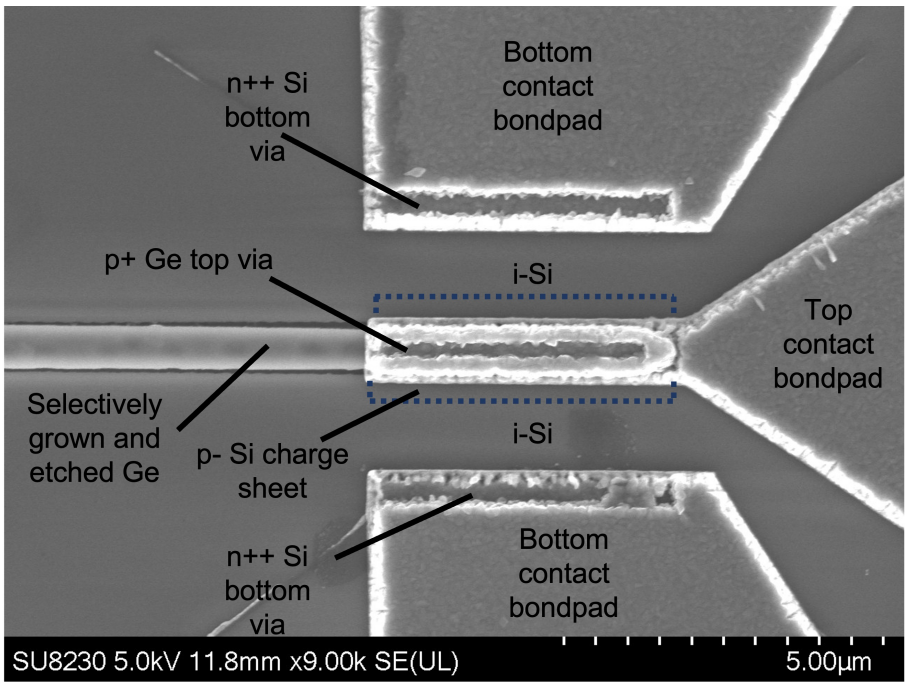

Figure 2. SEM image of fabricated selectively grown Ge-on-SI SPAD. The exposed sidewalls on the Ge make it possible to passivate

The top surface of the Ge was then implanted with boron to form a p^+ contact and activated at 400 °C for 60 seconds. The Ge was then passivated, and two passivations were compared. Firstly, a simple blanket 200 nm PECVD SiO_2 deposition was conducted, intending to approximate the passivation obtained from a CMP process. The second passivation involved a thermal oxidation of the Ge at 550 °C and a subsequent 200 nm PECVD Si_3N_4 deposition and forming gas anneal. The Si_3N_4 was necessary to protect the surface of the Ge, as GeO_2 formed from the oxidation process is water soluble. Vias were etched in the Si_3N_4 and SiO_2 in the aforementioned n^{++} and p^+ contact regions once again using RIE with CHF_3/Ar chemistry, and metal was deposited on top of the implants. Minimal contact resistivity was ensured via a contact anneal afterwards, and finally bond pads were defined, allowing electrical bias via probes or wire bonding. The completed device is shown in figure 2 with the Ge dimensions being 0.8 μm wide and 5 μm long with a 1.5 μm long Si multiplication region.

3. RESULTS

Dark current-voltage (IV) measurements of the devices were conducted on a Lakeshore Cryotronics cryogenic probe station, using a Keysight B1500a semiconductor parameter analyser. The two passivation techniques were compared in this way, one with thermal oxidation followed by 200 nm PECVD Si_3N_4 deposition and anneal and the other with no thermal oxidation and 200 nm PECVD SiO_2 deposition, shown in figure 3. When thermally oxidised, breakdown in the i-Si multplication region is observed by the sharp increase in current at 45-50 V. Without thermally oxidising the Ge and SiO_2 deposition, a significant rise in current prior to breakdown is noted at 30 V, followed by a shallower avalanche breakdown. The increased density of traps on the Ge surface from

the lack of optimal passivation creates a greater density of surface recombination sites and precipitates the rise in current.

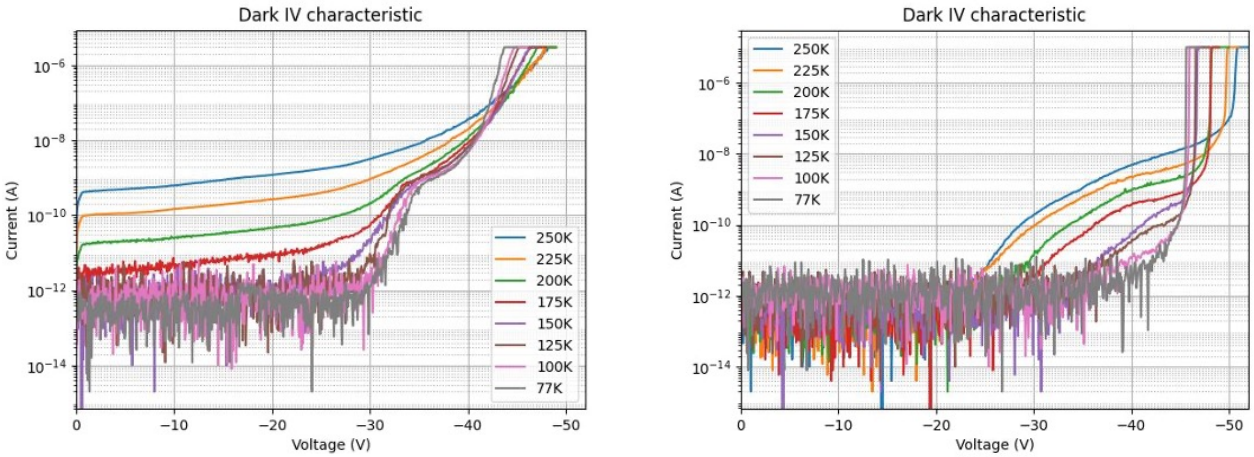

Figure 3. Temperature dependent IV measurements of Ge-on-Si SPADs passivated with PECVD SiO_2 (left) and thermal oxidation and PECVD Si_3N_4 (right)

The device's photoresponse was assessed at 175 K via surface-normal illumination from above, and a clear punch-through is observed at approximately 10 V reverse bias (figure 4) showing the presence of photo-generated carriers from Ge. Due to the small device size, an accurate responsivity could not be determined in this way. The activation energy was also extracted from dark IV measurements of both passivations in accordance with Shockley-Read-Hall recombination. The extracted energy in eV is shown in figure 5 as function of the voltage below V_{bd}, the breakdown voltage of the device. A trap-assisted-tunnelling mechanism is indicated as the activation energy remains below $E_g/2$ of Ge (0.33 eV) consistently before V_{bd}. However, the difference in passivation arises at less than 7.5 V before V_{bd}, where non-thermally passivated SPADs decline in activation energy towards breakdown and thermally passivated SPADs remain at 0.15 eV. The decline reveals an increase in recombination with higher electric field, and underlines further the effect of higher surface trap states on device IV performance.

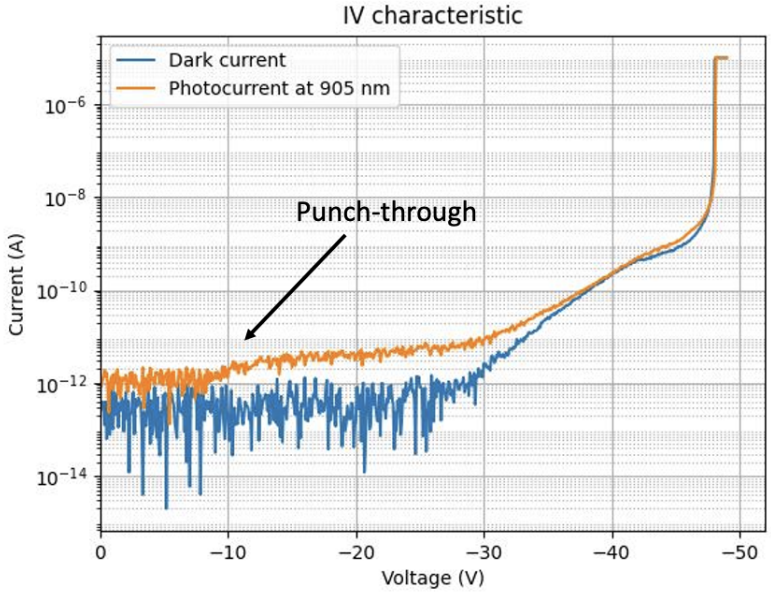

Figure 4. Photocurrent measurement taken at 905 nm and comparison with dark current at 175 K

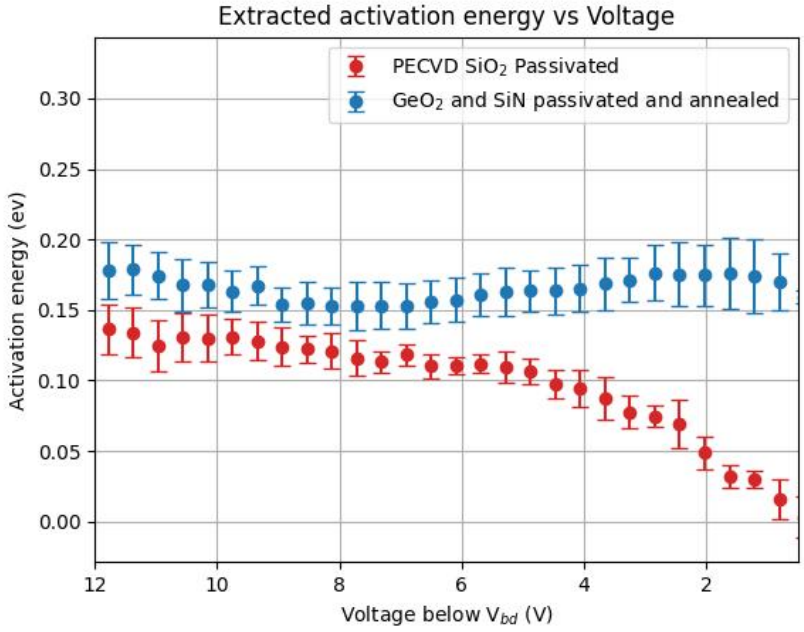

Figure 5. Extracted activation energy from dark current-voltage plots taken between 250 K and 175 K, assuming Shockley-Read-Hall recombination for both passivation techniques

Passivation effects were investigated further by fabricating capacitors on lightly p-doped Ge substrates with the passivation techniques described previously. Through low temperature capacitance-voltage (CV) and conductance-voltage (GV) measurements, the trap density D_{it} of the Ge interface could be extracted via the

conductance method.[15] Reduction in D_{it} is shown in figure 6 when thermal oxidation is performed, and the results are in line with previously reported D_{it} values of Ge oxidation.[16][17]

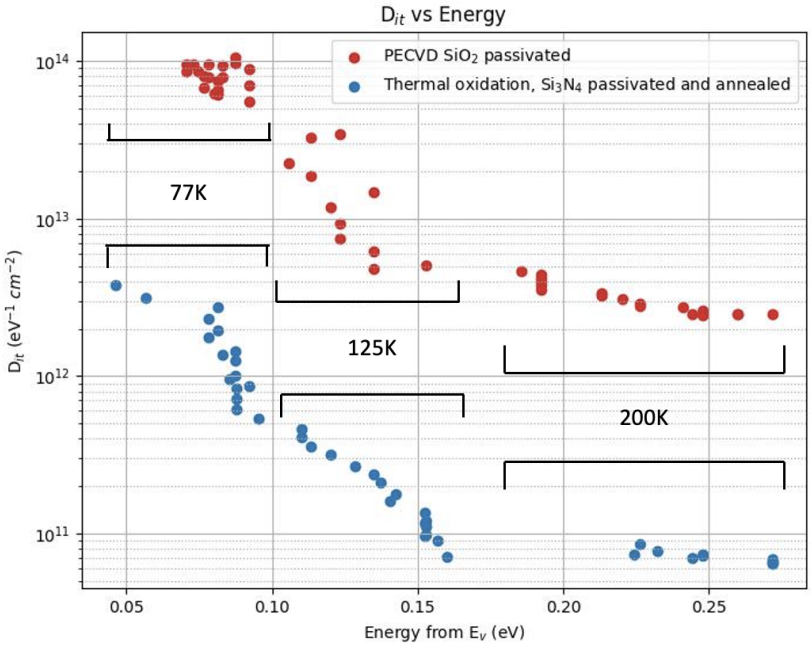

Figure 6. Calculated D_{it} values for both passivation techniques extracted from capacitance-voltage (CV) and conductance-voltage (GV) measurements taken at 77 K, 100 K, and 125 K

4. CONCLUSIONS

Selectively-grown Ge-on-SOI SACM structures were fabricated with exposed Ge sidewalls allowing for passivation variation and characterisation. Subsequent dark IV measurements and extracted activation energies assuming Shockley-Read-Hall recombination were conducted and showed superior device IV performance of thermally oxidised passivated devices relative to PECVD SiO_2, the latter expected to have similar passivation quality to CMP-based devices. Ge capacitors were fabricated and CV and GV measurements of these indicated dramatically lower D_{it} values when thermally oxidised, further supporting the hypothesis that reduced surface traps will lower dark current and improve device performance. Dependency on dark count rate (DCR), single photon detection efficiency (SPDE) and optimisation of charge sheet parameters are some of the possibilities for future work and research.

ACKNOWLEDGMENTS

The author would like to acknowledge the supported of the following grants: UK EPSRC EP/L016753/1, EP/S026428/1, EP/T001011/1, EP/T00097X/1, Innovate UK (44835), Royal Academy of Engineering (RF-201819-18-187, CiET2021_123).

REFERENCES

[1] Hadfield, R. H., "Single-photon detectors for optical quantum information applications," *Nature Photonics* **3**(12), 696–705 (2009).

[2] Tobin, R., Halimi, A., McCarthy, A., Laurenzis, M., Christnacher, F., and Buller, G. S., "Three-dimensional single-photon imaging through obscurants," *Optics Express* **27**(4), 4590 (2019).

[3] Kuzmenko, K., Vines, P., Halimi, A., Collins, R. J., Maccarone, A., McCarthy, A., Greener, Z. M., Kirdoda, J., Dumas, D. C. S., Llin, L. F., Mirza, M. M., Millar, R. W., Paul, D. J., and Buller, G. S., "3D LIDAR imaging using Ge-on-Si single-photon avalanche diode detectors," *Optics Express, Vol. 28, Issue 2, pp. 1330-1344* **28**(2), 1330–1344 (2020).

[4] IEC, "IEC-60825-1," *Tech Report* (2014).

[5] Véret, C., Curé, E., Arnulf, A., and Bricard, J., "Transmission by Haze and Fog in the Spectral Region 0.35 to 10 Microns," *JOSA* **47**(6), 491–498 (1957).

[6] Zhang, J., Itzler, M. A., Zbinden, H., and Pan, J. W., "Advances in InGaAs/InP single-photon detector systems for quantum communication," *Light: Science Applications 2015 4:5* **4**(5), e286–e286 (2015).

[7] Morozov, D. V., Casaburi, A., and Hadfield, R. H., "Superconducting photon detectors," *Contemporary Physics* **62**(2), 69–91 (2022).

[8] Loudon, A. Y., Hiskett, P. A., Buller, G. S., Carline, R. T., Herbert, D. C., Leong, W. Y., and Rarity, J. G., "Enhancement of the infrared detection efficiency of silicon photon-counting avalanche photodiodes by use of silicon germanium absorbing layers," *Optics Letters* **27**(4), 219 (2002).

[9] Dash, W. C. and Newman, R., "Intrinsic Optical Absorption in Single-Crystal Germanium and Silicon at 77°K and 300°K," *Physical Review* **99**(4), 1151 (1955).

[10] Vines, P., Kuzmenko, K., Kirdoda, J., Dumas, D. C. S., Mirza, M. M., Millar, R. W., Paul, D. J., and Buller, G. S., "High performance planar germanium-on-silicon single-photon avalanche diode detectors," *Nature Communications* **10**(1), 1086 (2019).

[11] Lu, Z., Kang, Y., Hu, C., Zhou, Q., Liu, H. D., and Campbel, J. C., "Geiger-mode operation of Ge-on-Si avalanche photodiodes," *IEEE Journal of Quantum Electronics* **47**(5), 731–735 (2011).

[12] Warburton, R. E., Intermite, G., Myronov, M., Allred, P., Leadley, D. R., Gallacher, K., Paul, D. J., Pilgrim, N. J., Lever, L. J., Ikonic, Z., Kelsall, R. W., Huante-Ceron, E., Knights, A. P., and Buller, G. S., "Ge-on-si single-photon avalanche diode detectors: Design, modeling, fabrication, and characterization at wavelengths 1310 and 1550 nm," *IEEE Transactions on Electron Devices* **60**(11), 3807–3813 (2013).

[13] Martinez, N. J. D., Gehl, M., Derose, C. T., Starbuck, A. L., Pomerene, A. T., Lentine, A. L., Trotter, D. C., and Davids, P. S., "Single photon detection in a waveguide-coupled Ge-on-Si lateral avalanche photodiode," *Optics Express* **25**(14), 16130 (2017).

[14] Luan, H. C., Lim, D. R., Lee, K. K., Chen, K. M., Sandland, J. G., Wada, K., and Kimerling, L. C., "High-quality Ge epilayers on Si with low threading-dislocation densities," *Applied Physics Letters* **75**(19), 2909 (1999).

[15] Engel-Herbert, R., Hwang, Y., and Stemmer, S., "Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces," *Journal of Applied Physics* **108**(12) (2010).

[16] Zhang, R., Iwasaki, T., Taoka, N., Takenaka, M., and Takagi, S., "Al2O3/GeOx/Ge gate stacks with low interface trap density fabricated by electron cyclotron resonance plasma postoxidation," *Appl. Phys. Lett* **98**(112902) (2011).

[17] Matsubara, H., Sasada, T., Takenaka, M., and Takagi, S., "Evidence of low interface trap density in GeO2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation," *Appl. Phys. Lett* **93**, 32104 (2008).