Space Shuttle: A Test Vehicle for the Reliability of the SkyWater 130nm PDK using OpenLane and the Google/E-fabless Shuttle Run for Future Space Systems

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I. Extended Abstract

The ASIC industry is experiencing a massive change in the recent years with more and more small and medium business entering the custom ASIC development. This trend is fueled by the recent open hardware movement and relevant government and privately funded initiatives. These new developments can open new opportunities in the space sector, which is traditionally characterised by very low volumes and very high non-recurrent (NRE) costs, if we can show that the produced chips have favourable radiation properties. In this ACM SRC entry, we describe the design and tape-out of Space Shuttle, the first test chip for the evaluation of the suitability of the SkyWater 130nm PDK and the OpenLane EDA toolchain using the Google/E-fabless shuttle run for future space processors.

A. Problem and Motivation

Until very recently, custom ASICs were very rare for small and medium companies due to the overall prohibitive cost of their production, which could only be afforded by few large companies.

This high cost comes mainly from the very expensive commercial EDA tools used for chip designs. However, recently there have been government initiatives such as DARPA's OpenLane/OpenROAD which supported the production of a fully open source EDA toolchain from hardware description languages down to GDSII.

This has been followed by private initiatives such as Google's support for an open source PDK in collaboration with SkyWater for their older 130nm technology, as well as with E-fabless for the sponsored production of multi-project wafers (MPW) of open source designs to test and mature the status of these tools.

The impact of this completely open source option for hardware designs can reduce the hardware production cost many orders of magnitude, lowering the barriers to entry and enabling the production of innovative designs and prototypes, which was not possible before.

One of the sectors that can benefit the most is space due to its different needs than other domains. Space frequently relies on older technology nodes for fabrication of its processors which are normally reused for decades. When the performance of these processors is not sufficient for a mission requirements, the system is normally supplemented with FPGAs. This drives up the cost of missions due to the inability to apply economy of scales in this sector.

However, this low volume production and very specific requirements create a perfect match for new revolution in the space silicon. Therefore, the objective of our project is to validate for the first time this process and tool-chain for space use.

II. Background and Related Work

Space electronics are susceptible to radiation effects such as single event upsets (SEUs) and single event latch-ups (SELs). These radiation effects are well known as well as solutions about how to mitigate them. An example of such mitigation techniques for radiation hardening are for example the ones applied to the widely used in space LEON3 processor[1] over an FPGA. Such mitigations are focused around single error bit flips. Other techniques[2] focus in time delays in redundant structures in order to prevent the same error to impact them in an identical way. Moreover, these methods use checkpoints in order to restore the correct state when these transient errors are detected but not corrected.

III. Approach and Uniqueness

The main goal of our project is to assess the reliability of the SkyWater 130nm manufacturing process and Open Source PDK using the open source OpenROAD EDA toolchain and the Google sponsored shuttle run through e-fabless. Moreover, we aim to evaluate different reliability mitigation techniques.

In order to do so, we have designed a prototype chip called Space Shuttle which has been submitted for tape-out during the second MPW run. In order to assess the reliability of the chip we require methods to be able to observe in a detailed way its internal state, so that not only we can identify whether errors

(e.g. bitflips) have occurred, but also to know which part of the design has been affected. For this reason, the initial reliability assessment has to be performed in a design with relatively low complexity, high level of control and with appropriate facilities to provide the required information.

The most vulnerable parts of a hardware design are its memory structures because they retain their previous values. Therefore, in our chip we have decided to focus on error detection and error correction specifically on flip-flops and registers which are the primary memory storage primitives. Therefore, our design is centered around a register file with 32, 32-bit registers implemented with flip-flops. This is because currently, the OpenRAM compiler is considered experimental and because we want to have more control over the memory structures to implement our detection and correction methods.

We have implemented multiple reliability solutions such as different degrees of replication and ECC around this register file, which can be selectively configured and combined (with some limitations), in order to reliably detect whether errors occur, and in case they do, whether they can be corrected. Moreover, we include a redundant Monitoring Unit consisting of detailed event counters for each of the registers. This way, we can also assess the protection level offered by these different reliability methods and study their trade-offs in order to guide future developments.

In particular, our design has implemented the following characteristics:

- 32, 32-bit register file implemented with flip-flops, organised in 8 banks which can be used in parallel. Each register value can be individually set or inspected. The register file can be either clocked with a user controled signal, offering full control, or with the default chip clock.
- 4 different protection mechanisms, each of which can be enabled selectively and in combination with others:
  - Error Correction Code (ECC): ECC with 1 bit correction and 2 bit correction.
  - Triple Redundancy: The input value is triplicated in the register file.
  - Shadow Register: The input value has a copy in the register file.[3]
  - ECC Shadow Register: The input value has a copy in the register file with ECC protection of 1 bit correction and 2 bit correction.[4]
- Duplicated Monitoring Unit: Individual 32-bit counters per register, reporting the write and read operations performed, as well as the number of detected and corrected errors. Both the monitoring registers and their combinational counter circuit is replicated, ensuring reliable information.

The design has been verified with gate level simulations and it comes with several tests focusing in the verification of different parts of the circuit. A total of 11 tests focus in the verification of the design using the internal I/O pins of the Caravel SoC used for interfacing in all MPW chip designs. 7 additional tests verify the Wishbone interface which allow accessing the performance counters.

IV. Results and Contributions

The Space Shuttle design is fully open-source [5] and can be modified and improved by the community. At the final synthesis the chip uses 2.22 mm^2 with a total of 75841 SkyWater cells targetting a frequency of 100 Mhz.

As a result of this work, we have successfully send the design to production inside the second e-fables Google-sponsored shuttle [6], that will be delivered in December 2021.

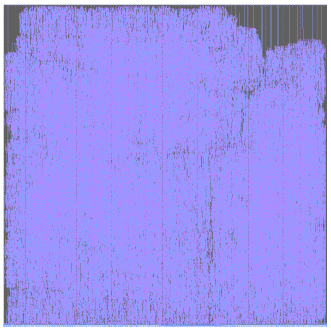

Fig. 1. Floorplan of the resulting chip

When it arrives will be initial tested in normal conditions in order to verify that design behaves and responds to the test that we develop for the simulation. Once it is verified under normal conditions and passes the tests, a set of samples will be send to do a proton base radiation testing in order to characterise its behaviour under radiation.

To our knowledge this is the first attempt to assess the reliability of this new combination of open source technologies, as well as among the first academic tape-outs performed within this program.

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