Optimization-based methodology to design the MMC's sub-module capacitors

Daniel Westerman Spier, *Member, IEEE,* Eduardo Prieto-Araujo, *Senior Member, IEEE,* Huijie Lyu, *Student Member, IEEE,* Jiawei He, Bin Li, *Senior Member, IEEE,* and Oriol Gomis-Bellmunt, *Fellow, IEEE*

Abstract

This paper proposes an optimization-based size reduction methodology for Modular Multilevel Converters (MMC), focusing on minimizing the converter's sub-module capacitor C_{SM}. The analysis is performed considering both the converter's current and voltage limitations and the Transmission System Operator (TSO) Fault Ride Through (FRT) requirements. By means of a steady-state analysis, the time-domain expressions of the converter's arms energies are obtained and their behavior throughout the MMC's operating range is shown. Based on these expressions, the optimization-based problem to reduce the C_{SM} size is developed and its constraints are imposed to ensure that the converter's voltage and current levels are within its design limitations. The suggested method is compared with different approaches for distinct active and reactive power set-points, where it is shown that the SM capacitor size can be reduced up to 24% in comparison with the method with worst performance and up to 7% regarding the best method used for comparison purposes. Furthermore, time-domain simulations of the MMC considering several AC voltage sags are performed in order to demonstrate that the dynamics of the SM capacitor and the arm applied voltages are within acceptable margins during the different operations.

Index Terms

Modular multilevel converter, converter station reduction, SM capacitor, SM capacitor design.

I. Introduction

MODULAR multilevel converters (MMC) have attracted the attention of the industrial community in several areas such as Onshore and Offshore High Voltage Direct Current (HVDC) transmission, variable frequency, reactive power compensation (STATCOM), etc., in the past decades [1]–[3]. In HVDC applications, MMCs have become the preferred choice among the different Voltage Source Converters (VSCs) due to its improved efficiency, reduced AC voltage harmonic content and easier scalability to higher voltage levels [4], [5]. However, the MMC requires a large number of components in comparison to classical two- and three-level VSC (e.g. active switches, arm inductors, sub-module (SM) capacitors, etc.). Such elements must be meticulously designed in order to minimize the installation costs and, along with the controllers, to maintain the converter properly operating under normal or faulted conditions [6], [7].

Among the different parts consisting the converter, the SM capacitors are responsible for more than 50% of its total size and 80% of the conversion station weight [8]. Therefore, reducing its size can have a great impact on the reduction of the installation cost of the converter, especially in offshore applications [9]. Prior research has been developed in the attempt of improving the design method of the SM capacitors. Authors in [10]–[12] mainly focused on the energy effects in their design procedure. In [10], the SM capacitance is minimized based on the maximum and minimum energies in the SMs. The design procedure is improved in [11], where the internal AC voltage of the converter is used to obtain the SM capacitance. Reference [12] analyses the SM capacitors energy considering three distinct operating regions and depending on the region in which the converter will be operated, an energy fluctuation is obtained. Based on this energy variation the equation proposed in [11] is employed to define the SM capacitance.

The previous approaches are further enhanced by the authors in [13], where they also consider the maximum allowed voltage in the SM capacitors defined by either the operating point (OP) or by design constraints. Reference [7] develops analytic optimized equations to calculate the optimal number of SM to be installed and the size of the capacitor to be added to each SM. However, the optimization only considers the maximum SMs capacitor voltage as its main constraint; thus, constraints to avoid overmodulations are ill-defined in the method. Until now, the methods were only focused on the maximum levels of energy, voltage and ripple to ensure that the SM capacitor peak voltage do not exceed its limits. When the C_{SM} minimum voltage levels are considered, thus preventing overmodulations, additional constraints regarding the minimum value of sum of the SM capacitor voltages and the arm inductance effects are included in formulation proposed by [14]. Whereas, [15] expand the effects of the arm inductance by considering them in the arm applied voltages. Furthermore, the paper also includes third harmonic voltage injection in order to reduce the voltage ripple. However, it only considers the DC components of the circulating currents.

Nevertheless, all the previous designing proposals consider that the converter is operated under normal AC and DC network conditions. Under such circumstances, the normal practice is to assume that the control of the MMC is properly designed in order to keep the SM capacitor voltage ripple within its limits. In [16], the voltage ripple is reduced by imposing third order voltages in the arms of the converter. Whereas [17], implemented a machine learning-based method integrated with Circulating Suppressing Current Control (CSCC) to extend the operating region of the converter during faults. However, as these methods

are non-energy-based control approaches, they will lead to undesired AC currents to flow into the DC side of the converter. By assuming energy-based control strategies, the circulating currents of the converter can be enhanced leading to a potential decrease in the SM capacitor voltage fluctuation. In [18], the operating region of the converter is extended by controlling the circulating current to ensure that the peak voltage of the SM are the same as the maximum requested one. [19] controls the circulating current in order to minimize the SM energy ripple. More advanced methods have been proposed in order to improve the usage of these currents as the one proposed in [20], where a comprehensive analysis of the internal currents is carried in the attempt of optimizing their usage by the controllers.

To the best of the authors knowledge, a methodology to optimize the design of the SM capacitance for MMC stations taking into consideration all the internal quantities of the converter, while also considering the Transmission System Operator (TSO) current requirements to support faulted networks and the MMC's limitations has not been proposed yet. In order to address such challenges, this paper proposes the following contributions:

- Derivation of the arm's energy expressions considering the internal voltages and currents of the converter and their limitations.
- Formulation of an optimization-based methodology to minimize the SM capacitance assuming specific or several OPs which can be either in normal or unbalanced AC/DC network voltage conditions.
- The algorithm ensures that the obtained SM capacitance is sufficiently large to maintain the proper power transfer between the AC and DC networks and to keep the internal power balance of the converter and, to be small enough to avoid exceeding the SM capacitor maximum and minimum allowed voltages.

In order to validate that the proposed optimization-based methodology to design the SM capacitor results in the minimum SM capacitor value for a proper operation of the converter, different OPs and network voltage conditions are analyzed analytically and through detailed time-domain simulations, where the converter is regulated assuming an energy-based control. In Section II, the system and the assumptions to model the SM energy are defined. Section III describes the proposed SM capacitor design methodology, while Section IV presents the analytical equations for the SM capacitor voltages. In Section V the suggested method is compared with different approach. In Section VI, the MMC's waveforms profiles are analyzed when the designed SM capacitance is employed assuming distinct AC network voltage scenarios. Finally, the conclusions are given in Section VII.

II. System description and assumptions

A. Converter quantities

Fig. 1 shows the scheme of a three-phase MMC. The converter has two arms per phase-leg k with $k \in (a, b, c)$, whereby each arm has $N^k_{u,l}$ number of sub-modules (SM) connected in series. The SM structure may vary according to the application, but the most used one is the half-bridge.

The DC network quantities are the total current I^{DC}_{tot} and the upper and lower poles DC voltages U^{DC}_u and U^{DC}_l. The MMC quantities are defined as follows; voltages applied to the upper and lower arms of the MMC are given as $u^k_{u,l}$. Similarly, the currents flowing through the converter are represented as $i^k_{u,l}$. The arm impedance and the equivalent impedances of the AC-side transformer are R_a, L_a, R_s and L_s. Finally, the AC grid quantities are the network voltage u^k_g and the AC-side currents i^k_s.

B. Assumptions to model the SM capacitor energy

The mathematical models derived in this paper are based on the following assumptions:

- The SM capacitors are considered to be fully charged.
- The voltages in the SM capacitors within the same arm are balanced and under steady-state conditions. This can be achieved by different control methods (e.g. Nearest Level Control [21]).
- The applied voltages and currents flowing through the converter have zero and first-order frequency terms. The injection of third-order frequency components is disregarded as it might cause the circulation of AC currents in the DC-side of the converter.
- The effects of the modulation index are not considered.
- The topology, voltage and current ratings for each individual SM are the same in all SMs used in the converter.

III. Description of the methodology

This section describes the optimization-based methodology to minimize the SM capacitance value. The suggested tool considers the optimal values for the DC and AC quantities of the MMC in order to comply with the TSO requirements in the form of injection/absorption of positive- and negative-sequence current components and the converter design limits during balanced and unbalanced AC/DC network voltage conditions. The proposed method, its flowchart is displayed in Fig. 2, can be used in two manners. Either by assuming an specific OP ($ii_{max} = 1$), or by assuming different OPs ($ii_{max} > 1$). In which the user can input different AC/DC network voltages and/or different active and reactive power set-points and analyze

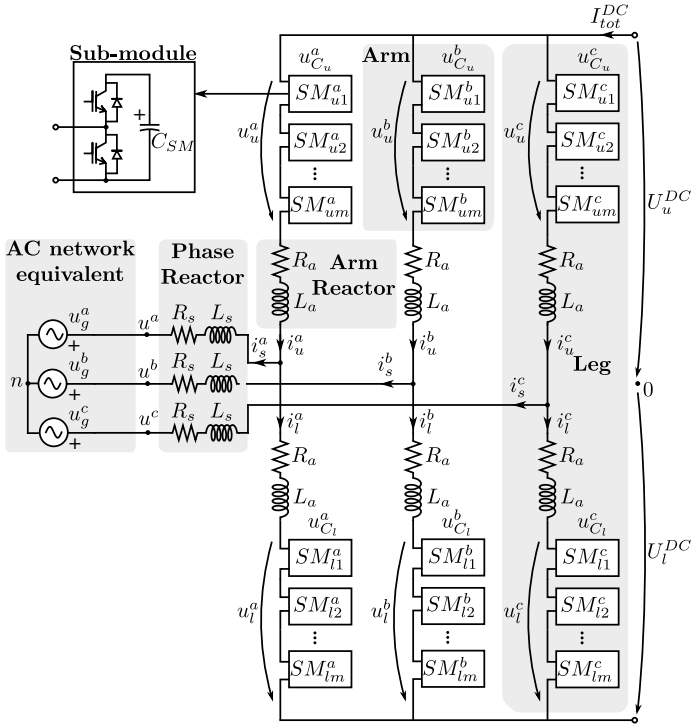


Fig. 1. Model of the MMC converter.

the effect of such changes in the sizing of the C_{SM}. In order to ensure that the resultant SM capacitance comply with all the TSO's and MMC's requirements, the second option is recommended. Thus, the algorithm will run consecutive times considering the user's voltages and power settings inputs, resulting in several of minimal $C_{SM}(ii)$ capacitance values (one for each specific OP). Finally, these values are stored in the vector $\mathbf{C}_{SM}$, whereby the capacitance size C_{SM} to be selected should be $C_{SM} = \max(\mathbf{C}_{SM})$.

As it can be noted in Fig. 2, the suggested SM capacitance designing tool requires different inputs that can be imposed by the user (e.g. voltage and power set-points), obtained by design (e.g. number of SM in each arm $N^k_{u,l}$, U_{SM}, $I^k_{u,l_{max}}$, etc.), or by the grid code requirements (as ΔI_r, $\Delta U_{max_{1,2}}$, etc.). Next, each one of the three steps required to run the methodology are defined.

- Step 1 - Calculate the initial equilibrium points of the converter. In this step, no optimization algorithm is required. The equilibrium quantities are obtained based on a system of equations describing the MMC's steady-state profile, as the one presented in [22]. The voltages and currents resultant from this equation system are required as the initial conditions of the next step in order to speed up the convergence time and improve its accuracy.
- Step 2 - In this step, the optimal MMC steady-state values are obtained through an optimization method which is formulated to maximize either the voltage or frequency support that the converter must provide during AC network voltage sags. The prioritization between the two types of support is defined in the objective function (OF) of this optimization problem according to the value of the weights $\lambda^{+-}_{I_{p,q}}$ given by the user, as shown in (1) and further explained presented in [23].

$$\max_{\substack{\underline{I}^k_{u,l}, I^{kDC}_{u,l}, \underline{U}^k_{u,l}, U^{kDC}_{u,l}, \\ \underline{U}_{n0}, \alpha^{+,-}, \beta^{+,-}}} \quad \lambda_{I_p^+}\alpha^+ + \lambda_{I_q^+}\beta^+ + \lambda_{I_p^-}\alpha^- + \lambda_{I_q^-}\beta^- \tag{1}$$

where the coefficients $\alpha^{+,-}$ and $\beta^{+,-}$ are used to regulate the active and reactive currents levels to be injected/absorbed by the AC network. In order to meet the TSO's Fault Ride-Through (FRT) requirements, the algorithm requires as inputs the TSO's current and voltage levels during the fault (ΔI_r, $\Delta U_{max_{1,2}}$, $\Delta U_{min_{1,2}}$). Finally, to ensure that the MMC's currents are within design limitations, their maximum values ($I^k_{u,l_{max}}$, $I^k_{s_{max}}$) are also necessary inputs for this algorithm. Although the optimization method used in this step acknowledge potential power transferred among the phase-legs and upper and lower arms, it disregards the SM capacitance in the converter. The effect of such element in the MMC's operation will be included in the next step.
- Step 3 - This step employs the proposed optimization to design C_{SM} (see Section III-A). Firstly, the algorithm requires as inputs, the internal and external voltages and currents of the converter, which are calculated in the previous two steps. Based on these values and the SM characteristics defined by design (e.g. $N, U_{C_{max}}, U_{SM}$), the suggested method attempts to minimize the value of C_{SM}. The algorithm is solved using the function *fmincon* from Matlab®, assuming a full cycle of

the AC grid (e.g. $T_s = 20$ ms for a 50 Hz grid)[1]; thus, the potential asymmetries in the SM capacitor voltages, which are related to the different OPs (see Section IV-B), can be fully considered in the formulation of optimization problem. This is necessary to ensure that throughout one operating cycle, the instantaneous arm applied voltages are smaller than the sum of the instantaneous SM capacitor voltages (overmodulation). This optimization method also considers the internal current limitations (defined by design), the maximum allowed voltage in the SM capacitor (defined by design), the minimum allowed voltage to be applied in each arm of the converter (defined according to the SM structure; 0 for half-bridge and $-u_C^k(t)$ for full-bridge) and the maximum and minimum allowed SM capacitance values (defined by design).

Although combining both optimizations from Step 2 and 3 is possible, the resultant algorithm problem would not ensure optimal values for the AC network currents or for C_{SM}. This is explained as different weights would be required in the OF for each specific component, leading to either a higher prioritization of the active and reactive currents injected or a higher prioritization to minimize the SM capacitance. By using two different optimization problems the prioritizations can be performed individually: TSO and converter current requirements (Step 2); minimum value of the SM capacitance C_{SM} respecting the MMC internal current and voltages limitations (Step 3). Therefore, the smallest value of C_{SM} can be guaranteed.

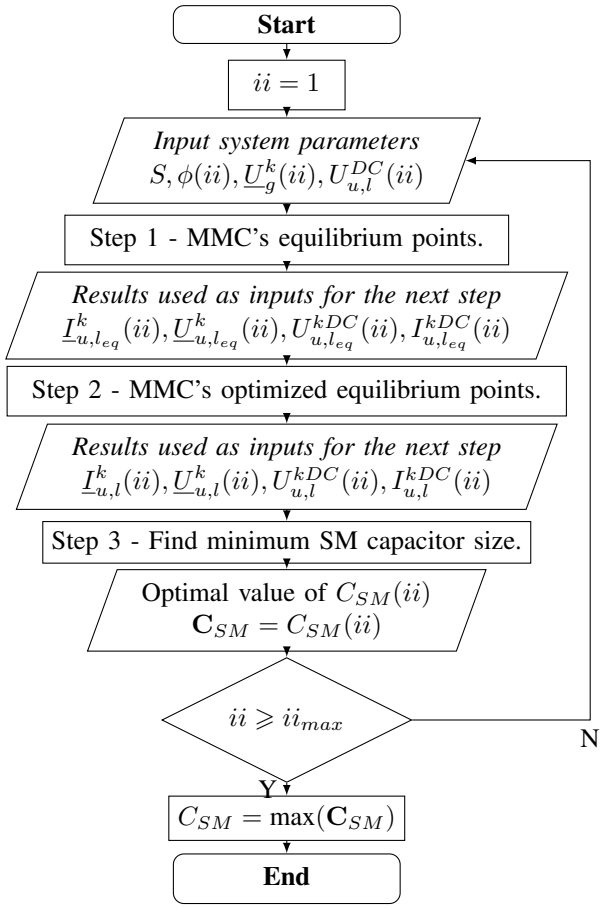


Fig. 2. Flowchart of the proposed methodology to optimize the SM capacitors considering different operating points, AC network voltages, TSO requirements and converter current limitations.

A. Proposed optimization algorithm to minimize the SM capacitances

Firstly, let us clarify that for problem formulation purposes, the phasor notation $\underline{X}^k = X_r^k + jX_i^k = X^k \angle \underline{\theta^k}$ will be adopted, with $x(t) = X^k \text{Re}\{e^{j(\omega t + \theta^k)}\}$ $\forall k \in (a, b, c)$. The optimization problem that enables to minimize the size of the SM capacitors while ensuring that the MMC's currents and voltages are kept within their design limits is shown next

$$\underset{\substack{\underline{I}_{u,l}^k, I_{u,l}^{kDC}, \underline{U}_{u,l}^k, \\ U_{u,l}^{kDC}, \underline{U}_{n0}, C_{SM}}}{\text{minimize}} \quad C_{SM} \tag{2a}$$

[1]Note that the inequality constraints (1o) to (1r) instead of being assumed as absolute values are mathematically model as time-domain sinusoidal trajectories that must be within the maximum and minimum values imposed by the converter limitations.

subject to

$$\underline{U}_{0n} = \underline{U}_g^k + \underline{Z}_s(\underline{I}_u^k - \underline{I}_l^k) + \underline{Z}_a\underline{I}_u^k + \underline{U}_u^k \tag{2b}$$

$$\underline{U}_{0n} = \underline{U}_g^k + \underline{Z}_s(\underline{I}_u^k - \underline{I}_l^k) - \underline{Z}_a\underline{I}_l^k - \underline{U}_l^k \tag{2c}$$

$$0 = \underline{I}_u^a + \underline{I}_u^b + \underline{I}_u^c \tag{2d}$$

$$\underline{I}_s^k = \underline{I}_u^k - \underline{I}_l^k \tag{2e}$$

$$0 = \sum_{k=a}^{c}\left[\text{Re}\left\{\underline{U}_u^k\underline{I}_u^k + \underline{U}_l^k\underline{I}_l^k\right\} + U_u^{kDC}I_u^{kDC} + U_l^{kDC}I_l^{kDC}\right] \tag{2f}$$

$$P_{u\to l}^k = \text{Re}\left\{\underline{U}_u^k\underline{I}_u^k - \underline{U}_l^k\underline{I}_l^k\right\} + \left(U_u^{kDC}I_u^{kDC} - U_l^{kDC}I_l^{kDC}\right) \tag{2g}$$

$$\begin{aligned} P_{a\to b} =& \text{Re}\left\{\ (\underline{U}_u^a\underline{I}_u^a + \underline{U}_l^a\underline{I}_l^a)\ \right\} + \left(U_u^{aDC}I_u^{aDC} + U_l^{aDC}I_l^{aDC}\right) \\ &- \left[\text{Re}\left\{\ \left(\underline{U}_u^b\underline{I}_u^b + \underline{U}_l^b\underline{I}_l^b\right)\ \right\} + U_u^{bDC}I_u^{bDC} + U_l^{bDC}I_l^{bDC}\right] \end{aligned} \tag{2h}$$

$$\begin{aligned} P_{a\to c} =& \text{Re}\left\{\ (\underline{U}_u^a\underline{I}_u^a + \underline{U}_l^a\underline{I}_l^a)\ \right\} + \left(U_u^{aDC}I_u^{aDC} + U_l^{aDC}I_l^{aDC}\right) \\ &- \left[\text{Re}\left\{\ (\underline{U}_u^c\underline{I}_u^c + \underline{U}_l^c\underline{I}_l^c)\ \right\} + U_u^{cDC}I_u^{cDC} + U_l^{cDC}I_l^{cDC}\right] \end{aligned} \tag{2i}$$

$$I_s^{kDC} = I_u^{kDC} - I_l^{kDC} \tag{2j}$$

$$I_{tot}^{DC} = I_u^{aDC} + I_u^{bDC} + I_u^{cDC} \tag{2k}$$

$$U_{tot}^{DC} = U_u^{kDC} + U_l^{kDC} + 2R_a\left(I_u^{kDC} + I_l^{kDC}\right) \tag{2l}$$

$$0 = 2\left(U_l^{aDC} - U_u^{aDC}\right) + \sum_{k=b}^{c}\left[U_u^{kDC} - U_l^{kDC}\right] \tag{2m}$$

$$0 = \left(U_u^{bDC} - U_l^{bDC} - U_u^{cDC} + U_l^{cDC}\right) \tag{2n}$$

$$I_{u,l}^k + I_{u,l}^{kDC} \leqslant I_{max}^{arm} \tag{2o}$$

$$u_{u,l_C}(t) \leqslant U_{C_{max}} \tag{2p}$$

$$0 \leqslant u_{u,l}^k(t) + U_{u,l}^{kDC}(t) \leqslant u_{u,l_C}^k(t) \tag{2q}$$

$$0 \leqslant C_{SM} \leqslant C_{SM_{max}} \tag{2r}$$

where U_{tot}^{DC} is the sum of the upper and lower DC poles' voltage. $\underline{U}_{n0}$ is the voltage between the AC grid neutral point n and the DC-poles common point 0. The active power transferred from the upper to the lower arms of the converter is set by $P_{u\to l}^k$, similarly $P_{a\to b}$ and $P_{a\to c}$ are the power transferred among the phase-legs of the converter. For the case studies presented in this paper, it is assumed that there is no power difference between the halves and phase-legs of the converter ($P_{u\to l}^k = P_{a\to b} = P_{a\to c} = 0$). The inequality (1p) set the maximum allowed voltage of the SM capacitor's sum, while inequality (1q) set the maximum and minimum allowed voltage to be applied into the upper and lower arms of the converter (the derivation of the time-domain expressions $u_{u,l_C}(t)^k$ is given in details in Section IV). Inequality (1r) limits the maximum SM capacitor $C_{SM_{max}}$. Note that the maximum voltage must be equal or smaller than the minimum value of the sum of the SM capacitor voltage in order to avoid overmodulation. The minimum allowed voltage to be applied into the SM is equal to zero, as the SM is assumed to be half-bridge (HB) topology. For full-bridge (FB) SMs, the minimum allowed voltage is set to $-u_C^k(t)$. If a hybrid MMC is assumed, where the arms contain both HB and FB SMs, the optimization still can be used. However, slight modifications are needed in order to adapt the time-domain voltage expression to consider the number of SMs that are HB and FB employed in (2p). Based on that, the inequality (2q) can be replaced by two other inequalities, one for the HB SMs and another for FB SMs. Finally, the inequality constrains are imposed as time-domain equations in the optimization algorithm as done in [23].

IV. Analytic model of the SM capacitor voltages

This section focuses on describing the SM capacitors' energy and voltage analytical expressions that are required in the formulation of the optimization problem presented in Section III. These terms are used in order to ensure that methodology keeps the SMs voltages within their respective maximum (set by the maximum allowed voltage of the component) and minimum (defined by the maximum applied voltages in the MMC's arms) levels. This is done by obtaining the oscillating instantaneous power and the AC and DC energy equations for each one of the six MMC's arms, which are later used to derive the instantaneous SM capacitor voltage model.

A. Instantaneous arm power and energy derivation

The instantaneous power for the upper and lower arms of the converter can be obtained by the product between its currents and voltages. Such quantities generally have DC and AC components which might be balanced or unbalanced, depending on the operating condition of the converter. Therefore, the generic expression describing the oscillating power for each individual arm unit can be described as

$$p^k_{u,l_{osc}}(t) = u^k_{u,l}(t) i^k_{u,l}(t) = \left(U^{kDC}_{u,l} + \hat{U}^k_{u,l}\cos(\omega t + \theta^k_{u,l})\right) \left(I^{kDC}_{u,l} + \hat{I}^k_{u,l}\cos(\omega t + \phi^k_{u,l})\right) \tag{3}$$

where $\theta^k_{u,l}$ and $\psi^k_{u,l}$ are the upper and lower arms' currents and voltages phase-angles, $U^{kDC}_{u,l}$ and $I^{kDC}_{u,l}$ are the upper and lower arms' DC voltages and currents, respectively and $\hat{U}^k_{u,l}$ and $\hat{I}^k_{u,l}$ are the halves peak AC voltage and currents magnitudes. Expanding the previous equation results in

$$\begin{aligned} p^k_{u,l_{osc}}(t) = {} & I^{kDC}_{u,l}U^{kDC}_{u,l} + U^k_{u,l}I^k_{u,l}\cos(\phi^k_{u,l} - \theta^k_{u,l}) + \\ & U^{kDC}_{u,l}\hat{I}^k_{u,l}\cos(\omega t + \phi^k_{u,l}) + I^{kDC}_{u,l}\hat{U}^k_{u,l}\cos(\omega t + \theta^k_{u,l}) + \\ & U^k_{u,l}I^k_{u,l}\cos(2\omega t + \theta^k_{u,l} + \phi^k_{u,l}) \end{aligned} \tag{4}$$

Once the MMC has reached steady-state, it can be assumed that the sum of the non-oscillating AC and the DC active powers is equal to zero, considering that the internal losses of the converter are negligible. If such condition is not met, the SM capacitors' would be either in charge or discharge mode; thus, steady-state conditions are not held. Therefore, the instantaneous oscillating arms' power can be reduced to

$$\begin{aligned} p^k_{u,l_{osc}}(t) = {} & U^{kDC}_{u,l}\hat{I}^k_{u,l}\cos(\omega t + \phi^k_{u,l}) + \\ & I^{kDC}_{u,l}\hat{U}^k_{u,l}\cos(\omega t + \theta^k_{u,l}) + U^k_{u,l}I^k_{u,l}\cos(2\omega t + \theta^k_{u,l} + \phi^k_{u,l}) \end{aligned} \tag{5}$$

Finally, the upper and lower arms' instantaneous steady-state oscillating energy is derived by integrating (5) over time; thus, resulting in

$$\begin{aligned} e^k_{u,l_{osc}}(t) = {} & \frac{U^{kDC}_{u,l}\hat{I}^k_{u,l}}{\omega}\sin(\omega t + \phi^k_{u,l}) + \\ & + \frac{I^{kDC}_{u,l}\hat{U}^k_{u,l}}{\omega}\sin(\omega t + \theta^k_{u,l}) + \frac{U^k_{u,l}I^k_{u,l}}{2\omega}\sin(2\omega t + \theta^k_{u,l} + \phi^k_{u,l}) \end{aligned} \tag{6}$$

As it can be observed from (6), the oscillating energy expression has in total three terms, in which two are related to the first-order frequency and the other one is a second-order frequency term. In order to reduce such equation and ease the derivation of the expression describing the equivalent arm capacitor voltage, the principles presented in [24] are employed. By doing so, the first-order terms can be combined into a single one, consequently, the instantaneous energy expressions can be reduced to

$$e^k_{u,l_{osc}}(t) = \mathbf{E^k_{u,lmax_\omega}}\sin(\omega t + \psi^{\mathbf{k}}_{\mathbf{u,l}}) + \mathbf{E^k_{u,lmax_{2\omega}}}\sin(2\omega t + \gamma^{\mathbf{k}}_{\mathbf{u,l}}) \tag{7}$$

where $\mathbf{E^k_{u,lmax_\omega}}$ and $\psi^{\mathbf{k}}_{\mathbf{u,l}}$ are the magnitude and phase-angle resultant from the combination of the two first-order frequency terms, respectively. Similarly, $\mathbf{E^k_{u,lmax_{2\omega}}}$ and $\gamma^{\mathbf{k}}_{\mathbf{u,l}}$ are the magnitude and phase-angle for the second-order term. These terms are described in details in the Appendix A.

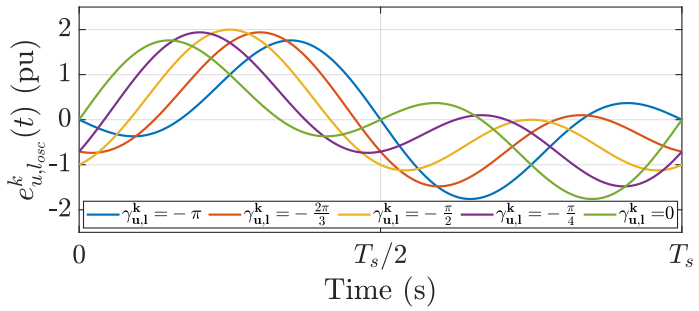
B. Analysis of energy ripple for the upper and lower arms'

Based on the energy expression derived in Section IV-A, the SM capacitor voltage equations can be obtained. However, it is important to notice that under distinct OPs, such energy expressions may present asymmetric behavior. This directly affects the maximum and minimum energy magnitudes, which must be considered while deriving the SM capacitance value. In order to provide further insights regarding these asymmetries, Fig. 3 depicts the waveforms of (7) during a full cycle of the grid ($T_s = 20$ ms), assuming that the sum of the first oscillating energies magnitudes and the first-order frequency phase-angle term are constant and equal to $\mathbf{E^k_{u,lmax_\omega}} = \mathbf{E^k_{u,lmax_{2\omega}}} = 1$ with $\psi^{\mathbf{k}}_{\mathbf{u,l}} = 0$, and that the phase-angle for the second-order frequency term $\gamma^{\mathbf{k}}_{\mathbf{u,l}}$ is variable.

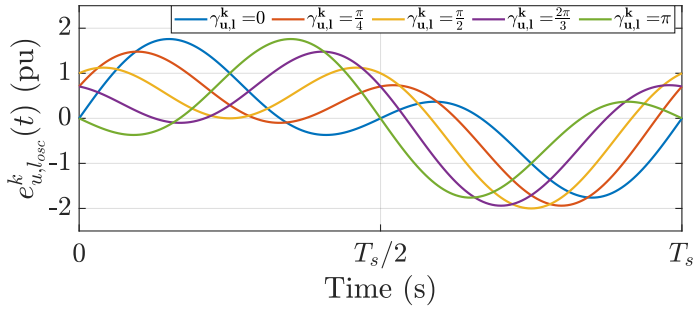
As shown in Fig. 3, the amplitude of the maximum and minimum oscillating energies can present asymmetrical behavior depending on the operating point. However, the peak energy levels is only one of the requirements when designing the SM capacitor. The maximum and minimum energy magnitudes can be derived when $\sin(\omega t + \psi^{\mathbf{k}}_{\mathbf{u,l}}) = \sin(2\omega t + \gamma^{\mathbf{k}}_{\mathbf{u,l}}) = 1$, thus,

$$E^k_{u,l_{oscmax}} = \mathbf{E^k_{u,lmax_\omega}} + \mathbf{E^k_{u,lmax_{2\omega}}} \leftrightarrow \tag{8a}$$

$$\leftrightarrow \omega t + \psi^{\mathbf{k}}_{\mathbf{u,l}} = \pm\pi/2 + n_1\pi, \text{for } n_1 \in \mathbb{Z} \tag{8b}$$



(a) $-\pi \leqslant \gamma^{\mathbf{k}}_{\mathbf{u,l}} \leqslant 0$.



(b) $0 \leqslant \gamma^{\mathbf{k}}_{\mathbf{u,l}} \leqslant \pi$.

Fig. 3. Time-domain waveforms of $E^k_{u,l}(t)$ (7) under different operating points.

$$\leftrightarrow 2\omega t + \gamma^{\mathbf{k}}_{\mathbf{u,l}} = \pm\pi/2 + n_2\pi, \text{for } n_2 \in \mathbb{Z} \tag{8c}$$

$$\leftrightarrow \pm\pi/2 + n_1\pi - \psi^{\mathbf{k}}_{\mathbf{u,l}} = \left(\pm\pi/2 + n_2\pi - \gamma^{\mathbf{k}}_{\mathbf{u,l}}\right)/2 \tag{8d}$$

$$\leftrightarrow \pi + 2n_1\pi - 2\psi^{\mathbf{k}}_{\mathbf{u,l}} = \pm\pi/2 + n_2\pi - \gamma^{\mathbf{k}}_{\mathbf{u,l}} \tag{8e}$$

$$\leftrightarrow \pm\pi/2 + (2n_1 - n_2)\pi = 2\psi^{\mathbf{k}}_{\mathbf{u,l}} - \gamma^{\mathbf{k}}_{\mathbf{u,l}} \tag{8f}$$

$$\leftrightarrow 2\psi^{\mathbf{k}}_{\mathbf{u,l}} - \gamma^{\mathbf{k}}_{\mathbf{u,l}} = \pm\pi/2 + n\pi \quad \forall k \in k = \{a, b, c\} \tag{8g}$$

C. Final expression of the instantaneous arm energy and derivation of the SM capacitor voltage

Until now, the analysis focused on deriving a mathematical expression to describe the MMC's arms energy oscillation for any OP. However, such term alone cannot calculate the actual levels of SM capacitor voltages. Such fact arises as the analysis assumes that the converter already reached the steady-state, thus the SM capacitors, in addition to the oscillating energy term, will also have an average energy level. Such energy term can be calculated as

$$E^k_{u,l_{AVG}} = \frac{1}{2} C_{SM} U^2_{SM} N^k_{u,l} \tag{9}$$

where C_{SM} is the SM capacitance value, $N^k_{u,l}$ is the number of available SM in each arm of the converter and U_{SM} is the SM rated voltage. Therefore, by adding the previous equation with the SM capacitors oscillating energy terms (6), the complete energy expression can be obtained and it is expressed as follows

$$e^k_{u,l}(t) = E^k_{u,l_{AVG}} + e^k_{u,l_{osc}}(t) = \frac{1}{2} C_{SM} U^2_{SM} N^k_{u,l} + \tag{10}$$
$$\mathbf{E^k_{u,lmax_\omega}} \sin(\omega t + \psi^{\mathbf{k}}_{\mathbf{u,l}}) + \mathbf{E^k_{u,lmax_{2\omega}}} \sin(2\omega t + \gamma^{\mathbf{k}}_{\mathbf{u,l}})$$

Finally, based on the energy expression (10), the sum of the instantaneous SM capacitor voltage used in the formulation of the optimization problem (see equations (1r) and (1q) in Section III-A), can be expressed by employing

$$E = \frac{1}{2} C U^2 \tag{11a}$$

$$u^k_{u,l_C}(t) = \sqrt{\frac{2e^k_{u,l}(t)}{C_{SM}}} \tag{11b}$$

$$u^k_{u,l_C}(t) = \left(\frac{2}{C_{SM}}\right)^{\frac{1}{2}} \left[\frac{1}{2} C_{SM} U^2_{SM} N^k_{u,l} + \right. \tag{11c}$$

$$\left. \mathbf{E^k_{u,lmax_\omega}} \sin(\omega t + \psi^{\mathbf{k}}_{\mathbf{u,l}}) + \mathbf{E^k_{u,lmax_{2\omega}}} \sin(2\omega t + \gamma^{\mathbf{k}}_{\mathbf{u,l}}) \right]^{\frac{1}{2}}$$

V. Performance and comparison with other methods

In this section, the proposed optimization-based SM capacitance design is compared with distinct design methods assuming balanced AC and DC network voltage conditions and the worst SM capacitor ripple scenario. Which, for the optimization algorithm such scenario arises when $\gamma^{\mathbf{k}}_{\mathbf{u,l}} = \pi/2$ (see Section IV-B), whereas for the other methods the worst condition happens when the power factor angle is equal to $\phi = \pi/2$. All the different methods consider the same MMC parameters, similar to the ones used in the HVDC link between Spain and France (INELFE), as shown in Table I.

TABLE I
System parameters

Parameter	Symbol	Value	Units
Rated power	S	1000	MVA
Rated power factor	$\cos\phi$	0.95 (c)	-
AC-side rated voltage	$\underline{U}_g$	320	kV
HVDC link voltage	U^{DC}	$\pm$320	kV
Phase reactor impedance	$\underline{Z}_s$	0.004+j 0.15	pu
Arm reactor impedance	$\underline{Z}_a$	0.01+j 0.14	pu
Converter modules per arm	$N^k_{u,l}$	400	-
C_{SM} voltage	U_{SM}	1.6	kV
Optimal weighting factor 1	$\lambda_{I_p^+}$	10^{-6}	-
Optimal weighting factor 2	$\lambda_{I_q^+}$	1	-
Optimal weighting factor 3	$\lambda_{I_p^-}$	10^{-9}	-
Optimal weighting factor 4	$\lambda_{I_q^-}$	10^{-3}	-
Maximum MMC arm current	I^{arm}_{max}	1.0795	pu
Maximum AC grid current	I^{AC}_{max}	1.1	pu
Maximum C_{SM} voltage	$U_{C_{max}}$	1.15	pu

A. Case study A - Full active/reactive power injection/absorption $\gamma^{\mathbf{k}}_{\mathbf{u,l}} = \phi = [-\frac{\pi}{2}, 0, \frac{\pi}{2}]$

In this case study, the SM capacitance values obtained from the optimization-based algorithm are compared with three other methods [11], [14] and [15] by assuming that the converter is either fully injecting/absorbing reactive power or fully injecting active power with balanced AC and DC network voltage conditions. As discussed in the Section IV-B, during reactive power injection/absorption, the SM capacitors are expected to experience maximum voltage ripple. For comparison purposes, the simulations are evaluated considering the same maximum allowed voltage ripple, time-step and in the same software (Matlab/Simulink®). In Table II, the capacitance values with each method are shown considering the three different OPs.

In Method I [11], the authors analyzed the average and maximum energies expressions of the MMC arms. Based on that, it derives two expressions for the minimum and maximum allowed energy levels that must be complied in the SM capacitor selection. Method II [14] proposes a method to select the SM capacitor which has to comply with three voltage requirements while considering the effects arm inductors will have in the arm currents. The SM capacitor is only selected if it meets the voltage ripple constraints (the value of the peak to peak ripple used was equal to 0.3 pu), the voltage capability constraint which is related to the value of SM capacitor voltage that is enough to synthesize the required arm voltage and the maximum voltage constraint. Method III [15] proposes an iterative methodology in which employs more degrees of freedom of the converter than Methods I and II in order to find the maximum, minimum and the SM capacitor voltage ripples. Firstly, the method calculates the operating region where the SM capacitor voltage reaches its maximum peak and ripple values. Then, based on these calculated values and their maximum allowed levels (inputs provided by the user which is similar for all methods 1.15 pu and 0.3 pu, respectively), the methodology finds to capacitor values one regarding the peak voltage level and another one for to comply with the ripple requirements. Finally, if the highest value SM capacitor calculated is selected. However, there are still degrees of freedom that none of the previous methods have not taken into consideration and none of them have been validated during AC voltage sags. During AC voltage sags, the voltage waveforms of the SM capacitors can be highly asymmetrical. And, if the SM capacitors design does not take such asymmetries into consideration, the value selected might not be sufficiently high in order to avoid the converter to exceed its limitations (see Section VI.

As it can be observed from Table II, all methods indicate similar results when the converter is injecting fully active power ($\phi = 0$). However, during the scenarios where it is either fully absorbing (e.g. STATCOM operation) or providing full reactive power (e.g. voltage support during AC network voltage sags), the methods presented contrasting SM capacitance values. In

TABLE II
CAPACITANCE DESIGN COMPARISON

ϕ	**Method**	**Capacitance** [mF]
$-\frac{\pi}{2}$	Proposed	9.8364
	Method I	7.7443
	Method II	12.7336
	Method III (with 3^{rd} harmonics)	9.7821
	Method III (without 3^{rd} harmonics)	9.6838
0	Proposed	6.3691
	Method I	5.5581
	Method II	9.0178
	Method III (with 3^{rd} harmonics)	6.4531
	Method III (without 3^{rd} harmonics)	6.5472
$\frac{\pi}{2}$	Proposed	9.0393
	Method I	3.8389
	Method II	11.9492
	Method III (with 3^{rd} harmonics)	9.7821
	Method III (without 3^{rd} harmonics)	9.6838

order to ensure that the values obtained with the different methods can be employed in the converter without leading to overmodulations, time-domain simulations are carried out. In Figs. 4 to 6, the waveforms of the applied voltages for the upper arms of the converter and the sum of the SM capacitor voltages are depicted assuming that the converter has achieved the steady-state. The simulations are performed employing an accelerated model of the MMC [25] using the Nearest Level Control (NLC) technique to calculate the number of active sub-modules in each arm [26] of the MMC. In addition, the converter is regulated by the energy based control proposed in [21].

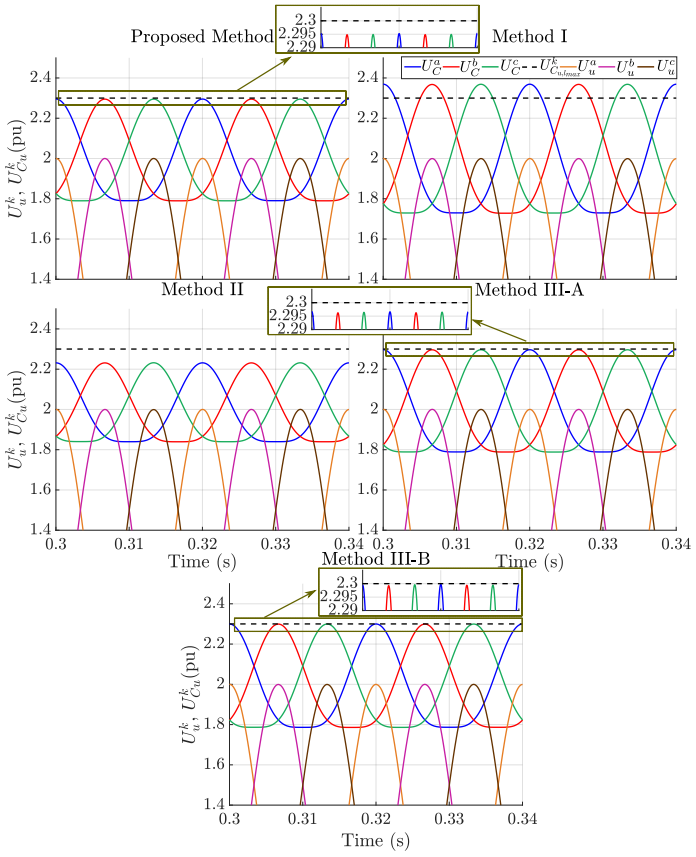


Fig. 4. Time-domain waveforms for the proposed method and Methods I to III-B of the upper arms applied voltages and the equivalent arm capacitor voltage $\phi = -\frac{\pi}{2}$.

Observing Fig. 4, it can be noted that the C_{SM} designed with Methods II, III-A, III-B and the proposed one is high enough to maintain the SM capacitor voltage level within the desired range. However, Method II leads to the oversizing such component, as the maximum SM capacitor voltage is far below its limit. On the other hand, Method I undersized the C_{SM}, resulting in high voltage ripples which are exceeding the design limitations of the component. Still, either Methods III-A, III-B or the

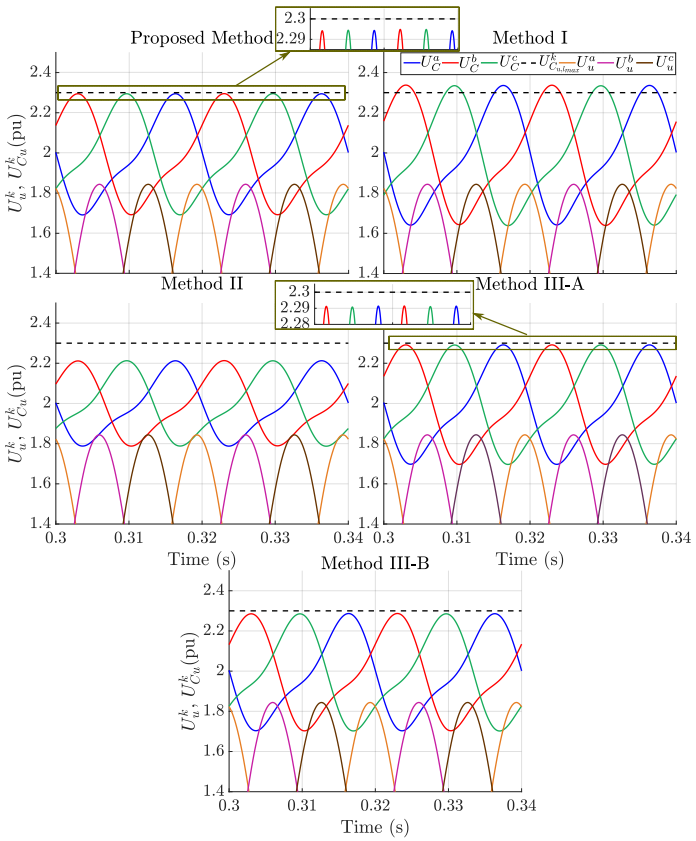


Fig. 5. Time-domain waveforms for the proposed method and Methods I to III-B of the upper arms applied voltages and the equivalent arm capacitor voltage for $\phi = 0$.

proposed one can be used to design C_{SM}, as their voltage differences between the maximum allowed capacitor voltage and the capacitor voltage peak values are small, whereby Method-III-B is the smallest.

During the scenario where the converter is fully injecting active power ($\phi = 0$), as displayed in Fig. 5, similar conclusions as the previous case can be drawn. The main difference is that for this condition, the C_{SM} calculated with proposed method is the most suitable option as the peak magnitude for the sum of the SM capacitor voltages is the closest one to its maximum allowed value (without exceeding it).

The last scenario analyzed in this case study assumes that the converter is fully absorbing reactive current($\phi = \frac{\pi}{2}$), as depicted in Fig. 6. It can be noted that the C_{SM} resultant from Method I is too small, consequently, the converter is under overmodulation. In comparison to the remaining designing methods, the proposed approach can reduce the magnitude of C_{SM} up to 24% in comparison to Method II and up to 7.6% in relation to Method III without reaching overmodulation or exceeding the maximum SM capacitor voltage level.

B. Case study B: Effects of the variation in the number of SM

In this case study, the effects caused by the variation in the number of available sub-modules $N_{u,l}^k$ over the SM capacitance C_{SM} is analyzed. The analysis is conducted for different OPs and it compares the proposed optimization-based design tool with the methods presented in the previous case study. The study considers that the average voltage in each SM capacitor U_{SM} varies based on $N_{u,l}^k$ in order to respect the relation ($U_u^{DC} + U_l^{DC} = U_{SM} N_{u,l}^k$). In Fig. 7, the relations among C_{SM}, $N_{u,l}^k$ and U_{SM} are displayed, whereby the $N_{u,l}^k$ is varied from 200 until 620 with incremental steps equal to 10.

As it can be noted from Fig. 7, during full active power injection (top-left figure), all methods present similar profile. While $N_{u,l}^k$ raises, the value of the SM capacitance also increases linearly whereas the SM voltage U_{SM} has a nonlinear reduction. However, under full reactive power consumption or injection scenarios (see top-right and bottom figures), Methods III-A and III-B have convergence issues. Such issues happen due to the formulation of the problem as their iteration requires the maximum allowed voltage and maximum ripple to respect certain conditions that can not be fully achieved after $N_{u,l}^k \geqslant 470$.

Methods I, II and the proposed one, on the other hand, are able to converge obtaining C_{SM} for all conditions analyzed. Method II leads to the oversizing C_{SM}, while Method I results in the smallest C_{SM} levels. As it was shown in Section V-A, when the SM capacitors obtained with Method I are used in the converter, it might lead to undesirable operations of the converter. Finally, the proposed approach is the most suitable one as it does not present any of the aforementioned drawbacks.

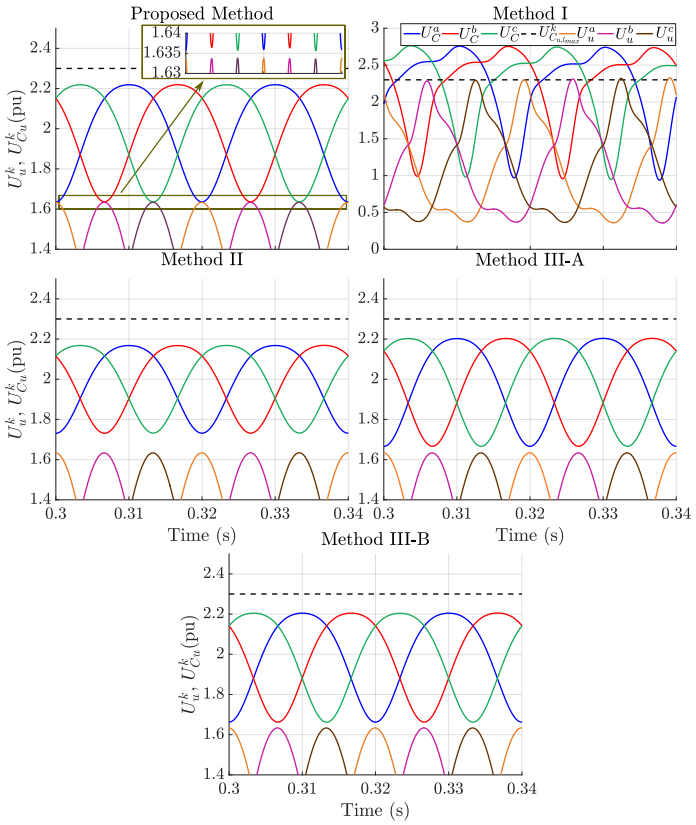


Fig. 6. Time-domain waveforms for the proposed method and Methods I to III-B of the upper arms applied voltages and the equivalent arm capacitor voltage $\phi = \frac{\pi}{2}$.

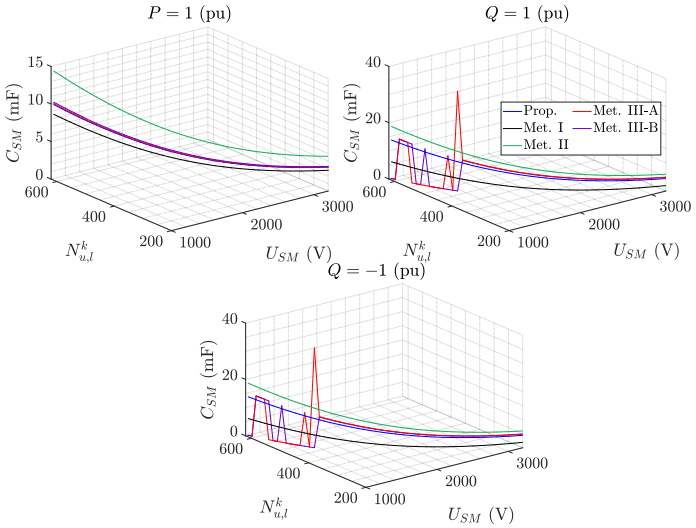


Fig. 7. Correlation between C_{SM} and number of installed SM assuming variable average SM capacitor voltage.

VI. Full Operation Range of the Converter

In this section, the proposed optimization-based SM capacitor design is run assuming that the converter is operated with nominal power, for several different active and reactive power set-points, as well as, AC network voltage scenarios. Each active and reactive power set-point is imposed by changing the power factor angle by a factor of $\pi/10$, whereas the real and imaginary components of the three-phase AC network voltage are also modified by a fixed value imposed in the $\alpha\beta 0$ reference frame. Under normal AC network voltage operation, the MMC must inject pure active power, however during voltage sag cases, the converter must inject/absorb reactive currents in order to provide voltage support (in accordance to the TSO's requirements [27]). Thus, the optimization algorithm will provide the minimal SM capacitance required to meet with those conditions, the converters constraints and, at the same time, respecting the SM capacitor maximum and minimum allowed voltages.

A. SM capacitance selection

The SM capacitor designed assuming the aforementioned conditions are shown in Fig. 8, where their optimal values are plotted for each active and reactive power set-points.For the x-axis, the SM capacitor multiplies with the cosine of the power factor angle, whereas for the y-axis the SM capacitor is multiplied by the sine of the power angle. In this way, it is possible to have an overview of the SM capacitor values required for whole operating region of the converter. Furthermore, for the regions in 8 where the value of C_{SM} is negative, its absolute value should be chosen. The negative sign just reflect that the converter is injecting active/reactive powers. As it can be noted, most SM capacitance magnitudes are obtained up to 10 mF. However, under few operating points analyzed, the device value can reach levels up to 18 mF. Although such value can ensure that the MMC is able to meet the TSO requirements while keeping the converter's quantities within their limitations for all analyzed cases, its implementation would lead to high installation costs due to its size and weight.

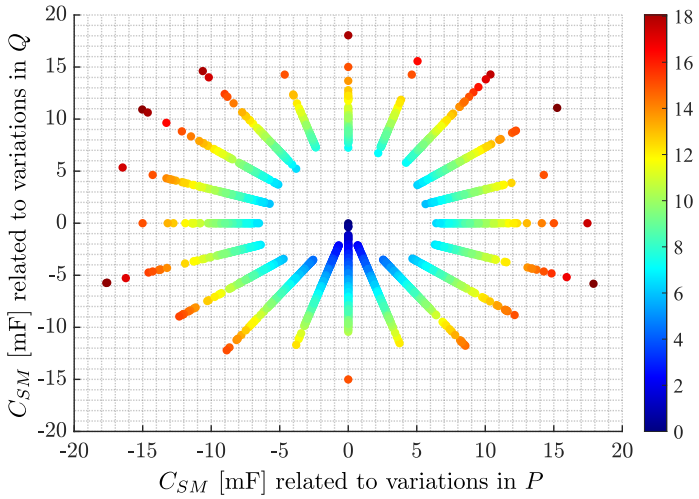


Fig. 8. Optimal C_{SM} for all the different OPs analyzed.

Further insights are observed in Fig. 9, in which the probability of occurrence (y-axis) during the several different scenarios considered (e.g. AC network voltage and PQ set-points) is given for the submodule capacitance (x-axis) obtained through the optimization algorithm[2]. As it can be observed, the highest occurrence rate happens when the SM capacitor magnitude is within $8-9$ mF. If a capacitance equals to $C_{SM} = 9$ mF is chosen,it can be ensured that during 86% of the different scenarios (obtained by summing the probability from 9 mF down to 0 mF) the MMC would be operated within the design limitations and respecting the TSO's condition. By increasing the SM capacitance, higher guaranteed rates can be obtained: for $C_{SM} = 9.5$ mF the rate is equal to 92% and $C_{SM} = 10$ mF results in rates equal to 94.3%. Once again, the trade-off between cost/weight and size plays a major role in the selection of the SM capacitor.

B. Time-domain waveforms during AC voltage sags

For this case study, time-domain simulations are performed considering two different SM capacitance values $C_{SM} = 9$ mF and $C_{SM} = 9.5$ mF, which as mentioned in Section VI-A would be able to meet the converter's and TSO requirements for 92 % of the cases. The main waveforms of the converter are analyzed for different AC network fault scenarios assuming the converter is injecting full active power prior to the faults, and when during the occurrence of the fault, the converter must inject/absorb reactive current components in accordance to the TSO's requirements [21], [27].

Firstly, the converter is operated under normal conditions, then at $t = 1$ s the faults are imposed in the AC network and they are cleared at $t = 1.5$ s. For all AC voltage sags studied, it is considered that $V = 0$ pu [28]. In Figs. 10 to 15, the upper and lower arms applied voltages $U^k_{u,l}$ and the sum of the SM capacitor voltages $U^k_{Cu,l}$ are depicted for a single-line-to-ground (SLG) fault, AC network singular voltage sag and internal voltage sag, respectively.

It can be noted that prior the fault and once the fault achieved the steady-state, either SM capacitor magnitude can be selected as they are respecting the converter's limits and the TSO requirements. In addition, the converter's arm applied voltages and the sum of the SM capacitor voltage dynamics are similar for all faults analyzed for both values of C_{SM}. Although the results indicate that the maximum allowed sum of the SM capacitor voltage is exceeded when the fault occurs or that the arm applied voltages are higher than the sum of the SM capacitor voltages during recovery phase, they happen during short time instants and they wont influence the overall performance of the converter during FRT conditions.

[2]Note that the red line represents the cumulative sum of the probabilities for each interval. If all the probabilities are summed up, they would result in a value equals to 1, representing 100% of the cases.

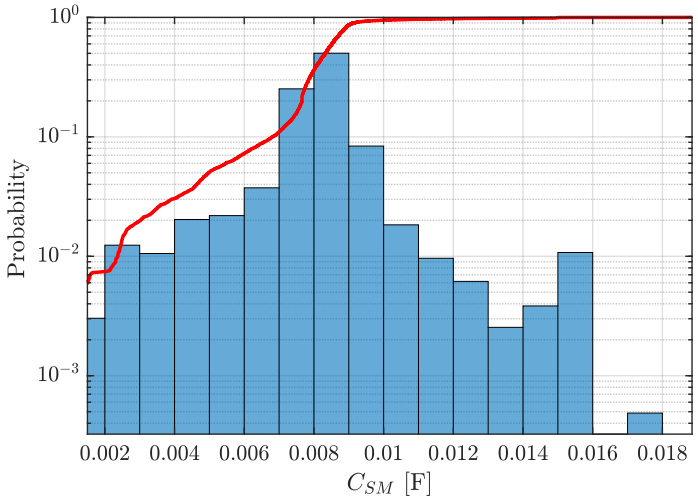


Fig. 9. C_{SM} histogram assuming different PQ and AC network voltage conditions.

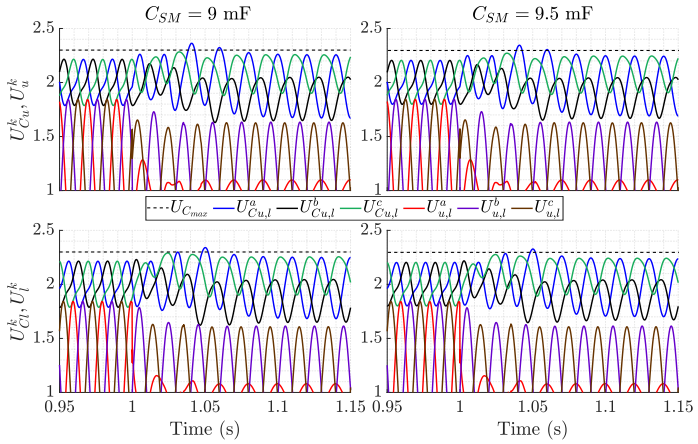


Fig. 10. Normal to fault during SGL fault.

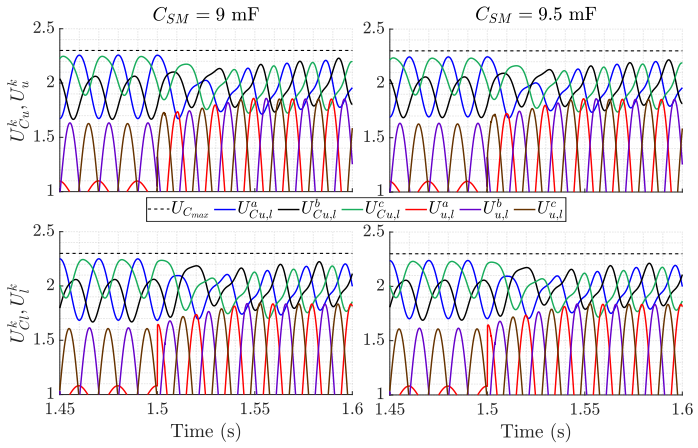


Fig. 11. Fault to normal during SGL fault.

By increasing the value the SM capacitor to $C_{SM} = 12$ mF, better dynamic response can be obtained. In Fig. 16, the waveforms of the converter are shown during the worst fault case presented earlier, AC network singular voltage sag, assuming $C_{SM} = 12$ mF. As it can be noted, throughout all the operation of the converter, the sum of the SM capacitor voltages are kept within limits and no overmodulation can be observed.

In order to ensure that for all AC network faults and active and reactive set-points the converters' limitations are not exceed, the maximum value of SM capacitance obtained from the proposed methodology should be employed, in this case $C_{SM} = 18$ mF. However, this highly conservative value would lead to a significant increase in volume, weight and costs of the converter

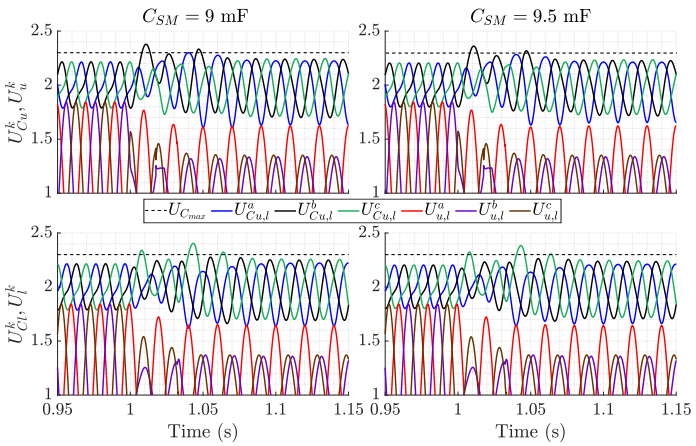


Fig. 12. Normal to fault during AC grid singular voltage sag type C.

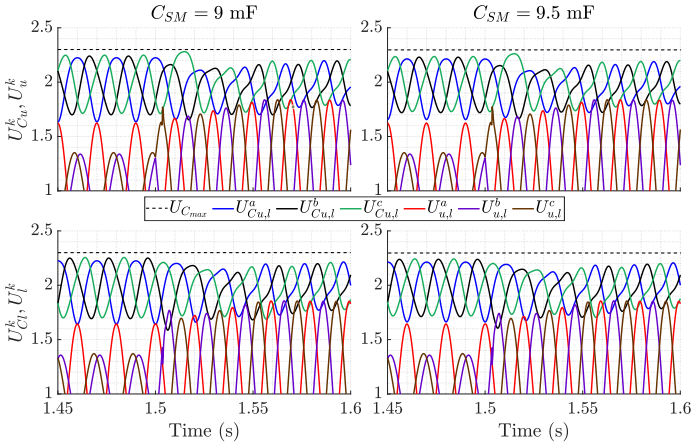


Fig. 13. Fault to normal during AC grid singular voltage sag type C.

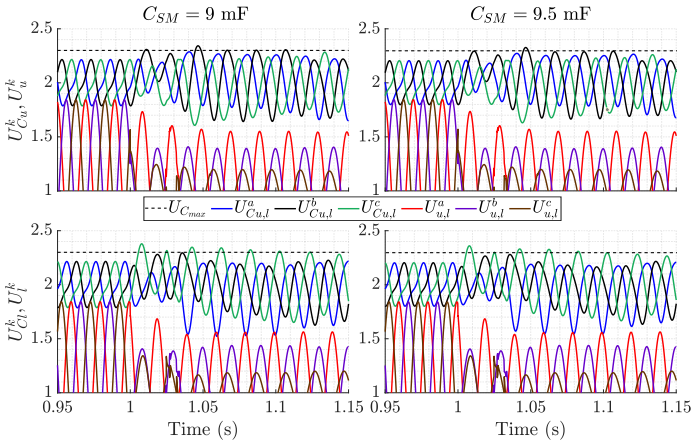


Fig. 14. Normal to fault during internal singular voltage sag type C.

station. Finally, for the converter configuration and control strategy used in the case studies, sub-module capacitors equal to $C_{SM} = 9$ mF could be feasible. Even though they might exceed some limitations transiently during severe faults, the overall performance of the converter was not affected.

VII. Conclusion

In this paper, an optimization-based methodology to design the SM capacitors of the MMC considering the converter's limitations and the TSO requirements during AC network voltage sags has been presented. Firstly, the instantaneous time-domain energy equations of the converter have been developed and their asymmetrical behavior during different OPs has been

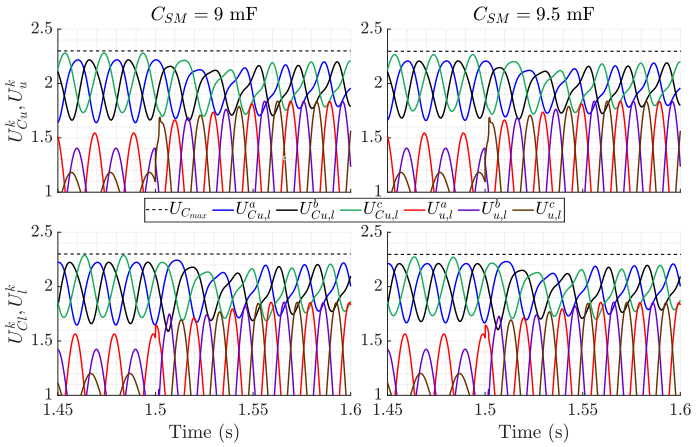


Fig. 15. Fault to normal during internal singular voltage sag type C.

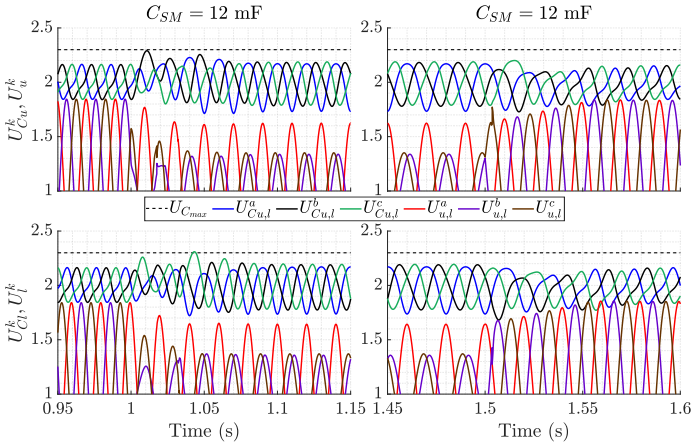


Fig. 16. Time-domain waveforms of the sum of the SM capacitor voltages and arm applied voltages for $C_{SM} = 12$ mF.

analyzed. Then, the suggested approach has been shown, whereby all its steps have been explained and validated by means of static and dynamic simulations. For the static validation, the proposed method is compared with different SM capacitor design approaches assuming different AC network active and reactive power set-points. It has been demonstrated that the optimization-based method can improve the SM capacitor design up to 24% in relation to the method with lowest performance and up to 7% in comparison with the method which considers more degrees of freedom in its analysis. Finally, for the dynamic simulations, different values of C_{SM} capacitors have been used in time-domain simulations of the converter considering different voltage sag scenarios, whereas both values presented similar responses.

APPENDIX A
DEFINITION OF THE FIRST AND SECOND ORDER ENERGY AND ANGLE TERMS

$$\mathbf{E^k_{u,lmax_\omega}} = \left(\left[\frac{U^{kDC}_{u,l}\hat{I}^k_{u,l}}{\omega}\cos(\phi^k_{u,l}) + \frac{I^{kDC}_{u,l}\hat{U}^k_{u,l}}{\omega}\cos(\theta^k_{u,l}) \right]^2 + \left[\frac{U^{kDC}_{u,l}\hat{I}^k_{u,l}}{\omega}\sin(\phi^k_{u,l}) + \frac{I^{kDC}_{u,l}\hat{U}^k_{u,l}}{\omega}\sin(\theta^k_{u,l}) \right]^2 \right)^{\frac{1}{2}} \tag{12}$$

$$\mathbf{E^k_{u,lmax_{2\omega}}} = \frac{U^k_{u,l}I^k_{u,l}}{2\omega} \tag{13}$$

$$\psi^{\mathbf{k}}_{\mathbf{u,l}} = \tan^{-1}\left(\frac{\frac{U^{kDC}_{u,l}\hat{I}^k_{u,l}}{\omega}\sin(\phi^k_{u,l}) + \frac{I^{kDC}_{u,l}\hat{U}^k_{u,l}}{\omega}\sin(\theta^k_{u,l})}{\frac{U^{kDC}_{u,l}\hat{I}^k_{u,l}}{\omega}\cos(\phi^k_{u,l}) + \frac{I^{kDC}_{u,l}\hat{U}^k_{u,l}}{\omega}\cos(\theta^k_{u,l})} \right) \tag{14}$$

$$\gamma^{\mathbf{k}}_{\mathbf{u},\mathbf{l}} = \theta^{k}_{u,l} + \phi^{k}_{u,l} \tag{15}$$

REFERENCES

[1] D. Van Hertem, O. Gomis-Bellmunt, and J. Liang, *HVDC Grids: For Offshore and Supergrid of the Future*, ser. IEEE Press Series on Power Engineering. Wiley, 2016.

[2] J.-J. Jung, H.-J. Lee, and S.-K. Sul, "Control strategy for improved dynamic performance of variable-speed drives with modular multilevel converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 2, pp. 371–380, 2015.

[3] J. H. D. G. Pinto, W. C. S. Amorim, A. F. Cupertino, H. A. Pereira, S. I. S. Junior, and R. Teodorescu, "Optimum design of MMC-based ES-STATCOM systems: The role of the submodule reference voltage," *IEEE Transactions on Industry Applications*, vol. 57, no. 3, pp. 3064–3076, 2021.

[4] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings,*, vol. 3, 2003, pp. 6 pp. Vol.3–.

[5] J. Peralta, H. Saad, S. Dennetiere, J. Mahseredjian, and S. Nguefeu, "Detailed and averaged models for a 401-level MMC–HVDC system," *IEEE Transactions on Power Delivery*, vol. 27, no. 3, pp. 1501–1508, 2012.

[6] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Main-Circuit Design*, 2016, pp. 60–132.

[7] C. Oates, "Modular multilevel converter design for VSC HVDC applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 2, pp. 505–515, 2015.

[8] Y. Tang, M. Chen, and L. Ran, "A compact MMC submodule structure with reduced capacitor size using the stacked switched capacitor architecture," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 6920–6936, 2016.

[9] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters—an overview," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3569–3578, 2014.

[10] M. Merlin and T. Green, "Cell capacitor sizing in multilevel converters: Cases of the modular multilevel converter and alternate arm converter," *IET Power Electronics*, vol. 8, no. 3, pp. 350–360, Mar. 2015.

[11] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 77–88, 2014.

[12] L. Lin, Y. Lin, C. Xu, and Y. Chen, "Comprehensive analysis of capacitor voltage fluctuation and capacitance design for submodules in hybrid modular multilevel converter with boosted modulation index," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 4, pp. 2369–2383, 2019.

[13] H. Bärnklau, A. Gensior, and S. Bernet, "Submodule capacitor dimensioning for modular multilevel converters," *IEEE Transactions on Industry Applications*, vol. 50, no. 3, pp. 1915–1923, 2014.

[14] Y. Tang, L. Ran, O. Alatise, and P. Mawby, "Capacitor selection for modular multilevel converter," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3279–3293, 2016.

[15] Z. Liu, K.-J. Li, J. Wang, Z. Javid, M. Wang, and K. Sun, "Research on capacitance selection for modular multi-level converter," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8417–8434, 2019.

[16] J. Li, G. Konstantinou, H. R. Wickramasinghe, C. D. Townsend, and J. Pou, "Capacitor voltage reduction in modular multilevel converters under grid voltages unbalances," *IEEE Transactions on Power Delivery*, vol. 35, no. 1, pp. 160–170, 2020.

[17] S. Wang, T. Dragicevic, Y. Gao, S. K. Chaudhary, and R. Teodorescu, "Machine learning based operating region extension of modular multilevel converters under unbalanced grid faults," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 5, pp. 4554–4560, 2021.

[18] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, L. Ängquist, and H.-P. Nee, "Capacitor voltage ripple shaping in modular multilevel converters allowing for operating region extension," in *IECON 2011 - 37th Annual Conference of the IEEE Industrial Electronics Society*, 2011, pp. 4403–4408.

[19] M. Winkelnkemper, A. Korn, and P. Steimer, "A modular direct converter for transformerless rail interties," in *2010 IEEE International Symposium on Industrial Electronics*, 2010, pp. 562–567.

[20] X. Li, Q. Song, W. Liu, S. Xu, Z. Zhu, and X. Li, "Performance analysis and optimization of circulating current control for modular multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 2, pp. 716–727, 2016.

[21] D. Westerman Spier, E. Prieto-Araujo, J. Lopez-Mestre, and O. Gomis-Bellmunt, "Improved current reference calculation for MMCs internal energy balancing control," *IEEE Transactions on Power Delivery*, pp. 1–1, 2021.

[22] D. Westerman Spier, J. L. Mestre, E. Prieto-Araujo, and O. Gomis-Bellmunt, "Steady-state analysis of the modular multilevel converter," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, 2019, pp. 4861–4866.

[23] D. Westerman Spier, J. M. Rodriguez-Bernuz, E. Prieto-Araujo, J. Lopez-Mestre, A. Junyent-Ferre, and O. Gomis-Bellmunt, "Real-time optimization-based reference calculation integrated control for MMCs considering converter limitations," *IEEE Transactions on Power Delivery*, pp. 1–1, 2021.

[24] D. Westerman Spier, J. L. Mestre, E. Prieto-Araujo, and O. Gomis-Bellmunt, in *3º Simpósio Ibero-Americano em Microrredes Inteligentes com Integraćão de Energias Renováveis*, 2019.

[25] J. Xu, C. Zhao, W. Liu, and C. Guo, "Accelerated model of modular multilevel converters in PSCAD/EMTDC," *IEEE Transactions on Power Delivery*, vol. 28, no. 1, pp. 129–136, 2013.

[26] Q. Tu and Z. Xu, "Impact of sampling frequency on harmonic distortion for modular multilevel converter," *IEEE Transactions on Power Delivery*, vol. 26, no. 1, pp. 298–306, 2011.

[27] B. O. del Estado, "Orden TED/749/2020, de 16 de julio, por la que se establecen los requisitos técnicos para la conexión a la red necesarios para la implementación de los códigos de red de conexión," no. 208, pp. 62 406–62 458, Aug. 2020.

[28] M. Bollen and L. Zhang, "Different methods for classification of three-phase unbalanced voltage dips due to faults," *Electr. Power Syst. Res.*, vol. 66, no. 1, pp. 59 – 69, 2003.