A Microcontroller-Based Interface Circuit for Three-Wire Connected Resistive Sensors

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***Abstract*— This article proposes and experimentally characterizes a novel microcontroller-based interface circuit to read three-wire connected resistive sensors, which are quite common in industrial applications to measure, for instance, temperature. The circuit relies on measuring, via an embedded digital timer, four discharging times corresponding to four different *RC* circuits, which include the sensor resistance and the parasitic resistance of the wires. A prototype has been built with a commercial microcontroller measuring resistances that correspond to a Pt100 thermal sensor and with different values of wire resistance. According to the experimental results, the error, with respect to the case with null wire resistances, is lower than 25 mΩ for a 5-m interconnecting cable. In addition, the non-linearity error (NLE) is lower than 0.02%–0.03% full-scale span (FSS), regardless of the wire resistances and also of any potential mismatch between them.**

***Index Terms*— Embedded system, microcontroller, remote sensor, resistive sensor, sensor interface electronics.**

I. Introduction

Many measurement systems, especially in the industry, rely on resistive sensors. Typical examples of them are resistance temperature detectors (RTD) and strain gauges, which are employed to measure temperature and mechanical stress, respectively. Due to limitations imposed by the application, some resistive sensors need to be located at a certain distance from the read-out circuit, thus requiring an interconnecting wire. This is what occurs, for example, when the measuring temperature range is wider than the operating range of the chips, which is, in the best scenario, between −50 °C and +125 °C. The parasitic resistance of the interconnecting wire can generate a significant error in the measurement, especially if the sensor resistance is low. For instance, for a standard copper wire with a parasitic resistance of 0.3–0.4 Ω/m [1], each meter of the cable causes an error of around 1 °C when measuring a platinum RTD with 100 Ω at 0 °C (also so-called Pt100). In addition, such a parasitic resistance depends on temperature, thus generating even more uncertainty in the measurement result.

To cope with the previous limitation, remote resistive sensors are usually connected to the circuit through a three- or four-wire connection. The former is less expensive, whereas the latter provides a more accurate measurement result. These connections are so common in industrial applications that many manufacturers commercialize their sensors with the three- or four-wire interconnecting cable included. The typical block diagram of a circuit intended for a three-wire connected resistive sensor is shown in Fig. 1. The sensor is connected to a Wheatstone bridge, the first lead being part of the sensor arm, the second of the balancing arm, whereas the third becomes one of the terminals of the bridge differential output [2]. This output is then amplified by a differential amplifier, converted to digital by an analog-to-digital converter (ADC), and finally read by a microcontroller unit (MCU). More compact design solutions have been recently suggested in the literature, for instance, the relaxation oscillator circuits with a time-based output signal proposed in [3] and [4]. In these circuits, however, some active devices (such as operational amplifiers, comparators, and switches) are still required between the sensor and the control and timing unit, which is usually implemented by an MCU.

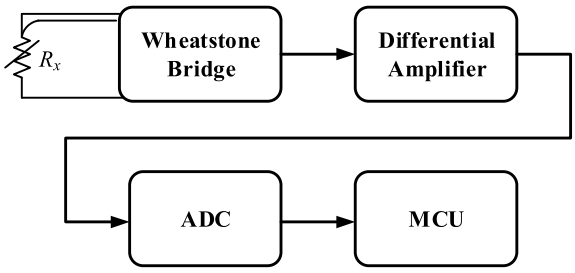

Fig. 1. Classical block diagram of a read-out circuit for a resistive sensor (R_x) with a three-wire connection.

With the aim of reducing the cost and energy consumption of the read-out circuit, the concept of a *direct interface circuit* (DIC), in which the sensor is directly connected to the MCU without either the amplifier or the ADC, has been proposed for the measurement of resistive [5], [6], [7], capacitive [8], [9], and inductive sensors [10]. Such a concept has also been applied to the measurement of remote resistive sensors through a two-wire connection [1], [11]. Its main limitation, however, is that several components and devices, such as a couple of twin diodes and switches, are required between the sensor and the MCU and, hence, it cannot be considered as a "pure" direct sensor-to-MCU connection.

II. Operating Principle

In the context presented in Section I, this article proposes the novel circuit shown in Fig. 2. This is based on the DIC proposed in [12] but applied to a three-wire connected resistive sensor, which is modeled by the sensor resistance (R_x) and the parasitic resistance ($R_{w1}-R_{w3}$) of the three lead wires. The circuit also includes a capacitor (C_d), a charging resistor (R_i), a reference resistor (R_{ref}), and a resistor (R_0) to limit the current during the discharge process. In addition, the parasitic resistance (R_p) of the MCU pin when this provides a digital "0" is considered in the analysis. This is initially assumed the same for the four pins involved in the measurement, although differences of around 0.2 Ω can be found in different families of commercial MCU, such as PIC and AVR [12].

The operating principle of the circuit in Fig. 2 is as follows. Through pin P1 and R_i, the capacitor C_d is charged to the voltage (V_1) related to a digital "1." Afterwards, P1 is set as an input (or in high-impedance, HZ, mode) and C_d is discharged toward the ground via an equivalent resistance that depends on the configuration of the other pins, as summarized in Table I. An embedded digital timer measures (actually, it performs a time-to-digital conversion) the time interval required to discharge C_d from V_1 to the threshold voltage (V_{TL}) of P1, as shown in Fig. 3. Note that the same pin (P1) is

Manuscript received 3 October 2022; revised 14 October 2022; accepted 20 October 2022. Date of publication 4 November 2022; date of current version 16 November 2022. The Associate Editor coordinating the review process was Dr. He Wen.

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Digital Object Identifier 10.1109/TIM.2022.3219492

TABLE I

STATE OF THE MCU PINS IN FIG. 2, EQUIVALENT RESISTANCE, AND RESULTING DISCHARGING TIME FOR EACH OF THE FOUR MEASUREMENTS

Measurement	P2	P3	P4	P5	Equivalent resistance	Discharging time
Offset	"0"	HZ	HZ	HZ	$R_{eq1} = R_0 + R_p$	$T_{off} = k \cdot R_{eq1}$
Reference	HZ	"0"	HZ	HZ	$R_{eq2} = R_{eq1} + R_{ref}$	$T_{ref} = k \cdot R_{eq2}$
Sensor	HZ	HZ	HZ	"0"	$R_{eq3} = R_{eq1} + R_{w3} + R_x + R_{w1}$	$T_s = k \cdot R_{eq3}$
Wire	HZ	HZ	"0"	HZ	$R_{eq4} = R_{eq1} + R_{w3} + R_{w2}$	$T_w = k \cdot R_{eq4}$

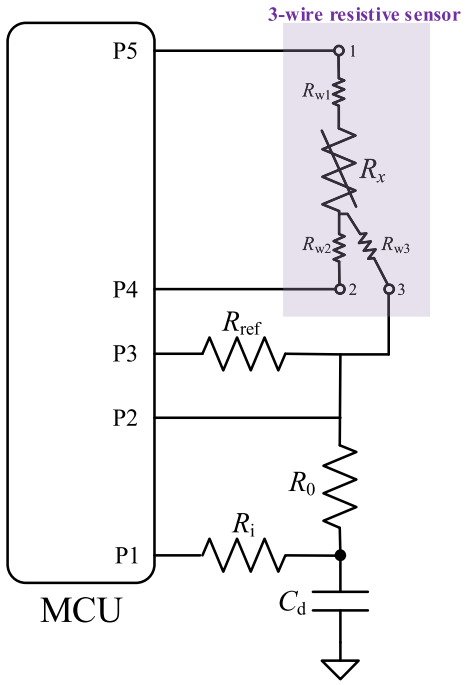

Fig. 2. Proposed MCU-based interface circuit for a three-wire connected resistive sensor.

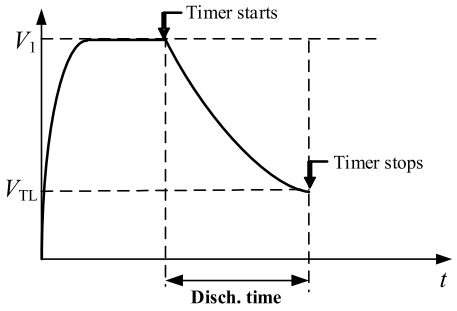

Fig. 3. Waveform of the voltage across C_d in Fig. 2 during the charge–discharge process.

always employed for both charging and detection of the threshold-voltage crossing and, hence, no mismatch problems are generated. The length of the discharging time is proportional to the equivalent resistance, as indicated in Table I, where $k = C_d \cdot \ln(V_1/V_{TL})$.

From Table I, four discharging-time measurements (T_{off}, T_{ref}, T_s, and T_w) are performed corresponding to the offset, reference, sensor, and wire measurement, respectively. Of course, for non-remote resistive sensors [12], the measurement of T_w is unnecessary, thus reducing the overall measuring time. Then, it is proposed to estimate the sensor resistance as

$$R_x^* = \frac{T_s - T_w}{T_{ref} - T_{off}} R_{ref} \tag{1}$$

Replacing the expressions of the four discharging times (given in Table I) in (1) results in

$$R_x^* = R_x + R_{w1} - R_{w2}. \tag{2}$$

According to (2), the measurement undergoes an offset error that depends on the difference $R_{w1} - R_{w2}$, but not on R_{w3}. Therefore, wires 1 and 2 should be as similar as possible, whereas the features of wire 3 are irrelevant. This is, actually, the same situation found when the conventional approach depicted in Fig. 1 is employed [13]. The schemes suggested in [1] and [11] do provide an output independent of the mismatch between R_{w1} and R_{w2}, but at the expense of employing two twin diodes at the sensor end.

If we assume that there is a mismatch (ΔR_p) between the different R_p involved in the measurement, the sensor resistance resulting from (1) can be approximated (considering $\Delta R_p \ll R_{ref}$) to

$$R_x^* \approx \left(R_x + R_{w1} - R_{w2} + \Delta R_{p54}\right)\left(1 + \frac{\Delta R_{p32}}{R_{ref}}\right) \tag{3}$$

where ΔR_{p54} and ΔR_{p32} are the mismatch between the parasitic resistances of pins 5 and 4, and 3 and 2, respectively. According to (3), such mismatches generate offset and gain errors. Supposing $\Delta R_{p54} = \Delta R_{p32} = 0.2\ \Omega$ and $R_{ref} = 100\ \Omega$, the corresponding offset and gain errors are expected to be 0.2 Ω and 0.2%, respectively.

III. EXPERIMENTAL RESULTS

A prototype of the circuit in Fig. 2 has been designed on a printed circuit board. The core of the circuit was a commercial low-cost 8-bit MCU (ATtiny2313 from Microchip) running at 20 MHz with a supply voltage of 5 V. The discharging time shown in Fig. 3 was measured via a 16-bit embedded timer with a time base of 50 ns. Resistors between 60 and 264 Ω were employed to emulate a Pt100 measuring temperatures between −100 °C and +450 °C. The parasitic resistance of the three wires was also emulated by three resistors, considering the four scenarios summarized in Table II. Note that a wire resistance of 2 Ω corresponds to a cable length of approximately 5 m. The actual value of all resistors was measured by a 7 1/2-digit digital multimeter (Keysight 34470A). The other components of the circuit in Fig. 2 were: $C_d = 4.7\ \mu$F, $R_i = 4.7\ \Omega$, $R_0 = 100\ \Omega$, and $R_{ref} = 100\ \Omega$. The capacitor was selected high enough to decrease the relative effects of the quantization in the timing process, but low enough to avoid the overflow of the timer. The resistor R_i was placed in the circuit to better reject the effects of power-supply interference [14], but this was selected quite low to reduce the charging time, to be precise: less than 1 ms for the capacitor selected. For each condition under test, the four time intervals (T_{off}, T_{ref}, T_s, and T_w) were measured a hundred times, thus estimating 100 values of the sensor resistance. The mean of those resistance values was employed

TABLE II

VALUE OF THE RESISTORS EMULATING THE PARASITIC RESISTANCE OF THE WIRES FOR THE FOUR SCENARIOS UNDER TEST

Scenario	R_{w1} (Ω)	R_{w2} (Ω)	R_{w3} (Ω)	Others
1	0	0	0	Reference scenario
2	2	2	2	Same nominal value, but the difference between actual values was ±2 mΩ
3	2	2	1	Intended mismatch to check the effects of R_{w3}
4	2	1	2	Intended mismatch to check the effects of $(R_{w1} - R_{w2})$

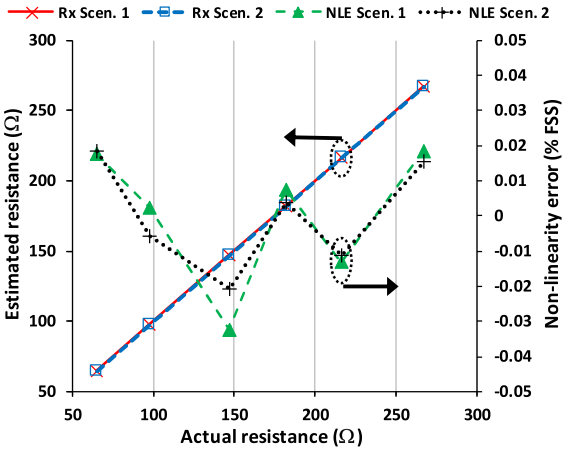

Fig. 4. Experimental I/O characteristic of the circuit in Fig. 2 for scenarios 1 and 2 indicated in Table II, and the corresponding NLE.

in the following representations to estimate the systematic error of the measurement.

Fig. 4 shows the experimental input–output (I/O) characteristic for scenarios 1 and 2, which correspond to 0- and 5-m interconnecting cables, respectively. With respect to the actual value of input resistance, the 0-m case showed an absolute error that was quite constant to −0.3 Ω. Therefore, according to (3), the prototype was mainly affected by the offset effects of ΔR_{p54}. If the sensor resistance was estimated using an individual observation, instead of the mean of 100 observations, the error increased (in the worst case) up to −0.4 Ω. This is mainly due to the noise affecting the voltage comparison shown in Fig. 3. The standard deviation of the population of 100 measurements was around 30–40 mΩ.

The 5-m case represented in Fig. 4 did not show a shifting of 4 Ω as would occur in a conventional two-wire measurement (i.e., 2 Ω corresponding to each wire), but the I/O characteristic was almost identical to the 0-m case; the small differences between them will be represented and explained later. Therefore, the effects of the wire resistances were clearly compensated for. Additionally, Fig. 4 also shows the non-linearity error (NLE), which was calculated by fitting a straight line to the experimental data using the least-squares method, and then expressed as a percentage of the full-scale span (FSS). Accordingly, the maximum NLE (in absolute value) was around 0.03% and 0.02% FSS for scenarios 1 and 2, respectively. Very

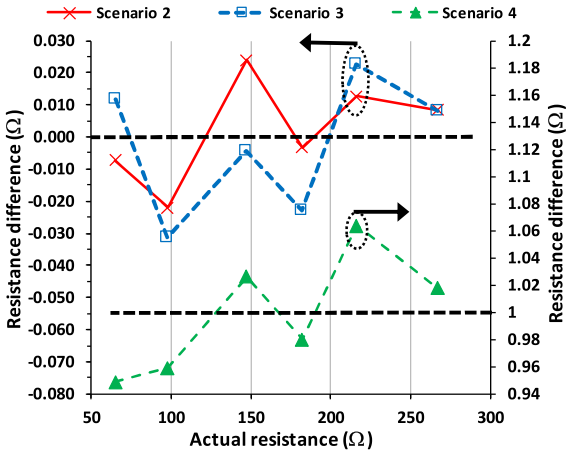

Fig. 5. Difference between the resistance estimated in scenarios 2–4 with respect to that one calculated in scenario 1.

similar values of NLE were obtained in scenarios 3 and 4. Note that, under the same conditions, a classical Wheatstone bridge offers a differential output voltage with an NLE higher than 10% FSS, which is 500 times higher. Consequently, the proposed circuit has a very remarkable linearity that is independent of the presence and also of mismatch of the wire resistances.

As indicated before, the I/O characteristics of the four scenarios under test were very similar. The difference between them, always using the results for scenario 1 as a reference, is represented in Fig. 5. For scenarios 2 and 3, the maximum difference (in absolute value) was 25 and 30 mΩ, respectively. Considering the low value of that error and its random performance, such an error can be mainly ascribed to the quantization affecting the time-to-digital conversion shown in Fig. 3. However, in scenario 4, the difference was higher, to be precise: 1 Ω ± 50 mΩ. This offset error agrees with (2) and the data given in Table II. Therefore, the mismatch between R_{w1} and R_{w2} causes an offset error, as predicted, whereas the mismatch between R_{w3} and the other two does not generate any error in the output.

IV. DISCUSSION AND COMPARISON

A comparison of the features of the proposed circuit versus the existing ones is summarized in Table III. The main advantages of the proposed circuit are: 1) the low number of external components required, to be precise: just a capacitor and a few resistors and 2) the low value of the NLE, which is at least three times smaller than those reported so far in the literature. On the other hand, the main limitation is that the estimation of the sensor resistance requires four charge–discharge cycles, thus resulting in an overall measuring time of 7 ms. Considering the other conversion times reported in Table III, the proposed circuit has an intermediate position in that sense. In case this conversion time is too long for a given application, it can be reduced by selecting a lower value of C_d. However, decreasing the value of C_d worsens the resolution of the measurement. Therefore, in order to reduce the conversion time and keep the resolution, the reduction factor of C_d and the increase factor of the operating frequency of the MCU should be the same.

Unlike the circuits suggested in [3] and [4], the topology presented in Fig. 2 is simpler but it is only applicable to resistive sensors with a single-element topology. In comparison with the circuits suggested in [1] and [11], which employ a two-wire configuration for the remote measurement, the circuit proposed herein does not require a

TABLE III
COMPARISON STUDY

Reference	Sensor configuration	Type of connection	External components [a]	Charge-discharge cycles	Range of resistance measurement	Overall measuring time (ms)	Maximum NLE
[1]	Single element	2 wires	2 diodes, 3 switches	3	[100, 146] Ω	5.3	1.04% FSS [b]
[3]	Single and differential	3 wires	1 OpAmp, 1 comparator, 2 switches, 1 PGA	2 [c]	[1k, 1M] Ω [d]	110	0.09% (single scenario)
[4]	Single, differential, and bridge	3 wires	1 comparator, 4 switches	3	[80, 150] Ω [800, 1500] Ω	30 (single scenario)	0.09% (single scenario)
[11]	Single element	2 wires	2 diodes, 2 switches, 1 555-timer	2	[100, 150] Ω	2.6	0.33% FSS
This work	Single element	3 wires	None	4	[60, 264] Ω	7	0.03% FSS

(a) Other than resistors and capacitors
(b) According to the comparative study reported in [11]
(c) But it involves the measurement of 3 time intervals
(d) A specific gain of the PGA (programmable-gain amplifier) was selected for each decade of the range

couple of twin diodes at the sensor end. Therefore, the measurement is not affected by the mismatch of those diodes and their thermal sensitivity.

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