CESTOR SOLVE DESIGN PROBLEMS

Protect power-LED strings from overcurrent

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A common method for driving multiple power LEDs is through two parallel strings. This inexpensive and less critical driver circuit can provide a lower voltage. However, the driver circuit must deliver twice the current of other methods and needs a circuit that halves the current in the two strings, regardless of the LEDs' forward voltages. The LEDs' forward-voltage tolerance is as high as 20%, and the voltages change with LED temperature and aging.

A current mirror performs this task well. If an LED breaks, it can cause destructive overcurrent. The current mirror, however, can safely partially protect two parallel, connected strings of any number of 350-mA power LEDs from these overcurrents (Figure 1).

The circuit can balance the currents between strings with a matching error of approximately 2% because of the equal voltages of 0.5V developed on 1.5Ω emitter resistors R₁ and R₂ with 1% tolerance. The voltage drop across resistor R₃ compensates for the mismatching of LED voltage drops and holds both Q₁ and Q₂ in the linear region. The voltage drop depends on how many LEDs make up the two strings.

If an LED of String 2 fails, however, no base current flows to transistors Q_1 and Q_2 , and they turn off. All LEDs in String 1 have automatic overcurrent protection. The circuit doesn't perform the same function if an LED in String



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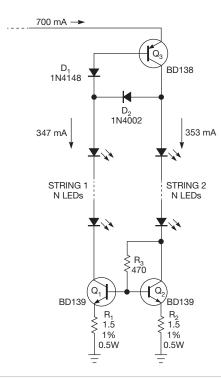
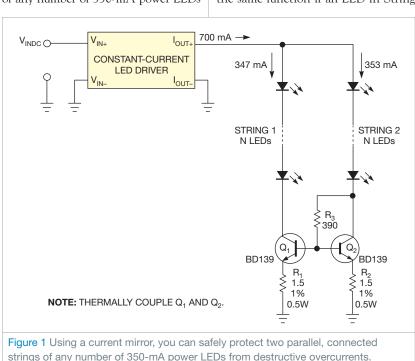


Figure 2 An LED in String 1 can fail because all of the 700-mA driver current flows into String 2, which needs some form of protection. You can solve this problem by adding only three components.



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1 fails because all of the 700-mA driver current flows into String 2, which needs some form of protection. You can solve this problem by adding only three components (**Figure 2**).

In normal operation, transistor Q_3 operates in its linear region with an emitter-collector voltage of 0.7V because both diodes D_1 and D_2 are forward-biased. The power dissipation of Q_3 is only about 0.5W, and it thus needs no heat sink. The 700-mA driver

current coming from the collector of Q_3 divides equally between the strings through steering diode D_2 , as the current mirror dictates. If an LED in String 1 fails, diode D_2 blocks the base current of Q_3 , turning it off. The driver current can no longer flow through String 2, safeguarding the LEDs.

You must compensate for diode D_2 's 0.7V voltage drop, which slightly increases the value of resistor R_3 . You can adapt the current mirror for driving

any type of LED without exceeding the absolute maximum rating of the transistors' collector current, which is 1.5A. You can test the current mirror with any 700-mA constant-current LED driver, or even a voltage regulator configured as a current source, such as National Semiconductor's (www.national.com) LM317 regulator. The circuit underwent testing, with the LM317 acting as a 700-mA current source with five LEDs per string.EDN

Simple flasher operates off ac mains

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Looking for a mains switch in the dark is easier if the switch contains a built-in neon or filament miniature lamp. Adding a small indicator to any mains switch is helpful. It is even better if the indicator flashes. This circuit makes a simple flasher using only four discrete components (Figure 1).

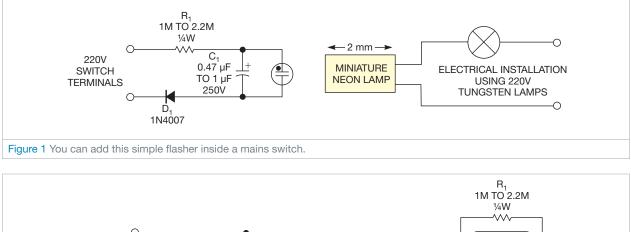
The neon lamp flashes at a frequency of 1 to 5 Hz, according to experimental values for resistance and capacitance. When the switch terminals are open, diode D_1 acts as a halfwave rectifier. Capacitor C_1 charges through resistor R_1 until the voltage on the capacitor exceeds the breakdown voltage of a miniature neon lamp. C_1 then discharges rapidly through the lamp, which flashes. You can access the switch terminals by prying off the front panel with a small screwdriver. This circuit can be installed inside the switch block. You assemble it on a 5×10-mm PCB (printed-circuit board).

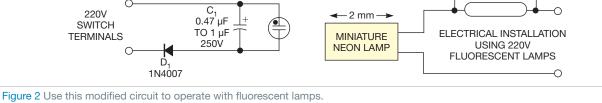
This flasher circuit works properly

only with 220V tungsten lamps. To use it with 220V fluorescent lamps, you must make a small modification

THIS CIRCUIT MAKES A SIMPLE FLASHER USING ONLY FOUR DISCRETE COMPONENTS.

(Figure 2). Disconnect resistor R_1 from the flasher circuit and place it in parallel with the starter of the fluorescent lamp, which is connected in series with the mains switch. EDN





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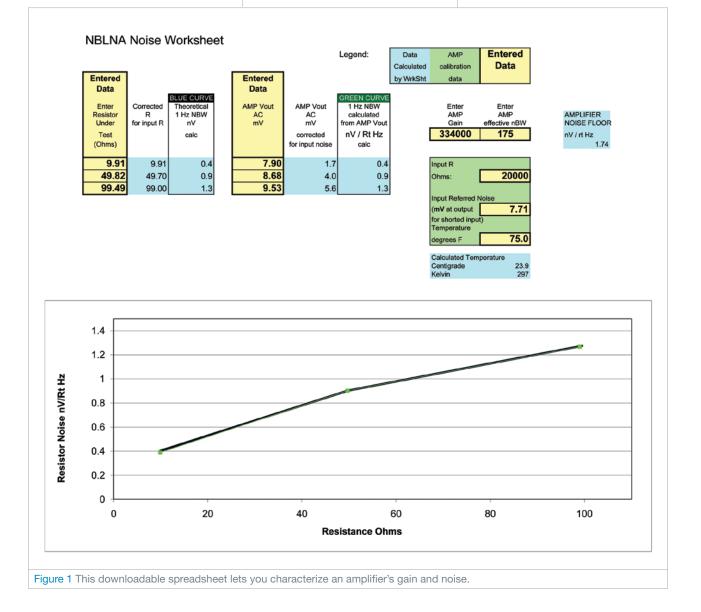
Use resistor noise to characterize a low-noise amplifier

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If you know or can estimate a low-noise amplifier's gain or noise bandwidth, you can measure the other spec using only a handful of resistors and an ac voltmeter (**Reference 1**). The method in this Design Idea uses the Johnson Equation, which describes the amount of noise a resistor generates (**Reference 2**). To find the missing parameter, measure an amplifier's output-noise voltage, first for a shorted input and then using a few resistors of different values. You can download an Excel spreadsheet that can calculate gain or noise bandwidth from the online version of this Design Idea at www.edn. com/110623dia.

To begin the measurement, place a short circuit across the low-noise amp's input terminals and measure the noise voltage with the voltmeter. Next, insert the resistors, one at a time, across the amplifier's inputs and measure the noise voltage at the output of the amplifier. Enter the measured output-noise voltages, the measured values of each resistor's resistance, the ambient temperature, and either the known or the estimated gain of the low-noise amp or the known or estimated effective noise bandwidth into the spreadsheet.

Using each of the measured resistance values, the spreadsheet plots a theoretical "blue" curve representing the Johnson noise in normalized units of nV/\sqrt{Hz} (Figure 1). You can compensate



the blue curve for any low-noise-amp input resistance. The graph also shows a "green" curve that represents the amplifier's calculated "excess" output noise—the measured output minus the amplifier's uncorrelated input-referred noise. The input-referred noise is an short-circuiting the amplifier's input terminals.

You can use a multimeter, such as Agilent's (www.agilent.com) 34410A, with a second-display math-average feature to fill in the measured outputnoise values (**Reference 3**). After you

A MULTIMETER HAS A SECOND-DISPLAY MATH-AVERAGE FEATURE THAT CAN BE USED TO FILL IN THE MEASURED OUTPUT-NOISE VALUES. USE THE OHMMETER FUNCTION TO MEASURE THE ACTUAL RESISTANCE VALUE.

uncorrelated noise signal that adds to any excess input noise as the square root of the sum of the squares of the noise voltages. You can find the amplifier's input-referred noise using its effectivenoise-bandwidth and gain values and measuring the output-noise voltage by connect each resistor to the amplifier's input terminals when the amplifier is on, reset the math average; wait until the new value settles down, which typically takes 10 seconds to approximately one minute; and record the average value for that resistor on the noise worksheet. Use the ohmmeter function to measure the actual resistance value and enter that value into the spreadsheet.

Enter the input parameters and measured output-noise values into the spreadsheet. Take a guess at the unknown parameter's initial value and then vary it until the green curve almost exactly overlaps the theoretical blue curve. When the curves overlap, you've found the missing parameter. You can then try what-if scenarios by varying both parameters.**EDN**

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Build a UWB pulse generator on an FPGA

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You can implement a digital \mathbf{N} UWB (ultrawideband) pulse generator in most FPGAs. The design lets you create a pulsed signal with a frequency that's twice the FPGA's clock frequency (Figure 1). A previous design relies on asynchronous delays to make pulses of the desired frequency. That design, however, requires an FPGA that supports tristate pullups, such as the Xilinx (www.xilinx.com) Virtex 2 (Reference 1). That approach also requires manual placement and routing. Today's FPGAs don't support tristate pullups. In addition, asynchronous delays vary with temperature. This Design Idea uses a synchronous-delay approach employing a combination of multiple clock phases. You can implement this design in all types of FPGAs.

The maximum clock frequency of the DCM (digital clock manager) and the flip-flops are the main limiting factors in this design. For example, the DCM of a Xilinx Virtex 4 can't exceed 400 MHz. An FPGA can generate signals of frequencies that are half the clock frequency because it takes two clock pulses to toggle the signal from zero to one and back. Thus, you can't directly generate frequencies greater than half the clock frequency. This design lets you generate pulsed signals higher than

half the clock frequency and reaches twice the clock frequency by using multiple clock phases from the DCM and synchronous delays smaller than one clock period.

Figure 2 shows the proposed pulse generator. It consists of three functional blocks, an OOK (on/ off-key) modulator, a synchronous-delay generator, and an edge combiner comprising an exclusive OR gate. The OOK modulator

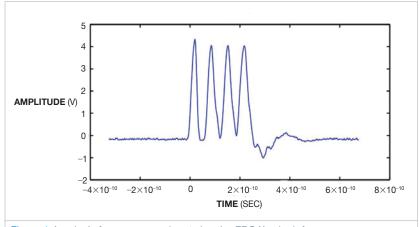
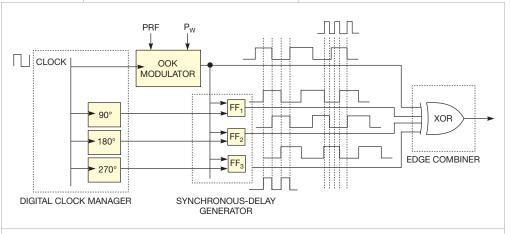


Figure 1 A pulse's frequency reaches twice the FPGA's clock frequency.

comprises an inverter that the pulserepetition-frequency signal triggers at every start of a new pulse. When a trigger occurs, the OOK circuit inverts a preinitialized signal to a time equal to a count value derived for a pulse width and remains zero until the next trigger. The OOK block generates a frequency that is one-half the clock frequency. This OOK output passes through the synchronous-delay generator, which generates three delayed versions of the OOK output.

These delays are smaller than one clock period. The clock phases in turn clock flip-flops FF_1 , FF_2 , and FF_3 , which

lag by 90, 180, and 270°, respectively. These delayed pulses then combine with the output of the OOK modulator using combinatorial logic to generate the desired frequency for the UWB pulses. The edge combiner performs an XOR (exclusive-OR) operation, which generates signal frequencies that depend on the edges you want to combine. Combining the output of the OOK edge with the output of FF1 generates a signal frequency equal to the clock frequency. Combining the edges of all outputs generates a signal frequency equal to two times the clock frequency. The DCM synchronizes these





delays, producing an accurate signal frequency. This design is less complex than the asynchronous-delay approach in **Reference 1.EDN**

REFERENCE Park, Youngmin, and David D Wentzloff, "All-digital synthesizable UWB transmitter architectures,"

Proceedings of the 2008 IEEE International Conference on Ultra-Wideband, Volume 2, 2008, http://bit. ly/j3wVuG.

Generate swept sine/cosine waveforms with two filters

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Demodulators, directional circuits, and other electronics applications often need two sine waves with a 90° difference in phase—a sine wave and its cosine wave. Engineers typically use analog filters to create the phase shift. This approach, however, offers a limited frequency range. Using the circuit in **Figure 1**, you can make a swept sine/cosine pair at frequencies of less than 1 Hz to 25 kHz.

The Mixed Signal Integration (www.mix-sig.com) MSFS5 selectable lowpass/bandpass switched-capacitor filter removes the harmonics from a square wave you apply to its inputs. The clock for the MSFS5 is 100 times the input square wave. The 74HC390 and 74HC74 form a divide-by-25 and a divide-by-two circuit. The Q outputs from the 74HC74 connect to the two divide-by-two circuits in the 74HC390A, which produces square waves that are 1/100 of the filter clock's frequency and are 90° out of phase from each other. A square wave at CMOS levels would saturate the filter, so the circuit uses resistor dividers R_1 through R_4 to reduce the signal's amplitude.

Figure 2 shows the output of the two filters at 20 kHz with a system clock of 2 MHz. Note that the phase reading on the scope is at -89.85°. When swept in frequency, the phase varies from -89 to -91°. **Figure 3** shows a 20-kHz Lissajous pattern.

Measuring the circuit's distortion using a spectrum analyzer and an Audio Precision (www.ap.com) audio analyzer shows a THD (total harmonic distortion) of -49 dB. Testing shows that the circuit has no discontinuity at the filter outputs with either FSK (frequency-shift keying) or FM (frequency modulation).EDN





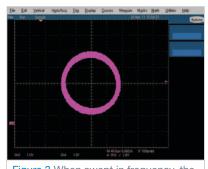


Figure 3 When swept in frequency, the phase varies from –89 to –91°.

