High-Speed Equalization and Transmission in Electrical Interconnections

Hogesnelheidsegalisatie en -transmissie in elektrische interconnecties

Yu Ban

Promotoren: prof. dr. ir. J. Bauwelinck, dr. ir. G. Torfs
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Universiteit Gent
Faculteit Ingenieurswetenschappen
en Architectuur
Vakgroep Informatietechnologie

Promotor: Prof. Dr. Ir. Johan Bauwelinck
Dr. Ir. Guy Torfs

Universiteit Gent
Faculteit Ingenieurswetenschappen en Architectuur

Vakgroep Informatietechnologie
Sint-Pietersnieuwstraat 41, B-9000 Gent, België

Tel.: +32-9-264.33.40
Fax.: +32-9-264.35.93

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Dankwoord

How time flies! Now I can still clearly remember the first day when I stepped into the door of the INTEC_design Laboratory. After 4.5 years of study and research as a PhD student in this pleasant atmosphere, the writing of this dissertation symbolizes the end of my 24 years student life. Truly, the road to persue a PhD degree is not always easy or flat, but full of challenges. Luckily I am not alone, as there are so many people around me, providing me with their guidance, assistance, encouragement and companionship. Without these, this PhD would not have been accomplished. So here I would like to thank you all, for helping me finally reach this stage.

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I extend my acknowledgment to my fellow labmates in the Design Lab, it was a great pleasure to work with all of you. I would especially thank Timothy De Keulenaer as we worked closely together during the past 4 years, and it was really an exciting moment when we got the 84Gbit/s transmission working. I would like to thank my colleagues: Guus Colman, Jasmien Put, Punithavathi Duraiswamy, Zhisheng Li, Christophe Van Praet, Jochen Verbrugghe, Xiao Li, Renato Vaernewyck, Ramses Pierco, Arno Vyncke, Bart Moeneclaey, Koen Verheyen, Wouter Soenen, Michael Vanhoecke, Marijn Verbeke, Jochem Verbist, Gertjan Coudyzer, Haolin Li and Joris Van Kerrebrouck. You all helped me and contributed to create an active and pleasant working environment.

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Ghent, May 2015

Yu Ban

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List of Acronyms

A

AM	Amplitude Modulation

B

BER	Bit Error Rate
BERT	Bit Error Rate Tester
BJT	Bipolar Junction Transistor
BP	BackPlane board
BR	Bit Rate
BW	Bandwidth

C

CPW	Coplanar Waveguide
CTLE	Continuous Time Linear Equalizer

D

DC	Daughter Card
DeMUX	Demultiplexer

DFE	Decision-Feedback Equalizer
DSP	Digital Signal Processing

E

ED	Error Detector
EF	Emitter Follower
ESD	Electrostatic Discharge

F

FFE	Feed-Forward Equalizer
FIR	Finite Impulse Response
FoM	Figure of Merit

G

GP	General Purpose
GSSG	Ground-Signal-Signal-Ground

H

HDTV	High-Definition Television

I

IC	Integrated Circuit
I/O	Input/Output

IP	Internet Protocol
IPTV	Internet Protocol Television
ISI	Inter-Symbol Interference

K

KVL	Kirchhoff's Voltage Law

L

LP	Low Power
LPF	Low Pass Filter
LSE	Least Square Error
LT	Line Termination

M

MOS	Metal Oxide Semiconductor
MPW	Multi-Project Wafer
M2M	Machine-to-Machine
MUX	Multiplexer

N

NRZ	Non-Return-to-Zero
NRZ-OOK	Non-Return-to-Zero On/Off Keying
NT	Network Termination

O

OFDM	Orthogonal Frequency-Division Multiplexing

P

PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PHY	Physical Layer
PPG	Pulse Pattern Generator
PRBS	Pseudo-Random Binary Sequence
PSD	Power Spectral Density

Q

QAM	Quadrature Amplitude Modulation

R

RX	Receiver

S

SDTV	Standard-Definition Television
Sinc	Cardinal Sine function
SNR	Signal-to-Noise Ratio

T

TML	Transmission Line

TR	Tuning Range
TX	Transmitter

U

UHDTV	Ultra-High-Definition Television
UI	Unit Interval

V

VGA	Variable Gain Amplifier
VNA	Vector Network Analyzer

Nederlandstalige samenvatting –Dutch Summary–

De niet aflatende groei van het dataverkeer en de toenemende verwerkingskracht van digitale chips vragen om steeds snellere chip-naar-chip en chip-naar-module interconnecties. Met toenemende datasnelheden zal de kwaliteit van de datasignalen echter meer en meer degraderen na transmissie over een printplaat (PCB) verbinding . Frequentie-afhankelijk verlies en overspraak leiden tot een gereduceerde oogopening, een gereduceerde signaal-tot-ruis verhouding en een toenemende inter-symbool-interferentie (ISI). Deze problemen vereisen het gebruik van betere signaalverwerking of betere PCB materialen om de bandbreedtebeperkingen te overwinnen en om de signaalintegriteit te verbeteren. Door een optimale combinatie van egalisatie en ontvangerelektronica, samen met bandbreedte-efficiënte modulatieschema's, kan de transmissiesnelheid over seriële elektrische verbindingen verhoogd worden. Bij de start van dit onderzoek, werkten de meeste industriële backplane connectoren, zoals gemaakt door FCI of TE connectivity, volgens IEEE of OIF specificaties, aan een maximale snelheid van 25 Gb/s.

Dit onderzoek kwam vooral tot stand in het kader van het IWT Shorttrack project. Het doel van dit onderzoek was om de transmissiesnelheid over elektrische backplanes te verhogen tot 100 Gb/s per kanaal voor toekomstige telecom- en datacom-systemen. Deze doelstelling ging veel verder dan de toenmalige stand van zaken, welke beperkt was tot 25 Gb/s voor duobinaire modulatie en 42.8 Gb/s PAM-4 transmissie over een Megtron 6 backplane met lage verliezen, echter gebruik makende van signaalverwerking in Matlab.

De succesvolle implementatie van een geïntegreerde zenderchip, beschreven in dit werk, en een geïntegreerde ontvangerchip, beschreven in het doctoraat van collega Timothy De Keulenaer, tonen duidelijk de haalbaarheid aan van seriële interconnecties voor meer dan 80 Gb/s met het potentieel om 100 Gb/s seriële verbindingen te realiseren in een recente chiptechnologie.

Naast onze bijdrage tot de stand van zaken in het domein van de zeer snelle zendontvangers en backplane transmissie in het algemeen, heeft de demonstratie van dit werk ook veel aandacht gekregen voor heel snelle optoelektronische communicatietoepassingen zoals toegangsnetwerken, actieve optische kabels en optische backplanes.

De achtergrond van dit onderzoek, een overzicht van dit werk en de organisatie van dit proefschrift worden geïllustreerd in Hoofdstuk 1. In Hoofdstuk 2 wordt een systeemanalyse voorgesteld die aantoont dat de kanaalverliezen de transmissiesnelheid over backplanes beperken. Om de seriële datasnelheid te verhogen over backplanes en om de signaaldegradatie te verminderen, worden verschillende technologieën besproken zoals signaal-egalisatie en modulatietechnieken. Eerst wordt er een prototype backplane kanaal met verbeterde connectoren van projectpartner FCI gekarakteriseerd. Dan wordt er een geïntegreerd transversaal feedforward egalisatie filter (FFE) voorgesteld, gebaseerd op een overschouwing van de kanaalperformantie, de analoge egalistie-mogelijkheden, implementatiecomplexiteit en vermogenverbruik.

NRZ, duobinair en PAM-4 zijn de meest eenvoudige modulatieschema's voor uiterst snelle elektrische backplane-communicatie. Na een vergelijking op basis van simulaties, werd het duobinair formaat geselecteerd voor zijn hoge bandbreedte-efficiëntie en zijn redelijke circuitcomplexiteit. Verschillende chiptechnologieën werden vergeleken en het ST 130 nm SiGe BiCMOS9MW proces (met een f_T groter dan 200 GHz) werd gekozen als compromis tussen snelheid en prototyping kost. Daarnaast biedt dit proces heel goede analoge opties met o.a. een geïntegreerd microstripmodel, dat gebruikt zal worden als vertragingselement in de FFE.

Hoofdstuk 3 illustreert het chipontwerp van de snelle backplane zenderchip, bestaande uit een multiplexer (MUX) en een 5-tap FFE. De 4:1 MUX combineert vier tragere datastromen tot 1 zeer snel NRZ signaal tot 100 Gb/s als input voor de FFE schakeling. Deze MUX werd ontworpen door collega dr. Zhisheng Li. De 5-tap FFE uit mijn onderzoek is geïmplementeerd met een nieuwe topologie met uitgebreide testmogelijkheden, zodat de FFE performantie individueel gekarakteriseerd kan worden in het tijd- en frequentiedomein, zonder de MUX te moeten loskoppelen. Dit helpt ook om de FFE instellingen te optimaliseren. Verschillende instelbare versterkerconfiguraties werden vergeleken. De Gilbert configuratie toont de meeste voordelen, met zowel een goede hoogfrequent performantie en een eenvoudige manier om positieve/negatieve versterking in te stellen. De totale chip, met inbegrip van de MUX en de FFE, verbruikt 750 mW uit een 2.5 V voeding en

beslaat een oppervlakte van 4.4 mm $\times$ 1.4 mm.
In Hoofdstuk 4 wordt de Tx chip gedemonstreerd tot 84 Gb/s. Eerst werd de FFE performantie gekarakteriseerd in het frequentiedomein, wat aantoonde dat de FFE duobinaire signalen kan maken tot 84 Gb/s. Naast de werking van de verschillende sub-blokken, werd ook de combinatie van MUX en FFE getest. De geëgaliseerde Tx signalen werden opgemeten voor verschillende kanalen en voor zowel NRZ en duobinair aan snelheden van 64 Gb/s tot 84 Gb/s. Dan werd een seriële transmissielink gedemonstreerd door toevoeging van een duobinaire ontvanger (doctoraat Timothy De Keulenaer). Het kanaal bestond hierbij eerst uit een paar 10 cm coax kabels en 5 cm FX-2 stripline transmissielijnen. Het 13.5 dB verlies bij de Nyquist frequentie werd gecompenseerd door de FFE. De ontvangerchip decodeerde het geëgaliseerde duobinaire signaal en demultiplexeerde het signaal naar vier NRZ uitgangen aan een vierde van de snelheid. Deze link had een bitfoutprobabiliteit (BER) van minder van 10^{-11}.
Ten slotte werd ook foutloze transmissie tussen zender en ontvanger gedemonstreerd over twee commerciële backplanes. Eerst werd er met een 11.5 inch Megtron 6 backplane aan een snelheid van 48 Gb/s aangetoond dat duobinair beter werkt dan NRZ voor lange kanalen. Later, werd er met een ExaMAX® backplane demonstrator, het maximum foutvrij kanaalverlies onderzocht aan een snelheid van 40 Gb/s. De oogpatronen en de BER metingen werden uitgevoerd voor zeer lange kanalen tot 26.25 inch. De resultaten tonen aan dat de ontworpen FFE, een groot totaalverlies van 37 dB bij de Nyquist frequentie kan overwinnen met foutvrije duobinaire transmissie, en voor een BER van 10^{-8} is zelfs een kanaalverlies van 42 dB overbrugbaar. Een overzicht van de conclusies is samengevat in Hoofdstuk 5, met een aantal suggesties voor verder onderzoek.

English summary

The relentless growth of data traffic and increasing digital signal processing capabilities of integrated circuits (IC) are demanding ever faster chip-to-chip / chip-to-module serial electrical interconnects. As data rates increase, the signal quality after transmission over printed circuit board (PCB) interconnections is severely impaired. Frequency-dependent loss and crosstalk noise lead to a reduced eye opening, a reduced signal-to-noise ratio and an increased inter-symbol interference (ISI). This, in turn, requires the use of improved signal processing or PCB materials, in order to overcome the bandwidth (BW) limitations and to improve signal integrity. By applying an optimal combination of equalizer and receiver electronics together with BW-efficient modulation schemes, the transmission rate over serial electrical interconnections can be pushed further. At the start of this research, most industrial backplane connectors, meeting the IEEE and OIF specifications such as manufactured by e.g. FCI or TE connectivity, had operational capabilities of up to 25 Gb/s.

This research was mainly performed under the IWT ShortTrack project. The goal of this research was to increase the transmission speed over electrical backplanes up to 100 Gb/s per channel for next-generation telecom systems and data centers. This requirement greatly surpassed the state-of-the-art reported in previous publications, considering e.g. 25 Gb/s duobinary and 42.8 Gb/s PAM-4 transmission over a low-loss Megtron 6 electrical backplane using off-line processing.

The successful implementation of the integrated transmitter (TX) and receiver (RX) [1], clearly shows the feasibility of single lane interconnections beyond 80 Gb/s and opens the potential of realizing industrial 100 Gb/s links using a recent IC technology process. Besides the advancement of the state-of-the-art in the field of high-speed transceivers and backplane transmission systems, which led to several academic publications, the output of this work also attracts a lot of attention from the industry, showing

[1] The duobinary receiver was developed by my colleague Timothy De Keulenaer, as described in his PhD dissertation.

the potential to commercialize the developed chipset and technologies used in this research for various applications: not only in high-speed electrical transmission links, but also in high-speed opto-electronic communications such as access, active optical cables and optical backplanes.

In this dissertation, the background of this research, an overview of this work and the thesis organization are illustrated in Chapter 1.

In Chapter 2, a system level analysis is presented, showing that the channel losses are limiting the transmission speed over backplanes. In order to enhance the serial data rate over backplanes and to eliminate the signal degradation, several technologies are discussed, such as signal equalization and modulation techniques. First, a prototype backplane channel, from project partner FCI, implemented with improved backplane connectors is characterized. Second, an integrated transversal filter as a feed-forward equalizer (FFE) is selected to perform the signal equalization, based on a comprehensive consideration of the backplane channel performance, equalization capabilities, implementation complexity and overall power consumption. NRZ, duobinary and PAM-4 are the three most common modulation schemes for ultra-high speed electrical backplane communication. After a system-level simulation and comparison, the duobinary format is selected due to its high BW efficiency and reasonable circuit complexity. Last, different IC technology processes are compared and the ST microelectronics BiCMOS9MW process (featuring a f_T value of over 200 GHz) is selected, based on a trade-off between speed and chip cost. Meanwhile it also has a benefit for providing an integrated microstrip model, which is utilized for the delay elements of the FFE.

Chapter 3 illustrates the chip design of the high-speed backplane TX, consisting of a multiplexer (MUX) and a 5-tap FFE. The 4:1 MUX combines four lower rate streams into a high-speed differential NRZ signal up to 100 Gb/s as the FFE input. The 5-tap FFE is implemented with a novel topology for improved testability, such that the FFE performance can be individually characterized, in both frequency- and time-domain, which also helps to perform the coefficient optimization of the FFE. Different configurations for the gain cell in the FFE are compared. The gilbert configuration shows most advantages, in both a good high-frequency performance and an easy way to implement positive / negative amplification. The total chip, including the MUX and the FFE, consumes 750 mW from a 2.5 V supply and occupies an area of 4.4 mm $\times$ 1.4 mm.

In Chapter 4, the TX chip is demonstrated up to 84 Gb/s. First, the FFE performance is characterized in the frequency domain, showing that the

FFE is able to work up to 84 Gb/s using duobinary formats. Second, the combination of the MUX and the FFE is tested. The equalized TX outputs are captured after different channels, for both NRZ and duobinary signaling at speeds from 64 Gb/s to 84 Gb/s. Then, by applying the duobinary RX [2], a serial electrical transmission link is demonstrated across a pair of 10 cm coax cables and across a 5 cm FX-2 differential stripline. The 5-tap FFE compensates a total loss between the TX and the RX chips of about 13.5 dB at the Nyquist frequency, while the RX receives the equalized signal and decodes the duobinary signal to 4 quarter rate NRZ streams. This shows a chip-to-chip data link with a bit error rate (BER) lower than 10^{-11}. Last, the electrical data transmission between the TX and the RX over two commercial backplanes is demonstrated. An error-free, serial duobinary transmission across a commercial Megtron 6, 11.5 inch backplane is demonstrated at 48 Gb/s, which indicates that duobinary outperforms NRZ for attaining higher speed or longer reach backplane applications. Later on, using an ExaMAX® backplane demonstrator, duobinary transmission performance is verified and the maximum allowed channel loss at 40 Gb/s transmission is explored. The eye diagram and BER measurements over a backplane channel up to 26.25 inch are performed. The results show that at 40 Gb/s, a total channel loss up to 37 dB at the Nyquist frequency allows for error-free duobinary transmission, while a total channel loss of 42 dB was overcome with a BER below 10^{-8}.
An overview of the conclusions is summarized in Chapter 5, along with some suggestions for further research in this field.

[2] Described in the PhD dissertation of Timothy De Keulenaer.

List of publications

Publications in international journals

- **Y. Ban**, T. De Keulenaer, G. Torfs, J.H. Sinsky, B. Kozicki and J. Bauwelinck, *Experimental evaluation of NRZ and duobinary up to 48 Gbit/s for electrical backplanes*, Electronics Letters, vol. 51, no. 8, pp. 617-619, April 2015.

- T. De Keulenaer, G. Torfs, **Y. Ban**, R. Pierco, R. Vaernewyck, A. Vyncke, Z. Li, J.H. Sinsky, B. Kozicki, X. Yin and J. Bauwelinck, *84 Gbit/s SiGe BiCMOS duobinary serial data link including serialiser/deserialiser (SERDES) and 5-tap FFE*, Electronics Letters, vol. 51, no. 4, pp. 343-345, February 2015.

- **Y. Ban**, T. De Keulenaer, Z. Li, J. Van Kerrebrouck, J.H. Sinsky, B. Kozicki, J. Bauwelinck and G. Torfs, *A wide-band, 5-tap transversal filter with improved testability for equalization up to 84 Gb/s*, accepted by the IEEE Microwave and Wireless Components Letters.

Publications in international conferences

- T. De Keulenaer, J. De Geest, G. Torfs, J. Bauwelinck, **Y. Ban**, J.H. Sinsky and B. Kozicki, *56+ Gb/s serial transmission using duobinary signaling*, Proceedings of IEC DesignCon, Santa Clara USA, January 2015.

- T. De Keulenaer, **Y. Ban**, G. Torfs, S. Sercu, J. De Geest and J. Bauwelinck, *Measurements of millimeter wave test structures for high speed chip testing*, 18th IEEE Workshop on Signal and Power Integrity (SPI), Ghent Belgium, May 2014, pp. 1-4.

- T. De Keulenaer, **Y. Ban**, Z. Li and J. Bauwelinck, *Design of an 80 Gbit/s SiGe BiCMOS fully differential input buffer for serial elec-*

trical communication, 19th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Seville, December 2012, pp. 237-239.

Publications in national conferences

- **Y. Ban**, G. Torfs and J. Bauwelinck, *High speed data transmission over electrical backplane channels*, 15th FEA PhD symposium, Interactive poster session, Ghent Belgium, December 2014.
- **Y. Ban** and J. Bauwelinck, *High-speed transmitter design for communication beyond 40 Gb/s*, 13th FEA PhD symposium, Presentation session, Ghent Belgium, December 2012.

Patents

- J. Bauwelinck, G. Torfs, **Y. Ban** and T. De Keulenaer, *Improvements in test circuits*, European patent application, EP14161772.0, filed in March 2014.

1

Introduction

Nowadays, people are increasingly relying on the internet and expecting ever faster connectivity to either their workplace or home. First of all, the impressive evolution of video-based internet consumption demands much higher data rates from data networks. Second, the implementations of internet protocol television (IPTV) have experienced a number of generations, from standard-definition television (SDTV), high-definition television (HDTV) and ultra-high-definition television (UHDTV), gradually evolving to 3D television. This development pushes the demand for widely deployed, high-bandwidth (BW) services [1]. Therefore, both internet users and content providers have been demanding larger and larger network BW supporting higher data rates. Meanwhile, factors expected to drive traffic growth further include global increases in the number of internet users, personal devices and machine-to-machine (M2M) connections. It has been predicted that from 2014 to 2019, global internet protocol (IP) traffic will increase 3-fold and reach 168 exabytes per month by 2019, which is depicted in Figure 1.1 [2].

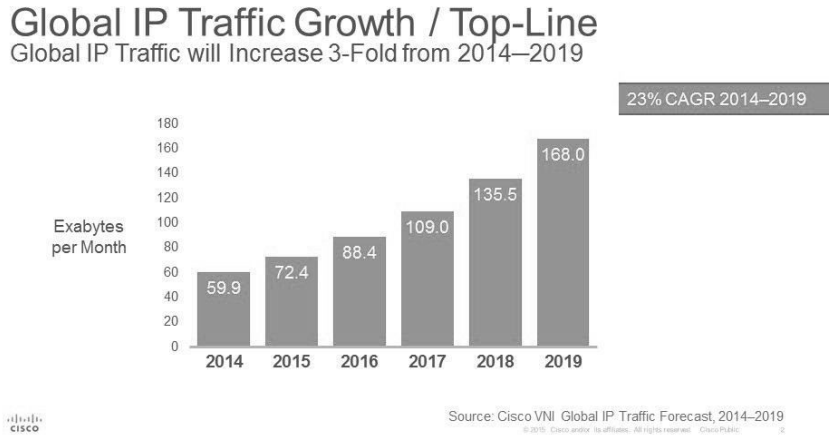

Figure 1.1: Global IP traffic growth

1.1 Background

1.1.1 Network architecture and access nodes

The ever increasing BW demands pose increasingly challenging requirements for network switches and core routers in high-speed data communication systems. As an essential part of network core routers, access nodes terminate various user connections (such as: xDSL, GPON, 10GPON) and aggregate the data from various end-users. This data stream is forwarded at a high speed along optical fibers in the internet backbone, metro and access networks. Figure 1.2 presents the general structure of a modern telecommunication network [3].

The progressive growth of network traffic from the data center to the end-users requires an ever faster data rate across the access nodes. Meanwhile, as the oversubscription rate [4] may decrease, it potentially triggers a faster growth on the internal capacity of access nodes compared to end-users. Moreover, some operators expect an even higher user BW and higher access rate for next-generation internet networks in the future. Therefore, a rapidly increasing BW requirement within access nodes, either internal or external, can be foreseen in next-generation data transmission networks [5].

The architecture of an access node, as shown in Figure 1.3, is a star topology. The interfaces towards the end-users are terminated on a card called line termination (LT) card, while the interfaces towards the metro network are terminated on a card called network termination (NT) card. All LT cards

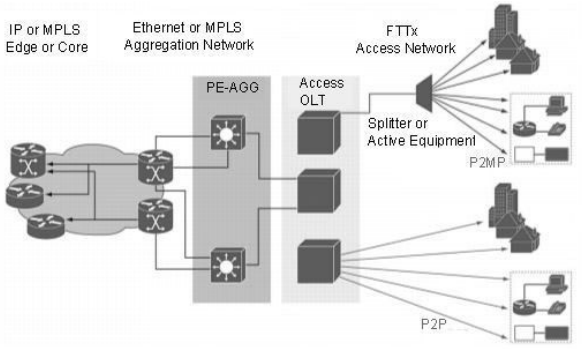

Figure 1.2: Network architecture overview

are connected with the NT card via a backplane. For redundancy reasons, sometimes a second NT is used. This architecture is called a star architecture because each LT card has a point-to-point connection with the NT card. Therefore, extending the throughout over a backplane is a critical part for enhancing the overall operational speed across access nodes [5] [6].

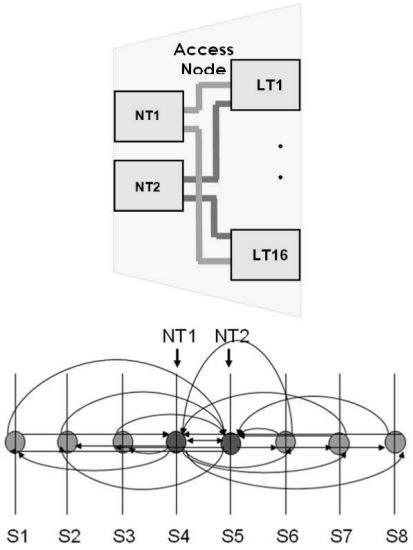

Figure 1.3: Access nodes with star architecture

At the beginning of this research, most industrial backplane systems operated at serial data rates between 10 Gb/s and 28 Gb/s per lane [7] [8]. These backplane systems consist of integrated backplane transceivers and indus-

trial backplane channels (including a big multi-layer PCB and connectors), such as manufactured by e.g. FCI Electronics or TE Connectivity [9].

1.1.2 Technical challenges

Extending the serial backplane channel throughput (e.g. beyond 40 Gb/s) is very challenging due to various aspects across the end-to-end communication channel.

First of all, a great challenge is the inter-dependency of the different aspects of the end-to-end solution. For example, the selection of the modulation scheme depends on the characteristics of the backplane traces / connectors. But the design of backplane connectors and the selection of backplane materials are relevant to the required system BW, which depends on the selected modulation scheme. Meanwhile, the design of transceiver electronics depends not only on the selected modulation and coding scheme, but also on the characteristics of the backplane channel: BW, linearity, noise, equalizer requirements...

Second, the transceiver design is highly challenging due to the very tough high-speed requirements, which went far beyond the state-of-the-art. The dependency between transceiver electronics and modulation format creates a challenge as different modulation schemes have specific characteristics and trade-offs among power dissipation, chip area and performance. Investigation of packaging technologies will also be necessary to eliminate the signal degradation along the connection between the die and the board. At high frequencies, reflections and termination issues due to process variation and parasitics also require investigation.

In addition, there is a challenge for the backplane and connector suppliers to enhance the BW of the passive backplane channel. Different backplane transmission line (TML) configurations (micro-strips, striplines, coplanar waveguides...) and dielectric materials (FR-4, Megtron6, Nelco 4000-13...) need to be investigated. Meanwhile, the design challenges of backplane connectors are manifold, due to their 3D structure and mechanical tolerances, including e.g. the connector to board termination and associated via holes. The impact of component tolerances on the component and system performance needs to be researched as well, since at high-frequency, small variations can have a significant impact.

Last, the modulation and coding challenge is to define schemes that maximize the throughput with minimal complexity (low-cost transceivers), taking into account the limitations of the connectors and reasonably priced backplane materials. At the targeted very high throughput, the design complexity becomes rapidly an important issue as additional interconnections

and additional circuit elements increase the amount of parasitics in the network, and it will be crucial to keep the complexity under control. In the meantime, besides NRZ, other schemes such as PAM-4 and duobinary will be investigated as well. These schemes, although being more complex, reduce the required BW, which could be beneficial in reducing the overall backplane cost. Another trade-off is the complexity of the modulation versus the required number of transceivers. The extra complexity and cost of a transceiver can be counteracted by the fact that fewer transceivers are necessary to provide a comparable capacity. Next to these challenges the resulting solution should be a green solution in the sense that power consumption per capacity unit should be reduced or comparable to current systems.
To answer all the above-mentioned technical questions, the INTEC Design lab was engaged in a big research project together with Alcatel-Lucent Bell Labs and FCI, with the objective to study and to demonstrate next-generation transceiver circuits with speeds well beyond state-of-the-art.

1.2 Overview of this work

This dissertation is mainly based on the author's research in the frame of the IWT project ShortTrack, over the past 4.5 years at the Design laboratory in the department of Information Technology (INTEC).
The overall innovation goal of ShortTrack was to investigate and to develop the building blocks to increase the transmission speed over electrical backplanes with reasonable power consumption, which enhances the overall system capacity and constrains cost. In this research, the first activities focused on the definition of the circuit specifications deriving from the system requirements and the initial assumptions of the channel characteristics. In parallel, various technologies and circuit techniques were explored to evaluate the feasibility of the inital specifications. The resulting requirements have been established end-to-end with a final goal to increase serial data rates up to 100 Gb/s per lane over electrical backplanes with on-board interconnects of around 10 cm long.
Backplane communication operating at high data rates poses great challenges as it requires a very high BW across the electrical link, while increased data rates face excessive frequency dependent attenuation, reflection and inter-symbol interference (ISI) [10]. These degrading effects become much more pronounced at higher frequencies as they scale more than linearly with frequency. As a result, in high-speed communication links, the received data waveforms can be significantly distorted after travelling through coaxial cables or printed circuit board (PCB) interconnects [11]. To compensate the ISI and to improve the channel BW efficiency, advanced

modulation and equalization were used in transmitter (TX) and receiver (RX) circuits. Besides, a 4-to-1 serializer which combined lower speed input signals to higher speed output signals was added in the TX. The serializer and its output buffer were designed together with our colleague Zhisheng Li.
Duobinary signaling is a valuable candidate of modulation formats, especially in band-limited eletrical transmission systems. Duobinary holds great potential for attaining high-speed or long-reach electrical transmission systems, as it utilizes the available BW more efficiently and allows confining the signal power spectral density (PSD) to lower frequencies compared to non-return-to-zero (NRZ). However, the implementation of the duobinary format involves a bit more complexity in the transceiver design due to the need for a precoder and decoder operating at the line rate.
The PCB traces in backplanes introduce frequency-dependent losses. Meanwhile, the parasitics introduced by the connectors, together with the termination resistors, generate a low-pass filter and further reduce the BW of the backplane link. All those effects introduce signal ISI and degrade the signal transmission performance, especially at high frequencies. Therefore, the development and optimization of high-speed electrical backplane channels is an important part in this project, mainly performed by project partner FCI Electronics.
My work focused on investigating and developing high-speed TX circuits, optimized for duobinary modulation. After the implementation of the TX and RX chips, together with my colleague Timothy De Keulenaer, we demonstrated an error-free, serial electrical duobinary transmission across an electrical backplane at a record speed, showing the potential to realize next-generation data links.
The results of this research can be applied in a variety of telecom and datacom systems, where high-speed electrical links are also relevant with various chip-to-chip / chip-to-module interconnects, as described in [12].

1.3 Organization of this dissertation

Chapter 1 presents the background of this research, an overview of this work and the organization of this dissertation. In this first chapter, high-speed access nodes, as essential parts connecting internet end-users with content providers, have been briefly described. As a core part of the access nodes, high-speed data transmission over electrical backplanes has been researched in this work, aiming to increase the serial data rate. In order to eliminate the signal degradation, Chapter 2 illustrates a system level analysis, and discusses several potential technical improvements, including sig-

nal equalization and modulation techniques. The design and optimization of a high-speed integrated TX, consisting of a multiplexer (MUX) and a 5-tap feed-forward equalizer (FFE), are illustrated in Chapter 3. The 5-tap FFE is implemented with an innovative topology for improved testability, such that the FFE performance can be individually characterized. Chapter 4 demonstrates the measurement results of the TX chip up to 84 Gb/s, showing progress beyond the state-of-the-art in both speed and power efficiency. Besides, system level measurements are performed in combination with an integrated RX chip. Error-free, electrical data transmission across various channels has been demonstrated, with serial data rates up to a record 84 Gb/s using duobinary modulation. Finally, this dissertation ends with a summary of the most important conclusions of this work in Chapter 5.

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2

Backplane systems and modulation schemes

2.1 Introduction

The relentless growth of data traffic and digital signal processing capabilities are demanding for ever faster interconnections between chips and other modules. Therefore, in the electrical backplane links, an increased channel bandwidth (BW) is required, in order to increase the transmission data rate. From the literature study, we found that most reported backplane systems are operating at the data rate of 10 Gb/s or 28 Gb/s per lane [1]- [3]. Recently, standard groups such as the IEEE P802.3bs 400 GbE and the OIF CEI-56G-VSR/MR have been looking into serial data rates above 50 Gb/s as the line rate of future generation physical layers (PHYs) [4]. In this section, we investigate the feasibility of serial backplane transmission beyond 40 Gb/s, and try to find the bottlenecks limiting the transmission performance. Therefore, a careful system level analysis and optimization is required.

At very high data rates, the signal quality in a low-cost printed circuit board (PCB) transmission line (TML) is severely impaired by frequency dependent losses leading to a reduced eye opening, reduced signal-to-noise ratio and increased inter-symbol interference (ISI). Meanwhile, as part of the channel, backplane connectors are very critical with respect to signal re-

flections and channel BW. In addition, advanced modulation and/or equalization are widely used in the transmitter (TX) / receiver (RX), in order to compensate the ISI and to improve the channel BW efficiency [5]. The performance of these techniques, together with new PCB technologies and backplane connectors, needs to be evaluated in order to satisfy both the specific channel throughput and power constraints [6]. Moving beyond 40 Gb/s data rate, however, poses great challenges on the integrated circuit design due to the semiconductor technology limitations and the related layout parasitics, which will degrade the chip performance, especially at high frequencies. Therefore, care has to be taken in the selection of the IC fabrication process, taking into account the circuit design limitations, while minimizing the power consumption and chip cost.

2.2 Backplane channel and design challenges

A backplane system groups a number of electrical PCBs (e.g. daughter boards) through a number of backplane connectors, which are placed in parallel on a backplane board, as illustrated in Figure 2.1. A backplane is commonly used as a backbone in routers or network switches in servers and network attached storage arrays, to realize high-speed communcation between several PCBs. In addtion, cable backplanes using coaxial cables are recently employed as an alternative for traditional PCB backplanes, due to its advantages of lower loss and higher flexibility. In this work, we mainly focused on the conventional backplane concepts using PCB traces as signal paths.

2.2.1 Backplane channel

A typical backplane system is depicted in Figure 2.1, showing two daughter cards (DC) and one backplane board (BP). The DCs are plugged into the BP, by using through-hole backplane connectors. One DC receives the electrical / optical signals from external networks or external equipment, and sends the signal to the other DC via the backplane system. As presented in Figure 2.1, the transceiver chips are mounted in packages and located on the DCs, with one chip on each side. Therefore, a full signal path over the backplane channel from one chip to the other chip is generated. The backplane channel consists of the traces on two DCs, the trace on the BP as well as two backplane connectors.

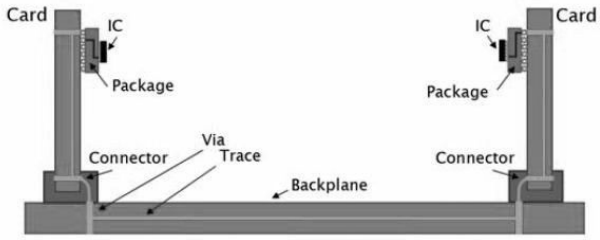
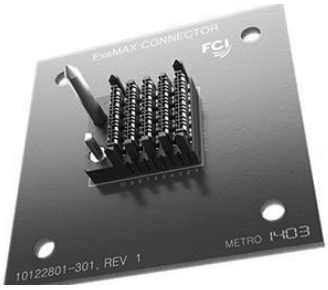


Figure 2.1: A typical backplane system [7]

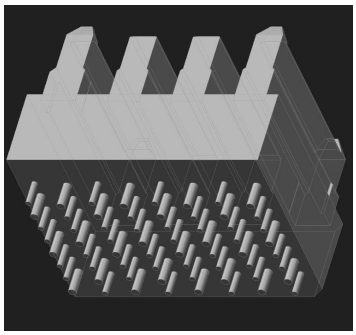
2.2.2 Bandwidth limitation

At the start of this research, industrial backplane connectors, such as manufactured by e.g. FCI or TE connectivity, had operational capabilities up to 25 Gb/s. The FCI ExaMAX® connector is depicted in Figure 2.2 and Figure 2.3. [9] shows that it is possible to transmit a serial 25 Gb/s signal over a 17 inch copper backplane including two ExaMAX® connectors.

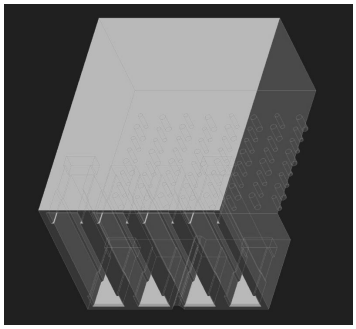
Header



Receptacle



3D view of the header



3D view of the receptacle

Figure 2.2: FCI ExaMAX® backplane connector [8]

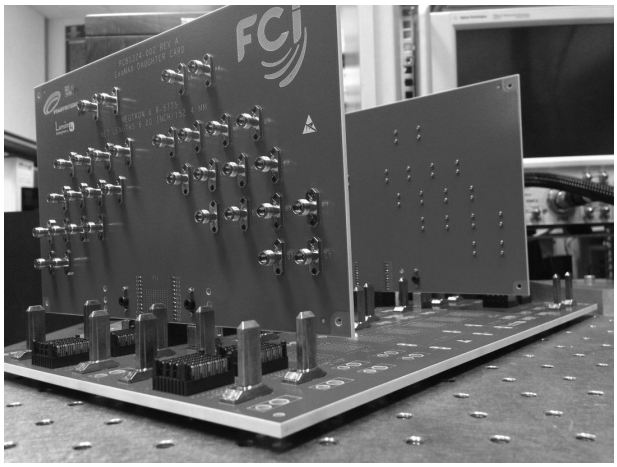


Figure 2.3: FCI ExaMAX® backplane

Figure 2.4 elaborates our measurement results of a 17 inch long ExaMAX® backplane channel, including a 5 inch BP and two 6 inch DCs.

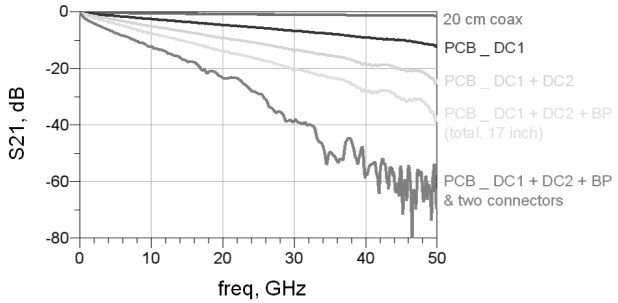
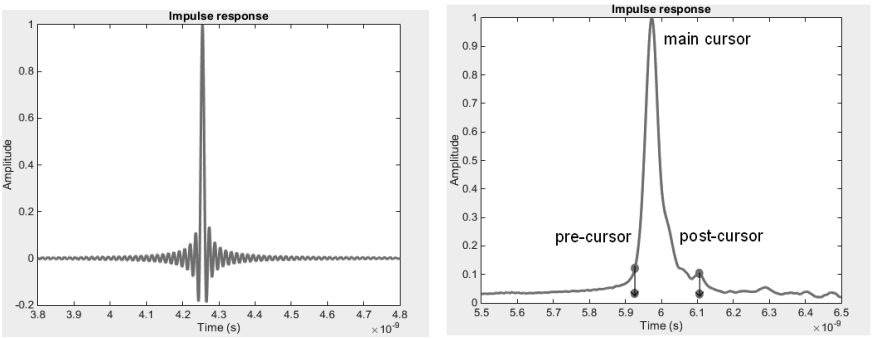


Figure 2.4: Measured loss of a FCI ExaMAX® backplane

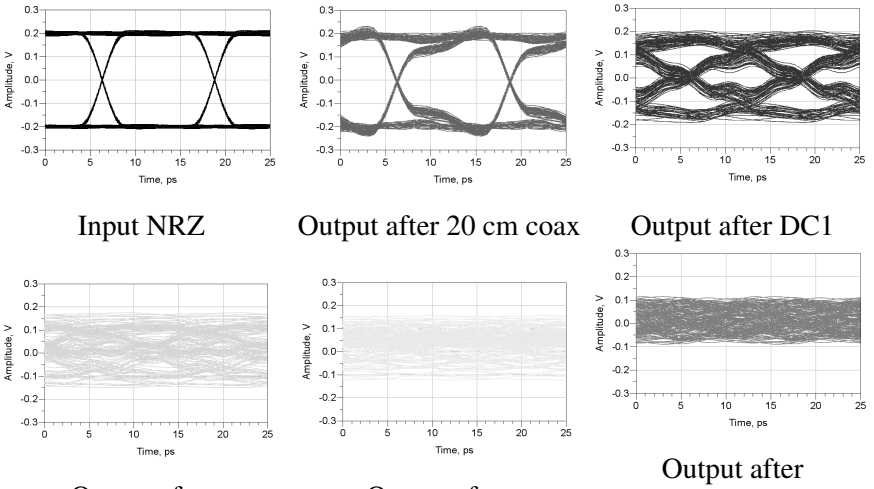
The impulse response, shown in Figure 2.5, of a 17 inch (around 43 cm) ExaMAX® channel, extended with 20 cm coax test cables, is calculated from the frequency response shown in Figure 2.4. The impulse response of the ExaMAX® channel is clearly broadened due to the limited BW of the channel, resulting in pre- and post-cursors.
Transmitting a serial 80 Gb/s non-return-to-zero (NRZ) signal without equalization over the 17 inch ExaMAX® backplane demonstrator provides the output eye diagrams shown in Figure 2.6. It is clear that, due to the BW limitation, the output eye diagrams are totally closed when operating the ExaMAX® backplane demonstrator at 80 Gb/s. This result indicates that the performance of currently available backplane channels needs to be im-



20 cm coax 43 cm FCI ExaMAX® backplane

Figure 2.5: Impulse response of a FCI ExaMAX® backplane

proved, in order to enhance the serial data rate. Such improvements are underway in the form of e.g. cable backplanes or orthogonal backplane connections [10].



Input NRZ Output after 20 cm coax Output after DC1

Output after DC1 + DC2 Output after DC1 + DC2 + BP Output after DC1 + DC2 + BP & two connectors

Figure 2.6: 80 Gb/s NRZ signal transmission over different sections of a commercial ExaMAX® backplane without equalization

As shown in Figure 2.4, the performance of the backplane channel is mainly limited by the BW of the backplane connector, and the slope of the channel insertion loss that is mainly attributed to the trace length and dielectric ma-

terial. Meanwhile, there are several notches in the frequency response due to the impedance mismatch from the routing geometries and the connector via holes. All those BW-limiting effects need to be minimized in order to realize high speed signal transmission. In high speed backplane applications, as the channels have low-pass filter characteristics, a perfect narrow pulse transmitted at the input of the channel is greatly attenuated in amplitude and the received pulse becomes much wider at the channel output, with several pre- and post-cursors around the main cursor caused by pulse dispersion and the low-pass filter characteristics. In the meantime, due to the reflections caused by impedance discontinuities, ripples can be found in the received waveform at the output of the backplane link. Each of those effects degrades the quality of the signal transmission by increasing the ISI and this makes it increasingly difficult for the RX to recover the transmitted bit sequences. For the same link, the time-domain response of a pulse with the same width is deterministic, and the ISI effect will become worse at higher data rate as the period of the transmitted signal decreases. Therefore, ISI is one of the dominant factors that limit the maximum achievable data rate over a high speed backplane channel. In this work, the bottlenecks for transmitting a high speed signal over a copper backplane system are investigated, so that an appropriate solution for these bottlenecks will be generated.

2.2.3 Backplane implementation

As mentioned above, a backplane signal is generated on one DC (with a TX chip) and travels along a number of PCB traces in order to arrive at the other DC (with a RX chip). The frequency-dependent losses of the PCB traces introduce signal attenuation. In the meantime, the parasitics introduced from the connectors, together with the termination resistors of the channel, generate a low-pass filter and further reduce the BW of the backplane link. All those effects introduce signal ISI and degrade the signal transmission performance, especially at high frequencies.

Therefore, in order to achieve high speed data communication between transceiver chips, the frequency response of the whole backplane channel needs to be evaluated and each part of the backplane channel needs to be modelled and included in simulations. In the following parts, the characteristics of backplane traces and connectors are briefly illustrated.

2.2.3.1 Transmission line traces

The frequency-dependent attenuation of backplane traces is mainly due to conductor losses and dielectric losses. At high frequencies, due to skin effect, the current flows along the edge of the metal trace, which reduces the actual metal cross section. Therefore, the resistance and conductor loss of a TML increases with frequency. Dielectric loss is another dominant factor which determines the total TML losses. In high speed applications a PCB designed with a low loss tangent (tan δ) material is preferred due to its lower loss at high frequencies. Besides the materials used in a TML, the configuration of the TML also plays a considerable role with respect to performance.

There are several types of TMLs that can be used as transmission path to convey electromagnetic waves or high speed signals at radio frequencies, such as: micro-strips, striplines, coplanar waveguides (CPW) and coaxial lines. Taking the physical structures and dimensions of backplane systems into account, micro-strips and striplines are the two most common TML structures in backplane links [11]. Compared to micro-strips, striplines always offer larger BW and higher isolation, so lower crosstalk between adjacent traces. Meanwhile, due to the sandwiched structure of striplines, with a strip conductor located between a pair of groundplanes, the capacitance per meter is higher (compared to microstrips) so that a stripline PCB is always much thicker for a given impedance (such as 50 Ω) and the strip width is smaller (compared to microstrips), so closer to fabrication constraints. Therefore, it is harder and more expensive to manufacture a stripline PCB than a micro-strip PCB. However, in general, thanks to its better performance, it is recommended to implement high-speed backplane links with striplines [12]. In Table 2.1 the parameters of the most commonly used materials are elaborated. FR-4 is commonly used in low cost PCB design. However, it has a high frequency-dependent loss. Therefore, for high speed board design, other materials with lower dielectric loss are considered [9]. As presented in Table 2.1, compared to FR-4, the RO4000 series and Megtron6 have a lower dielectric loss. For instance, currently Megtron6 is commonly used in high speed BPs [16] [17]. However, Megtron6 is much more expensive than FR-4 [18] [19]. Therefore, people are trying to find alternative materials, with a better performance-cost ratio. As shown in Table 2.1, FX-2 has a lower frequency-dependent loss than Nelco 4000-13 and a comparable loss as Megtron6. Therefore, it has been accepted as an alternative material for high frequency signal traces [20] [21].

	Dielectric constant (Dk)	Dielectric loss (Df)
FR-4	4.4	0.02@ 1 GHz
RO4003 [13]	3.38	0.0027@ 10 GHz
RO4350 [13]	3.48	0.0037@ 10 GHz
Megtron6 [14]	3.4	0.002@ 1 GHz
Nelco 4000-13	3.7	0.01@ 1 GHz
FX-2 [15]	3.44	0.0015@ 1 GHz

Table 2.1: Materials parameters

For our measurements, FX-2 striplines were chosen as the BP traces. In order to evaluate the PCB traces performance, several FX-2 striplines are fabricated and the losses of different lengths are measured and presented in Figure 2.7.

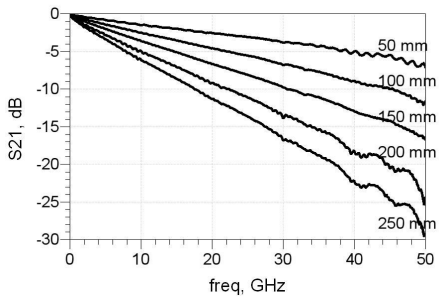


Figure 2.7: Measured loss of FX-2 PCB striplines

2.2.3.2 Backplane connectors

High speed backplane connectors for data rates beyond 40 Gb/s are very challenging to develop. Also the connector to board transition and the assiciated via holes or stubs are very critical to optimize, as depicted in Figure 2.2. In [22], it has been identified that backplane via stubs introduce capacitances and behave as a low pass filter (LPF). Due to the intrinsic and complex physical nature, increasing the BW of via holes is one of the most critical challenges. In the meantime, backplane via stubs are one of the main sources of frequency selective reflections. For example, a stub as short as one mm, may introduce unacceptable impedance discontinuities

and mismatch, and cause signal reflection or resonances in the frequency range of interest, which greatly degrade the signal transmission quality. Thus, in order to minimize the noise caused by the reflections, an optimal footprint design between the connector and board termination becomes very improtant, in combination with via backdrilling. In addition, at high frequencies, every small detail of the connectors becomes important. For example, the skew between the lanes in each differential pair needs to be compensated in the connector design. Resonances on ground pins / structures caused by standing waves need to be avoided as well. All these details need to be considered in order to increase the BW of backplane connectors and backplane links. In addition, the crosstalk between the channels needs to be minimized as well, in order to realize parallel multi-channel signal transmission in the backplane [23].

After understanding the physical phenomena and the related design details, we are aware of the main bottlenecks that limit the BW of backplane connectors in backplane systems. By applying an optimal combination of connector footprints with less parasitics, an improved impedance matching of via holes / stubs, together with a reduced coupling between different channels, the capacity of backplane connectors will be pushed higher by connector manufacturers and backplane system designers.

In our measurements, a test structure consisting of an improved backplane connector (provided by FCI) and two 5 cm, FX-2 differential striplines is evaluated. Figure 2.8 and Figure 2.9 illustrate the measurement setup and measurement results respectively.

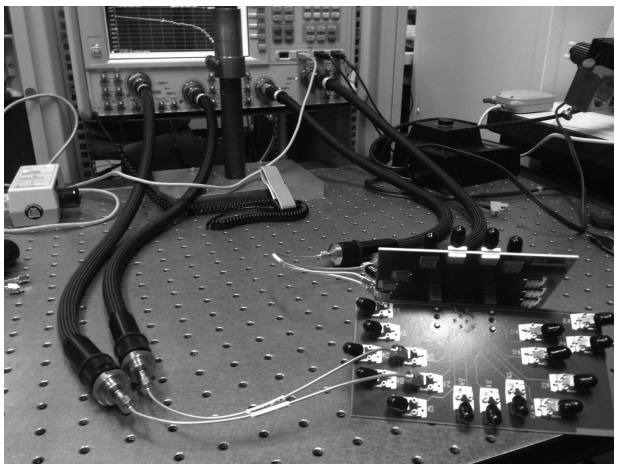


Figure 2.8: Measurement setup of the FCI backplane connector

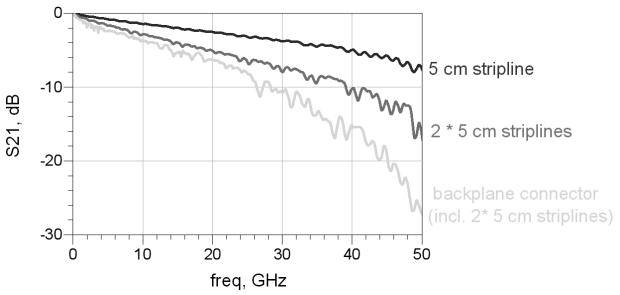


Figure 2.9: Frequency response of the FCI prototype backplane connector

2.2.4 Prototype backplane

Next to the frequency response measurements on the ExaMAX® backplane demonstrator, which was depicted in Figure 2.4, we also measured a prototype backplane channel using the FX-2 PCB traces and one backplane connector. As shown in Figure 2.10, this backplane connector was looped back twice (using cable 1) to emulate a backplane, consisting of DC traces, two backplane connectors as well as BP traces.

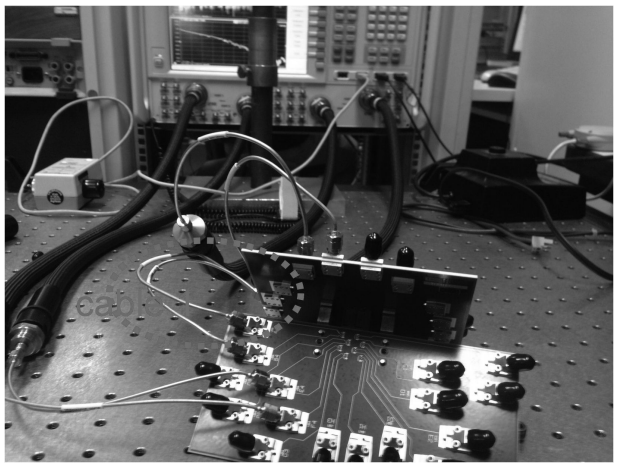


Figure 2.10: FCI prototype backplane

As illustrated in Figure 2.11, the total loss of the prototype backplane (including three 20 cm coax cables) is around 25 dB at 30 GHz. Compared to the commercial ExaMAX® backplane demonstrator, the prototype channel has a much lower loss, less ripple and broader BW.

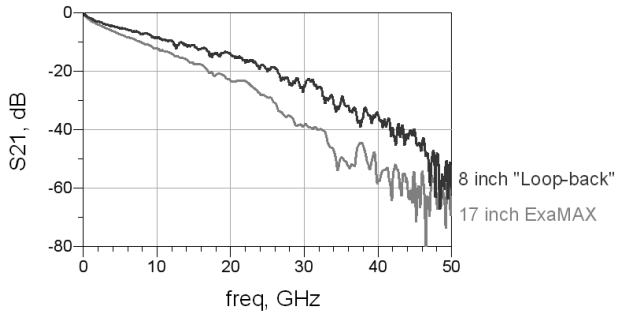


Figure 2.11: Frequency response of the FCI prototype backplane

2.3 Transmitter design challenges

2.3.1 Overview

Data rates beyond 40 Gb/s per lane require a high BW across the electrical channel. Meanwhile, the increased data rate faces higher attenuation as well as ISI caused by the lossy TML traces and backplane connectors. These degrading effects become much more pronounced at higher frequencies as they scale more than linearly with frequency. As a result, the received data waveforms can be significantly distorted after travelling through PCB interconnects and backplane connectors. Therefore, an equalizer compensates the channel by attenuating the low-frequency content of the input signals with respect to the higher frequencies, in such a way that the resulting spectrum after the channel seems unaffected.

Ideally, the equalizer implements the inverse function of the channel, so that the combined transfer function is flat. In this way, equalizers overcome the low-pass frequency response of the channel, effectively extending the useful BW. At the same time, due to the fact that the loss characteristics of the backplane channels are quite different depending on the trace lengths and the board materials, the channel equalization needs to be adaptive [5]. Therefore, in high-speed backplane transmission design, there are always trade-offs among the channel performance, the signal transmission rate and equalizer complexity.

In various communication systems with < 10 Gb/s throughput, such as G.fast or WiFi, one finds complex modulation and complex signal processing schemes to approach the Shannon capacity of the link [24]. However, for high-speed links, especially for electrical backplane systems operating beyond 40 Gb/s, due to the speed limitations of digital-to-analog converters (DAC) or analog-to-digital converters (ADC), it is impractical to im-

port the same complicated signal processing algorithms into the transceiver chips with current IC technology, without introducing unacceptable circuit complexity, latency and power consumption. Therefore, in ultra-high speed transmission links, in order to compensate the channel loss and to reduce ISI for an improved signal transmission quality, some simpler signal processing techniques, such as analog equalization and multi-level modulation, need to be considered, which are easier to realize and to implement on chip.

2.3.2 Equalizer functions

If the data rate of a signal is higher than two times the BW of a channel, the signal quality degrades, generating unwanted phenomena, such as reduced-eye opening, jitter and ISI.
Such BW limitations can be overcome with an equalizer located at the TX or the RX. For example, when a data source sends a signal to an equalizer, the equalizer can introduce predistortion in the signal such that the signal output from a channel located after the equalizer is essentially unchanged with respect to the signal output from the data source. In other words, the equalizer acts as a filter that implements the inverse characteristic of the channel so that the usable frequency range is extended for high data rate signals. Feed-forward equalizers (FFE), decision-feedback equalizers (DFE) and continuous time linear equalizers (CTLE) are three kinds of equalizers which are commonly used in electrical data transmission systems.

2.3.2.1 Feed-forward Equalizer (FFE)

In a high speed electrical transmission link, it is common to implement an FFE, or more specifically, a finite impulse response (FIR) filter in the transceiver, to perform signal equalization. The simplest FFE structure is a 2-tap FFE, whose conventional implementation is shown in Figure 2.12 [25].
As shown in Figure 2.12, the FFE consists of two variable gain cells (C_0 and C_1) and one delay element (z^{-1}). The output of the 2-tap FFE, is given by the weighted sum of the current and the previous bit, as expressed in equation (2.1), where a_i represents the amplification of the gain cell C_i:

$$y(n) = a_0 \cdot x(n) + a_1 \cdot x(n-1) \tag{2.1}$$

Figure 2.13 illustrates the 2-tap FFE operation with some example waveforms. As shown in Figure 2.13, with certain tap weights, the FFE can boost the output signal for alternating input bits (1, -1 or -1, 1), thus ”emphasizing” the high-frequency components in the input sequence. The lower-

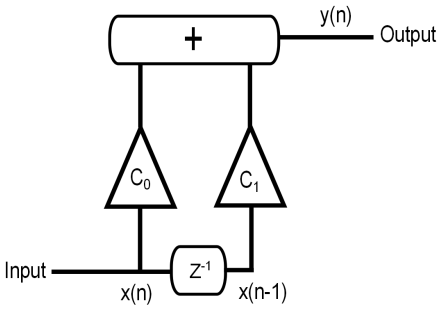


Figure 2.12: Conventional 2-Tap FFE topology

frequency components, associated with consecutive identical input bits, experience a lower gain in this example. Using this configuration, the FFE generates a so-called pre-emphasis on the input signal, effectively compensating the high-frequency loss of the transmission channel, to improve the signal integrity and to reduce ISI.

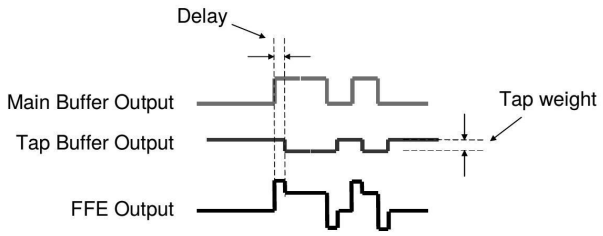


Figure 2.13: Output waveforms of a 2-Tap FFE [26]

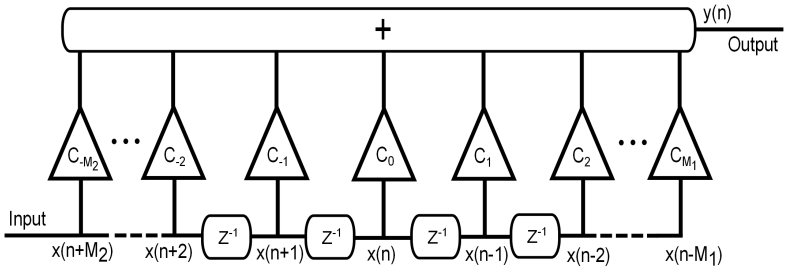


Figure 2.14: M-Tap FFE topology

Figure 2.14 presents a more general M-tap FFE topology, extended from the 2-tap FFE example. As shown in Figure 2.14, the FFE consists of M

gain cells and M-1 delay elements. By adding up delayed, weighted bits to the current bit, the output of the M-tap FFE is expressed in equations (2.2) and (2.3), where a_i represents the amplification of the gain cell C_i:

$$y_n = \underbrace{a_0 \cdot x(n)}_{\text{(main cursor)}} + \sum_{i=1}^{M_1} \underbrace{a_i \cdot x(n-i)}_{\text{(post-cursors)}} + \sum_{j=1}^{M_2} \underbrace{a_{-j} \cdot x(n+j)}_{\text{(pre-cursors)}} \tag{2.2}$$

$$M = M_1 + M_2 + 1 \tag{2.3}$$

To successfully apply an FFE in a data transmission link, the M taps of the FFE need to be correctly weighted and summed, so that pre- and post-cursors ISI introduced by a given channel can be eliminated. Meanwhile, the tap weight and tap sign need to be tunable, in order to be adaptive for different application targets, such as: channel characteristics and data rates. Because of its relatively modest design complexity and power consumption, previous publications about electrical backplane links typically employed a digitally controlled FFE based on a FIR filter to compensate the channel loss and to enhance the data rate with adjustable equalization techniques [2] [6] [27]. Table 2.2 illustrates an overview of the reported FFE implementations beyond 40 Gb/s.

Ref.	[27]	[28]	[29]
Process	180 nm SiGe	65 nm CMOS	65 nm CMOS
Topology	7-tap FFE	4-tap FFE	7-tap FFE
Data rate	49 Gb/s	64 Gb/s	40 Gb/s
Power	750 mW	78 mW	80 mW
Power / Data Rate	15.3 pJ/bit	1.2 pJ/bit	2 pJ/bit

Table 2.2: An overview of reported FFEs beyond 40 Gb/s

2.3.2.2 Decision-feedback Equalizer (DFE)

Unlike an FFE which generates a linear FIR filter to equalize the actual transmitted signal waveform, a DFE makes use of logical decisions on previously received symbol bits to predict the channel response and to estimate the signal ISI in the current symbol bit.
In Figure 2.15, a typical signal with strong ISI is shown, resulting in digital decision errors [26].

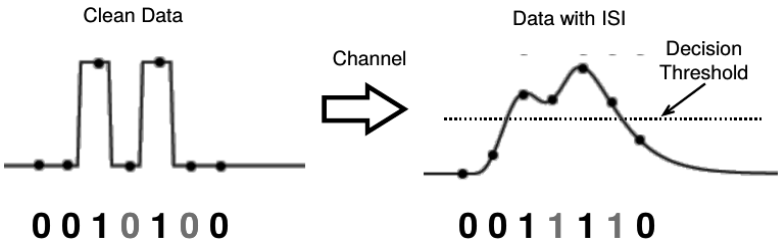


Figure 2.15: A digital signal degraded by ISI causing bit errors

As illustrated in Figure 2.15, severe ISI leads to signal tails from earlier bits overlapping with the following bits, which inevitably results in decision errors when applying a static decision threshold. Therefore, in order to make correct decision, the threshold of a DFE is dynamically adjusted, depending on the data history. For example, as depicted in Figure 2.16, when the previous bits were 1 and 1, then the threshold moves up; on the other hand, when the previous bits were 0 and 0, then the threshold moves down. In such way, the effective tails of the earlier bits are "compensated", and the influence on the decision of the following bits is greatly mitigated [30]. As such, the equalization function of DFEs is quite different from that of FFEs, which pre-emphasizes data transitions such that the static decision threshold would still work.

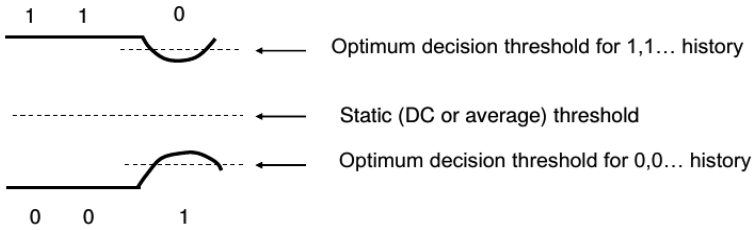


Figure 2.16: Basic DFE function to eliminate errors

The typical topology of an M-tap DFE is depicted in Figure 2.17. As shown in Figure 2.17, an M-tap DFE consists of M variable gain cells, M-1 delay elements and a comparator, forming a feedback loop [26]. The output of an M-tap DFE is expressed in equation (2.4), where a_i represents the amplification of the gain cell C_i:

$$y_d(n) = y(n) + \sum_{i=1}^{M} a_i \cdot sgn\{y_d(n-i+1)\} \tag{2.4}$$

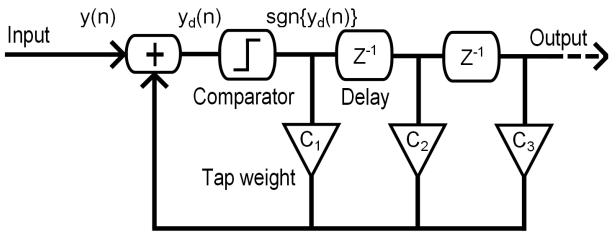


Figure 2.17: M-Tap DFE topology

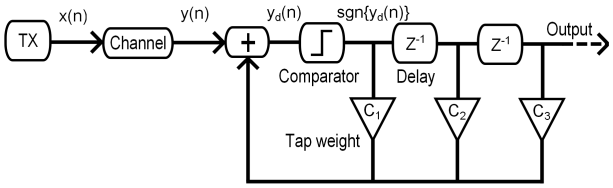


Figure 2.18: An electrical link employing an M-tap DFE

Depending on previous bit values (using earlier decisions), the threshold of the comparator is dynamically moved up or down, to obtain an updated optimum decision threshold and to mitigate digital errors. Therefore, employing a DFE in a electrical link (shown in Figure 2.18), the ISI of the output signals is greatly eliminated. For error-free DFE operation, the comparator decisions can be written as:

$$sgn\{y_d(n)\} = x(n) \tag{2.5}$$

Unlike FFEs, in DFEs there is no BW boost at high frequencies. Therefore, DFEs do not amplify (high-frequency) noise or crosstalk, which is an advantage over FFEs. However, compared to FFEs, there are several disadvantages for DFEs. First of all, as the DFE feedback loop including signal multiplication, summation, comparison and delay operations needs to close in one UI, the circuit design of a high-speed DFE (beyond 40 Gb/s, UI below 25 ps) becomes very challenging [30]. Second, a DFE cannot remove the pre-cursor ISI, but only the post-cursor ISI. In addition, the DFE architecture is a lot more complicated than the FFE architecture. E.g. a DFE requires an optimum decision threshold which needs to move up or down depending on the data history, leading to increased design complexity and power consumption [30]. Last but not least, as a DFE determines the decision threshold and logic value of the currently received bit mainly based on the logical decision of the previously transmitted bits, the decision errors on the previous bits will propagate and affect the accuracy of the logical

decision for the current bit.

DFEs have been commonly applied in digital communication systems and mixed signal implementations, due to their advantages of lower noise amplification and lower noise propagation compared to FFEs. However, in a high speed electrical link beyond 40 Gb/s, a DFE has considerable drawbacks on the circuit implementation complexity and power consumption. Nowadays, in many industrial high-speed link implementations, both FFEs and DFEs are applied, to remove both pre- and post-cursors ISI effectively, e.g. an FFE is implemented in the TX and a DFE is implemented in the RX. An overview of the recently reported DFE implementations is illustrated in Table 2.3.

Ref.	[30]	[31]	[32]
Process	130 nm SiGe	90 nm CMOS	90 nm CMOS
Topology	1-tap DFE	4-tap DFE	1-tap DFE
Data rate	80 Gb/s	18 Gb/s	19 Gb/s
Power	4000 mW	100.2 mW	38 mW
Power / Data Rate	50 pJ/bit	5.6 pJ/bit	2 pJ/bit

Table 2.3: An overview of recently reported DFEs

2.3.2.3 Continuous time linear equalizer (CTLE)

CTLE is also a common technique, to compensate the frequency-dependent channel loss and to improve the signal integrity. Unlike a DFE that achieves equalization with discrete-time signals in a digital way, a CTLE realizes equalization in an analog way. Similar to FFEs, the basic concept of equalization using a CTLE is to pre-emphasize input signals by generating some kind of shaping on the transmission link, to reverse the channel frequency response and to remove signal ISI [33].

CTLEs can be implemented in a purely passive way using only resistors, inductors and capacitors, or in an active way e.g. applying differential amplifiers with CTLE. In electrical backplane transmission systems, CTLEs are commonly implemented with a high-pass transfer function as the channel typically has a LPF characteristic. A typical passive CTLE topology using resistors and capacitors is depicted in Figure 2.19 [26].

The transfer function of this CTLE circuit is defined in equation (2.6):

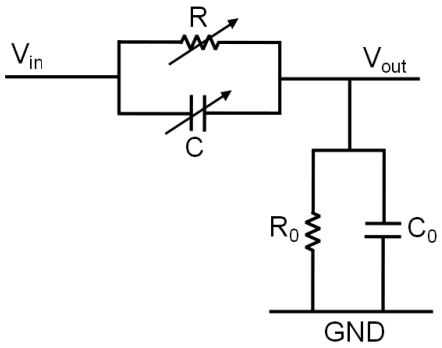


Figure 2.19: A typical passive CTLE topology

$$A_v(s) = \frac{R \cdot (1 + s \cdot R_0 \cdot C_0)}{R + R_0 + s \cdot R \cdot R_0 \cdot (C + C_0)} \tag{2.6}$$

As illustrated in equation (2.6), the resistors R and R_0 (load resistor) determine the low-frequency loss, and the capacitors C and C_0 (load capacitance) determine the high-frequency loss. Therefore, by adding a tunable R/C network, the low-frequency components of the R_0/C_0 network are reduced by the R-R_0 divider, while the high-frequency components are enhanced by the C-C_0 divider. In this way, the transfer function can be flattened over frequency.

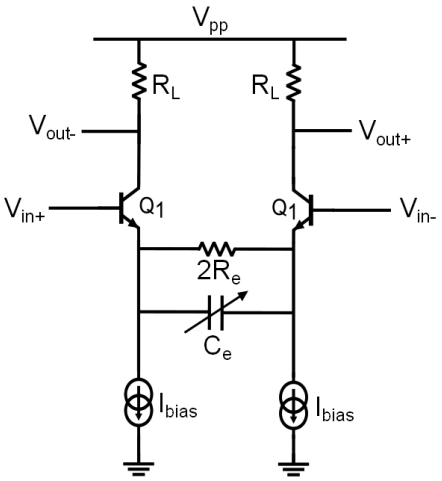


Figure 2.20: A typical active CTLE employing amplifiers

Figure 2.20 shows an example of a typical active CTLE, consisting of an

amplifier with a high-frequency boost. The voltage gain of the differential amplifier as a function of frequency is given by equation (2.7):

$$A_v(s) = g_m{}' \cdot R_L = \frac{g_m \cdot R_L}{1 + g_m \cdot \frac{R_e}{1+s \cdot R_e \cdot 2C_e}} \tag{2.7}$$

As shown in equation (2.7), the DC gain is defined by R_L and R_e. At high frequencies, C_e reduces the degeneration impedance, hence improving the effective $g_m{}'$ and enlarging the BW. Therefore, the digitally controlled C_e generates tunable frequency-domain peaking to reshape the channel response.

Compared to an FFE or a DFE, a passive CTLE has the advantage of low cost and low power consumption, while it provides very good linearity. An active CTLE (e.g. with R-C degeneration) typically provides a high pass transfer function with a certain frequency peaking, to "convert" channel LPF characteristics. Therefore, the relative location of the zeros and poles in the amplifier determines the magnitude and the peaking frequency. By tuning the amplifier parameters (e.g. R_e and C_e in Figure 2.20), the peaking and DC gain are controlled, to adapt to different channel characteristics. For high-speed electrical systems beyond 20 Gb/s, however, the channel complexity varies greatly, from a simple chip-to-chip interconnect to a complicated backplane channel with long PCB traces and connectors. Running at such serial data rates on those complex interface applications, the signal quality is greatly degraded, making it almost impossible to guarantee sufficient signal margins with a equalization process like CTLEs [34]. Therefore, in most 10G+ serial backplane links, CTLEs are implemented in combination with other types of equalizers (e.g. FFEs or DFEs), to equalize the channel response and to improve the signal integrity [33]- [36]. An overview of the recently reported CTLEs implemented together with FFEs or DFEs is illustrated in Table 2.4.

Ref.	[33]	[35]	[36]
Process	28 nm CMOS	90 nm CMOS	65 nm CMOS
Topology	CTLE + 2-tap DFE	CTLE+ 1-tap DFE	CTLE + 1-tap DFE
Data rate	32 Gb/s	20 Gb/s	21 Gb/s
Power	240 mW	40 mW	34.2 mW
Power / Data Rate	7.5 pJ/bit	2 pJ/bit	1.63 pJ/bit

Table 2.4: An overview of recently reported CTLEs

2.3.2.4 Conclusion

A summary of the advantages / disadvantages of FFEs, DFEs and CTLEs in terms of equalization capability and circuit implementation is listed in Table 2.5.

	FFE	DFE	CTLE
Equalization	On actual waveform	On previous decision	On actual waveform
ISI cancellation	Pre- and post-cursors	Only post-cursors	Pre- and post-cursors
Error propagation	No	Yes	No
Noise propagation	Yes	No	Yes
Circuit implementation	Adaptive FIR filter	Feedback loop	RCL or active circuit
Power consumption	Low	High	Very low

Table 2.5: A general comparison of FFEs, DFEs and CTLEs

As presented in Table 2.5, FFEs have the advantages of circumventing the error propagation problem and contributing less power consumption for the same number of taps, while DFEs have the advantages of lower noise amplification and propagation. Meanwhile, FFEs outperform DFEs in terms of circuit implementation complexity for high-speed links. For example, the delay element in a FIR filter is related with the symbol period, whose implementation complexity could be low by using passive delay lines. However, in DFEs, the timing requirement must be met for all feedback paths, which have to complete within one symbol period to ensure accurate ISI cancellation [25]. Therefore, the circuit complexity of DFEs is unavoidably increasing with frequency.
Backplane channels with a “smooth” (low ripple, no notches) frequency response, can be equalized with only FFEs and / or CTLEs, with the gentle roll-off of the channel being compensated by reducing the DC swing and boosting the high-frequency components with pre-emphasis. However, for certain channel characteristics, DFEs outperform FFEs and CTLEs. For example, a channel containing notches cannot be precisely resolved solely by linear equalization techniques, as no amount of boost is sufficiently strong in power to be received at the notch frequency. In such cases, a feedback circuit such as a DFE is required. In this work, after a comprehensive consideration of the expected backplane channel performance, the FFE topology has been selected to perform the signal equalization bacause of its capabilities, implementation complexity and power consumption.

2.3.3 Transmitter topology

The proposed TX topology is depicted in Figure 2.21.

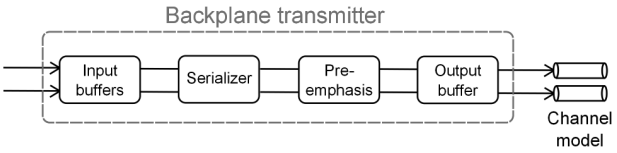


Figure 2.21: Transmitter topology

As digital chips, e.g. FPGAs, are limited in interface speed (e.g. 25 Gb/s already requires FPGAs with special transceiver blocks), a serializer combining several input signals is needed to feed the high-speed FFE in the TX. As commercial multiplexers (MUX) operating beyond 80 Gb/s are, unfortunately, very expensive ($>$ 10k euros) and power hungry (around 5 W for the 80 Gb/s Micram MUX shown in [37]), an on-chip MUX, developed by my colleague dr. Zhisheng Li, is integrated in the TX. To overcome the BW limitation of the backplane channel located between the TX and RX, an FFE preceding the channel introduces predistortion and reshapes the input signal, so that after the channel the RX captures a reasonably clean signal.

2.4 Modulation

In a high speed electrical link, in addition to the signal equalization, an effective modulation scheme is also necessary in order to improve the BW efficiency of the backplane channel. Apart from NRZ, which is a simple two-level modulation scheme, partial response multi-level modulation, pulse amplitude modulation (PAM), quadrature amplitude modulation (QAM) and orthogonal frequency-division multiplexing (OFDM) have also been extensively applied in communication systems to transmit high data rate signals over band-limited channels. Advanced modulation techniques improve the spectral efficiency. On the other hand, they increase the circuit complexity [22]. In this research, we encountered different factors limiting the performance, such as the realizable length of an equalizer filter, the sensitivity of the RX circuit as well as the related overall power consumption of the TX and the RX. Therefore, the selection of the modulation scheme is very much depending on the feasibility of the transceiver that implements the modulation scheme, and on the expected useful BW of the channel, including connectors.

2.4.1 Modulation techniques

The most advanced schemes, such as OFDM, require very high speed ADCs and DACs. However, as presented in Table 2.6, they are power hungry. Moreover, digital signal processing of such high-speed signal formats also consumes hundreds of mWs.

Ref.	Technology	Sampling rate (GS/s)	Resolution (Bit)	Input BW (GHz)	Power (W)
Fujitsu ADC [38]	40 nm CMOS	55-65	8	20	1.2
IBM ADC [39]	32 nm SOI CMOS	90	8	19.9	0.667
NTT DAC [40]	0.5 µm InP HBT	60	6	-	1.8

Table 2.6: High-BW ADCs and DACs

Therefore, in this work, considering the very high bit rate requirements, low-complexity modulation schemes were investigated, as these can be implemented without DACs and ADCs, with a reasonable design complexity. However, low-complexity schemes are spectrally less efficient, thus requiring sufficient bandwidth after equalization, making the circuit design very challenging again.
First, NRZ, as a very simple and well understood modulation format, is investigated. Second, a partial response technique, duobinary, presents a little increase on circuit complexity over NRZ but requires only around half of the BW, and is therefore a promising candidate. In addition, PAM-4, as an another alternative, transmits two bits in one single symbol. So PAM-4 also reduces the required BW by half but with a higher implementation complexity compared to NRZ [5]. All of the above-mentioned modulation formats are investigated in this section, in order to verify how well the spectral properties of these modulation techniques match the expected channel characteristics.

2.4.1.1 NRZ

As shown in Figure 2.22, non-return-to-zero on/off keying (NRZ-OOK) is a very simple two-level modulation format. As a very basic amplitude modulation (AM) scheme, it has been popularly utilized in electrical interconnects. Due to the simplicity of the transceiver logic, NRZ is still the most widely adopted modulation format in backplane transmission systems. In addition, as only two levels are involved in the signal, the spacing or open-

ing between the two levels is of course at its maximum and higher compared to multi-level signals, as long as the system bandwidth is high enough with respect to the baud rate of course. Finally, only a single thresholder, which may be realized as a comparator, is necessary at the RX. Currently, most of the industrial backplane systems, employing NRZ, operate at serial data rates between 10 Gb/s and 25 Gb/s per lane, with a transmission distance of up to 1 m [41]- [43].

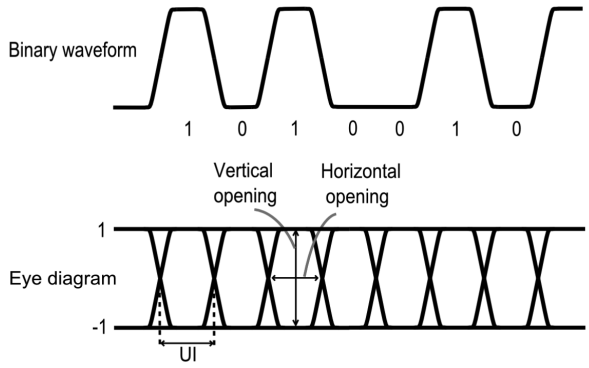


Figure 2.22: NRZ waveform and eye diagrams

The main disadvantage of the NRZ format is the higher spectral occupancy compared to advanced modulation formats. The NRZ spectrum is given by equation (2.8), where T represents the bit period [44]:

$$S_{NRZ}(f) = 10 \cdot log10(abs(sinc^2(T \cdot f))) \tag{2.8}$$

As depicted in Figure 2.23, the first spectral null of an NRZ signal is at the signal data rate frequency, and most of the signal power stays in the main lobe between 0 Hz and 70% of the data rate frequency. That means that in order to transmit an NRZ signal, a channel BW of more than 70% of the data rate is required. Therefore, the NRZ format faces a BW limitation at growing serial data rates in backplane systems. In conclusion, the signal attenuation at the highest frequencies, together with the impact of signal reflections, makes the channel equalization very complicated.

2.4.1.2 PAM-4

PAM operates on the principle of encoding multiple bits onto one of multiple levels in a single symbol, thereby reducing the signaling rate and required BW of the format. Recently, PAM-4 signaling has been applied in

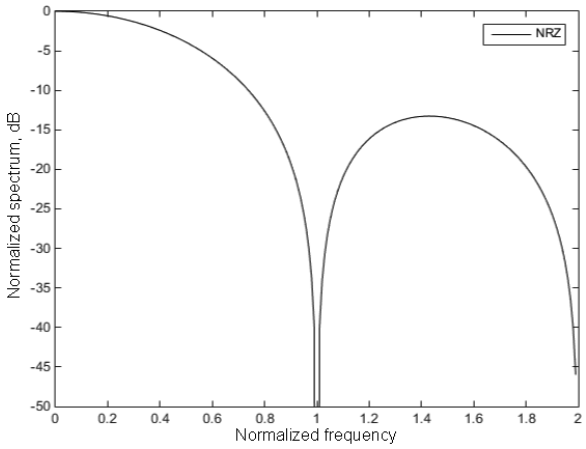


Figure 2.23: Spectrum of NRZ signals

high speed electrical links, in order to overcome the channel BW limitation [5] [6] [16]. As shown in Figure 2.24, PAM-4 signals consist of four levels, and the eye diagrams are a stack of three "NRZ eyes".

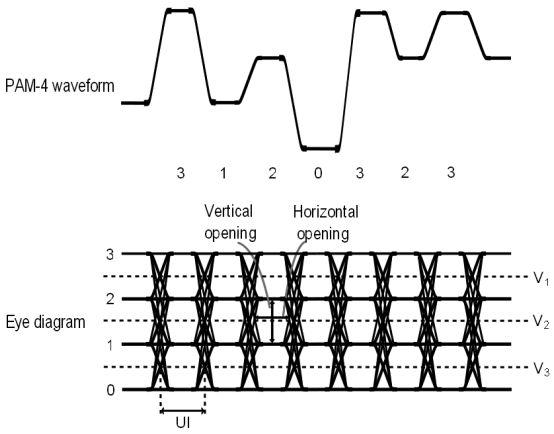


Figure 2.24: PAM-4 waveform and eye diagrams

The PAM-4 spectrum is given by equation (2.9), where T represents the bit period [44]:

$$S_{PAM-4}(f) = 10 \cdot log10(abs(sinc^2(2 \cdot T \cdot f))) \tag{2.9}$$

The spectrum of PAM-4 signals is illustrated in Figure 2.25.

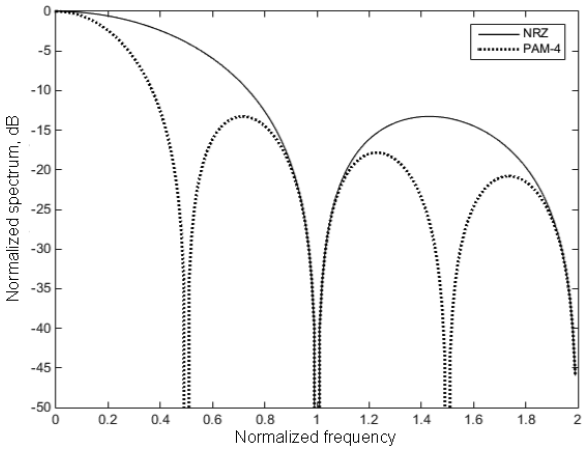


Figure 2.25: Spectrum of PAM-4 signals

By carrying two bits in each single symbol, PAM-4 reduces the required channel BW by 50%. Therefore, compared to two-level NRZ, PAM-4 applies four levels instead of two, and reduces the symbol rate, ending up with less ISI as the signal fits more efficiently into the available channel BW. Meanwhile, the signal-to-noise ratio (SNR) at the RX input, i.e. after equalization, needs to be 9.5 dB better than NRZ, in order to overcome the loss of the separation between the signal levels [16].

While reducing the symbol rate by half and relaxing the channel BW requirement, the multilevel nature of PAM-4 modulation leads to increased complexity of the transceiver [45]. First of all, the PAM-4 equalizer needs to be constructed from two parallel equalizer paths requiring twice the number of gain cells, one path for the MSB and one path for the LSB, followed by a summing block [46]. At the PAM-4 RX, multiple thresholders (V_1 to V_3 shown in Figure 2.24) are necessary to distinguish signal levels; Second, compared with a same speed, same voltage swing NRZ signal, a PAM-4 signal has only around 1/3rd of the vertical eye opening for each eye. Last but not least, the front ends of both the PAM-4 TX and RX require high linearity, to correctly map the multiple signal levels. The advantage of PAM-4 over NRZ, in terms of circuit complexity, is that the requirement on the serializer (depicted in Figure 2.21) is relaxed as the MSB and LSB are summed together instead of interleaving the bits at twice the speed. So, multiplexing multiple data streams to half-rate streams is sufficient in the case of PAM-4.

While having only 1/3rd of vertical eye opening compared to NRZ eyes

with the same voltage swing, PAM-4 has a wider horizontal eye opening due to smaller ISI. Meanwhile, considering the channel loss, the PAM-4 eyes will be attenuated less than the NRZ eye for the same bit rate, because the PAM-4 spectrum is at lower frequency. The main benefits of PAM-4 modulation stem from the fact that the BW requirements on the transceiver front-end as well as the channel between the TX and RX are relaxed compared to NRZ. However, on the other hand, the presence of multiple signal levels and transitions results in increased susceptibility to ISI and increased SNR requirements compared to NRZ modulation. To summarize, despite the disadvange of increased implementation complexity of the transceiver chips, PAM-4 modulation is a valuable alternative in high-speed electrical backplane transmission systems, where the available band-limited channels degrade the quality of high symbol rate modulation formats [41].

2.4.1.3 Duobinary

As one type of partial response techniques [47], duobinary signaling utilizes the available BW more efficiently than NRZ. The waveform and eye diagram of duobinary signals are illustrated in Figure 2.26.

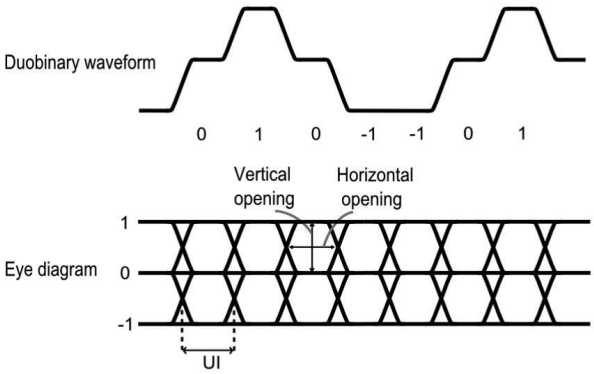


Figure 2.26: Duobinary waveform and eye diagrams

Mathematically, the duobinary signal is defined as the sum of the present bit and the previous bit in the binary data sequence, expressed in equation (2.10):

$$y[n] = x[n] + x[n-1] \tag{2.10}$$

The duobinary spectrum is given by equation (2.11), where T represents the bit period [44]:

$$S_{Duobinary}(f) = 10 \cdot log10(abs((sinc(T \cdot f) \cdot \frac{1 + exp(-j2\pi T \cdot f)}{2})^2)) \\ = S_{PAM-4}(f) \tag{2.11}$$

Figure 2.27 presents the spectrum of duobinary signals, where 90% of the signal power stays in the main lobe of a sinc function between 0 Hz and the half rate frequency [5]. Therefore, a channel BW close to 50% of the data rate is sufficient to implement a full speed duobinary front-end. Moreover, duobinary signaling can use the intrinsic BW limitation of the channel as part of the desired frequency response, reducing the stringent requirement of a more flattened response for the equalizer compared to NRZ [2]. Therefore, compared to NRZ modulation, the requirements for equalization in the case of duobinary modulation are much relaxed.

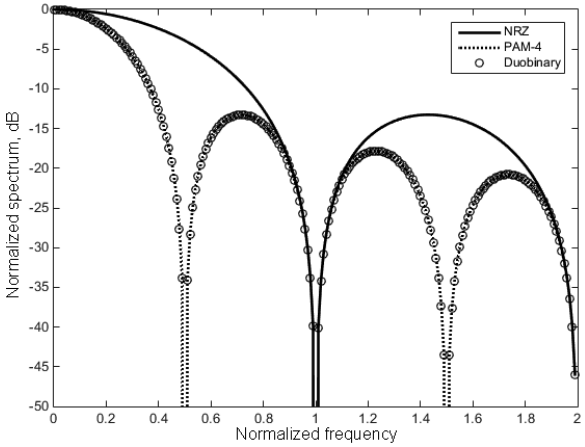


Figure 2.27: Spectrum of duobinary signals

The implementation of duobinary formats involves a bit more complexity in the transceiver design due to the need for a precoder and decoder operating at the line rate. The equalizer hardware is, however, less difficult compared to NRZ, while the link should show a certain linearity due to the three levels in duobinary signals. At the duobinary RX input, the SNR needs be at least 6 dB better than NRZ, in order to overcome the loss of the separation between the signal levels [44].
In conclusion, despite the disadvantage of increased implementation complexity of the transceiver chips, duobinary modulation becomes a very in-

teresting alternative due to its BW efficiency in high-speed electrical backplane transmission systems [2]- [6].

2.4.1.4 Polybinary

The concept of duobinary modulation can be extended to more than 3 levels as illustrated in [48]. Duobinary modulation is in fact a particular case of the family of polybinary signaling. Polybinary signals can have as many as M levels, as discussed in [49]. Polybinary modulation is a multilevel partial response technique in which the original binary symbols are first pre-coded and subsequently algebraically summed. Therefore, two consecutive elements in polybinary can differ in value by only one level. By mapping symbols in sequence into even and odd numbered levels, each digit in the resulting sequence can be independently detected despite its strong correlation property. Such sequence has the property that the information content becomes redistributed into lower frequencies.
A polybinary signal with five levels (M=5), provides a competitive advantage over duobinary, stemming from a reduced BW occupancy. Therefore, it becomes an interesting alternative for high-capacity backplane transmission systems [49]. In Figure 2.28, the waveform and eye diagram of a five-level polybinary signal are depicted [50].

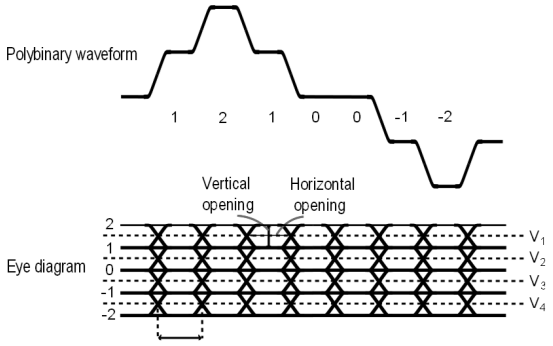


Figure 2.28: Five-level polybinary waveform and eye diagrams

The five-level polybinary spectrum is given by equation (2.12), where T represents the bit period [51]:

$$S_{Polybinary}(f) = 10 \cdot log10(abs(sinc^2(4 \cdot T \cdot f))) \tag{2.12}$$

The spectrum of five-level polybinary signals is illustrated in Figure 2.29. As shown in Figure 2.29, a channel BW up to 25% of the data rate is theoretically sufficient to implement a full speed polybinary front-end. Moreover, polybinary signaling can use the intrinsic BW limitation of the channel as part of the desired frequency response, reducing the BW requirements compared to duobinary modulation formats [48].

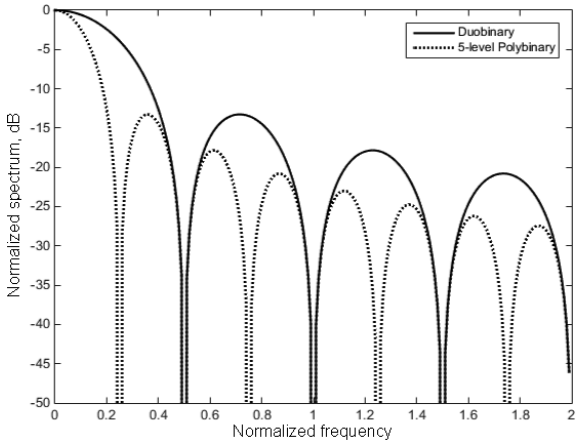


Figure 2.29: Spectrum of five-level polybinary signals

However, applying polybinary formats in backplane transmission systems leads to a higher complexity in circuit design. First of all, compared to duobinary and PAM-4 signaling, polybinary requires a higher SNR in the data transmission link, to correctly precode and decode the multi-level signal. Second, unlike PAM-4, although the frequency range occupied by polybinary formats is reduced, the operating symbol rate in the precoder and decoder is still the original line rate. Third, the multilevel nature of polybinary signals requires multiple thresholders in the polybinary RX to distinguish between multiple levels, requiring higher sensitivity. As a result, the improvements in signal performance achieved through narrower BW occupancy are reduced by the multi-level signal detection process [49]. In summary, polybinary signaling provides a technical solution to overcome band-limited, high-capacity backplane links, however requiring a significantly increased circuit design complexity or requiring an ADC with some digital signal processing (DSP) to extract the data [52]. In this work, taking high-speed electronics requirements and circuit design complexity into account, low-complexity modulation formats, such as NRZ, duobinary and PAM-4, were further investigated, in order to ensure the highest possibility to achieve a successful chip-level and system-level implementation.

2.4.2 Eye diagram simulations

As discussed before, NRZ, duobinary and PAM-4 are considered as the three most realistic modulation schemes in this research for ultra-high speed electrical backplane communication. NRZ is a simple and popular modulation format, due to the easy implementation and extensive compatibility. However, due to the severe BW limitation of the channel, a spectrally more efficient modulation format, such as duobinary or PAM-4, is preferred. In this part, eye diagram simulations and a comparison of the three modulation formats are presented to show the signal transmission along channels with different BWs. From the results, we can observe, for each type of modulation, how the output signals degrade with different band-limited channels. Meanwhile, a comparison of the transmission performance with the three modulation techniques can be concluded, based on the output signal quality after the same BW-limited channel for the same data rate of 80 Gb/s.
In the simulation, a Bessel filter with different 3 dB BWs is applied as the channel. As Bessel filters have a linear phase response in the passband, the output signal after the channel preserves the waveform in the passband, with a minimum output jitter [53].

2.4.2.1 NRZ

The simulated 80 Gb/s NRZ signals after Bessel channels with 3 dB BWs of the full bit rate, 0.66 bit rate, 0.5 bit rate, 0.33 bit rate and 0.25 bit rate (BR) are presented in Figure 2.30.
As illustrated in Figure 2.30, although the modulation itself is the simplest, the NRZ modulation requires a wide BW. Selecting 90% of the bit energy of a square pulsed modulated NRZ signal as the minimum BW requirement results in 2/3 of the BR [54]. When the channel BW is lower than 1/2 BR, the vertical eye opening of the output signal starts to decrease rapidly, due to the reduced slew rate caused by the BW limitation.

2.4.2.2 Duobinary

Recalling Figure 2.30, the eye diagrams of 80 Gb/s NRZ transmission over channels with less than 1/2 BR BW are repeated in Figure 2.31. Comparing the eye opening of the "NRZ" output signals, we can find that with the channel BW decreasing, especially when the BW is lower than 0.33 BR, the NRZ eyes become smaller and smaller. However, the duobinary eyes become more pronounced than the NRZ eyes. From the comparison of the transient simulation results, we can conclude that duobinary signaling survives a stricter BW limitation, so it requires less channel BW compared to

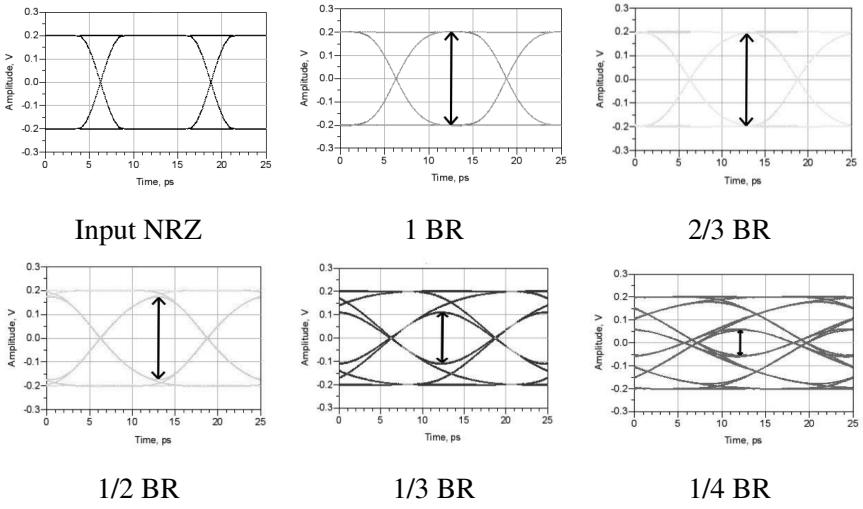


Figure 2.30: Transient simulation of 80 Gb/s NRZ signal transmission with different Bessel BW channels

NRZ signaling with the same data rate. This phenomena intuitively indicates that duobinary signaling is a valuable modulation format, especially in band-limited systems.

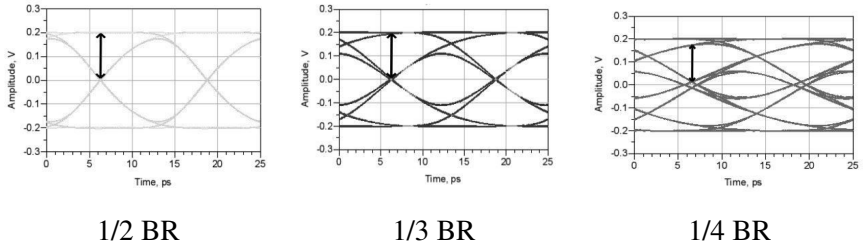
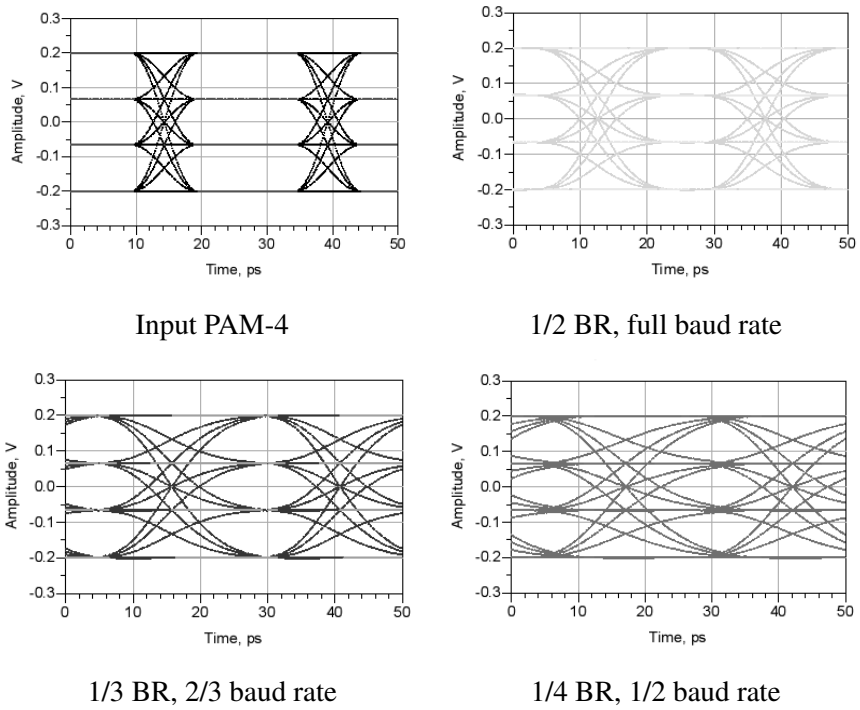


Figure 2.31: Transient simulation of 80 Gb/s NRZ signals, illustrating the duobinary eye opening with different Bessel BW channels.

2.4.2.3 PAM-4

Eye diagrams of PAM-4 signaling at 40 Gbaud after transmission over the different Bessel band-limited channels are depicted in Figure 2.32.
Comparing Figure 2.32 with Figure 2.31, PAM-4 requires a comparable channel BW as duobinary [44]. This is because PAM-4 reduces the symbol



Input PAM-4 1/2 BR, full baud rate

1/3 BR, 2/3 baud rate 1/4 BR, 1/2 baud rate

Figure 2.32: Transient simulation of 40 Gbaud PAM-4 signal transmission with different Bessel BW channels

rate by half and fits the signal efficiently into the available channel BW. Therefore, the PAM-4 format is a worthful alternative modulation technique applied in high speed electrical links.

2.4.3 Conclusion

In this work, the duobinary format was selected among the three modulation techniques. First of all, duobinary signaling has a more efficient BW utilization compared to NRZ. The NRZ spectrum is twice as wide as that of a duobinary signal for the same data rate. Moreover, unlike NRZ, duobinary signaling can make good use of the intrinsic BW limitation of the channel as part of the desired frequency response, reducing the stringent requirements for the equalizer to totally flatten the channel response which is difficult especially at very high frequencies [2].
Therefore, in this work, the FFE is applied to generate a duobinary frequency response by combining the low-pass channel characteristic and the

FFE finite impulse response. As a duobinary signal occupies only half of the BW of an NRZ signal with the same speed, the circuit requirement for the FFE applying the duobinary format is dramatically reduced. Therefore, using the same IC technology, the decreased circuit requirements make it possible to achieve a higher data rate. However, duobinary also has some disadvantages which should be taken into account in the backplane and circuit design. For example, compared to NRZ signaling, duobinary signaling is more sensitive to frequency-domain ripples [55]. Meanwhile, employing duobinary increases the complexity of the RX, due to the demand of decoding the duobinary signal back to the NRZ signal. The reception and the decoding of duobinary signals is discussed extensively in the PhD of our colleague Timothy De Keulenaer [54].

2.5 Technology selection

The technology selection is a trade-off between system requirements and design variables. In our case, a very fast semiconductor IC technology is needed in order to provide sufficient performance to ensure a very high BW for the data rate up to 80 Gb/s. Typically, as a rule of thumb, the transition frequency (f_T) of the transistors should be 5 to 10 times the application frequency, indicating a technology with a f_T above 320 GHz in this case, which was not accessible during the technology selection. This left us with the state-of-the-art SiGe BiCMOS or CMOS technologies, which were available at the beginning of this work.

2.5.1 BiCMOS and CMOS

A BiCMOS technology allows the integration of bipolar junction transistors (BJT) in analog blocks, together with metal oxide semiconductor (MOS) transistors in digital blocks, thus combining the advantages of high-frequency BJT devices and low-power logic gates of MOS transistors. As the transceiver front-ends contain a considerable amount of analog and mixed-signal functions, while the analog performance (BW, jitter, RX noise, non-linear distortion, drive strength...) will determine the overall link performance, a BiCMOS technology is a very interesting process for this research.
In general, compared to MOS transistors, BJTs are better options for high-speed implementations, due to their faster speed, higher current capability, and larger transconductance (g_m) than MOS transistors with an equal current. Meanwhile, BiCMOS devices offer many advantages where high load current sinking and sourcing are required, as the high current gain of BJTs greatly improves the output drive capability compared to conventional

CMOS devices. Moreover, BJTs allow a higher dynamic range over MOS transistors, due to their lower noise, better large-signal performance as well as higher breakdown voltages [56]. In addition, BiCMOS technologies are less susceptible to temperature and process variations, resulting in lower variability in the final electrical parameters and circuit performance [57]. Of course, the trade-offs around the technology selection are very application dependent. For this work, we mainly considered the technical performance parameters, but for high-volume products, one may make a different trade-off between analog and digital performance leading to CMOS.

Concerning CMOS technologies, of course a sufficiently fast process would be required for this high-speed application, such as 40 nm CMOS or 65 nm silicon on insulator (SOI) CMOS, both showing a f_T around 250 GHz [58] [59]. In a SOI CMOS process, the substrate is replaced by a layered silicon-insulator-silicon substrate, in order to reduce device parasitic capacitance and thereby improving the high-frequency performance.

For a given BiCMOS node, a comparable CMOS technology typically needs to be scaled two generations further to achieve a similar f_T. For example, MOS transistors in a 65 nm CMOS technology provide similar speed as the BJTs in an 130 nm BiCMOS technology. Therefore, compared to BiCMOS devices, a CMOS process with a similar speed has the advantage of smaller minimum feature size in digital circuit parts. However, in the analog parts, the benefit from CMOS scaling is much less than in their digital counterparts. For example, in analog circuit design, we need transistors with not only high f_T, but also with a large dynamic range, which is however limited by the breakdown voltages. Meanwhile, compared to BiCMOS technologies, the circuit design gets more complicated in the fastest CMOS technologies due to declining core voltages, higher metal parasitic capacitances, increased process variations and design rules [57].

In terms of chip costs, the fabrication price of an IC technology increases exponentially with every new miniaturization step [60]. Therefore, compared with CMOS technologies, a BiCMOS technology has a better cost-performance ratio (e.g. for the same f_T of around 250 GHz, a 65 nm CMOS technology is almost twice as expensive as an 130 nm SiGe BiCMOS technology). Therefore, a BiCMOS technology is preferred in this work. However, the cost numbers are not publicly known and depend a lot on the volume as well.

2.5.2 130 nm SiGe BiCMOS

Moving towards a minimum feature size of 130 nm, several SiGe BiCMOS processes provide a high f_T (up to 250 GHz). In Table 2.7, an overview

of the available BiCMOS processes is summarized. It is also important to note that at this moment a 55 nm SiGe BiCMOS process would be a very interesting technology to evaluate, due to the smaller minimum feature size and higher f_T of 320 GHz. This new ST microelectronics process was recently released in 2015 for multi-project wafer (MPW) runs, and was not available during our research.

Foundry	Process	Technology node (µm)	f_T / f_{Max} (GHz)	BV_{CEO} (V)
IBM [61]	BiCMOS8HP	0.13	200 / 270	1.77
ST [62]	BiCMOS9	0.13	160 / 160	1.7
ST [62]	BiCMOS9MW	0.13	230 / 280	1.6
ST [63] *	BiCMOS55	0.055	320 / 370	1.5
IHP [64]	SG13S	0.13	250 / 300	1.7
IHP [64] **	SG13G2	0.13	300 / 500	1.7
TowerJazz [65]	SBC18H2	0.18	200 / 200	1.9
TSMC [66]	0.18SiGe	0.18	120 / 120	2.3

* This new ST microelectronics process was recently released in 2015 (Circuits multi-project).

** This new IHP process was released in 2015 (Europractice).

Table 2.7: Overview of state-of-the-art BiCMOS processes

As elaborated in Table 2.7, the BiCMOS9MW process provided by ST microelectronics was the best available solution as it offers both a very high f_T and integrated microstrips. The IHP SG13S technology offers a slightly higher f_T, but a microstrip model is not available in that technology and there were no CMOS digital cells available in the design kit due to a legal issue between IHP and the digital IP provider, which was resolved beginning of 2013.

In addition, considering the chip fabrication cost of the MPW runs as listed on [67], the price per unit of area of ST 130 nm SiGe BiCMOS technology is only half the price of ST 65 nm CMOS technology.

In conclusion, based on all reasons mentioned above, the ST 130 nm SiGe BiCMOS9MW technology was selected in our design. All simulations and designs in the following sections of this work are performed using BiCMOS9MW, unless a different technology is explicitly mentioned.

2.6 Summary

In this chapter, several technologies have been introduced and discussed, including signal equalization as well as modulation techniques, in order to overcome the channel BW limitation, by either enlarging the channel BW or improving the signal BW efficiency. By applying an optimal combination of an improved backplane channel, an efficient equalization technique, together with a suitable modulation format and a very fast IC technology, the transmission data rate over an electrical backplane can be pushed beyond 80 Gb/s, as we will show in the following Chapters.

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3 Backplane transmitter

3.1 Transmitter architecture

Recalling the transmitter (TX) topology presented in Section 2.3.3, the proposed TX architecture including an intermediate multiplexer (MUX) test output is depicted in Figure 3.1. At the end of this chapter, a more extensive transmitter architecture will be shown in Figure 3.41.

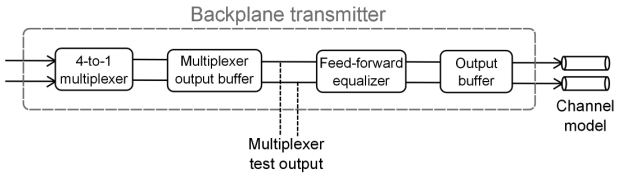


Figure 3.1: Transmitter architecture

An on-chip MUX combines four lower rate NRZ streams into a higher rate differential NRZ signal stream, towards the input of the on-chip equalizer via an intermediate buffer. A feed-forward equalizer (FFE) preceding the band-limited channel introduces a pre-emphasis on the input signal, in order to reverse the distortion incurred by the channel and to apply duobinary shaping, so that the receiver (RX) captures a reasonably clean input signal after the channel.

3.2 Multiplexer

3.2.1 Introduction

This part describes the design of a SiGe BiCMOS 100 Gb/s 4-to-1 MUX. This MUX was developed by our colleague dr. Zhisheng Li. It is presented here to describe the complete TX which we applied in the backplane system evaluations presented in Chapter 4. The MUX has four 25 Gb/s data inputs, one 50 GHz sinusoidal clock input, one 100 Gb/s data output to the FFE and one 100 Gb/s NRZ test output. The MUX can cover a very large data rate range and has a phase alignment function to set the optimal phases of the clock and data signals.

3.2.2 Topology

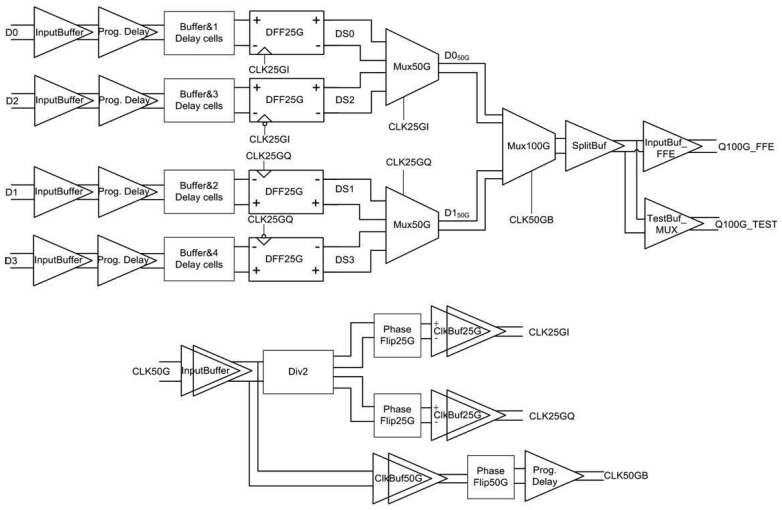


Figure 3.2: Topology of the MUX

Figure 3.2 illustrates the tree-like topology of the MUX. All the high speed signals in Figure 3.2 are differential. First, D0, D2 and D1, D3 are combined to two 50 Gb/s outputs via two 2-to-1 MUX blocks (MUX50G) working at 25 GHz clock frequency. Subsequently the two 50 Gb/s outputs are combined to the final 100 Gb/s output via a 2-to-1 MUX block (MUX100G) working at 50 GHz clock frequency. In Figure 3.2, $D0 \sim D3$ are the four 25 Gb/s input data signals, CLK50G is the 50 GHz input clock, Q100G_FFE is the 100 Gb/s output to the FFE and Q100G_TEST is the test output.

The clocks used in the MUX are generated by the 50 GHz differential input clock CLK50G. The four input data streams don't need to be perfectly synchronized on the printed circuit board (PCB), as the programmable delay cells in the data chains can tune the phase of the input data to optimize it with respect to the clock signal at the input of the DFF25G blocks. The MUX consumes around 550 mW, from an operational supply voltage of 2.5 V.

3.2.3 Interface

Conventional bipolar differential amplifiers are used in the input buffers of the data and clock signals. 40 Ω is placed between the input and supply for impedance matching. Two DC-blocking capacitors are placed at the input of the clock input buffer to remove the DC component. The schematics of both data and clock input buffers are elaborated in Figure 3.3 and 3.4, respectively.

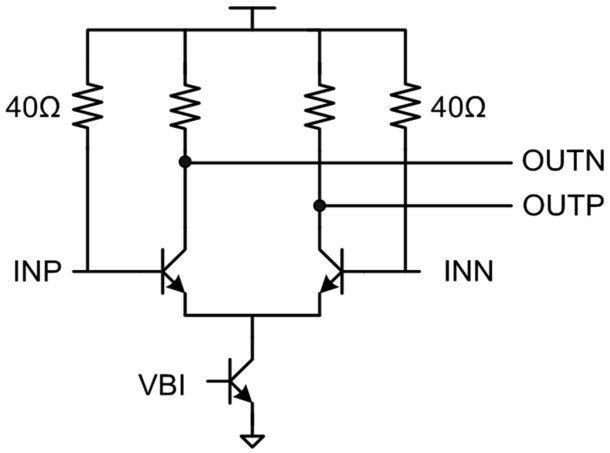


Figure 3.3: Schematic of the data input buffer

To allow seperate testing of the MUX, a split buffer is designed to drive two output signals. The input and output buffers, e.g. the MUX test buffer and the output buffer, have the same topology, except that the input buffers have no emitter follower (EF). The output buffers of the MUX are shown in Figure 3.5 and 3.6. It consists of an AC-coupled EF as input, used to eliminate DC offsets, followed by a common-emitter amplifier as the output stage. Emitter degeneration is employed to enlarge the bandwidth (BW) [1]. In addition, because of the physical layout, there is a relatively long distance

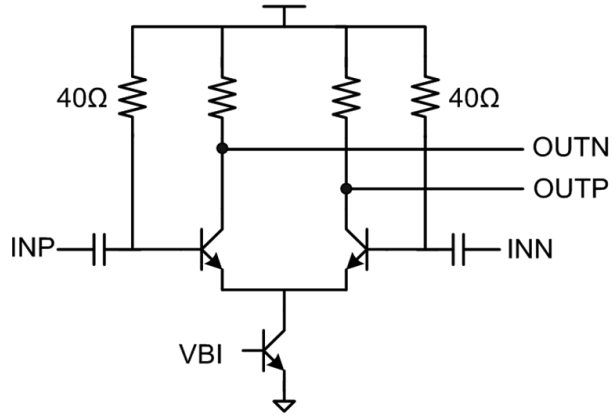


Figure 3.4: Schematic of the clock input buffer

between the MUX and the FFE (several hundreds of µm). Differential on-chip transmission lines (TML) are placed between the MUX and the FFE.

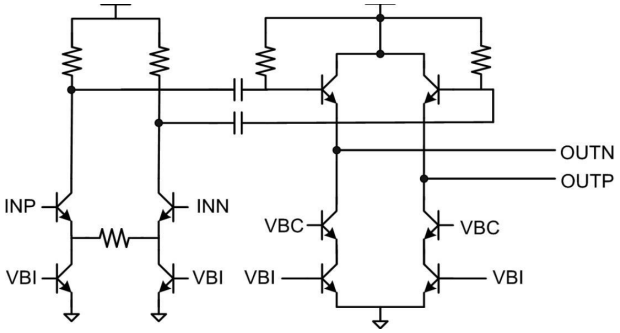


Figure 3.5: Schematic of the output buffer

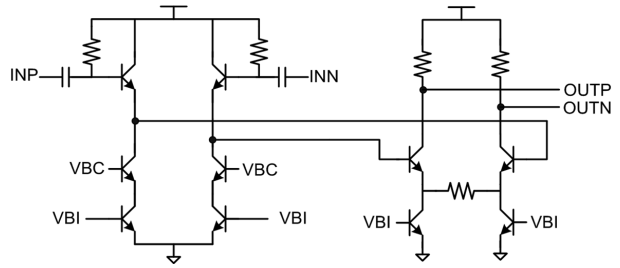


Figure 3.6: Schematic of the test output buffer

An overview of the DC and AC input and output characteristics of the different buffers is elaborated in Table 3.1.

Block		Value
Data input (Differential)	DC (V) Amplitude p-to-p (mV)	$1.5 \sim 2.5$ Typ. 200
Clock input (Differential)	DC (V) Amplitude p-to-p (mV)	DC-blocked Typ. 300
Test output (Differential)	DC (V) Amplitude p-to-p (mV)	2.41 Typ. 350

Table 3.1: Simulation results of the interface

During the final experiments, the amplitude and phase controls of the MUX clock are adjusted with respect to the measurement setups, which is illustrated in Section 4.3.1. The current control of each sub-block is mainly used for the optimization of the test output quality and power consumption. All settings are changed via a custom SPI interface.

3.2.4 Simulation results

The simulated eye diagrams of the test MUX output and the FFE input are depicted in Figure 3.7 and 3.8, respectively. The peak-to-peak jitter of the test output and the FFE input is 450 fs and 850 fs, respectively. In practical terms, the process, temperature and supply variations may result in different delays on the same sub-blocks in the four-channel input streams. Therefore, to ensure proper delays between all elements, the control bits should be adjusted accordingly.

3.3 Feed-forward equalizer

3.3.1 Introduction

As data rates rise beyond the channel BW, the signal integrity is degraded, showing e.g. reduced eye opening, increased jitter and inter-symbol interference (ISI). The limitations of the channel are typically overcome with an equalizer. Feed-forward equalization is one of the most common equalization techniques used in serial data paths as introduced in Chapter 2. Generally, an FFE is a filter that implements the inverse characteristic of the channel so that the usable frequency range is extended for high data rate signals. The FFE equalizes voltage waveforms by summing up the

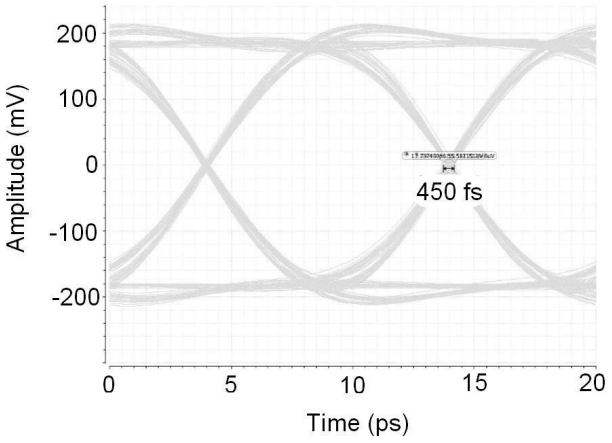


Figure 3.7: Simulated eye diagram of the test output

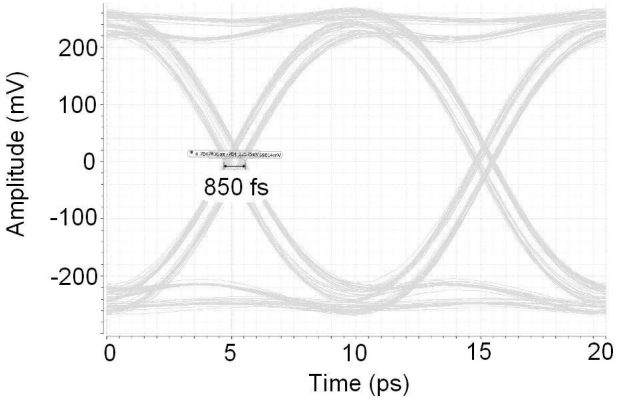


Figure 3.8: Simulated eye diagram of the FFE input

voltage levels from multiple controlled taps representing the weight of preceding and following voltage level samples. The summation is continuous over the entire waveform. Compared to other equalization techniques, such as decision-feedback equalization, the feed-forward equalization technique only corrects the voltage levels of the transmitted or the received waveform with information about the analog waveform itself. Therefore, the chip design is less complicated and requires less power consumption. In this work, an FFE is applied in between the data source (e.g. a MUX) and the channel, in order to improve the signal transmission quality in the electrical backplane system.

In this section, the design of a high speed FFE in 0.13 µm SiGe BiCMOS

up to 80 Gb/s is presented. The main signal path in the FFE takes the input data from the on-chip MUX and drives the external channel to the RX chip. By setting the coefficients of the gain cells via the SPI interface, the FFE intends to overcome the BW limitation of the backplane channel and to shape the channel response in such a way that a duobinary signal is provided at the input of the RX chip. To facilitate testing, an additional signal path is integrated, that allows to test the FFE without MUX.

3.3.2 FFE Topology

3.3.2.1 Conventional FFE topologies

First, a conventional FFE topology is illustrated in Figure 3.9.

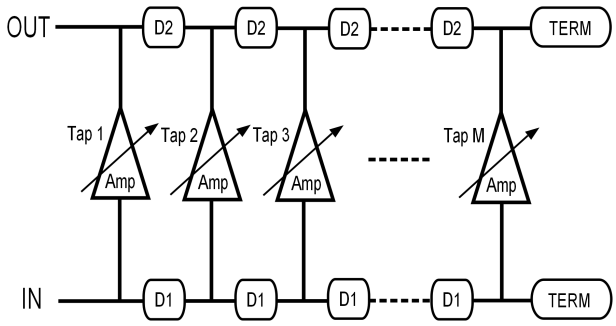


Figure 3.9: Conventional FFE topology (1)

The delay of each tap is implemented by two separate delay elements: one at the input of the equalizer and one at the output, with the overall delay of each tap being the sum of the two individual delays:

$$Tap_{delay} = D1 + D2 \tag{3.1}$$

The amplification of each tap in between the input and output implements different filter coefficients or tap weights. In this FFE topology, the output of the equalizer, as shown in Figure 3.9, is located at the same side as the input signal.
Another conventional solution is depicted in Figure 3.10, where the input and output are located at the opposite sides of the equalizer, which minimizes the parasitic coupling between the input and the output. However, in this case the tap delay is given by the difference between the two individual delay elements, which requires a longer delay element compared to topology 1.

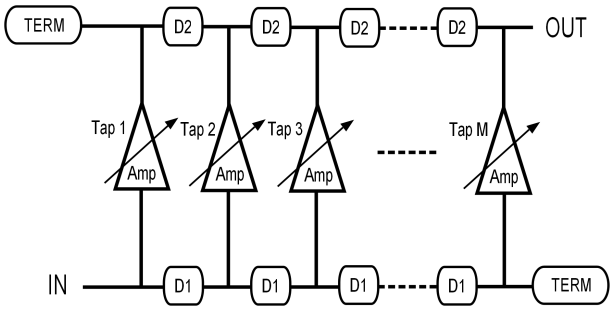


Figure 3.10: Conventional FFE topology (2)

$$Tap_{delay} = D1 - D2 \tag{3.2}$$

3.3.2.2 Proposed FFE topology for improved testability

A problem occurs when the FFE or its functionality needs to be tested. For example, when the amplification of the gain cells in the FFE has to be measured. In a practical system, the FFE may be soldered between other circuit components on a PCB. As such, it is impossible to test the FFE individually without disconnecting the FFE from the PCB and inserting an external data source, which however introduces a lot of extra work and which degrades the signal quality, especially at high frequencies.
The FFE may also be integrated in the same integrated circuit as other electronic building blocks. Adding test ports next to the conventional input and output ports would disturb the high-frequency signal because extra circuitry is required on the high speed data path to allow either an internal data signal or an external test signal to be connected to the FFE input and output. This extra circuitry, however, introduces extra power consumption and additional parasitics degrading the signal quality and BW of the data path.
In this work, we proposed a new FFE topology, extended with test ports such that the FFE characteristics can be fully tested, while the normal data signal path remains untouched, so that consequently the additional circuits do not influence the normal operation. The proposed FFE topology is presented in Figure 3.11.
As shown in Figure 3.11, it is an M-tap FFE, consisting of M variable gain stages as well as 2(M-1) delay elements located at the input and output of the equalizer symmetrically. By applying additional input and output test buffers on the other side of the FFE, we introduce an extra signal path along

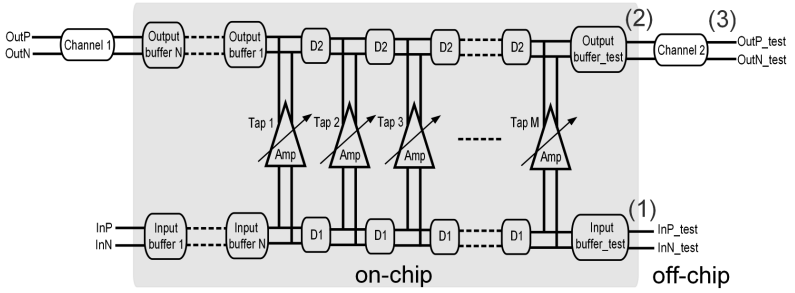


Figure 3.11: Proposed FFE topology with additional test ports

the equalizer. In both clockwise and counter-clockwise travelling direction, the upper and lower delay elements are summed together as the tap delay:

$$Tap_{delay} = D1 + D2 \tag{3.3}$$

Therefore, by setting the coefficients for each gain stage, we can introduce pre-distortion for the input signal in order to shape the channel frequency response for different modulation schemes, including: NRZ, duobinary, PAM-4 and so on. The input test buffer and output test buffer are directly connected to the input/output (IO) pads of the chip, which allows us to test the equalizer separately without making physical changes on the chip afterwards. In addition, the interconnection between the test buffer and the IO pads can be carefully designed with the test buffers in order to achieve good matching and small reflections, which will further extend the buffer BW and increase the operational data rate of the equalizer during the measurement.

The block diagram of the FFE realized in this work with the proposed topology is depicted in Figure 3.12. The FFE consists of five gain stages in a transversal 5-tap filter topology. At the left hand side of the FFE, the input buffer connects with the output of an on-chip MUX. The linear output buffer will drive the differential FFE output signal on a channel with 85 Ω differential characteristic impedance. The choice of 85 Ω differential as the value of the termination resistors is made after a trade-off between the BW and the power consumption. It helps to increase the BW of the backplane channel and the circuit output network including the output buffer, pad capacitances and packaging parasitics. However, it reduces 15% of the output swing using the same steering current of the output buffer. Therefore, more current and power will be consumed to keep the same output swing. At the right hand side of the FFE, the test input buffer connects with an external differential signal generator (e.g. pulse pattern generator) to test the

FFE in the time-domain without the on-chip MUX. The test input and output buffer have the same function as the input and output buffer, however, driving the differential signal in the opposite direction. Therefore, the tap weight settings of the five gain stages have to be mirrored when testing the FFE in the other direction. Each input and output buffer has an individual enable/disable switch, in order to choose the operating mode.

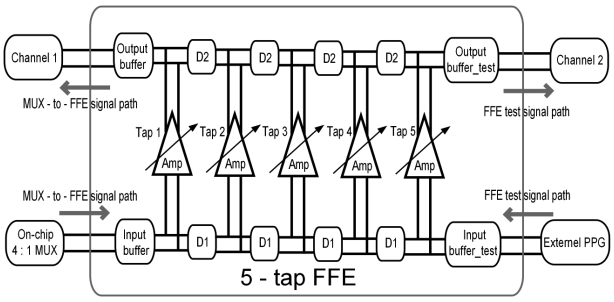


Figure 3.12: Fully integrated FFE structure

The relationship between the input and output of the FFE is given in equation (3.4). A_i represents the tap weight and T represents the time delay between the neighboring taps.

$$Y(t) = \sum_{i=1}^{5} (A_i \cdot X(t - (i-1) \cdot T)) \tag{3.4}$$

3.3.3 Circuit design

As illustrated in Figure 3.12, the proposed 5-tap FFE (the selection of the number of taps will be presented in Section 3.3.5.2) consists of gain cells, delay cells and input / output buffers. The detailed design of each part is illustrated in this section.

3.3.3.1 Delay lines

A delay element can be implemented by using either an active delay buffer or a passive on-chip TML. On-chip TMLs have been applied in various FFEs as low-loss delay elements, because of their very high BW and low power dissipation compared to active delay buffers [2]. TMLs can be made by microstrip lines, coplanar waveguides (CPW) or lumped elements. In a lumped element TML, on-chip LC (inductor and capacitor) sections are cascaded as passive delay elements. At high frequencies, the LC artificial

TML can make use of the parasitic capacitances of the transistors in the gain cell as part of the LC section. Therefore, compared to the active delay buffer method where gain cell input and output parasitic capacitances limit the BW, the lumped LC delay elements can absorb the parasitics and reduce the BW degradation. However, lumped LC delay elements have several disadvantages which degrade their high speed performance. First, as multiple inductors would be connected in series in the FFE, the parasitic resistances of the accumulated inductors restrict the realizable number of FFE taps and the total delay of all taps. Second, in order to predict the overall FFE performance, an accurate model of on-chip inductors provided by the foundry is necessary, which is however not always available.
In this design, on-chip microstrip lines were selected for the low-loss delay elements. Apart from the benefits of a very high BW and low power dissipation mentioned above, the length of half-symbol spaced TMLs becomes shorter for higher frequencies, which results in an acceptable chip area. In the FFE, each delay element between two neighboring taps consists of two TML sections, one located at the top and one at the bottom of the FFE, providing a one symbol delay between neighboring taps, as shown in Figure 3.12. Each TML section is 750 µm long in order to obtain a half symbol delay at 100 Gb/s signal rate and a 50 Ω characteristic impedance. Therefore, the nominal delay of each TML section is 5 ps, adding up to a neighboring tap delay of 10 ps and a total delay of 40 ps for a 5-tap FFE, resulting in a maximum delay of 4 symbols for 100 Gb/s input signals. The on-chip TMLs are all meanderingly shaped in order to reduce the chip length.

- TML simulation results

The simulated return loss, insertion loss and phase shift of one TML section are depicted in Figure 3.13.
The input and output TMLs of the FFE are terminated by on-chip resistors. For the input termination, we can directly use the 50 Ω load resistors of the input buffer. For the output termination, the TMLs connect with the base terminals of the EF transistors in the output and test output buffer. Therefore, on-chip resistors are added to terminate the 50 Ω output TML [3]. In our proposed FFE, lower value 35 Ω on-chip resistors are applied in order to improve the matching by compensating the input impedance of the output buffer. In this way, better impedance matching at both the input and output TML in the FFE is obtained considering frequencies beyond 50 GHz as illustrated in Figure 3.14. The input TML matching is good beyond 100 GHz and the output TML matching is extended from 72 GHz to 89 GHz. However, the lower resistor value requires higher current and power consumption, to keep the same signal amplitude.

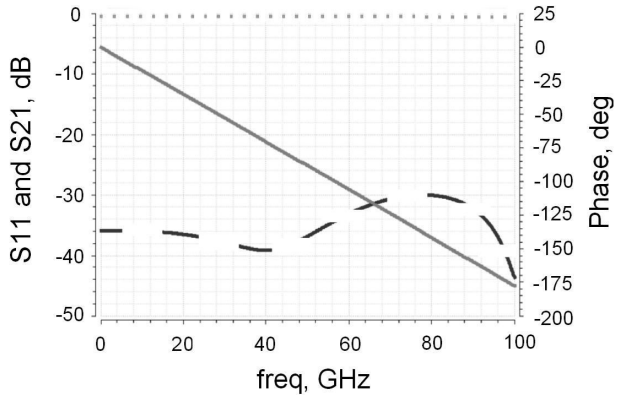


Figure 3.13: Return loss (dashed), insertion loss (dotted) and phase shift (solid) of one TML section

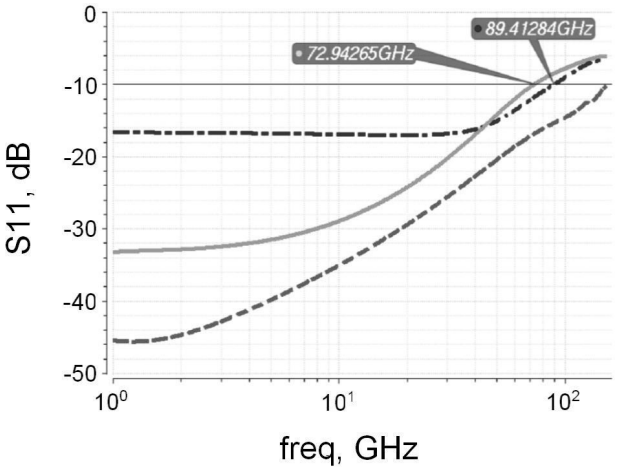


Figure 3.14: TML matching of input (dashed) and output (50 Ω: solid, 35 Ω: dashdotted)

- TML measurement results

Considering the very high BW required for the FFE TML sections, one should always be careful about simulation results and verify with measurements wherever possible. For this purpose, we added a number of TML test structures to a test chip. To do the measurements, probe measurements were performed. This minimizes the influence of additional interconnect structures and facilitates the comparison with simulation results. These measurements were done at ALU in Crawford hill and later repeated in the

INTEC_design Lab.
The first TML structure was designed using the available microstrip model in the ST BiCMOS9MW design kit. The ST TML test structure has a length of 215 µm and is designed with a Z_C of 50 Ω which results in a TML width of 12.4 µm on the signal layer [3]. However the total width of the TML structure is 100 µm, including the ground planes.
Next to the foundry provided TMLs, slow-wave TMLs were also included on the test chip, using the shielded "alternating wide and narrow portions" for CPW lines [4]. In the proposed slow-wave CPW (S-CPW) structure, the signal layer consists of a plurality of cells, where each cell has a narrow portion and a wide portion alternatively. The narrow and wide portions of the signal trace generate a cascade of low Z_C / high Z_C TML sections (resulting in an average impedance of 50 Ω), in order to create spatially separated energy storage and to increase the propagation constant of the TML [5]. The operating BW of the S-CPW is determined by the length and pitch of the narrow / wide sections. Therefore, each S-CPW cell should be made as short as possible, which is however limited by the minimal trace width and spacing rules of the technology. It has been shown that S-CPW structures have an improved slow-wave effect, with increased inductance and capacitance per unit length, compared to conventional CPW structures.
As a theoretical background of TMLs, the phase velocity v, wavelength λ and characteristic impedance Z_C are respectively given by equations (3.5), (3.6) and (3.7), where f stands for the operating frequency, L and C stand for the inductance and capacitance per unit length of the TML, respectively:

$$v = \lambda \cdot f \tag{3.5}$$

$$v = \frac{1}{\sqrt{L \cdot C}} \tag{3.6}$$

$$Z_C = \sqrt{\frac{L}{C}} \tag{3.7}$$

The equations listed above show that the wavelength λ of a signal with frequency f can be made shorter in the TML, while the characteristic impedance Z_C remains unchanged, by increasing L and C with the same factor. As such, a slow-wave TML has the advantage of being shorter for the same phase shift and hence requires a smaller chip area than conventional CPW structures. However, compared to the ST microstrip models, the attenuation constant of a S-CPW is comparable, or higher, owing to the different TML cross section and the corresponding dielectric substrate material difference caused by the layer stack of the semiconductor process. As the S-CPW

can be fabricated by conventional CMOS or BiCMOS technologies [4], we added two test S-CPW structures into the test chip, to characterize their RF performance and to compare the results with the standard ST microstrip TMLs. Additionally, in the S-CPW test structure, floating metal strips are placed under the S-CPW, to improve the effective propagation constant. In this test structure, the implemented S-CPWs have the same length as the ST microstrips (which will result in more phase shift), and a total structure width of around 25 µm to ensure the impedance matching to 50 Ω.
Figure 3.15 shows the probing setup of the TML test structures. The probing is performed with two ground-signal-signal-ground (GSSG) high speed (up to 50 GHz) differential probes (Picoprobe 50A-GS-150-SG) [6], providing both insertion loss and return loss.

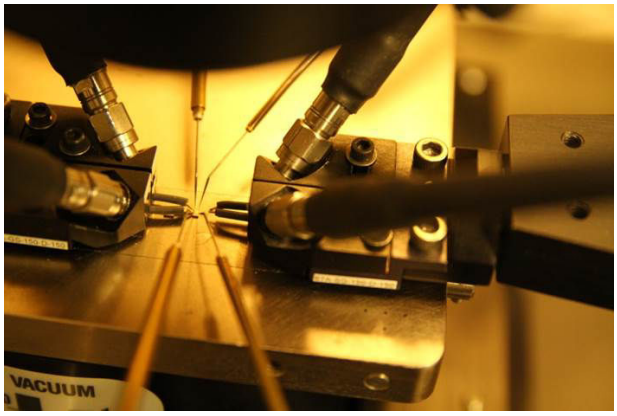


Figure 3.15: Probing setup of on-chip TML test structures

Figure 3.16 presents the layout of the test structures. Two slow-wave TMLs and an ST microstrip can be seen, all of them are connected to the same signal pads to save area. To probe the different structures, the TMLs were disconnected later on using a focused ion beam (FIB) operation.
Figure 3.17 illustrates the measurement results. As only GSSG probes were available at the time of these measurements, while the bonding configurations of the test structures were ground-signal-ground (GSG), only one side of the GSSG probe was used. This resulted in calibration errors which can be seen in the plot of the reflection coefficients. However, we were able to derive some useful conclusions. For example, we found that the phase difference between the two slow-wave structures and the microstrip structure is not very pronounced. This was possibly due to variations in the landing of the probes between different dies, and the relatively short test features, but anyhow the expected advantage of S-CPWs was not shown.

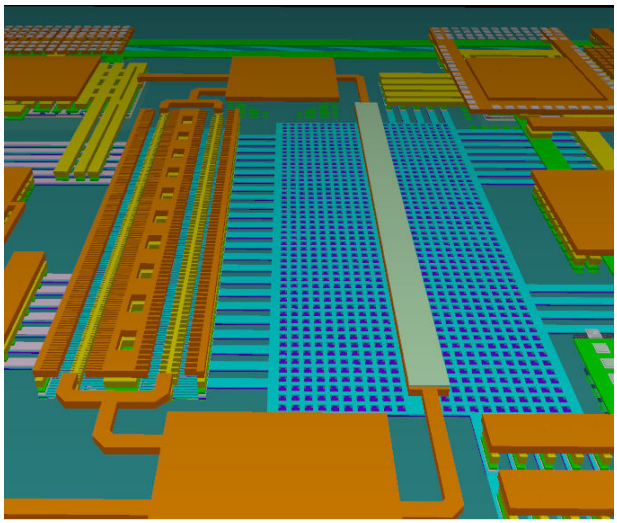


Figure 3.16: Layout of the measured TML structures

Moreover, on the plot of the insertion losses, one can clearly see that the loss of the slow-wave structures is substantially higher than the loss of the ST microstrip structure.
The high loss of the slow-wave TMLs, in combination with the limited gain in the FFE made us conclude that the available ST models would provide a safer approach towards a working prototype. Hence, the ST microstrip lines were used in the final prototype.

3.3.3.2 Gain cells

As shown in Figure 3.18, the gain cells are one of the most important sub-blocks in the FFE design. These cells realize the equalization coefficients or tap weights. As such, the gain control range and the BW of these gain cells will largely determine the FFE performance. In this part, first, the circuit design of the variable gain stages is elaborated. Second, the performance degradation due to layout parasitics is presented, together with an analysis of a potential instability due to a parasitic colpitts oscillator. Long on-chip traces and the related layout parasitics were extracted using EMX as an EM solver for this analysis. Last, the post-layout simulation results for both AC and transient response are summarized, and these results are compared to other similar designs.

- Gain cell schematic design

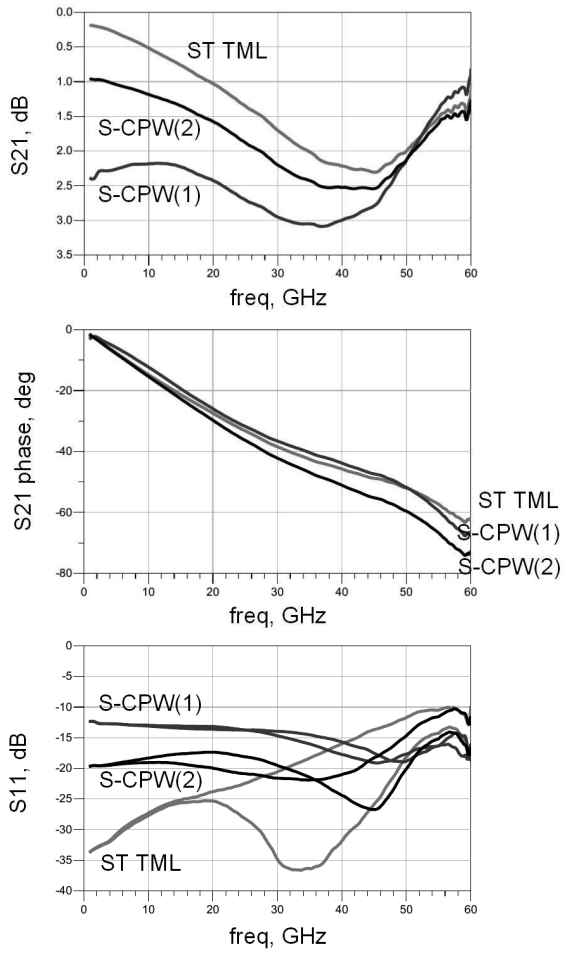


Figure 3.17: Overview of the on chip TMLs, in red the ST TML, in blue and black two different types of slow-wave TMLs

The gain cell is designed to obtain a large tunable gain range, with a flat linearly controllable amplitude response. Therefore, the gain stage can be considered as an analog multiplier with a high speed data input and a low speed control signal. To examine the gain controlling function of the gain cells, different variable gain amplifier (VGA) topologies are illustrated and compared.

The most straightforward topology of a VGA is a differential pair, with a variable tail current, which is controlled by a bias voltage, as shown in Figure 3.19.

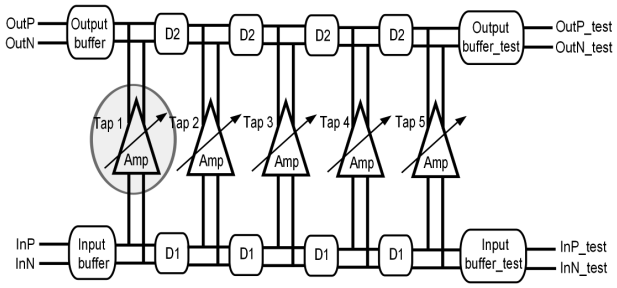


Figure 3.18: 5-tap FFE building blocks

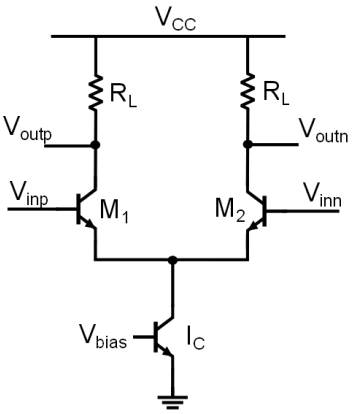


Figure 3.19: Basic VGA configuration with a differential pair

In a differential pair, the small-signal gain is a function of the tail current. The two transistors M_1 and M_2 in the differential pair provide a simple means of steering the tail current to one of the two output branches. Therefore, as depicted in Figure 3.19, the control voltage V_{bias} determines the tail current I_C and hence the gain of the VGA.
In this topology, the voltage gain A_v is given by equations (3.8) $\sim$ (3.10):

$$V_{in} = V_{inp} - V_{inn} \tag{3.8}$$

$$V_{out} = V_{outp} - V_{outn} \tag{3.9}$$

$$A_v = \frac{V_{out}}{V_{in}} = -g_m \cdot R_L \tag{3.10}$$

Therefore, the voltage gain of a differential pair VGA varies from zero (if I_C = 0) to a maximum value determined by the steering tail current. As an apparent shortcoming of this VGA topology, it is impossible to amplify the input by both a positive and a negative gain value, which is a critical requirement for the VGAs in the FFE, as the FFE tap weights can be either positive or negative.

This problem can be overcome by combining two differential pairs in a VGA, as shown in Figure 3.20 [7]. Similar to the basic differential pair amplifier depicted in Figure 3.19, the common-emitter transistors in the differential pairs transform the RF input voltages into RF currents, which are controlled by tail currents I_{c1} and I_{c2}. The collectors of the transistors are cross-connected to the load resistors R_L, in order to combine the outputs of the two differential pairs into a single differential output. As the RF currents through the transistors in the two differential pairs are cross-connected to the same load, the output voltage is the subtraction of the two differential outputs. The implemented gain magnitude and the sign of the VGA are controlled by the tail currents I_{c1} and I_{c2}. Assuming $Q_1 \sim Q_4$ are identical, by exchanging the tail currents I_{c1} and I_{c2}, the sign of the amplifier gain is reversed, while keeping the gain magnitude unchanged.

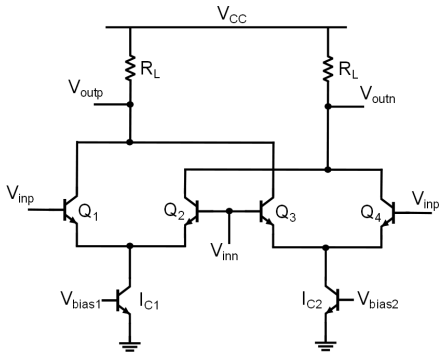


Figure 3.20: Typical VGA configuration with two differential pairs

In this topology, the voltage gain A_v is given by equations (3.11) $\sim$ (3.16), where g_{m1} and g_{m2} denote the transconductance of the transistors in the first and second differential pair, respectively:

$$V_{in} = V_{inp} - V_{inn} \tag{3.11}$$

$$V_{out} = V_{outp} - V_{outn} \tag{3.12}$$

$$V_{outp} = V_{CC} - R_L \cdot (I_{Q1} + I_{Q3}) \tag{3.13}$$

$$V_{outn} = V_{CC} - R_L \cdot (I_{Q2} + I_{Q4}) \tag{3.14}$$

$$V_{out} = -R_L \cdot (I_{Q1} - I_{Q2}) + R_L \cdot (I_{Q4} - I_{Q3}) \tag{3.15}$$

$$A_v = \frac{V_{out}}{V_{in}} = (g_{m2} - g_{m1}) \cdot R_L \tag{3.16}$$

Equation (3.16) shows that the voltage gain of the amplifier is determined by the tail currents I_{c1} and I_{c2}: If $I_{c2} = 0$, then $A_v = -g_{m1} \cdot R_L$, and if $I_{c1} = 0$, then $A_v = g_{m2} \cdot R_L$. For $I_{c1} = I_{c2}$, $A_v = 0$, and the outptut voltage becomes zero. Therefore, the bias voltages V_{bias1} and V_{bias2} need to adjust the tail currents I_{c1} and I_{c2} in opposite directions so that the gain of the amplifier changes monotonically.
To adjust the tail currents in opposite directions, a differential pair replaces the tail current circuits in Figure 3.20, leading to the gilbert cell topology, as depicted in Figure 3.21. Similar to the VGA topology shown in Figure 3.20, if there is a large difference between V_{bias1} and V_{bias2}, then the tail current I_C is completely steered to one of the top differential pairs and the voltage gain A_v reaches its most positive or most negative value. If V_{bias1} = V_{bias2}, then the tail current is equally steered to the top differential pairs, leading to a zero voltage gain.

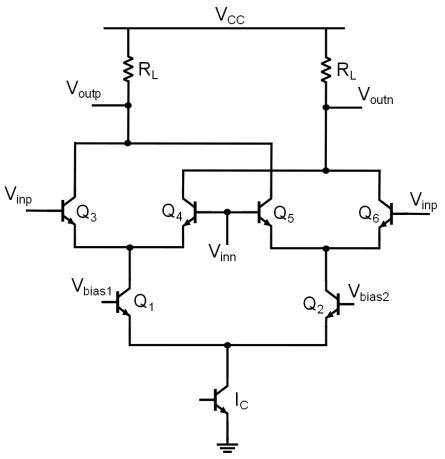


Figure 3.21: Typical VGA configuration with gilbert cell (1)

In the gilbert cell, the input signal of the top differential pairs and the control voltage on the bottom pair can be exchanged while still obtaining a VGA, leading to another VGA topology, which is illustrated in Figure 3.22. In this topology, the signal-summing amplifier senses the input voltage by the bottom differential pair, and realizes the gain adjustment by changing the base voltages of the transistors of the top differential pairs. Compared to the gilbert cell with configuration (1), this circuit configuration has a better performance at high frequencies, owing to the gain control stage operation as common-base transistors. So, this multi-transistor configuration has a smaller unwanted capacitive feedback, achieved by a smaller Miller effect. However, being a cascode structure, the gilbert cell requires a higher voltage headroom compared to a simple differential pair.

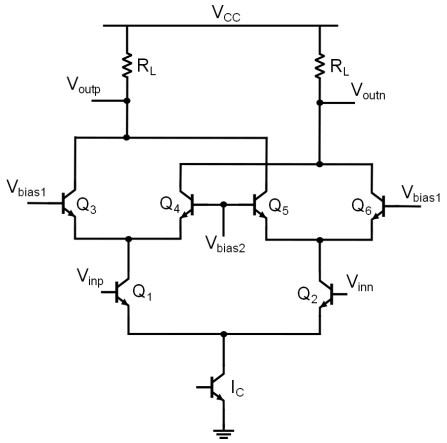


Figure 3.22: Typical VGA configuration with gilbert cell (2)

Due to the capabilities of realizing both positive and negative amplification, as well as a good performance at high frequencies, the gilbert configuration (2) is implemented in the gain cells of the FFE.
The resulting 1-stage amplifier, extended with cascode transistors, emitter degeneration and emitter followers at the inputs, is depicted in Figure 3.23. This extended circuit topology improves the high frequency performance, because the cascode configuration has a large BW, thanks to a reduced Miller effect. Emitter followers are applied to drive the degenerated differential pairs and to introduce a DC level shift in order to optimize the DC headroom of the transistors. Meanwhile, as the EF has a high input resistance and a low output resistance, it reduces the loading of the preceding signal source, to alleviate the RC bandwith limitation between the two stages. As the EF has a near-unity gain, the BW of the EF can be very

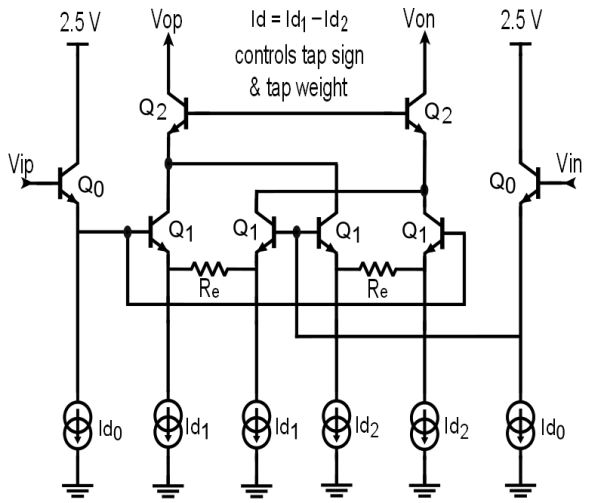


Figure 3.23: Variable gain stage, controlled by the tail current difference I_d = I_{d1} - I_{d2}

large, although its actual BW still depends on the transistor parameters, the EF bias current and the load to be driven. Meanwhile, due to the RLC parasitics of the relatively long trace between the EF and the gilbert cell (around 150 µm on-chip), the voltage gain of the EF becomes frequency dependent. The reason for the relatively long interconnections becomes clear in Section 3.3.6, when considering the overall layout of the gain cells between the input and output delay elements of the FFE.

Therefore, the BW of the FFE gain cell, including an EF and a gilbert cell, depends on the transistor parameters, the bias currents, the output load and the layout parasitics. Keeping these factors in mind, it becomes difficult to calculate the theoretical BW of the gain cell without simulation tools.

In this design, the gain cell is optimized to achieve a BW above 50 GHz and a high tunable gain range of 40 dB such that the tap coefficients are able to compensate the frequency response of the channel [8].

Apart from the BW requirements, the input and output impedances of the gain stages, presented to the input and output TMLs, are expected to be independent of the tap weights and sufficiently high in order to minimize reflections over the TMLs between different taps. The proposed variable gain stage consists of a pair of differential EF and a high BW VGA, as shown in Figure 3.23. The EFs are placed in front of the VGA in order to increase the input impedance for inputs Vip and Vin and to minimize the reflections along the input TML sections. The cascode transistors in the

VGA act as an open collector driver stage, with a high output impedance for outputs Vop and Von, which directly connects to the load resistors via the on-chip TMLs. In addition, Re is applied to the VGA in order to enlarge the BW. The gain of the VGA is controlled by two current DACs, I_{d1} and I_{d2} in Figure 3.23, whose overall structure is elaborated in Figure 3.24.

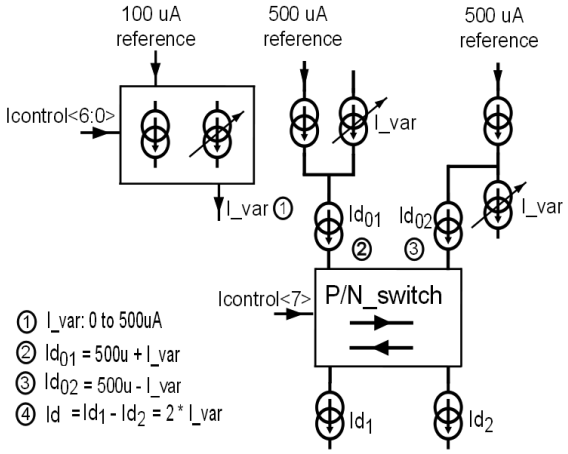


Figure 3.24: Current DAC

The VGA consists of two cross-coupled differential pairs (transistors Q1 in Figure 3.23). By varying the tail currents I_{d1} and I_{d2}, the gain of the positive and negative branch can be changed. The output current of both differential pairs are respectively added through the cascode transistors Q2. The sum of I_{d1} and I_{d2} is kept constant, making sure the bias conditions, i.e. the voltage over the output resistor and the currents through the cascode transistors, are fixed. In this way the gain of the VGA can be tuned without changing the total tail current of the cascode transistors, which helps to maintain high f_T biasing and high BW operation of the VGA irrespective of the gain setting [7].

The voltage gain of the VGA is linearly controlled by I_d, the current difference flowing through the Q2 cascode pair. This gain is given by equations (3.17) and (3.18), where V_T represents the thermal voltage and R_{load} represents the load impedance of the VGA, which is $17.5\,\Omega$ in this design to ensure a very wide BW, as explained in the previous section.

$$A_v = \frac{g_m}{1 + \frac{R_e}{2} \cdot g_m} \cdot R_{load} = \frac{\frac{I_d}{V_T}}{1 + \frac{\frac{I_d}{V_T} \cdot R_e}{2}} \cdot R_{load} \tag{3.17}$$

and when $\frac{\frac{I_d}{V_T} \cdot R_e}{2} \ll 1$:

$$A_v = \frac{I_d}{V_T} \cdot R_{load} \tag{3.18}$$

The tunable range of I_d in this design is from 0 µA to 1000 µA, which is digitally controlled by a 7-bit control word (shown as Icontrol <6:0> in Figure 3.24) with around 8 µA current steps. One more control bit is applied on the P/N output switch (depicted as Icontrol <7> in Figure 3.24) in order to control the sign of the control current I_d.

- Gain cell layout

Circuits with very high BW can only achieve their schematic-level performance when all circuit elements are optimally positioned to optimize the critical internal layout parasitics and to allow for the best possible interconnection between blocks and subblocks in the top level chip layout. As a relatively long distance between the input and the output of the gain cell needs to be bridged (distance between input and ouput TML), the VGA was split into two parts in order to divide the long inductive interconnection in pieces with lower, more manageable parasitics.
In addition, the investigation of the layout circuit presents the possibility of a parasitic colpitts oscillator. A schematic representation of the cascode transistors of the variable gain stage together with the layout parasitic components is depicted in Figure 3.25. The parasitic collector-emitter capacitance, collector-base junction capacitance and the inductance of the trace connecting the VGA and the output TML segments, generate a loop-back colpitts circuits, which could give rise to parasitic oscillation. A simplified parasitics model of the cascode transistor is illustrated in the top-right corner of Figure 3.25. The inductive output trace L, transistor junction parasitics C_3 and the series combination of C_1 and C_2 generate a parallel LC resonant tank circuit. The frequency of the colpitts oscillation is approximately the resonant frequency of the LC tank circuit, which is the parallel combination of inductor L, capacitor C_3 and the series capactiance of C_1

and C_2. Therefore, the oscillation frequency f_o is given by equations (3.19) and (3.20):

$$C_{eff} = \frac{C_1 \cdot C_2}{C_1 + C_2} + C_3 \tag{3.19}$$

$$f_o = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{eff}}} \tag{3.20}$$

Assuming the output trace of the gain cell has a length of 400 µm, with a parasitic inductance of around 400 pH, then the colpitts circuit starts to oscillate at 50 GHz when the combined parasitic capacitance C_{eff} reaches 25 fF.
The transistor junction capacitances depend on the transistor sizes. Therefore, to avoid the circuit oscillation, care needs to be taken for the transistor dimensioning and the layout to minimize the parasitic capacitances. Meanwhile, the length of the output traces connecting the VGA and the output TML segments was reduced to 60 µm so that the resulting parasitic resonance is so high in frequency, that the transistor cannot sustain the oscillation. Reducing the maximum interconnect length can be realized by placing the output section of the VGA in between the two differential traces of the output TML, as shown in Figure 3.26. The gain cell has a total area of 0.04 mm^2.

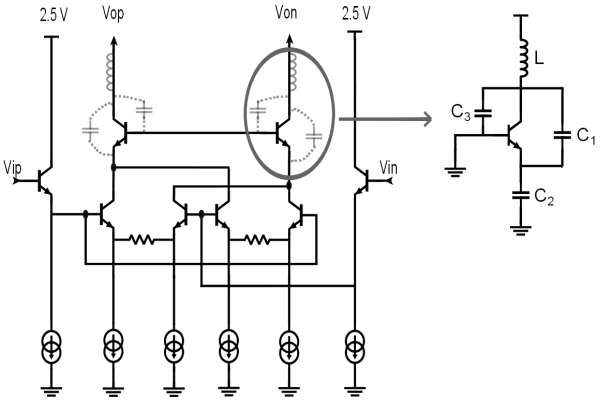


Figure 3.25: Parasitics causing resonances in the FFE

- Gain cell simulation results

The VGA circuit is simulated including the extracted layout parasitics and EM models for the relatively long on-chip traces.

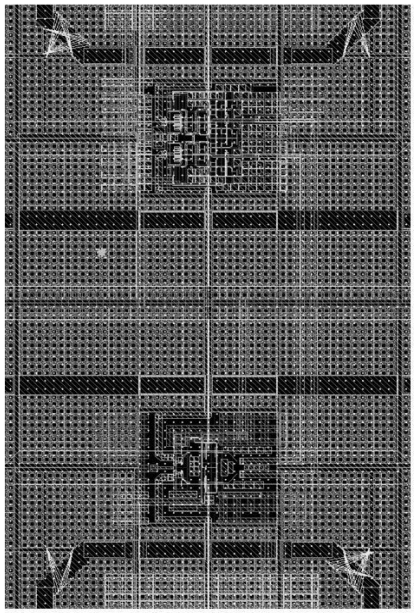


Figure 3.26: Gain cell layout

In the small-signal simulations, as depicted in Figure 3.27 and Figure 3.28, a tunable gain range of 42 dB is achieved, with a BW above 52 GHz.

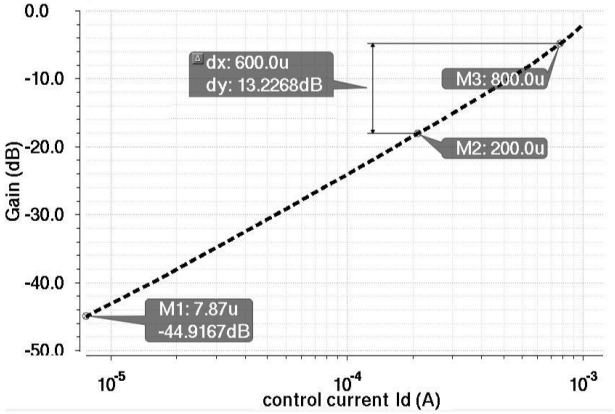


Figure 3.27: Tunable gain as function of control current I_d

The gain is linearly controlled by the tail current difference I_d, which is linearly generated by the current DAC making the gain tuning easy and

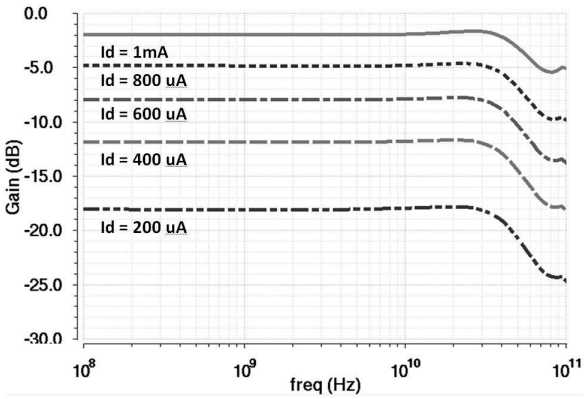
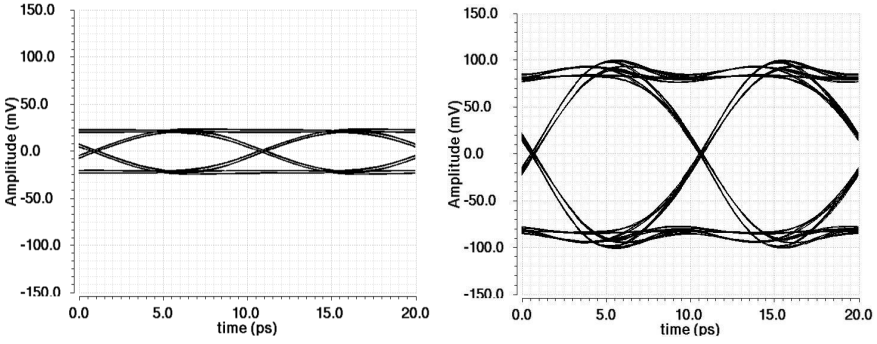


Figure 3.28: Frequency response for different control current settings

accurate. The maximum and minimum gain are obtained by setting the controlled current to 1000 µA and 7.9 µA.

The time-domain simulations, shown in Figure 3.29, illustrate the potential towards 100 Gb/s, with clear eye diagrams for two different gain settings. The two eye diagrams are obtained by setting I_d to 200 µA and 800 µA respectively, corresponding to a 4 times gain difference (which is 12 dB as depicted in Figure 3.27). When applying a PRBS 15 (with a period length of $2^{15} - 1$) differential input signal with 0 fs jitter to the gain cell, the peak-to-peak jitter of the output signal becomes around 400 fs, which is very low. The gain cell consumes 12 mA, from a 2.5 V supply voltage, resulting in a power consumption of 30 mW.



(a) (b)

Figure 3.29: 100 Gb/s output eye diagram for (a) I_d = 200 µA and (b) I_d = 800 µA, yielding a 12 dB gain difference

- Performance overview

An overview of the reported VGAs in literature is given in Table 3.2. A figure of merit (FoM) capturing the gain, BW and power consumption (P_{dc}) is defined in equation 3.21:

$$FoM = \frac{P_{dc}}{Gain \cdot BW} \tag{3.21}$$

From Table 3.2 it is clear that the presented VGA has the largest tuning range (TR) and occupies the smallest chip area. Recently, in april 2015, a 4-tap, 64 Gb/s FFE paper was published in the IEEE Journal of Solid-State Circuits (JSSC) [12]. In that work, using 65 nm CMOS technology, which is scaled two generations further than the technology we used, the VGA has a lower power consumption. However, our proposed VGA provides a larger BW and a higher TR.

Ref.	Technology	BW	Gain	TR	P_{dc}	Active area	FoM
		(GHz)	(dB)	(dB)	(mW)	(mm^2)	(mW / GHz)
[9]	180 nm SiGe BiCMOS	1.9	7.8	18.4	12.2	0.048	2.62
[10]	250 nm SiGe BiCMOS	30	11.5	11.5	560	0.756	4.97
[11]	130 nm CMOS	9	2.5	2.5	40	1.5	3.33
[12]	65 nm CMOS	44	-	36	19	-	-
This work	130 nm SiGe BiCMOS	52	-1.9	42	30	0.04	0.72

Table 3.2: An overview of reported VGAs

3.3.3.3 FFE input and output buffers

- Buffer schematic design

As shown in Figure 3.18, input and output buffers are put in front of and after the FFE. The input buffer drives the NRZ signal from the MUX output to the FFE input. The output buffers drive the following TML loads while still maintaining certain voltage / current swings. As such, the input buffers can be non-linear, limiting amplifiers, while the output buffers should be linear to preserve the pre-emphasis transients in the FFE signal and to support duobinary modulation.
Typical differential pairs are often applied, for their following advantages. First, the differential pairs are primarily sensitive to the difference between two input voltages, and insensitive to the input common mode voltage, allowing a high degree of input common mode noise rejection. Second, the

output swing can be easily controlled by changing the tail current. Third, the total supply current remains constant no matter which arm is sourcing the tail current, making sure the bias condition, i.e. the voltage across the tail current circuit, is fixed, which brings in a limited current variation. The schematic of a basic emitter-coupled differential pair, is shown in Figure 3.30.

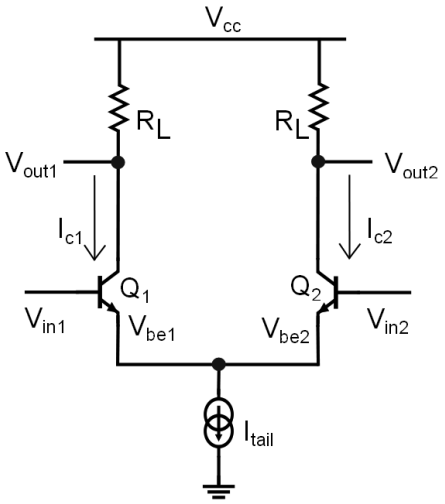


Figure 3.30: Emitter-coupled differential pair

From Kirchhoff's voltage law (KVL) around the input signal loop, the transistor base-emitter voltage and its input voltage are related by:

$$V_{in1} - V_{be1} + V_{be2} - V_{in2} = 0 \tag{3.22}$$

Assuming the load resistors are small enough so that the transistors do not operate in saturation, and assuming that both transistors are active with $V_{be1} \geq V_T$ and $V_{be2} \geq V_T$, then the simplified Ebers-Moll model shows that:

$$I_{c1} = I_{S1} \cdot e^{V_{be1}/V_T} \tag{3.23}$$

$$I_{c2} = I_{S2} \cdot e^{V_{be2}/V_T} \tag{3.24}$$

When transistors Q_1 and Q_2 are identical,

$$I_{S1} = I_{S2} \tag{3.25}$$

then combining equations (3.22) $\sim$ (3.25) yields:

$$\frac{I_{c1} - I_{c2}}{I_{c1} + I_{c2}} = \frac{e^{\frac{V_{in1} - V_{in2}}{V_T}} - 1}{e^{\frac{V_{in1} - V_{in2}}{V_T}} + 1} \tag{3.26}$$

$$\frac{\Delta I_c}{I_{tail}} = \frac{e^{\frac{\Delta V_{in}}{V_T}} - 1}{e^{\frac{\Delta V_{in}}{V_T}} + 1} = tanh(\frac{\Delta V_{in}}{2 \cdot V_T}) \tag{3.27}$$

Equation (3.27) derives the required input voltage to achieve full switching of the tail current for the differential pair circuit without degeneration. This mode of operation is often used for NRZ signals. Full current switching requires I_{c1} to be equal to I_{tail} and I_{c2} to be equal to 0, or vice versa. Therefore, the left part of equation (3.27) is equal to 1. When the magnitude of ΔV_{in} is greater than 4 times the thermal voltage V_T, which is about 104 mV at room tempature, the right part of equation (3.27) is almost equal to 1. As the chip needs to function over a wide temperature range, a differential input swing of higher than 104 mV is required to achieve a full switching of the tail current.

As the main FFE input is driven by the on-chip MUX, which provides a full-rate NRZ signal, the FFE input and output buffers are designed to have a sufficient BW for NRZ signals up to 100 Gb/s. Therefore, a certain amount of emitter degeneration ($2R_E$) and a cascode configuration are chosen in the buffer, as shown in Figure 3.31, in order to increase the BW by introducing a certain amount of peaking and by minimizing the influence of Miller effect.

The voltage gain of degenerated differential pairs is derived by equation (3.17). Under the condition of $g_m \cdot R_E \gg 1$, the voltage gain depends almost exclusively on the ratio of the resistors R_L/R_E rather than the transistor's temperature-dependent intrinsic characteristics. Therefore, the distortion and stability characteristics are improved, at the expense of a reduction in gain, which is acceptable for buffers. In addition, an EF stage is added in front of the differential pair, as a unity-gain level shifter in order to reduce the input common-mode level and to adjust to the input voltage of the cascode circuit. The EF has a high input resistance and a low output resistance. It is widely used as impedance transformer to reduce the loading of the preceding signal source by the input impedance of a following stage. The low output impedance reduces the RC time constant in between both stages, which helps to mitigate the BW limitation at the input.

The schematic of the FFE input / output buffers is shown in Figure 3.31. However, due to the different specifications, the dimensioning of the circuit elements is different for both buffers.

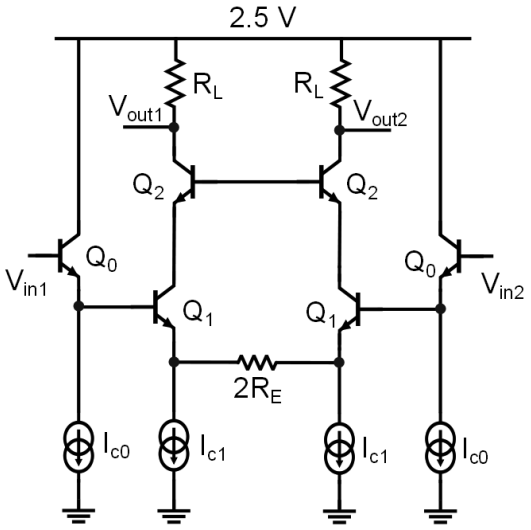


Figure 3.31: FFE buffer schematic

- Bandwidth and output parasitics

In the output buffer design, the presence of the external load or the duobinary RX reduces the output resistance, resulting in a lower RC product of the output network, which increases the output BW. On the other hand, due to the required high output levels (so that the duobinary RX receives a sufficiently strong signal), the tail current of the differential pair has to be higher than in the input buffer. Therefore, to maintain a high f_T, the transistors in the output buffer are larger (e.g. with an emitter length of 5.4 µm vs. 3.6 µm), which introduce a greater amount of parasitic capacitances (estimated around 15 fF). Apart from the transistor perspective, there are several other factors influencing the BW, which need to be considered in the output buffer design. For example, considering the IO pads and electrostatic discharge (ESD) protection diodes (with a parasitic capacitance of around 80 fF), assembly parasitics and layout parasitics, the total parasitic capacitance loading of the output buffer is around 150 fF, which has a significant influence on the BW of the output buffer. However, there are long on-chip traces connecting to the output pads, which introduce a certain parasitic inductance. These parasitic inductances are used as series peaking to increase the BW, as in [13].

- Simulation results

The frequency-domain and time-domain simulation results of the output buffer, taking the layout and packaging parasitics into account, are depicted in Figure 3.32 and Figure 3.33, respectively. A DC gain of around 3.2 dB and a 3 dB BW of 67.5 GHz are achieved, with a 100 Gb/s output swing of about 450 mV.

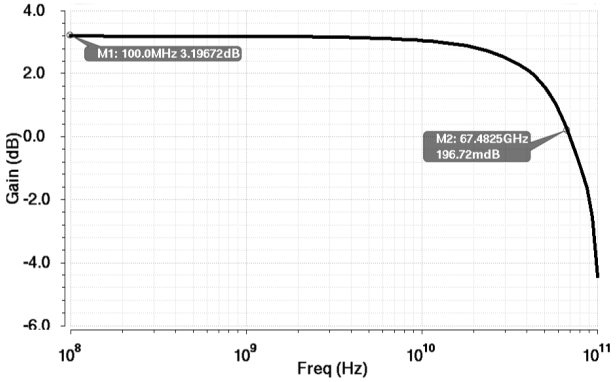


Figure 3.32: Frequency response of the output buffer

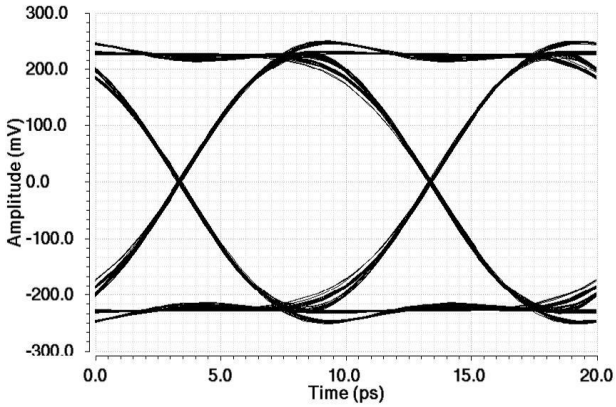


Figure 3.33: Eye diagram of the output buffer

3.3.4 Implementation of the 5-tap FFE

Figure 3.34 shows the implementation of the 5-tap FFE. The variable gain cell is the most critical sub-block in the FFE design, as discussed in the previous section. These gain cells realize the equalization coefficients or tap weights. Therefore, each gain stage can be considered as an analog

multiplier with a high speed data input and a low speed control signal. In addition, by keeping the summed current of both differential pairs constant, the current flowing through the TML termination resistor is constant, thus keeping the bias voltage of the FFE output buffer constant.

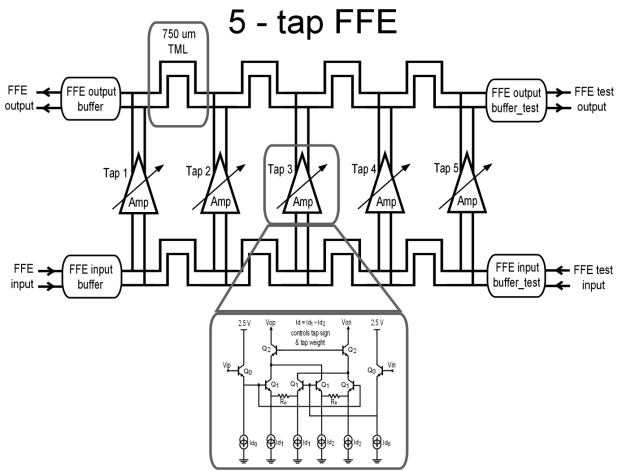


Figure 3.34: 5-tap FFE block diagram

Meanwhile, thanks to the high input and output impedance, the gain cells add a negligible load on the input and output TML, minimizing the reflection over the TML. The overall delay between neighboring taps is defined as the sum of the delay at the input and output TML.
In this FFE design, each meandered TML section between the gain cells is 750 µm long and is designed to have a Z_C of 50 Ω. Meanwhile, the input and output TML are terminated by on-chip resistors.

3.3.5 Simulation results

By setting the correct gain coefficient for each tap in the FFE, the frequency response of the channel can be shaped. As discussed in Section 2.4, besides NRZ, duobinary signaling was studied because it utilizes the available BW more efficiently than NRZ. The NRZ spectrum is twice as wide as that of a duobinary signal for the same data rate. Moreover, unlike NRZ and PAM-4, duobinary signaling can use the intrinsic BW limitation of the channel as part of the desired frequency response, reducing the stringent requirement of a totally flattened response for the equalizer [14]. As introduced in Section 2.4.1.3, a duobinary signal is defined as the sum of the present bit and the previous bit in a binary sequence, which is expressed in equations (3.28) and (3.29) where T represents the bit period:

$$y[n] = x[n] + x[n-1] \tag{3.28}$$

$$H(f) = \frac{Y(f)}{X(f)} = \frac{1}{2} \cdot [1 + exp(-j2\pi fT)] \tag{3.29}$$

3.3.5.1 Small-signal simulations

Looking at the spectrum of a duobinary signal, almost 90% of the signal power is in the main lobe of a sinc function between 0 Hz and half the data rate [15], which means that shaping the channel up to 50 GHz is theoretically enough for applications using a 100 Gb/s data rate. To evaluate the channel shaping capabilities of the FFE, the frequency responses of a number of FX-2 PCB striplines are first measured with different lengths, which are shown in Figure 3.35.

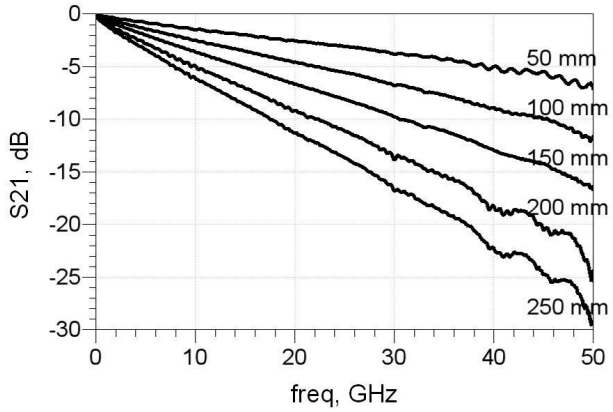


Figure 3.35: FX-2 stripline channel characteristics

The tap weights are derived for the different channels, to generate the corresponding duobinary impulse response and transfer function. The tap weights of the FFE are obtained by tuning the coefficients in order to reshape the low pass response of the channel so that the overall transfer function approximates the first lobe of the ideal 100 Gb/s duobinary channel, which is presented in Figure 3.36 (blue dotted).
As depicted in Figure 3.36, the original channel, the FFE shaped channel as well as the ideal duobinary channel are presented together. The FX-2 PCB striplines are measured up to 50 GHz. Hence, the frequency response of the FFE shaped channel above 50 GHz is not valid. The solid line represents a normalized FFE shaped channel, 2.12 dB below the dashdotted line over the

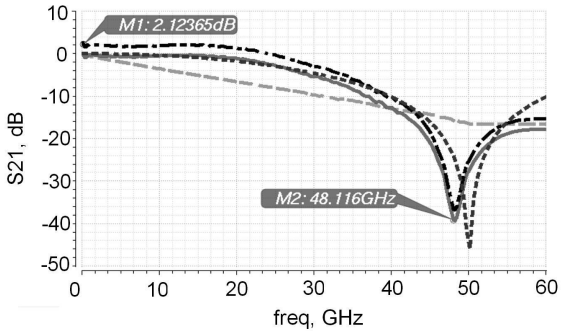


Figure 3.36: Frequency response: measured loss of 150 mm TML (dashed), FFE shaped (dashdotted), normalized channel (solid), ideal 100 Gb/s duobinary (dotted)

whole frequency range, to allow a better comparison with the ideal curve. From Figure 3.36, we can observe a good agreement between the first lobe of the FFE shaped channel and the ideal duobinary channel. The remaining difference is mainly due to the finite number of FFE taps and the limited range (40 dB) of the tap gain control. This remaining difference is, however, as shown by the large-signal transient simulations, low enough.
Another way to optimize the FFE coefficients is based on the measurements of the frequency response of each tap at its maximum gain. After 5 measurements, the frequency responses of the 5 FFE taps are converted into the time-domain by calculating the impulse response. As the FFE output can be considered as a linear combination of the impulse responses of each FFE tap, the complete system including the equalized channel and the FFE can be modelled as the convolution of the channel impulse response and the linearly combined FFE taps. Therefore, using the measured impulse response of each FFE tap, a combined FFE response can be applied to fit the channel to an idealized duobinary impulse response. In this way, the pre-cursors and post-cursors of the FFE are derived and optimized, to achieve a best fitting. An illustration of the FFE parameter optimization based on the taps frequency-domain measurements will be elaborated in Section 4.3.2.

3.3.5.2 Transient simulations

In this part, transient simulation results of the eye diagrams for NRZ and duobinary are presented for different numbers of equalizer taps. For both modulation schemes, the FFE works with NRZ input data, only the tap weigths are chosen differently in order to optimize the NRZ pattern or to

produce duobinary signals. As the measured FX-2 PCB stripline characteristics are only valid up to 50 GHz, only equalized output eye diagrams for 100 Gb/s duobinary and 50 Gb/s NRZ are discussed.
In order to obtain the optimal number of FFE taps, the eye openings for the different numbers of FFE taps are investigated and shown in Figure 3.37. From this figure, we can conclude that larger eye openings can be achieved by increasing the number of taps up to 5. However, above 5, the benefit is negligible due to the higher accumulated signal reflections over the on-chip TML. Hence, the selection of the FFE taps number for the final prototype is based on a trade-off between theoretical channel tuning accuracy and practical high speed signal degradation over the on-chip TML.

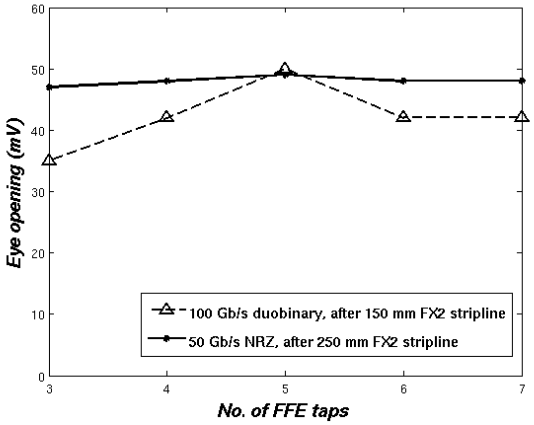
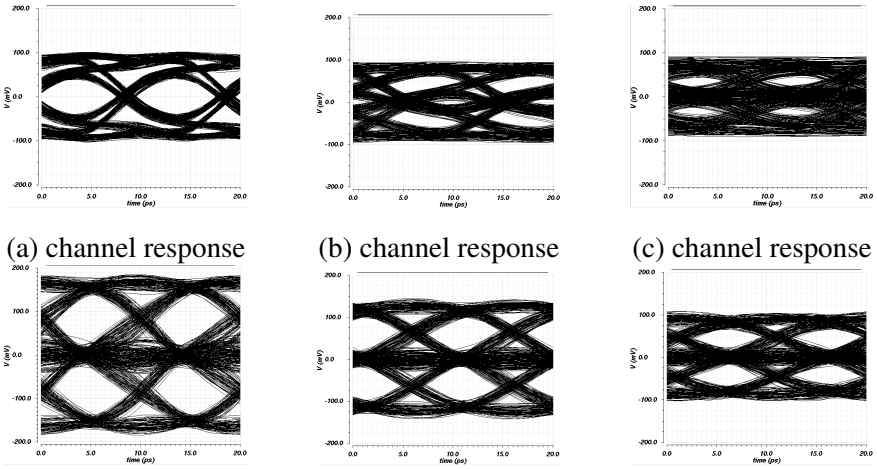


Figure 3.37: Number of FFE taps comparison

The simulated 100 Gb/s output eye diagrams after the measured PCB striplines with 3 different lengths are presented in Figure 3.38. These figures show that the channel-shaped NRZ input is still a reasonable NRZ signal after 50 mm (in subfigure a), however it becomes an almost duobinary signal after 100 mm and 150 mm traces (in subfigures b and c), which indicates that the equalization for a 100 Gb/s NRZ output would be limited by the channel length and that duobinary signaling becomes more interesting for longer PCB traces.
The eye diagrams of the equalized duobinary output signals after the PCB striplines are presented in Figure 3.38. These figures illustrate that the FFE provides a great improvement in eye opening and a reduction of the ISI induced jitter for the data transmitted over the BW-limited channels. From the simulated output signals after the FFE and after the channels, it is shown that the duobinary signals show very good eye openings and that eye open-



(a) equalized for duobinary (b) equalized for duobinary (c) equalized for duobinary

Figure 3.38: Simulated 100 Gb/s eye diagrams before and after applying 5-tap FFE on measured traces for (a) 50 mm, (b) 100 mm and (c) 150 mm. The simulation without FFE simply shows the channel response.

ing of the equalized output signal decreases with the increasing trace length and channel loss, as expected.

3.3.6 Layout

The layout and the die micrograph of the FFE circuit, are depicted in Figure 3.39 and Figure 3.40. The FFE was fabricated in 0.13 µm SiGe BiCMOS technology, featuring an f_T value of over 200 GHz [16]. The differential input and output TML are clearly visible in the layout, with the gain cells located in between. The differential input signals enter at the bottom left of the circuit and the outputs are taken from the top left, while the bias and control signal pads are located along either the top or the bottom. The output signal pads are arranged in a GSSG configuration, with a pitch matching high frequency probes (150 µm) [6]. The total area of the equalizer circuit is around 3.5 mm^2, and the length and width is around 2.5 mm and 1.4 mm, respectively.
In the final chip layout, apart from the analog design of the FFE, a digital SPI register is added. During the experiments, the tap weights of the FFE are optimized with respect to the interconnect channels, via the SPI interface. Meanwhile, according to the measurement setups, the input and output FFE buffers are selectively enabled, in order to determine the sig-

nal flow direction over the FFE, for measuring the whole TX or for only measuring the FFE individually.

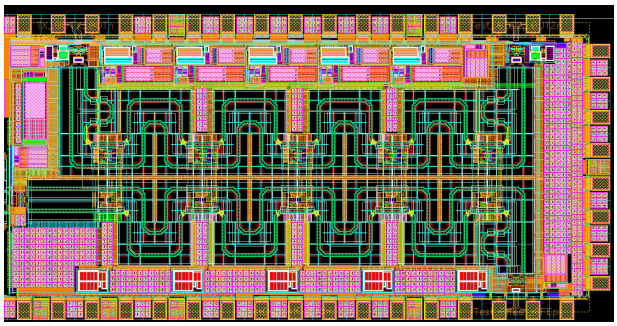


Figure 3.39: Layout view of the FFE

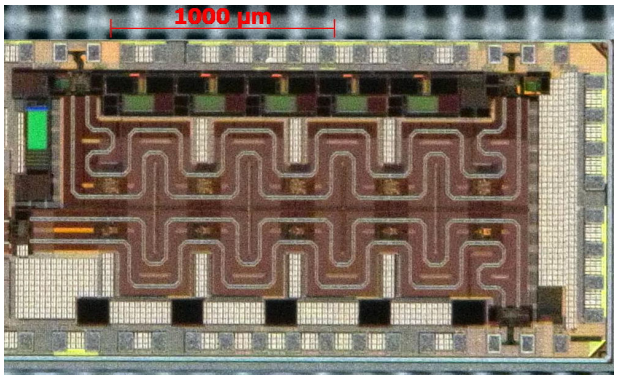


Figure 3.40: Die micrograph of the FFE

3.3.7 Conclusion

The design and layout of the FFE potentially operating at 100 Gb/s for high speed backplane communication were presented in Section 3.3. The 5-tap FFE is capable of reshaping the frequency dependent loss of PCB traces up to 50 GHz. The equalizer topology is based on a transversal filter with on-chip microstrip TMLs as delay cells. The patented FFE architecture introduces an extra input and output buffer, which allows for measuring and evaluating the FFE performance individually, without disconnecting the MUX. The proposed equalizer is designed in 0.13 µm SiGe BiCMOS technology, occupying an area of 3.5 mm^2 and consuming around 213 mW

from a 2.5 V power supply. From the simulation results, the FFE is shown to work up to 100 Gb/s over measured PCB striplines with up to 20 dB of loss at 50 GHz. The proposed equalizer significantly reduces ISI and produces open duobinary eyes with 50 mV per side eye amplitude after a 150 mm FX-2 PCB stripline.

3.4 Transmitter overview

3.4.1 Top-level design

By combining the MUX block and the FFE block together, the complete backplane TX chip is assembled. The building blocks of the TX chip are summarized in Figure 3.41. The MUX combines four quarter-rate input data streams (up to 25 Gb/s) to a full-rate NRZ data stream, used to drive the FFE. The FFE drives a high speed output signal onto the backplane trace, and, with appropriate tap settings, generates an equalized output signal after the channel. To compensate the channel loss, the FFE introduces pre-distortion on the transmitted signal waveforms and diminishes the ISI effects.

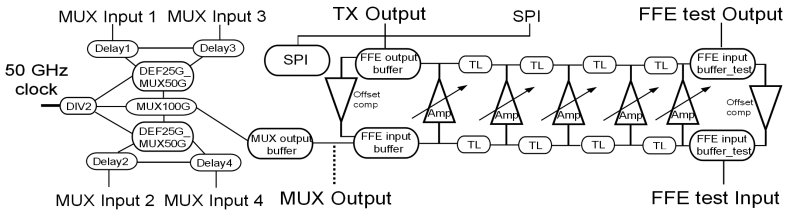


Figure 3.41: Transmitter building blocks

3.4.2 Layout

An overview of the IO pins of the TX chip is depicted in Figure 3.42. The complete chip has 72 IO pins, with a pin-to-pin pitch of 150 µm. All high speed differential inputs and outputs are designed as GSSG to enable probe measurements. The MUX is located at the left side of the chip, and the FFE is located at the right side. The 50 GHz input clock signal of the MUX is applied in the middle of the left-hand side of the chip, in order to keep the same distance to the four channels of the input data traces. The test output of the MUX and the output of the complete MUX-FFE TX are located in the bottom-middle and top-middle of the chip respectively, with enough space from the MUX input pins, in order to avoid the crosstalk between

the high speed signals. Furthermore, additional FFE test input and output pins are added to this chip, allowing to test the FFE separately. They are located in the bottom-right and top-right of the chip. Last but not least, the IO pins are assigned up-down symmetrically, so that for either flip-chip or bond-wire packaging, the chip pinout matches the PCB as much as possible. For example, when testing the FFE separately, the PCB designed for flip-chip packaging can be reused for the chip with wirebonding, the only reassignment would be the pinout of the custom SPI controller.

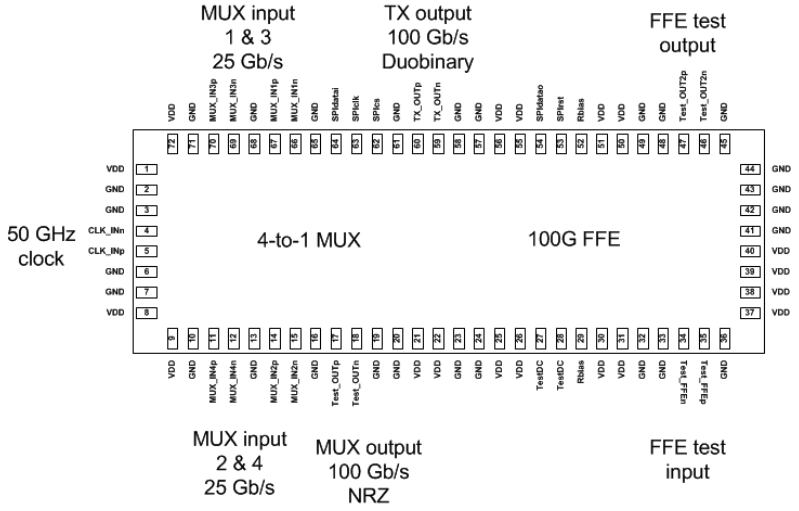


Figure 3.42: Pinout of the transmitter chip

Apart from the high speed signal pins and the digital SPI pins, there are 45 power and ground pins around the chip. Some of these power and ground pins are put in the corners of the chip for an easier decoupling on the PCB board. The other power and ground pins are grouped in pairs, in order to make the supply traces wider for a better decoupling on the PCB boards. In addition, the resistor bias pin for the reference input current is duplicated symetrically on the chip so that the chip keeps functioning when one of these bumps would disconnect. The total area of the chip is around 5.8 mm^2, with a length and width of around 4.2 mm and 1.4 mm respectively. The assembled layout is depicted in Figure 3.43, and the micrograph photo of the TX die is presented in Figure 3.44.

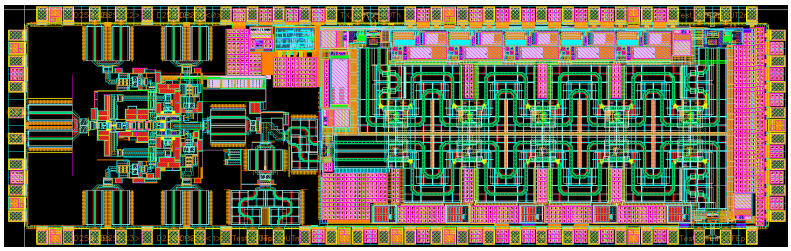


Figure 3.43: Layout view of the backplane transmitter

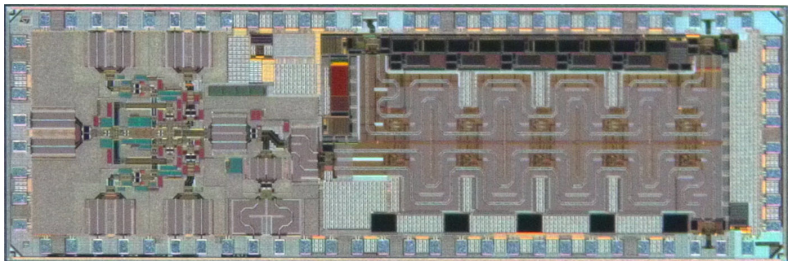


Figure 3.44: Die micrograph of the transmitter chip

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4 Experimental evaluations

4.1 Introduction

Chapter 4 presents the performance evaluation of the different backplane transmitter (TX) blocks and various link experiments through a commercial backplane. In Section 4.2, the measurement instruments are presented. In Section 4.3, the measured performance of the on-chip 4-to-1 multiplexer (MUX), feed-forward equalizer (FFE) and final TX combining both MUX and FFE are discussed. Subsequently, in Section 4.4 and 4.5, the link experiments with various channels, including printed circuit board (PCB) traces, backplane connectors and a commercial backplane, are presented. Extensive bit error rate (BER) measurements were taken to evaluate the different transmission channels at various speeds, including the duobinary receiver (RX). Finally, an overview of the tranmitter performance is concluded in Section 4.6.

4.2 Measurement instruments

The circuits designed in this work support bit rates above 80 Gb/s using duobinary formats. This requires high speed measurement instruments with a high bandwidth (BW) exceeding 40 GHz.
The INTEC Design laboratory has built-up a well equiped measurement facility, allowing us to perform thorough testing for RF and broadband com-

ponents and systems up to 67 GHz. The available high speed test equipment during this work, for both frequency-domain and time-domain measurements, is listed below:

- Anritsu MG3696B, a signal generator up to 67 GHz;
- Agilent PNA-X N5247A, a four-port 67 GHz vector network analyzer (VNA);
- Agilent DCA 86100C, a sampling oscilloscope up to 70 GHz, with remote sampling heads;
- SHF 12100B, a pulse pattern generator (PPG) for data rates up to 50 Gb/s;
- SHF 11100B, an error detector (ED) for data rates up to 50 Gb/s.

Meanwhile, during the measurements we also had the opportunity to borrow a top-notch Anritsu MP1800A, a 4-channel 32 Gb/s signal quality analyzer (including both PPG and ED modules), which allowed us to perform the transient and the BER measurements beyond 50 Gb/s.

4.3 Transmitter

The final integrated TX consists of a 4-to-1 MUX and a 5-tap FFE. Both sub-blocks are first measured independently and finally the combination of both is evaluated. As explained in Section 3.3.2, the final FFE has configurable test ports. This allows us to test the FFE performance independently, in both the time and frequency domain.
Because the TX operates at very high speed, chip packaging with minimal parasitics is needed. Wirebonding and flip-chip bonding are two typical chip-scale assembly technologies for broadband applications. As a rule of thumb, wirebonding typically introduces a parasitic inductance of 1 nH for each mm wire length, and in practice for each bonding wire the parasitic inductance is difficult to go below 0.3 nH [1]. Considering the value of the parasitic inductances, wirebonding is typically used up to 25 Gb/s or 40 Gb/s [2].
To solve the BW limitations, flip-chip interconnections have been extensively employed [3]- [7]. An overview of flip-chip bonding, measurement results, flip-chip models as well as the practical implementation, is elaborated in [3]. Flip-chip bonding has several advantages over wirebonding. First of all, as the chips are flipped and directly attached on the test board,

the flip-chip interconnections can be made very short (few tens of μm), which decreases the parasitic inductance to as low as 20 pH [4]; Second, compared to wirebonding, flip-chip pads can be smaller, with parasitic capacitances as low as 20 fF [4] [5] [7], not considering electrostatic discharge (ESD) protection structures. In summary, compared to wirebonding, flip-chip bonding introduces much lower interconnection parasitics and therefore contributes to better wideband performance, showing that BWs exceeding 50 GHz are possible employing flip-chip bonding [7]. Therefore, in this design, the TX chip is assembled directly on a test board with flip-chip bonding.

4.3.1 MUX measurements

4.3.1.1 Experimental setup

First, the MUX was measured seperately. In order to measure the MUX function, three clock signals (f_0, $f_0/4$ and $f_0/16$) are required in the test setup. A clock signal Clk_{out} is required at frequency f_0 being half the line rate. Meanwhile, a rat race coupler is applied in the clock signal path in order to provide a differential clock signal to the block. A 4-times divided reference clock $f_0/4$ is provided to the Anritsu MP1800A, a four channel PPG. This pattern generator provides the 4 data streams at a quarter line rate to the input of the MUX. A 16-times divided reference clock $f_0/16$ is provided as trigger signal to the Agilent DCA 86100C sampling oscilloscope. As the three clock signals require different frequencies, while there is only one signal generator (Anritsu MG3696B) available, both SHF 12100B and SHF11100B are applied to divide the clock signal and to distribute the various clocks to the TX chip and the measurement instruments.

The measurement setup is illustrated in Figure 4.1.

In this setup, it is key to provide a sufficiently strong clock signal to the chip for the MUX to operate optimally. The clock signals travel from the SHF12100B to the chip along a few cables and PCB traces, which introduce attenuation, especially at mm-wave frequencies. For example, at 50 GHz, the overall loss across the clock signal path is around 16 dB. Therefore, in order to ensure a sufficiently strong input clock signal for the chip, the amplitude of the output clock signal from the SHF12100B is set to its maximum 700 mV peak-to-peak. This can be done by adjusting the input clock level to the device to its maximum 710 mV peak-to-peak. Meanwhile, the interconnections between the test board and the clock generator SHF12100B should be made as short as possible.

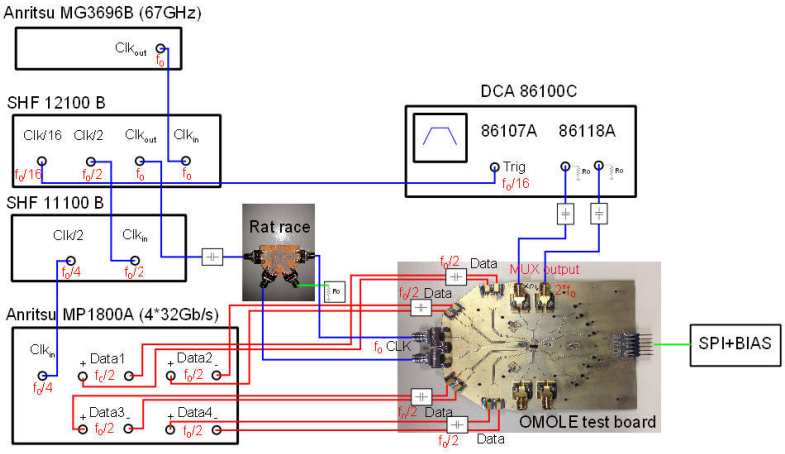


Figure 4.1: MUX measurement setup

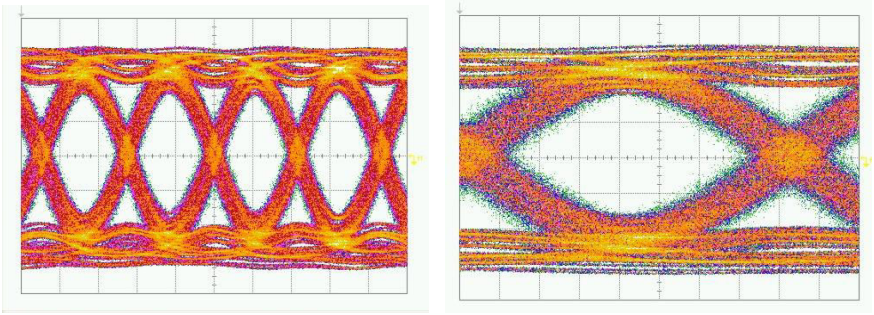
4.3.1.2 Results

The test output of the MUX is connected to a pair of tapered differential microstrip lines of around 3.5 cm long to a pair of 1.85 mm connectors.

First, the MUX was measured at 64 Gb/s by feeding four 16 Gb/s inputs. By tuning the output frequency of the signal generator Anritsu MG2695B, the MUX output could be measured with different data rates up to 100 Gb/s. The 4-to-1 MUX is tested with four input channels of PRBS 7 (with a period length of $2^7 - 1$). Each data channel has a single ended voltage swing of 500 mVpp.

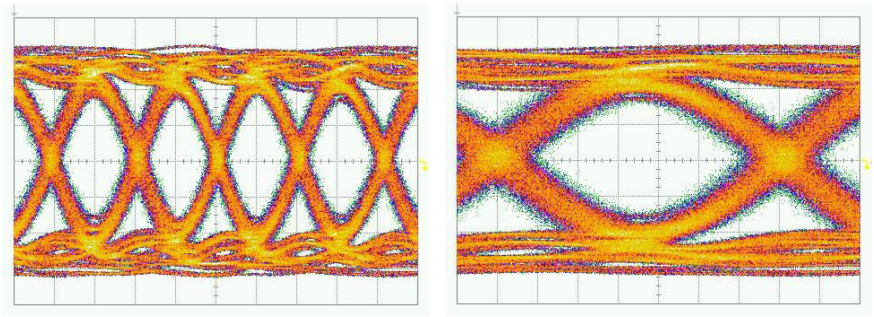
The MUX output was measured by an Agilent 86118A oscilloscope with 70 GHz dual remote sampling heads. The eye diagrams of the MUX differential output at 64 Gb/s, 72 Gb/s, 84 Gb/s and 100 Gb/s are depicted in Figure 4.2, Figure 4.3, Figure 4.4 and Figure 4.5. The resulting eye openings are 204.8 mV, 193.5 mV, 180 mV and 144 mV, respectively. As shown in the figures, the eye openings of the MUX output become smaller with higher data rate, due to the loss of the PCB test board. In this measurement setup, the MUX output was measured after the output transmission line (TML), which is around 3.5 cm on the test board. This PCB trace introduces a certain amount of signal attenuation, depending on the operational

frequencies. For example, at 50 GHz, the overall loss of the MUX output trace is around 9.3 dB.



7.5 ps/div, f_0=32 GHz 2 ps/div, f_0=32 GHz

Figure 4.2: 64 Gb/s output eye diagram of the 4:1 MUX

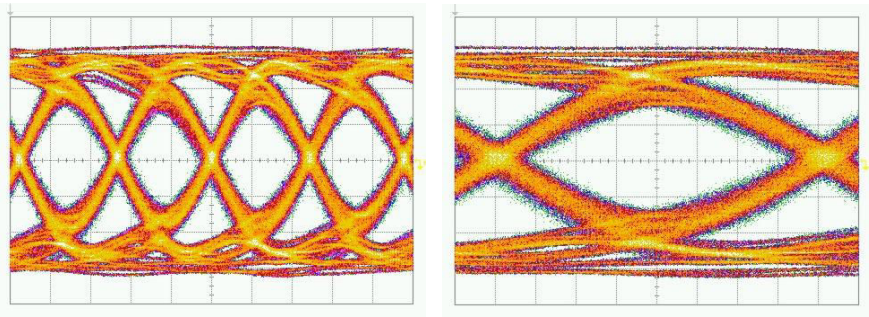


6.3 ps/div, f_0=36 GHz 2 ps/div, f_0=36 GHz

Figure 4.3: 72 Gb/s output eye diagram of the 4:1 MUX

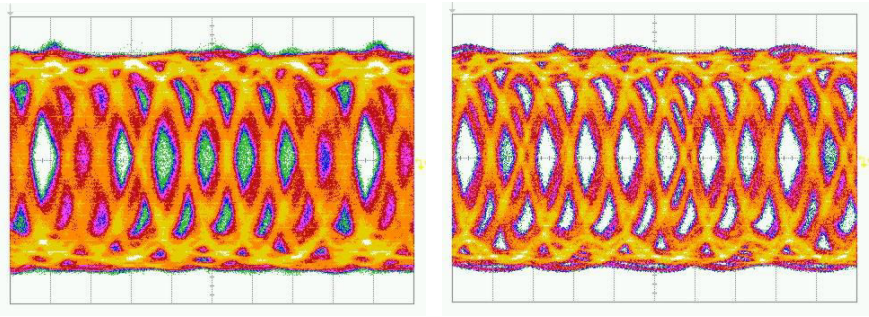
4.3.1.3 Conclusion

The measurement results show that the 4:1 MUX is able to work up to 100 Gb/s. Compared to the MUX output at lower speed, e.g. 84 Gb/s, the eye quality of the 100 Gb/s output signal is degraded, partly due to the limited clock amplitude available to the MUX. As presented in Figure 4.5, the 100 Gb/s MUX output performance is improved by applying a stronger clock signal to the chip. It indicates that in a better setup, the measurement results should be better and the eye quality should be improved.



5 ps/div, f_0=42 GHz 1.5 ps/div, f_0=42 GHz

Figure 4.4: 84 Gb/s output eye diagram of the 4:1 MUX



10 ps/div, f_0=50 GHz 10 ps/div, f_0=50 GHz, with stronger clock signal

Figure 4.5: 100 Gb/s output eye diagram of the 4:1 MUX

Additionally, it should be noted that, in this measurement setup, the MUX output was captured after the TMLs on the test board, which introduce an extra BW limitation. Therefore, for high data rate outputs (such as 84 Gb/s and 100 Gb/s), it would be beneficial to measure the MUX output via high BW probes on both the clock input and the MUX output. This will not only increase the BW of the MUX output, but also reduce the attenuation of the clock signal caused by the test board (e.g. the clock traces on the test board introduce a 12.9 dB loss at 50 GHz).

4.3.2 FFE measurements

4.3.2.1 Frequency domain

The frequency response of the FFE was measured with an Agilent PNA-X N5247A and two GSSG high speed differential probes (Picoprobe 50A-GS-150-SG) [8]. In comparison to the conventional FFE topology, with on-chip resistors to terminate the on-chip TMLs, a special test configuration is added to the FFE allowing to easily measure its behavior.

- Experimental setup and results

The experimental setup is depicted in Figure 4.6. Applying a probe station with two GSSG probes on the FFE test input and output pads, the FFE can be measured in the frequency domain. The settings of the FFE are programmed via a custom SPI interface.

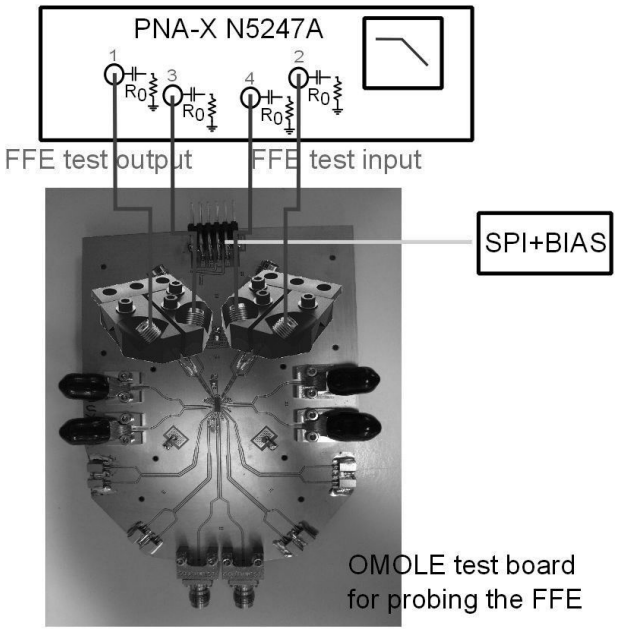


Figure 4.6: FFE measurement setup

In order to look into the performance of the sub-block in the FFE, the frequency response is measured while turning on only one gain cell to its maximum gain and turning off the other four gain cells. Based on the frequency response of each FFE tap at the maximum gain, the impulse response of each FFE tap is calculated and presented in Figure 4.7. As shown in Figure

4.7, the impulse response of the FFE depends on the position of the enabled gain cell.

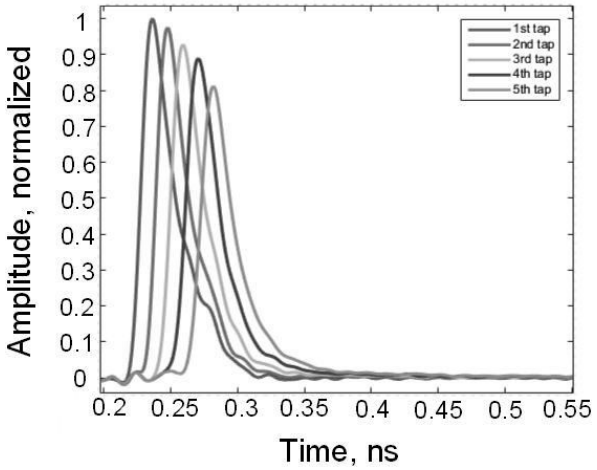


Figure 4.7: Impulse response

From Figure 4.7, it can be observed that the later taps have a lower output swing, which is caused by the frequency-dependent loss introduced by the on-chip TMLs. Each FFE tap is separated in time by a delay of around 12 ps, corresponding to the time delay between the neighboring taps of the FFE. Therefore, the delay introduced by each section of on-chip TML is around 6 ps.
The measured time delay introduced by the 750 µm on-chip TML is around 6 ps, which is about 20% more than what we expected and simulated in Section 3.3.3. It indicates that the actual phase shifts, or more specifically, the capacitive loading on the TML was underestimated. As illustrated in Figure 4.8, an extra pair of 20 fF parasitic capacitances between the TML and ground will increase the phase shift by 20%, and therefore contribute to an increased time delay from 5 ps to 6 ps. Analyzing the layout of the on-chip TML, this extra delay may be partly due to the capacitive loading of the FFE gain cells and the metal dummies added underneath the TML. In order to fulfill the metal density requirements of the process, several dummy pieces at different metal layers were placed underneath the TML.

- FFE parameters optimization

Recalling the brief illustration of the FFE coefficient derivation in Section 3.3.5, a detailed FFE parameter optimization based on the frequency do-

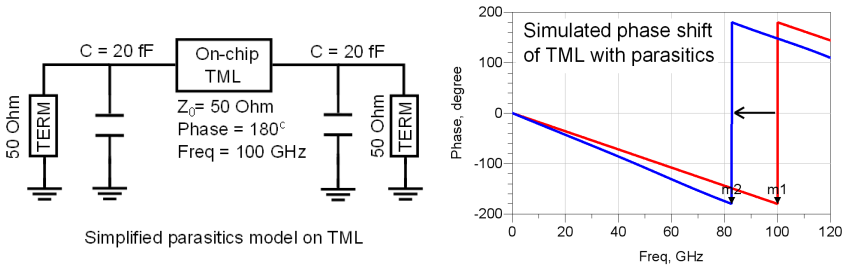


Figure 4.8: Increased on-chip TML phase shift with parasitics

main measurement is presented in this section.
From the gilbert cell implementation, one can assume that the gain of the taps is linear with the control current. As a result, the FFE output can be calculated as a linear combination of the impulse responses of the FFE taps. The complete system can be modeled as the convolution of the channel impulse response and the FFE taps or by multiplying them in the frequency domain and recalculating the impulse responses.

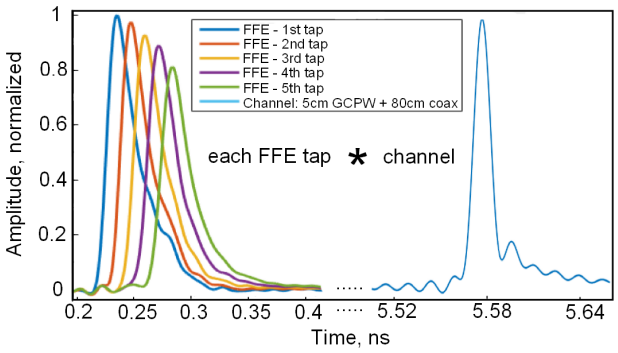


Figure 4.9: Impulse responses of each FFE tap and a lossy channel

Figure 4.9 presents the impulse responses of each FFE tap and a lossy channel. This lossy channel consists of a 5 cm RO4003C differential grounded coplanar waveguide (GCPW) trace [9] and a pair of 80 cm coaxial cables. The equalized channel response can be simulated by convolving the measured channel response with a linear combination of the measured impulse responses [10]. The coefficients of this linear combination are optimized using a gradient search algorithm to obtain a least square error (LSE) fit between the simulated response and a desired reference pulse [11]. In this way, the optimal value of pre-cursors and post-cursors in the FFE is se-

lected. Taking 84 Gb/s signalling as an example, the resulting equalized channel response fitted to NRZ or duobinary response is shown in Figure 4.10.

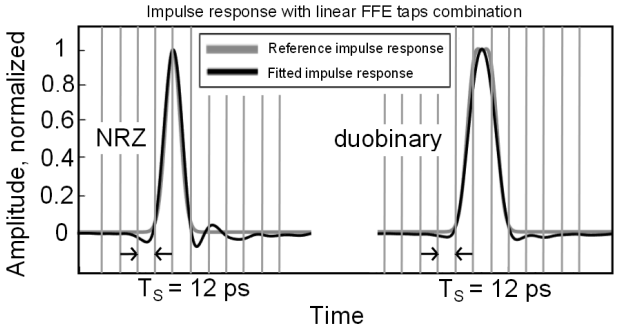


Figure 4.10: Equalized channel response fitted to NRZ or duobinary response

As shown in Figure 4.10, it is clear that the FFE is capable of matching the main cursors of the NRZ or duobinary channel. There is some remaining fitting error, resulting in residual ISI, which is however sufficiently small, proven by the evident NRZ or duobinary output shown in Figure 4.11.
In the next section, this FFE functionality is verified by the measured output eye diagrams (Figure 4.26 and Figure 4.27).

4.3.2.2 Time domain

In this part, the FFE functionality is verified in the time domain by eye diagram and BER measurements. As discussed in Section 3.3.2, thanks to the test configuration, the proposed FFE can be measured in two reverse directions, with the FFE input either from the output of the MUX, or from the external PPG. Therefore, the selection of the measurement setup depends on the available bit rate of the PPG. If the FFE is measured using the FFE test input-to-output signal path, then a single-channel data source is required. On the other hand, if the MUX-to-FFE signal path is used, then a quarter data rate is sufficient, however requiring four data channels applied in parallel. The block diagrams of the two measurement setups are shown in Figure 4.12. In Section 4.3.2, we demonstrate the time-domain measurements using the FFE test configuration and in Section 4.3.3, we illustrate the time-domain measurements using the MUX-to-FFE signal path.

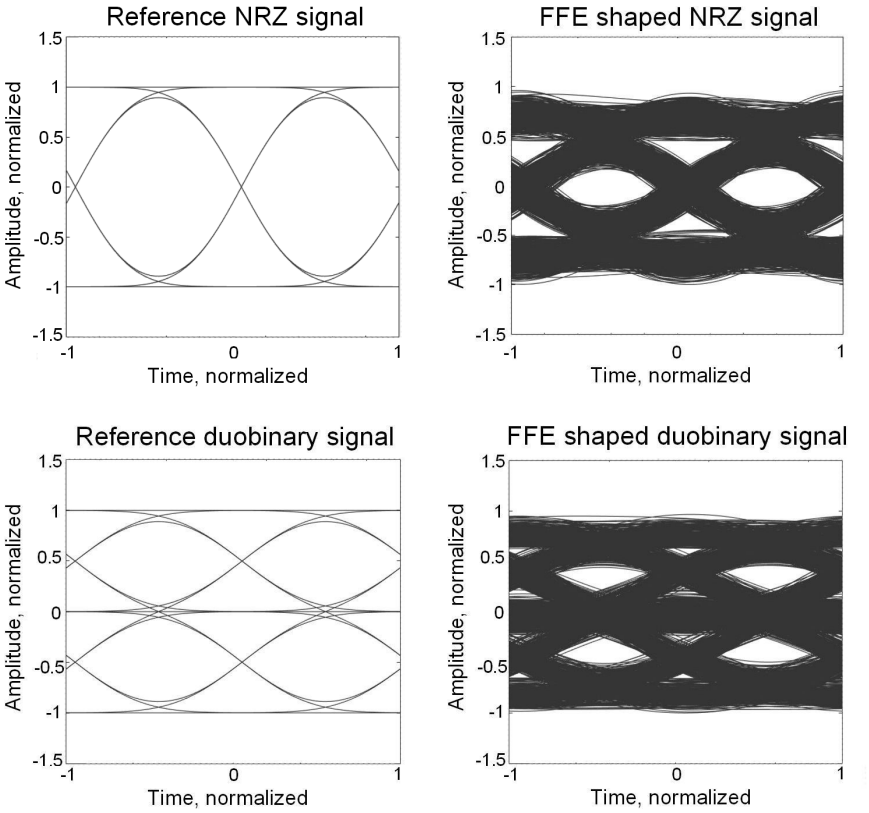


Figure 4.11: Simulated eye diagrams of the impulse response fitting

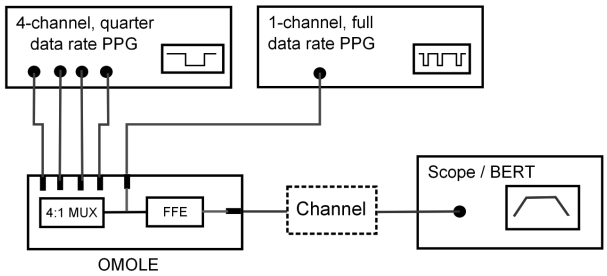


Figure 4.12: Block diagram of two optional time domain measurement setups

The experimental setup, with the external single-channel NRZ data source (up to 50 Gb/s or 56 Gb/s), is depicted in Figure 4.13.
As depicted in Figure 4.13, the data generator is connected to the test board

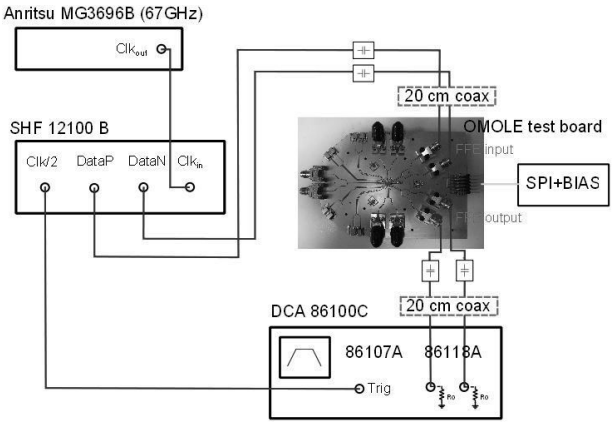


Figure 4.13: Time domain FFE measurement setup through the FFE test input / output

using a pair of 20 cm coax cables and two DC blocks. Meanwhile, the output of the FFE is connected to the scope / bit error rate tester (BERT) via a second pair of 20 cm coax cables and two DC blocks. Each of the coax cables adds a certain amount of losses. Figure 4.14 shows the measured loss of the RF coax cable. A 20 cm coax cable has about 1 dB of loss at 28 GHz.

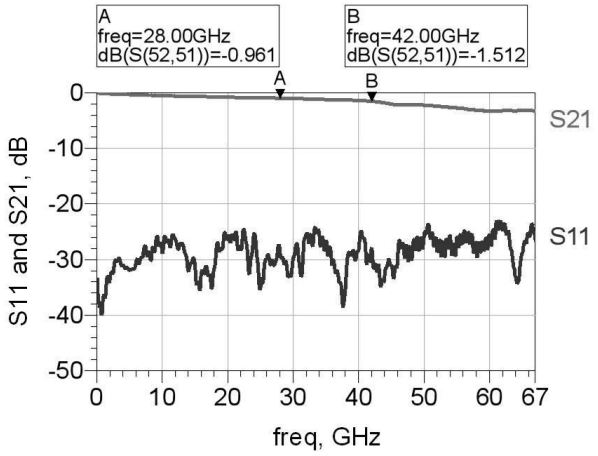


Figure 4.14: Loss and reflection of 20 cm coax cable

The amount of losses added by the test board depends on the input selection. In Figure 4.15, the additional loss in case of applying an external 56 Gb/s input is illustrated. At 28 GHz, the additional channel loss from

the test board is around 5.9 dB.

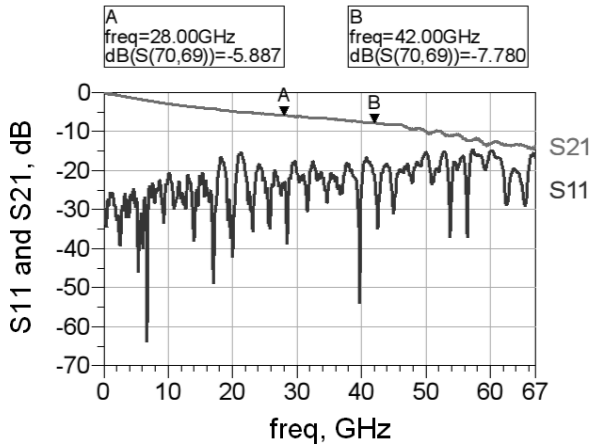


Figure 4.15: Loss and reflection of the output trace on the test board

The losses added by the different components in the experimental setup are summarized in Table 4.1. At 28 GHz, a total loss of 6.9 dB is added by the measurement environment.

	Channel loss at 28 GHz
FFE test output trace	5.9 dB
Coax FFE to scope	1.0 dB
Total loss	6.9 dB

Table 4.1: Summary of the losses added by the measurement environment

The FFE frequency domain measurements showed that the FFE is able to shape the channel up to 42 GHz, which indicates the capability to generate duobinary signals up to 84 Gb/s. In this part, the performance of the FFE is verified by time domain experiments showing the eye diagrams. However, the maximum data rate that we could apply to the FFE test input port was limited by the measurement equipment available in the lab. As shown in Figure 4.13, the maximum speed of the PPG SHF12100B is specified to be 50 Gb/s. Under good circumstances (e.g. low room temperature), the PPG output can be pushed to 56 Gb/s. However, at this speed there are some inherent bit errors generated by the PPG itself, with a back-to-back (PPG and ED directly connected) BER of around 10^{-9}. This means that in this

setup, the value of the measured BER at 56 Gb/s will not be absolutely correct, however, the measured output eye diagram and BER can still present a reasonable indication on the data transmission performance.
The 56 Gb/s equalized duobinary output eye diagram is presented in Figure 4.16, which has a very good vertical and horizontal eye opening of 57 mV and 12 ps (around 0.67 UI), respectively. Considering the eye quality of the FFE output, it is clear that this equalized signal can be decoded error-free by a proper duobinary RX. Such link experiments will be illustrated in Section 4.4 and 4.5.

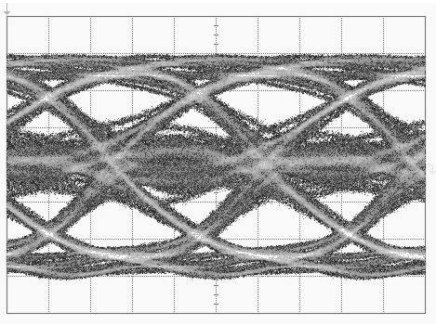


Figure 4.16: 56 Gb/s duobinary (PRBS 7) eye diagram of the FFE (5 ps/div, 50 mV/div)

4.3.3 Transmitter measurements

After showing the correct operation of the different building blocks, the combination of the MUX and FFE is tested. This is done by switching the output of the MUX to the input of the FFE instead of routing the MUX output to its output buffer. The block diagram of the time-domain measurements using the MUX-to-FFE signal path is elaborated in Figure 4.17.

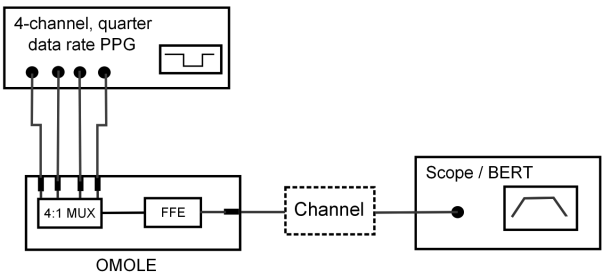


Figure 4.17: Block diagram of the TX time-domain measurement setup

4.3.3.1 Experimental setup

The experimental setup is depicted in Figure 4.18. The experimental connection between the test instruments and the test board inputs is the same as in Figure 4.1, where the MUX output is measured. The only difference is that the output of the MUX is sent to the input of the FFE, insteading of being measured directly. The TX output port is connected to the scope, via four different channels, in order to evaluate the equalization capabilities of the measured FFE for different channel losses. The settings of the FFE coefficients are adjusted via a custom SPI interface.

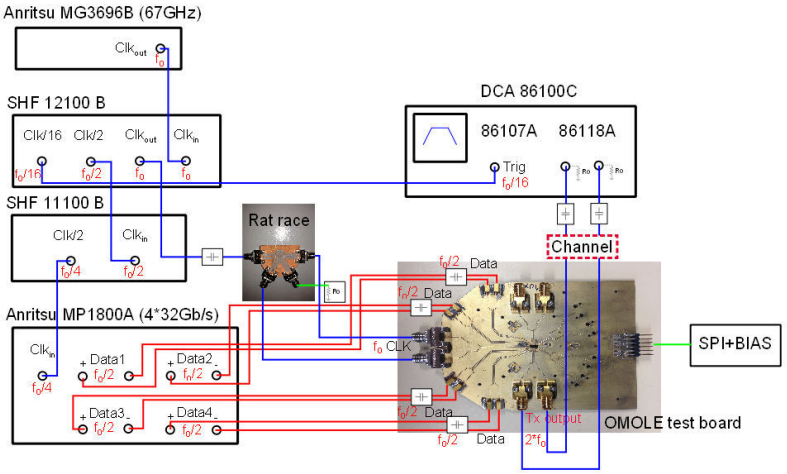


Figure 4.18: TX measurement setup

As analyzed in Section 4.3.2, the amount of losses added by the test board depends on the input selection. In Figure 4.19, the added loss of the TX output trace is illustrated. At 50 GHz, the added channel loss is 8.7 dB.
Using this setup, the eye diagram measurements were performed, while the FFE was used to compensate the channel loss, by means of introducing predistortion on the MUX signal waveform, in order to generate a maximum eye opening after the lossy channel.

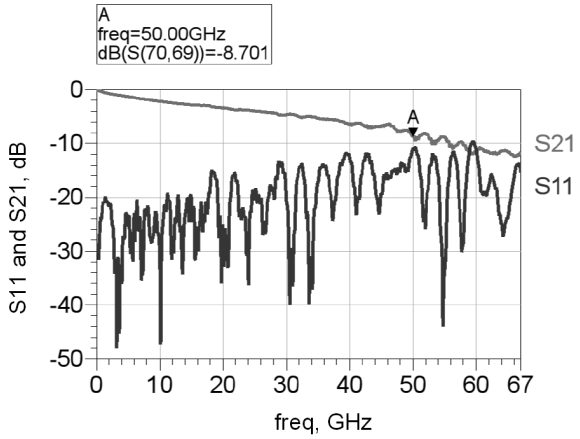


Figure 4.19: Loss and reflection of the TX output trace on the test board

4.3.3.2 Results

First of all, to verify the tap delay of the FFE, each of the five gain cells is turned on one-by-one, showing the tap-period delayed MUX outputs. As presented in Figure 4.20, the measured delay of the MUX outpus between neighboring taps is around 12 ps (12.36 ps, 12.25 ps, 11.53 ps, 12.07 ps), showing a good agreement with the FFE frequency domain measurements in Section 4.3.2.

To verify the operating range of the FFE, four different channels were added to the test board via coaxial connectors. The loss of the complete channels, including the TX output trace and the external channels, were measured and depicted in Figure 4.21.

By setting the correct coefficients for the FFE, the frequency response of the channel is shaped as expected which generates an open eye (either NRZ or duobinary) after the channel. These measurements illustrate that at maximal speed, NRZ is more difficult or more demanding for the FFE as the duobinary eye looks almost perfect.

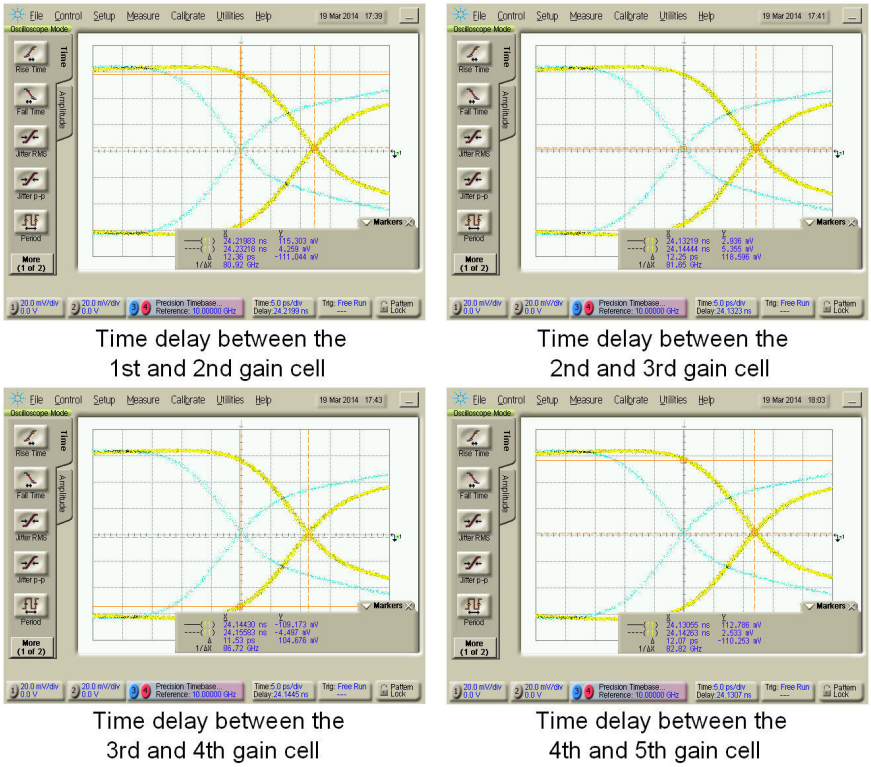


Figure 4.20: Measured tap delays of the FFE

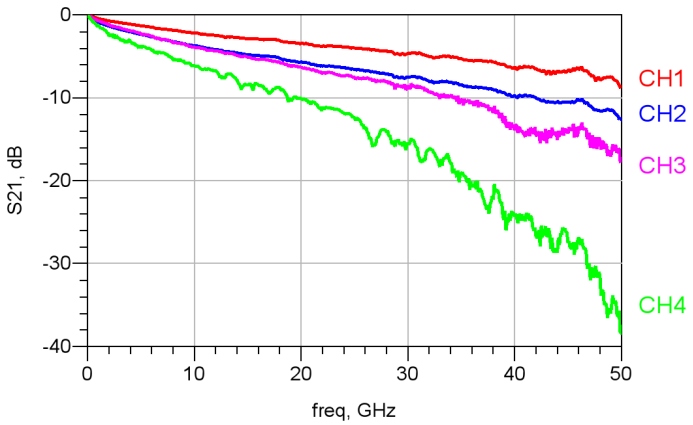
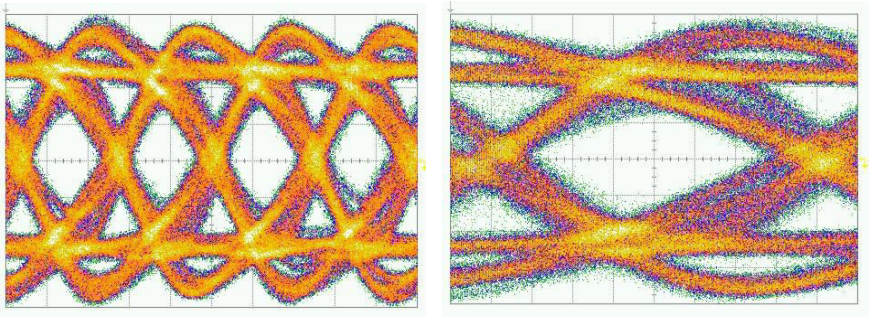


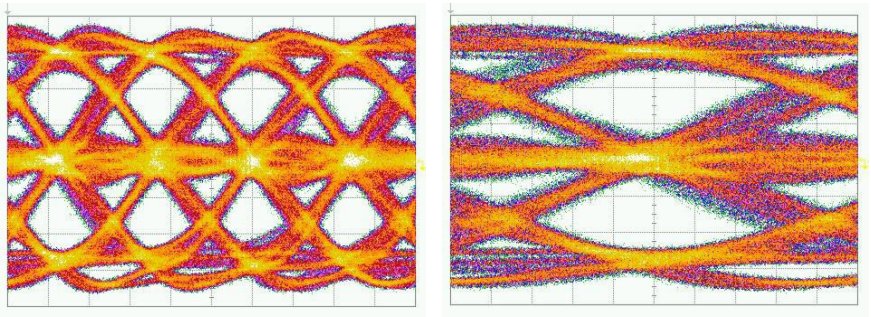
Figure 4.21: Measured loss of various channels

Channel 1: 5 cm coax By setting the tap weights in the FFE, the eye diagrams of the equalized NRZ and duobinary output after Channel 1 at 84 Gb/s are generated as illustrated in Figure 4.22 and Figure 4.23. The NRZ eye opening is 41 mV, while the duobinary eye opening is 47 mV.



5 ps/div, f_0=42 GHz 1.5 ps/div, f_0=42 GHz

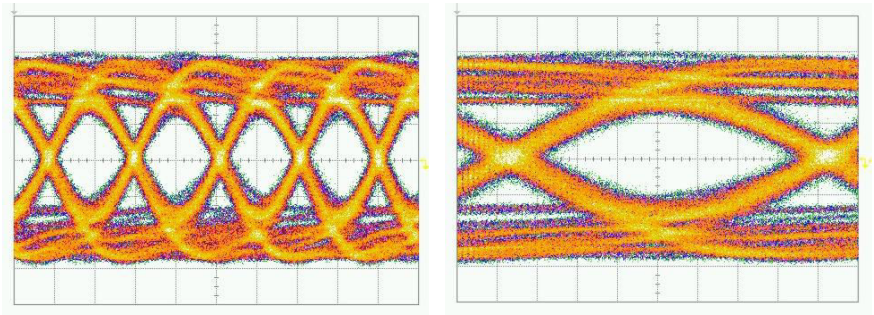
Figure 4.22: 84 Gb/s after Channel 1: NRZ



5 ps/div, f_0=42 GHz 1.5 ps/div, f_0=42 GHz

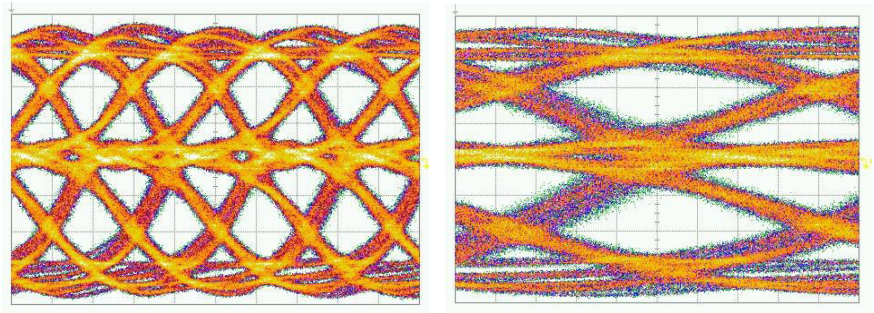
Figure 4.23: 84 Gb/s after Channel 1: Duobinary

Channel 2: 80 cm coax By setting the tap weights in the FFE, the eye diagrams of the equalized NRZ and duobinary output after Channel 2 at 64 Gb/s and 84 Gb/s are generated as presented in Figure 4.24, Figure 4.25, Figure 4.26 and Figure 4.27. The NRZ eye openings at 64 Gb/s and 84 Gb/s are 49 mV and 32 mV, respectively, while the duobinary eye openings at 64 Gb/s and 84 Gb/s are 49.6 mV and 38 mV, respectively.



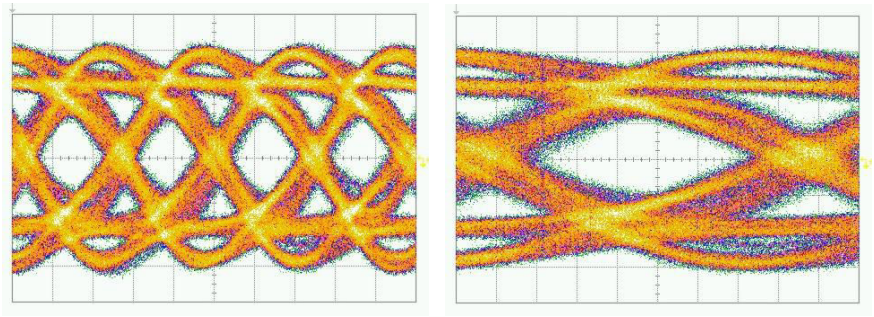
7.5 ps/div, f_0=32 GHz 2 ps/div, f_0=32 GHz

Figure 4.24: 64 Gb/s after Channel 2: NRZ



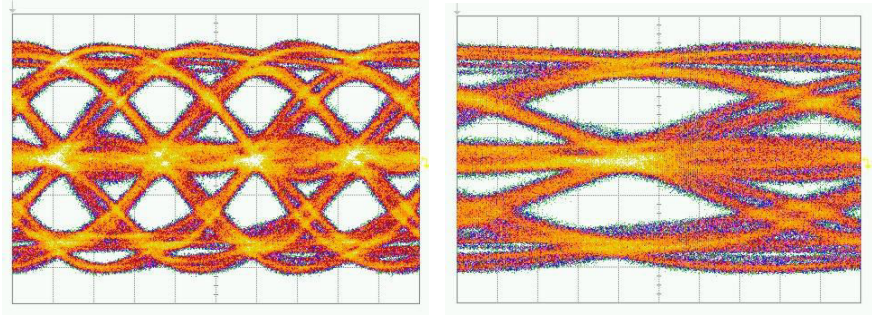
7.5 ps/div, f_0=32 GHz 2 ps/div, f_0=32 GHz

Figure 4.25: 64 Gb/s after Channel 2: Duobinary



5 ps/div, f_0=42 GHz 1.5 ps/div, f_0=42 GHz

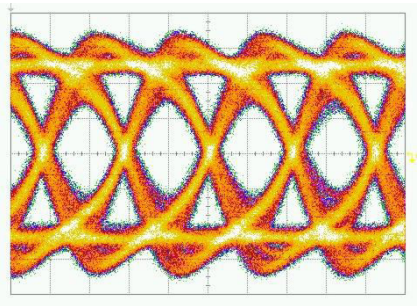
Figure 4.26: 84 Gb/s after Channel 2: NRZ



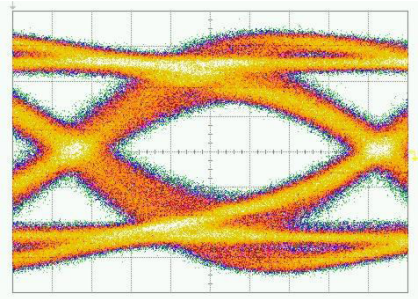
5 ps/div, f_0=42 GHz 1.5 ps/div, f_0=42 GHz

Figure 4.27: 84 Gb/s after Channel 2: Duobinary

Channel 3: 5 cm coax + 5 cm FX-2 differential stripline + 5 cm coax
By setting the tap weights in the FFE, the eye diagrams of the equalized NRZ and duobinary output after Channel 3 at 64 Gb/s and the eye diagrams of the equalized duobinary output at 84 Gb/s are generated as shown in Figure 4.28, Figure 4.29 and Figure 4.30. The NRZ eye opening at 64 Gb/s is 32 mV, while the duobinary eye openings at 64 Gb/s and 84 Gb/s are 39.5 mV and 26 mV, respectively. Due to the BW limitation of Channel 3, open eye diagrams after the channel at 84 Gb/s NRZ were not obtained.

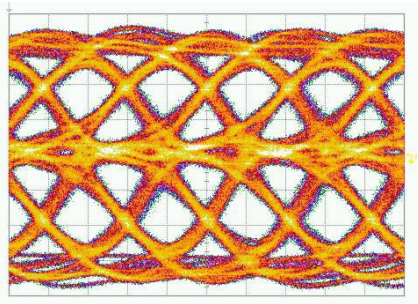


7.5 ps/div, f_0=32 GHz

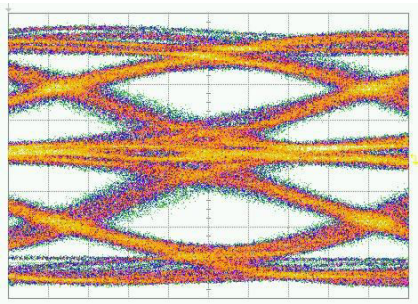


2 ps/div, f_0=32 GHz

Figure 4.28: 64 Gb/s after Channel 3: NRZ

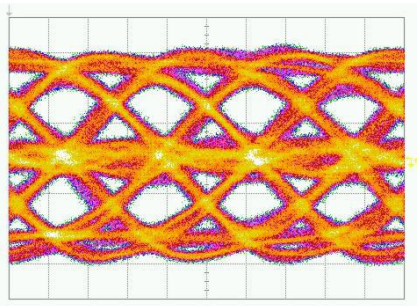


7.5 ps/div, f_0=32 GHz

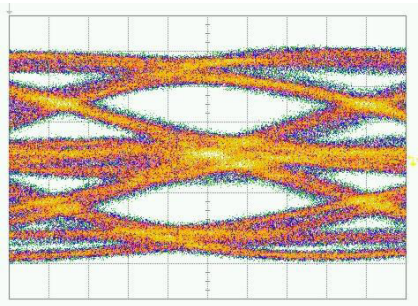


2 ps/div, f_0=32 GHz

Figure 4.29: 64 Gb/s after Channel 3: Duobinary



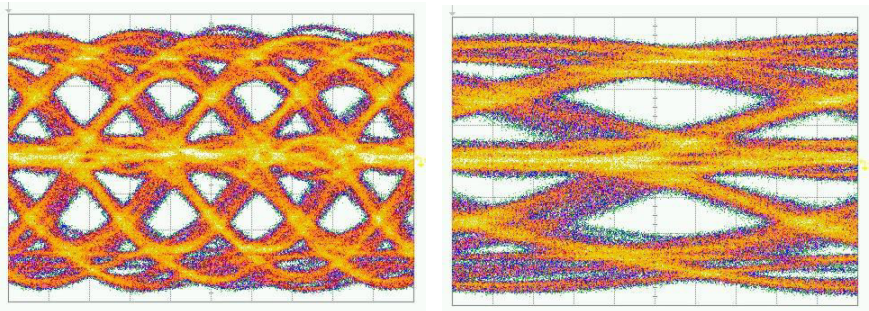
5 ps/div, f_0=42 GHz



1.5 ps/div, f_0=42 GHz

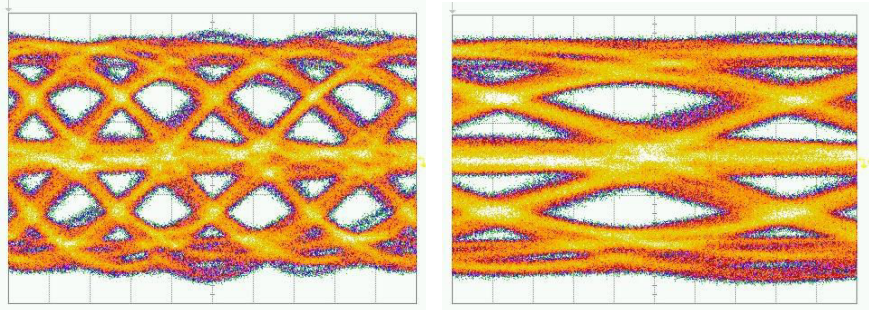
Figure 4.30: 84 Gb/s after Channel 3: Duobinary

Channel 4: 5 cm coax + backplane connector + 5 cm coax By setting the tap weights in the FFE, the eye diagrams of the equalized duobinary output after Channel 4 at 64 Gb/s and 72 Gb/s are generated as illustrated in Figure 4.31 and Figure 4.32. The duobinary eye openings at 64 Gb/s and 72 Gb/s are 26.5 mV and 16 mV, respectively. Due to the BW limitation of Channel 4, no open eye diagrams were achieved for the equalized NRZ output at 64 Gb/s, 72 Gb/s and 84 Gb/s, while duobinary failed only at 84 Gb/s.



7.5 ps/div, f_0=32 GHz 2 ps/div, f_0=32 GHz

Figure 4.31: 64 Gb/s after Channel 4: Duobinary



6.3 ps/div, f_0=36 GHz 2 ps/div, f_0=36 GHz

Figure 4.32: 72 Gb/s after Channel 4: Duobinary

4.3.3.3 Conclusion on the FFE measurements

An overview of the measurement results for all these channels with regards to NRZ and duobinary in different data rates is summarized in Table 4.2 and 4.3.

	64 Gb/s	72 Gb/s	84 Gb/s
Channel 1	–	–	√
Channel 2	√	–	√
Channel 3	√	–	√
Channel 4	√	√	X

Table 4.2: A summary of the measured FFE outputs with different data rates for duobinary

	64 Gb/s	72 Gb/s	84 Gb/s
Channel 1	–	–	√
Channel 2	√	–	√
Channel 3	√	X	X
Channel 4	X	X	X

Table 4.3: A summary of the measured FFE outputs with different data rates for NRZ

The extensive FFE measurements show that the FFE is able to work up to 84 Gb/s. This maximum data rate for duobinary is determined by the 12 ps tap spacing of the on-chip TMLs. As expected, the eye opening of the equalized output signal decreases with an increasing channel loss. Compared with NRZ, duobinary modulation is preferable for transmitting higher data rate signals over lossy channels, as duobinary signaling has a higher spectral efficiency compared to NRZ and makes use of the intrinsic BW limitation of the channels as part of the desired duobinary frequency shaping. This leads to a higher eye opening and lower overshoot for duobinary signals.
In this measurement setup, the time-domain FFE function was tested compensating a channel consisting of the traces on the test board, combined with an external channel. So for the channels with too high losses for

84 Gb/s, we showed the measurement results at lower data rates. To measure the standalone FFE functionality, it would be interesting to measure the TX output on the die by using high BW probes on both the clock input and the TX output. This will not only help to improve the MUX signal quality at the input of the FFE, but it will also increase the BW of the TX output, allowing to measure the actual performance of the FFE without the trace losses introduced by the test board.

4.4 Transmitter to receiver data links over PCB traces

After verifying the TX functionality, the TX is connected to the RX, which allows for further data transmission evaluation using BER measurements. The TX receives four NRZ data streams, combines them to one aggregated stream and performs predistortion on this signal using the FFE. This predistorted signal is transmitted over a channel located between the TX and RX, forming an NRZ or duobinary shaped waveform at the input of the RX. In case of duobinary, the RX captures the waveform and after some initial amplification it will extract the upper and lower eye of the duobinary waveform, which will be provided to the XOR and demultiplexer (DeMUX) circuit, used to decode the duobinary waveform and to split the received waveforms into 4 parallel lanes at the quarter-rate.
In this section, the TX-to-RX link measurements are demonstrated either back-to-back, or via differential PCB traces. In Section 4.5, serial data link measurements over commercial backplanes are presented.

4.4.1 Experimental setup

The back-to-back measurement setup is illustrated in Figure 4.33. In this setup, a clock signal is needed for both TX and RX, provided via a power splitter. This passive power splitter will introduce an extra 6 dB loss in the clock path. Recalling the MUX eye quality degradation at very high frequencies due to limited clock amplitude, a reduced performance at very high frequencies beyond 80 Gb/s is again expected.
During the different experiments, the setup was not altered, only the channel was adapted. The DC voltage levels of the TX output and RX input are not identical. Therefore, two high BW DC block capacitors are located between the two boards. In a practical backplane system, these DC blocks can be soldered on the TMLs. One lane of the DeMUX outputs is connected to the ED module of the Anritsu MP1800A, in order to complete the data tranmission loop, which allows to measure the BER of this communication channel. All the measurements are performed using four-channel

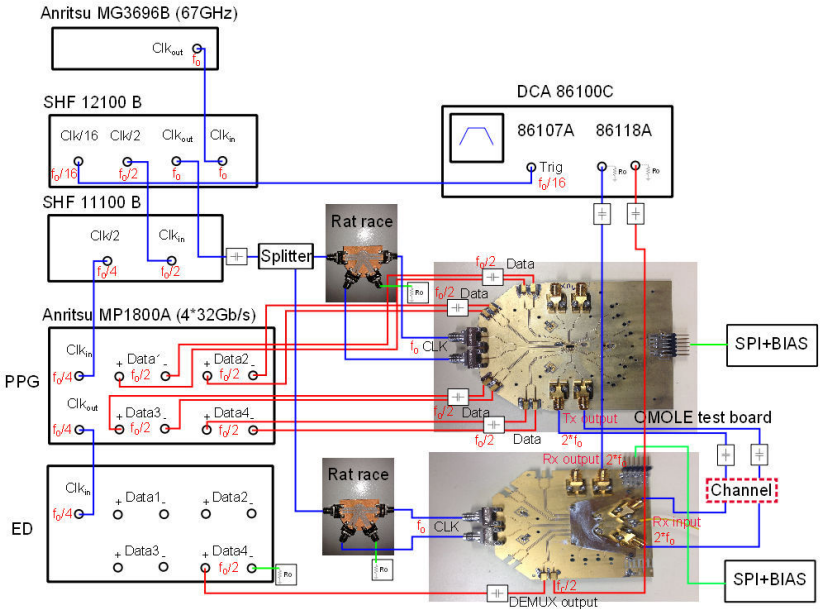


Figure 4.33: TX-to-RX measurement setup

MUX inputs of PRBS 7.

4.4.2 Results

To measure the performance of the TX/RX combination, two channels are added in between the two boards: a 10 cm coax pair or a 5 cm FX-2 differential PCB trace. These will form the total, to be compensated channel, together with the PCB traces on the TX and the RX test board. The loss of this complete channel, consisting of the PCB test boards plus an extra 10 cm coax pair (CH1) or a 5 cm FX-2 differential PCB trace (CH2) was measured with a VNA using high frequency probes on empty test boards. The obtained frequency characteristics are presented in Figure 4.34.

Channel 1 was measured using 64 Gb/s, 72 Gb/s and 84 Gb/s signals. For channel 2 only 64 Gb/s was measured. For each configuration the FFE coefficients were adapted to realize optimal channel shaping and the RX threshold levels are adapted for every measurement. At higher bit rates, duobinary modulation is used as the channel losses can be more easily compensated due to the higher spectral efficiency of the modulation format.

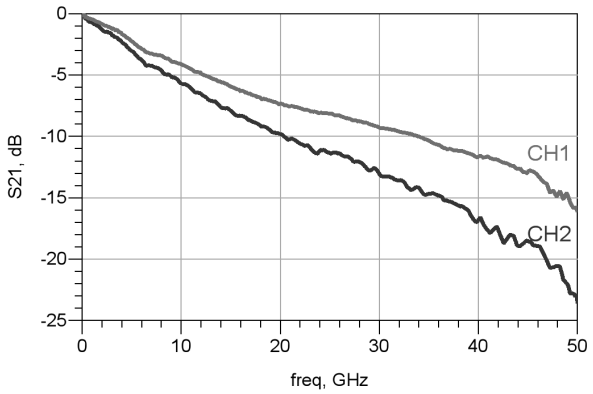
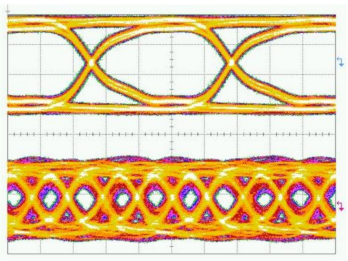


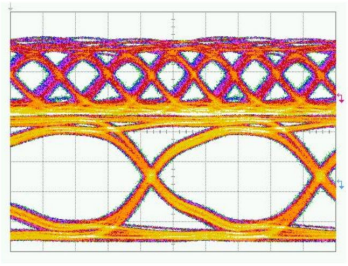
Figure 4.34: Measured loss of the complete channels between TX and RX

Channel 1: PCB test boards with 10 cm coax The serial chip-to-chip interconnection at 64 Gb/s, 72 Gb/s and 84 Gb/s over a 10 cm coax is tested. Equalization is performed to realize 64 Gb/s NRZ and duobinary modulation at 72 Gb/s and 84 Gb/s. After shaping the channel and determining the correct RX thresholds, 10^{-12} error-free data communcation at the output of the RX DeMUX was achieved in all of the three cases. The single-ended eye openings of the DeMUX outputs are around 180 mV, with the eye diagrams of the RX test output and DeMUX output depicted in Figure 4.35.

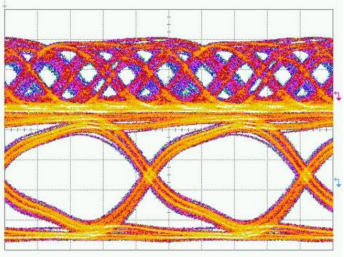
Channel 2: PCB test boards with 5 cm coax + 5 cm FX-2 differential stripline + 10 cm coax The serial chip-to-chip interconnection over Channel 2 is tested at 64 Gb/s. Equalization is performed to realize both NRZ and duobinary modulation over the channel. By setting the tap weights in the FFE and the threshold voltages in the level shifter, 10^{-12} error-free data communcation at the output of the RX DeMUX was achieved in both cases. The single-ended eye openings of the DeMUX outputs are around 180 mV, with the eye diagrams of the RX test output and DEMUX output illustrated in Figure 4.36.
It is clearly visible that there is still margin to increase the speed, but due to the limited available time with the Anritsu BER test equipment, it was not possible to test at higher data rates.



TX: 64 Gb/s NRZ, 15 ps/div
upper: DeMUX output, lower: RX test output

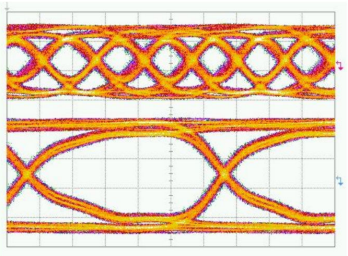


TX: 72 Gb/s duobinary, 10 ps/div
upper: RX test output, lower: DeMUX output

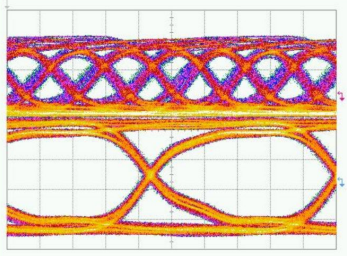


TX: 84 Gb/s duobinary, 10 ps/div
upper: RX test output, lower: DeMUX output

Figure 4.35: TX-to-RX interconnects with Channel 1



TX: 64 Gb/s NRZ, 10 ps/div
upper: RX test output, lower: DeMUX output



TX: 64 Gb/s duobinary, 10 ps/div
upper: RX test output, lower: DeMUX output

Figure 4.36: TX-to-RX interconnects with Channel 2

4.4.3 Conclusion

An overview of the measurement results of the two channels in different data rates is summarized in Table 4.4 and 4.5.

	64 Gb/s	72 Gb/s	84 Gb/s
Channel 1	–	√	√
Channel 2	√	–	–

Table 4.4: A summary of the back-to-back measurements with different data rates for duobinary

	64 Gb/s	72 Gb/s	84 Gb/s
Channel 1	√	–	–
Channel 2	√	–	–

Table 4.5: A summary of the back-to-back measurements with different data rates for NRZ

The back to back interconnection of TX and RX is demonstrated to work up to 84 Gb/s. The TX is able to compensate the channel losses from the test board and the external coaxial cable, and the RX is able to receive the equalized signal and to decode the signal correctly, showing 10^{-12} error-free chip-to-chip data communication.

In order to measure the BER of the data link, it is crucial to generate a serial PRBS sequence at the MUX output, by properly setting the delays between the four channels of the MUX inputs. Both equalized NRZ signaling and duobinary signaling are shown to work, while duobinary modulation performs better for higher data rates as it uses the channel BW more efficiently.

In addition, it is observed that a sufficiently strong clock amplitude is critical to ensure a good performance for both TX and RX. In this measurement setup, the clock amplitude is not sufficiently strong due to the limited output level from the clock signal generator and the signal attenuation over the coaxial cables. We observed the performance improvement by varying the clock amplitude. Therefore, a stronger clock signal is needed to compensate the loss over the cables and the PCB traces in the clock chain, or high BW probes should be used to apply the clock inputs to the chips to get rid of the signal attenuation over the traces on the test boards.

Finally, in order to achieve the error free result at 84 Gb/s, the settings of the FFE and the RX level shifters were derived by first looking at the RX test outputs and then further optimized by looking at the ED until the BER of the data link improved to 10^{-12}, which we consider as error-free.

4.5 Transmitter to receiver data links over commercial backplanes

4.5.1 Introduction

In this section, we investigate the transmission performance over a Megtron 6 backplane link, applying the same FFE to evaluate both NRZ and duobinary in a fair way for different rates and interconnect lengths. By changing the response of the equalizer, the transmitted data format over the backplane can be either standard two-level NRZ signaling or partial response duobinary signaling. In this way, a transmission comparison between NRZ and duobinary using the same equalizer and the same backplane characteristics is performed. The BER measurement clearly illustrates that duobinary allows transmission over a longer backplane at the same rate or at higher rate over the same backplane. Finally, we demonstrate the electrical duobinary transmission over two kinds of commercial backplane demonstrators, with data rates beyond 48 Gb/s. This operational serial data rate is faster than previously reported electrical backplane links [12]- [15], and is nearly two times the intended speed of the commercial backplane channels.

4.5.2 TE STRADA Whisper backplane demonstrator

4.5.2.1 Backplane channels

As illustrated in Figure 4.37, the backplane used in this experiment is a customer evaluation backplane intended for 25 Gb/s transmission, fabricated with Panasonic Megtron 6 material, including STRADA Whisper connectors between the backplane board (BP) and the daughter cards (DC) [16]. In this part, we operated the experiments with backplane channel lengths from 11.5 inch to 27 inch, and extended their performance through real-time duobinary signal generation and real-time signal processing.

Figure 4.37: TE STRADA Whisper backplane demonstrator

The insertion losses of the backplane transmission channels are measured and depicted in Figure 4.38.

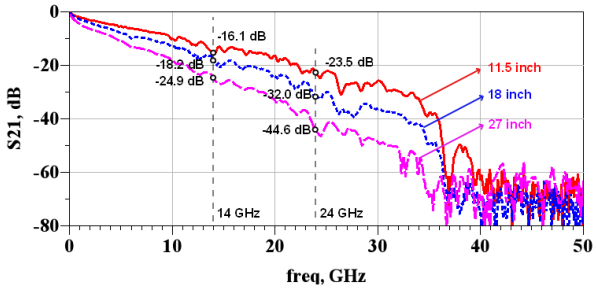


Figure 4.38: Insertion loss of backplane demonstrator channels with lengths of 11.5 inch, 18 inch and 27 inch

4.5.2.2 Experimental setup

The measurement setup is shown in Figure 4.39. The output of the data source is differential, which is directly launched into the differential inputs of our high BW, 5-tap FFE with a neighboring tap delay of around 12 ps. The FFE chip is flip-chipped on a test circuit board. The differential output of the FFE is connected to one DC of the backplane via a pair of phase matched 20 cm RF cables. On the other side of the channel, the other DC of the backplane is differentially connected to the RX front-

end, via another pair of 20 cm cables. The FFE provides pre-emphasis, so that the equalized output signal after the transmission channel, including a Megtron 6 backplane, PCB test boards and RF cables, is shaped to either an NRZ or a duobinary signal. The RX chip, which is able to receive either NRZ or duobinary signals, consists of a duobinary front-end which decodes the duobinary signal to NRZ, and a 1-to-4 DeMUX which is differentially connected to the ED module (SHF 11100B).

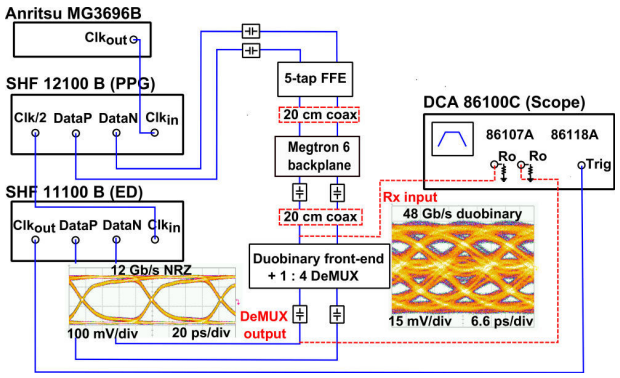


Figure 4.39: Experimental test setup for 48 Gb/s duobinary serial transmission over an 11.5 inch Megtron 6 backplane

Figure 4.40 depicts the losses added by the FFE and the RX PCB test boards. Each of the coax cables adds a certain amount of loss to the total link, which is around 1.5 dB at 50 GHz.

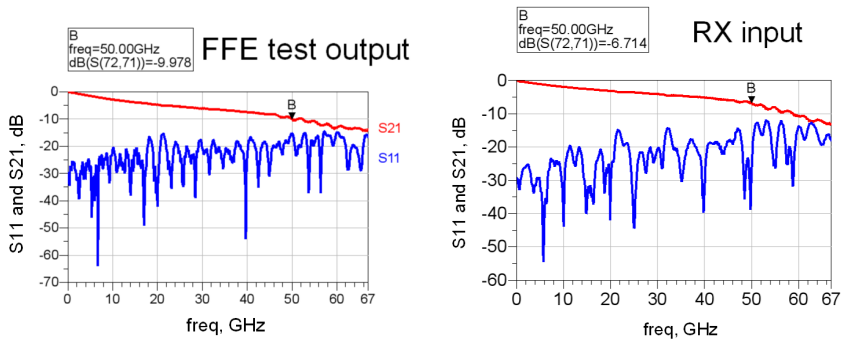


Figure 4.40: Loss and reflection of the PCB traces added to the backplane channel

The overall insertion loss of the backplane transmission channels is measured and depicted in Figure 4.41.

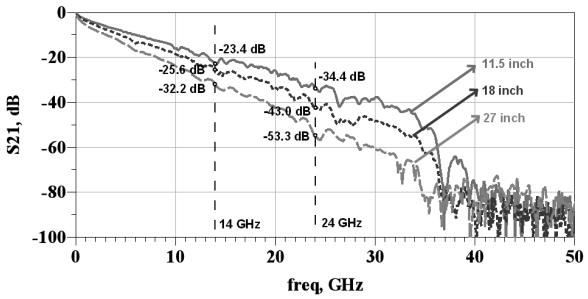


Figure 4.41: Channel insertion loss including TE backplane and the PCB test boards

4.5.2.3 Results

Eye diagrams of the received NRZ and duobinary signals with different data rates and over different lengths of backplane channels are presented. For both modulation schemes, the FFE works with NRZ input data, only the tap weights are chosen differently in order to optimize the NRZ pattern or to produce a duobinary signal. All backplane transmission experiments were carried out differentially. In Figure 4.42, the equalized output eye diagrams after an 11.5 inch backplane channel with increased data rates up to 48 Gb/s are illustrated, with the backplane channel equalized by the available FFE. Due to the remaining channel losses, however, it is important to remark that the equalized NRZ signals actually start to look like duobinary signals beyond 36 Gb/s, as presented in Figure 4.42. This observation, intuitively indicates that at high data rate, it is more efficient to decode duobinary signals than to put more effort (so more FFE taps) on the equalization of the NRZ signals.

In order to compare the equalization performance of NRZ signaling to duobinary signaling over higher loss channels, the equalized output eye diagrams of 28 Gb/s NRZ signals and 28 Gb/s duobinary signals are presented in Figure 4.43. One can see that beyond 18 inch, the equalized duobinary signals have higher eye openings than NRZ, which implies that it is easier to decode duobinary than NRZ.

In order to verify and compare the backplane transmission performance, the BER of NRZ and duobinary signaling is measured over an 11.5 inch backplane link with increasing data rates from 28 Gb/s to 48 Gb/s (Figure 4.44). Moreover, a BER lower than 10^{-13} is measured using 28 Gb/s duobinary signaling for a 27 inch long backplane, while a much higher BER of around 10^{-3} is measured for 28 Gb/s NRZ over the 27 inch backplane. This com-

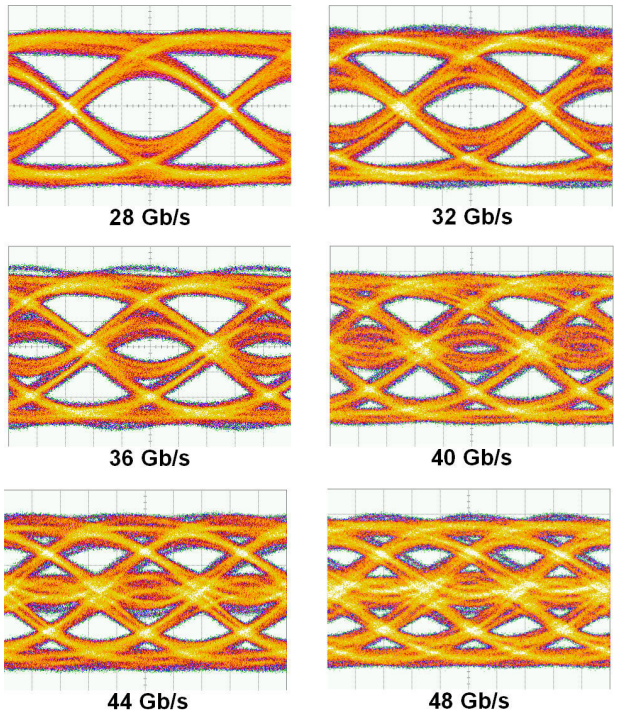


Figure 4.42: Equalized eye diagrams after applying 5-tap FFE through an 11.5 inch backplane (vertical: 15 mV/div, horizontal: 6.6 ps/div)

parison of NRZ and duobinary transmisson over a backplane channel with the same equalizer and RX electronics, concludes that duobinary signaling can be applied to transmit higher data rates over the same backplane length, or to transmit over a longer backplane channel at the same speed.

4.5.2.4 Conclusion

In this section, we have demonstrated a 48 Gb/s duobinary serial data link over a Megtron 6 backplane. By optimizing the equalizer and duobinary decoder characteristics, data transmission with a BER lower than 10^{-13} is measured across an 11.5 inch backplane, with transmitted data rates up to 48 Gb/s, which is almost two times the intended speed of the backplane channel. This result indicates that duobinary, compared to NRZ, is an interesting modulation format that can be applied in high speed or long reach backplane applications, outperforming NRZ in either data rate or channel length.

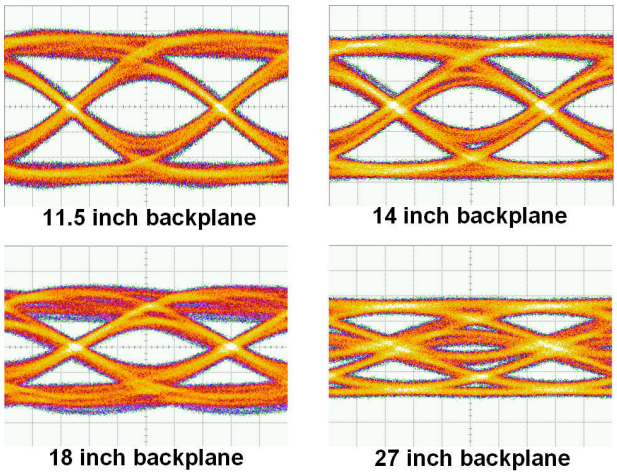


Figure 4.43: Equalized 28 Gb/s output eye diagrams after applying 5-tap FFE through different backplane lengths (vertical: 15 mV/div, horizontal: 6.6 ps/div)

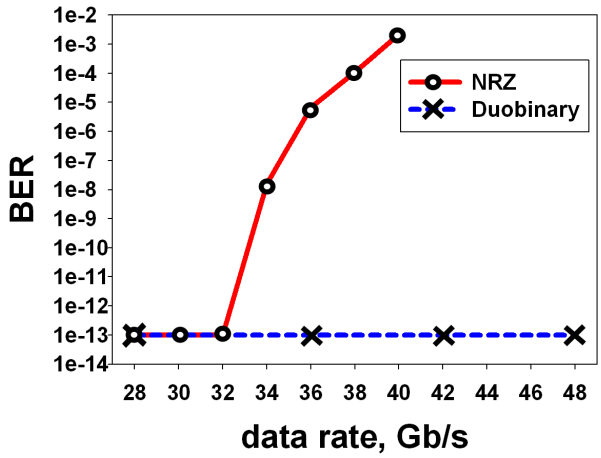


Figure 4.44: NRZ and duobinary BER measurements with increasing data rates over an 11.5 inch backplane

4.5.3 FCI ExaMAX® backplane demonstrator

4.5.3.1 Backplane channels

As shown in Figure 4.45, the backplane used in this experiment is a customer evaluation backplane demonstrator, consisting of two DC plugged

into a BP using 2 ExaMAX® connectors.

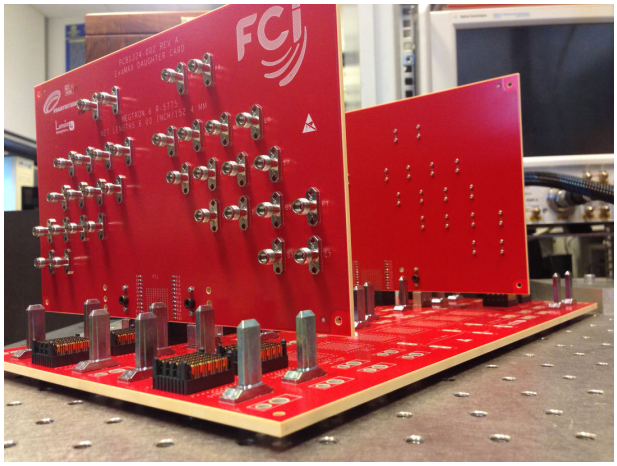


Figure 4.45: FCI ExaMAX® backplane demonstrator

The BP has 24 PCB layers, with a thickness of 4.1 mm. The DC has 18 PCB layers, with a thickness of 2.4 mm. The trace lengths on the BP vary between 1.7 inch and 26.75 inch, and the trace length on each of the DCs is 6 inch. This results in a minimum total interconnection length of 13.7 inch (35 cm). Similar to the TE STRADA Whisper backplanes, the material used for building the BP and DC of the FCI ExaMAX® backplane demonstrator is also Megtron 6, which introduces a channel loss of around 1.3 dB per inch at 28 GHz.

4.5.3.2 Experimental setup

The time-domain backplane transmission measurement setup illustrated in Section 4.5.2 is reused for these experiments, with the only change of replacing the TE STRADA Whisper backplane by the FCI ExaMAX® backplane demonstrator. The signal after the FFE travels along the FFE output trace on the test board, a pair of 20 cm coax cables, the FCI ExaMAX® backplane channel, a second pair of 20 cm coax cables and the input trace on the RX test board, to finally reach the RX duobinary front-end. Each component in the signal path adds a certain amount of loss to the overall link loss. A summary of the losses added by the experimental setup is listed in Table 4.6.

	Channel loss at 20 GHz
FFE test output trace	4.8 dB
Coax TX test board to FCI backplane	0.8 dB
FCI backplane	IL dB
Coax FCI backplane to RX test board	0.8 dB
RX input trace	3.1 dB
Total loss	9.5 + IL dB

Table 4.6: Summary of the losses added by the experimental setup

As elaborated in Table 4.6, at 20 GHz, a total loss of around 9.5 dB is added by the measurement setup, including the PCB test boards and the coax cables.
The overall insertion loss of the channel between the FFE and the RX duobinary front-end, including the backplane channel and the losses introduced by the experimental setup, is depicted in Figure 4.46.

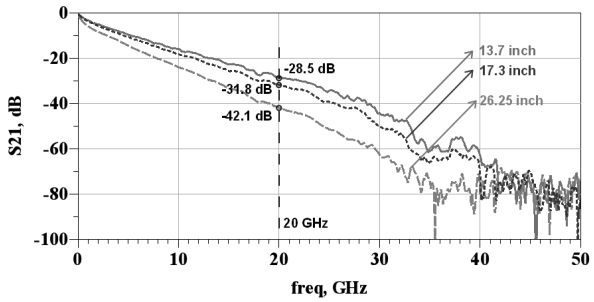


Figure 4.46: Channel insertion loss including FCI backplane and the PCB test boards

4.5.3.3 Results

The time-domain measurements started with a 40 Gb/s data rate on the shortest backplane link, which is 13.7 inch long (around 34.8 cm). The overall channel loss at the Nyquist frequency (20 GHz) is 28.5 dB, resulting in a duobinary output (after the backplane), with a vertical and horizontal eye-opening of 18.2 mV and 15 ps (0.6 unit interval) respectively, compared to the corresponding TX output (before the backplane) with an eye-opening

of 93.4 mV and 19.1 ps (0.76 unit interval) at 40 Gb/s. Both eye diagrams are shown in Figure 4.47.

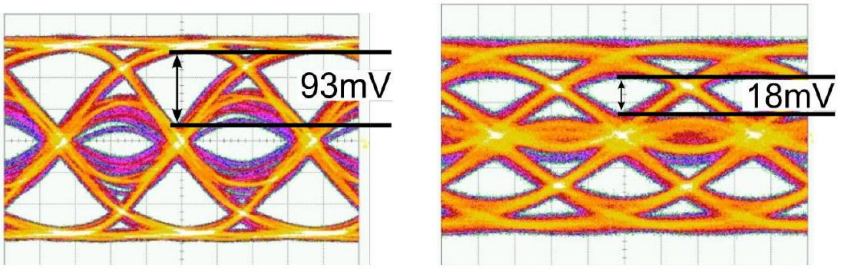


Figure 4.47: 40 Gb/s output eye diagrams travelling across a 13.7 inch FCI backplane channel (Left figure: vertical 50 mV/div, horizontal 7 ps/div; Right figure: vertical 20 mV/div, horizontal 7 ps/div)

The duobinary output after the 13.7 inch backplane, which is presented in Figure 4.47, gives an error-free data transmission when connected to the RX duobinary decoder. In order to explore the maximum channel length and the maximum channel loss for 40 Gb/s data transmission over the FCI ExaMAX® backplane demonstrator, the eye-pattern and BER measurements over longer backplane channels (17.3 inch, 20 inch and 26.25 inch) are performed. Longer backplane channels lead to higher frequency-dependent losses and smaller output eye-openings. The duobinary outputs after 20 inch and 26.25 inch backplane channels are depicted in Figure 4.48. with a vertical eye-opening of 11 mV and 5 mV, respectively. In each of the measurements with different lengths, the FFE and duobinary decoder is optimized, in order to achieve the best transmission performance.
The BER measurements of the 40 Gb/s signal over different channel lengths are presented in Figure 4.49. Error-free duobinary transmission is achieved up to the 20 inch backplane, with a total channel loss of up to 36.8 dB at the Nyquist frequency. And for an overall channel loss of 42.1 dB (over a 26.25 inch backplane), a BER below $5 \cdot 10^{-9}$ is achieved, which is acceptable for a data link with forward error correction (FEC) within the current 25 Gb/s IEEE 802.3bj standard [17].
Moving towards higher speed signals over the shortest 13.7 inch backplane link, the maximum data rate over the FCI backplane with ExaMAX® connectors is explored. In Figure 4.50, the equalized output eye diagrams with increased data rates up to 56 Gb/s are depicted, with vertical eye-openings of 6.8 mV at 50 Gb/s, and of 6 mV at 56 Gb/s, respectively.
In order to verify the transmission performance, the BER of the duobinary

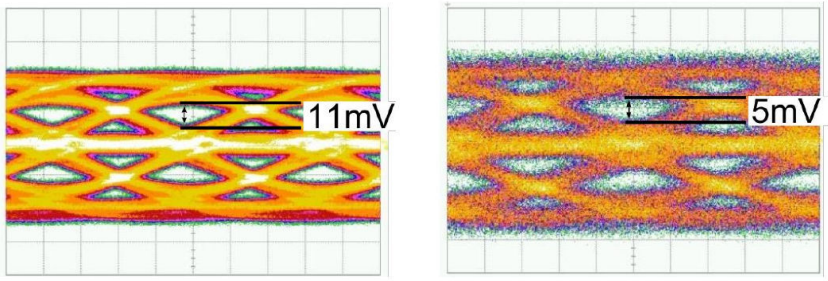


Figure 4.48: 40 Gb/s output eye diagrams travelling across different backplane lengths (Left figure: vertical 20 mV/div, horizontal 7 ps/div; Right figure: vertical 10 mV/div, horizontal 5 ps/div)

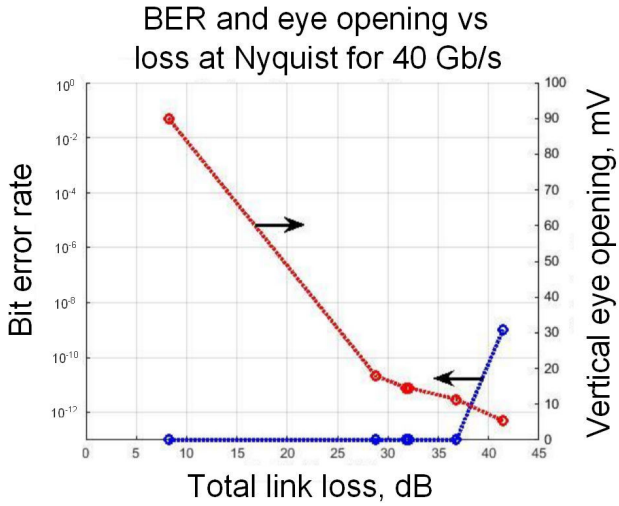


Figure 4.49: The vertical eye-opening (red) and the BER (blue) as a function of the overall channel loss at the Nyquist frequency for 40 Gb/s signal transmission over the FCI backplane

signaling is measured, with a BER lower than 10^{-13} up to 50 Gb/s. At 56 Gb/s, the obtained BER is lower than $5 \cdot 10^{-9}$, which is more than sufficient assuming FEC is applied.

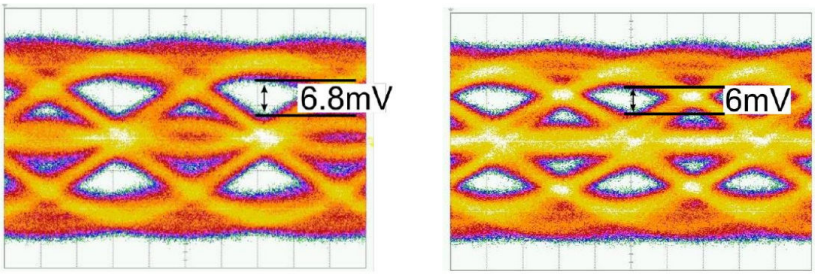


Figure 4.50: Output eye diagrams through a 13.7 inch FCI backplane (vertical: 10 mV/div, horizontal: 5 ps/div)

4.5.3.4 Conclusion

In this experiment, it is shown that 56 Gb/s data transmission across the currently available backplane channels and with mature SiGe BiCMOS chip technology is possible using duobinary signaling and using an FFE with only 5 taps. No other types of equalization techniques (e.g. decision-feedback equalization, continuous-time linear equalization) have been applied in the experimental setup. The measurement results indicate that it is possible to transmit 56 Gb/s duobinary signals successfully over a backplane channel with up to 40 dB of losses at the Nyquist frequency.

4.6 Conclusion

The 4-to-1 MUX is able to output up to 100 Gb/s serial NRZ data, the FFE is able to shape a smooth channel to a 84 Gb/s duobinary channel. The RX is able to receive and decode an 84 Gb/s duobinary signal and the XOR/DeMUX is able to clock in the data and complete the decoding of the duobinary signal and to output 4 quarter rate data streams.
The TX and RX, connected with a 10 cm coaxial cable, showed a serial 84 Gb/s duobinary transmission link with a BER lower than 10^{-11}. This test was done using an Anritsu MP1800A BER analyser with 4 output data streams running at 21 Gb/s. The electrical transmission between the TX and the RX over two commercial Megtron 6 backplanes was demonstrated at 48 Gb/s and 50 Gb/s respectively. To our best knowledge, until the date of publishing, they were the fastest serial electrical duobinary links over an electrical backplane, with a measured BER lower than 10^{-13} [10] [18].

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5 Conclusion

5.1 Summary of this work

This dissertation presents high-speed signal equalization and transmission in electrical interconnections. An integrated TX chip including a 5-tap FFE has been developed to be employed in backplane communication systems, using NRZ or duobinary modulation formats. As digital chips (e.g. FPGAs), are limited in interface speed to 32 Gb/s, an on-chip MUX combining four channels of lower-speed input signals is required and implemented in the TX chip to feed the high-speed FFE, which was the main focus of my research. This requirement triggered the conception of an innovative FFE circuit architecture, allowing to characterize the MUX and the FFE separately [1]. Apart from the integrated circuit implementation, after mounting the designed chips on the test boards with flip-chip bonding, system level demonstrations have been performed at record speeds, leading to several national and international publications, both in journals and in proceedings of conferences.

This research was mainly performed under the IWT ShortTrack project, aiming to develop high-speed backplane solutions and transceivers for next-generation telecom systems and data centers. The background of this research, an overview of this work and the organization of this dissertation are illustrated in Chapter 1.

In Chapter 2, a system level analysis is presented, showing that BW limi-

tations due to frequency dependent losses are the dominant factors limiting the transmission speed over backplanes. In order to enhance serial data rates over backplanes and to reduce the signal degradation, several technologies have been discussed, including signal equalization and modulation techniques. First, a prototype backplane channel was characterized. Second, a transversal filter as FFE has been selected to perform the signal equalization, based on a comprehensive consideration of the backplane channel performance, equalization capabilities, implementation complexities and overall power consumption. NRZ, duobinary and PAM-4 are the three most common modulation schemes for ultra-high speed electrical backplane communication. After a system level simulation and comparison, the duobinary format has been selected due to its high BW efficiency and reasonable circuit complexity. Last, different IC technology processes were compared and the ST 130 nm SiGe BiCMOS9MW process (featuring an f_T value of over 200 GHz) was selected, based on a trade-off between speed and chip cost. Meanwhile its design kit also provided an integrated microstrip model, which is utilized as the delay element in the FFE.

Chapter 3 illustrates the chip design of the high-speed integrated TX, consisting of a MUX and a 5-tap FFE. The 4:1 MUX combines four lower rate streams into a high-speed differential NRZ signal for the FFE input. The 5-tap FFE is implemented with a novel topology for improved testability, such that the FFE performance can be characterized, in both frequency- and time-domain, without disconnecting the MUX, which also helps to perform the coefficient optimization of the FFE [2]. The total chip, including the MUX and the FFE, consumes 750 mW from a 2.5 V supply and occupies an area of 4.4 mm $\times$ 1.4 mm, showing progress beyond the state-of-the-art in both speed and power efficiency.

In Chapter 4, the TX chip operating at up to 84 Gb/s is demonstrated. First of all, the 4:1 MUX is measured up to 100 Gb/s. An open eye is obtained at the MUX output up to 84 Gb/s. The output eye quality at 100 Gb/s is, however, degraded, due to the BW limitation of the PCB test traces and due to a limited clock amplitude available to the MUX. Second, the FFE performance is characterized in the frequency domain, showing that the FFE is able to work up to 84 Gb/s using duobinary formats. Besides the operation of the sub-blocks in the TX, the combination of the MUX and the FFE is tested. The TX chip performance is evaluated at different data rates between 64 Gb/s and 84 Gb/s driving four channels with different frequency-dependent losses for both NRZ and duobinary signaling. After applying an integrated RX, a serial electrical transmission link is demonstrated across a pair of 10 cm coaxial cables or a 5 cm FX-2 differential stripline, at 84 Gb/s and 64 Gb/s respectively. The 5-tap FFE compensates a total loss between

the TX and the RX of about 13.5 dB at the Nyquist frequency, and the RX receives the equalized signal and decodes the duobinary signal to 4 channels of quarter rate NRZ. This allows chip-to-chip data communication with a BER lower than 10^{-11} [3]. Last, the electrical data transmission between the TX and the RX over two commercial backplanes is demonstrated. In [4], an error-free, serial electrical duobinary transmission across a commercial Megtron 6, 11.5 inch backplane is demonstrated at 48 Gb/s, which indicates that duobinary outperforms NRZ for attaining high-speed or long-reach backplane transmission. Later on, using an ExaMAX® backplane demonstrator, duobinary transmission over electrical backplanes is verified and the maximum allowed channel loss for a 40 Gb/s transmission is explored [5]. The eye pattern and BER measurement over a longer backplane channel up to 26.25 inch are performed. The results show that a total channel loss up to 37 dB at the Nyquist frequency can be compensated to achieve an error-free duobinary transmission, and a total channel loss of 42 dB at the Nyquist frequency can be compensated to achieve a BER lower than 10^{-8}.
Some suggestions for further research in this field are provided in the next section.

5.2 Future work

First of all, as mentioned in the introduction of this work, the relentless growth of data traffic and increasing signal processing capabilities are demanding ever faster electrical interconnects. By using more advanced semiconductor processes with smaller feature size, the electronic transceiver performance will be improved, with higher speed or lower power consumption. At the same time, the continuously increasing fabrication precision has opened possibilities to optimize the electrical channel characteristics. Therefore, it is believed that, after attacking these technological boundaries, the transmission rate over serial electrical interconnections can be pushed further towards 112 Gb/s, with a comparable or even lower total power consumption. Besides electrical links, optical applications such as active optical cables can also benefit from the presented circuits.
Second, all research effort will be in vain if support from the industry is missing. Therefore, an intensive collaboration with industrial partners should eventually contribute to the standardization of next generation electrical backplane transmission system, which is a crucial aspect for broad-scale development and deployment. This research work successfully demonstrated a serial 50 Gb/s data transmission over a 30 cm backplane, which suggests the potential realization of 400 Gb/s Ethernet transceivers with 8

lanes at 50 Gb/s.
Last but not least, although this work contributes to the advancement of the state-of-the-art in the field of high-speed transceivers and backplane transmission, some extra features (e.g. adaptive FFE with automated coefficients calibration, clock and data recovery) are still required for a commercially easy-to-use system. Also the chip area of the TX can be significantly reduced to lower the cost or to integrate multiple TXs in a multi-lane chip.

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