Design and Technology of Ultra Thin Chip Packages for High-Frequency Applications up to 60 GHz

Ontwerp en technologie voor ultradunne chipverpakkingen voor hoogfrequentietoepassingen tot 60 GHz

Liang Wang

Promotoren: prof. dr. ir. J. Vanfleteren, dr. W. De Raedt, dr. ir. M. Cauwe
Proefschrift ingediend tot het behalen van de graad van
Doctor in de Ingenieurswetenschappen: Elektrotechniek

Vakgroep Elektronica en Informatiesystemen
Voorzitter: prof. dr. ir. J. Van Campenhout
Faculteit Ingenieurswetenschappen en Architectuur
Academiejaar 2013 - 2014

UNIVERSITEIT GENT

ISBN 978-90-8578-654-2
NUR 959
Wettelijk depot: D/2013/10.500/87

Ghent University
Faculty of Engineering and Acchitecture
Centre for Microsystmes Technology

Promoters:

Prof. dr. ir. Jan Vanfleteren (Ghent University)

Ir. Walter De Raedt (IMEC)

Dr. ir. Maarten Cauwe (Ghent University)

Other Members of the Examination Committee:

Prof. dr. ir. Rik Van de Walle (Ghent University), *Chairman*

Prof. dr. ir. Johan Bauwelinck (Ghent University), *Secretary*

Prof. dr. ir. Bart Nauwelaers (KU Leuven)

Ir. Philippe Kertesz (Thales Airborne Systems)

Table of Contents

Summary

In recent years, the demand for communication bandwidth has been growing rapidly. In order to have a higher bandwidth, the operating frequency needs to be increased proportionally. The current research focuses on developing a communication system working at 60 GHz, which is appealing as the next generation wireless standard. One of the main challenges in developing the 60 GHz system is how to package the RF CMOS chips with high efficiency and low cost. This is not an easy task can be accomplished using existing package technologies, such as advanced wire bonding or flip chip. Although the wire bonding technique can achieve a fairly small pitch connection, its long bonding wires also introduce excessive parasitic inductance, which can not be well compensated. The parasitic factors require excessive power and degrade the performance achieved at chip level. The flip chip assembly, on the other hand, can improve the high frequency performance of the mounted package. However, flip chip puts rather strict requirements on the substrate where the chip is mounted on. First the substrate has to be rigid and second the size and pitch of the substrate has to match dimension of the bond pads on the chip. This makes it difficult to flip chip package advanced RF chip using standard low cost board.

In order to overcome the current limitation of conventional packaging technologies, CMST has developed a unique concept for packaging ultra-thin chips: the Ultra Thin Chip Package (UTCP). In this technology, silicon chips with thickness below 30 µm can be embedded inside organic resin, composing of cured spin-coated polyimide layers. The interconnection to the chip is realized by forming micro-via through the coated top polyimide film to chip bond pads. The micro-via based connection is able to meet the fine pitch requirement for the chip connection. Moreover, a fan out design on the package level can bridge the pitch mismatch between the chip and coarse circuit board. The UTCP is able to be used independently or serves as an interposer, which can be further embedded inside PCB or FCB (flexible circuit board) and replace the needs for directly embedding of bare die. Furthermore, the known good die (KGD) problem is solved, because the functionality of UTCP can be easily tested before embedding it in the main board.

So far UTCP is designed and fabricated as a single chip package for low frequency application (<5 GHz) only. The aim of this PhD is to exploit the use of UTCP to go beyond the current limitation and develop design strategies for embedded modules at radio frequency up to 60 GHz. Such work opens a door for ultra-miniaturized high speed system and gives a cost effective powerful hybrid solution for the next generation RF packaging.

According to the main objective and the scope of this PhD work, the fabrication process of the UTCP technology is first optimized to make it more suitable for high volume manufacturing and high speed transfer. All individual process steps of UTCP technology are discussed in detail in Chapter 2. The original dielectric material PI-2611 is replaced by a photo-sensitive polyimide HD-4110. By using the new material, the generation of microvias can be achieved by generic photolithography process, which is more reliable than laser ablation and more cost-effective compared to dry etching based microvia generation. An easy release of the UTCP from the rigid carrier is obtained by introducing an evaporated potassium chloride (KCl) film before the deposition of base polyimide layer. The result is a very thin and flexible chip package with a total thickness around 50 µm.

Another further improvement of UTCP fabrication is presented in Chapter 3. Flat package topography is a key to build up multilayer structure on the UTCP package. An innovative self-alignment lithography step is introduced to make a cavity in dielectric for chip thickness compensation by using the chip itself as a photo-mask. The realized flat UTCP does not increase its total thickness and still can be released from the carrier. The feasibility of the updated fabrication process is verified by DC electrical test and several reliability tests. Desired flexibility and reliability is observed.

Chapter 4 presents high frequency material characterization of HD-4110, which is used in UTCP fabrication. A 3D full wave simulation is employed for modeling and parameter extraction. Its dielectric constant and loss tangent factor is extracted from 10 MHz up to 60 GHz. The extracted material property is well fitted by a rational dielectric model, which satisfies the causality constraints.

Two types of transition structure were fabricated for high frequency connection of UTCP embedded chips. Their design, fabrication and characterization are discussed in Chapter 5. One type of connection is CPW to CPW transition and the other type is MSL to CPW transition. The transmission and reflection coefficient is extracted for both transition

structures from 10 GHz up to 60 GHz. A good impedance matching and small insertion loss can be achieved by both transition structures. Compared with the results of the other advanced package methods from literatures, the UTCP package shows one of the best performances.

The thin film deposition technique for the UTCP fabrication can also be applied to produce thin film passive devices. In the frame of EU SHIFT project, off-chip RF passives are produced based on thin film technology. Finally, Chapter 6 briefly describes the process flow and shows measurement results of the realized passive elements including resistor, spiral inductors and a low pass filter. Since the applied fabrication technique is compatible with the UTCP processing, the passive elements and the UTCP can be integrated together to work as a complete system.

Samenvatting

De vraag naar bandbreedte voor communicatietoepassingen is recent sterk gestegen. De toename in bandbreedte wordt veelal gerealiseerd door de werkingsfrequentie op te drijven. Het huidige onderzoek legt zich toe op het ontwikkelen van een communicatiesysteem dat werktbij 60 GHz, in overeenstemming met de toekomstige standard voor draadloze gegevensoverdracht. Een van de belangrijkste uitdagingen in de ontwikkeling van een dergelijk hoogfrequent systeem is een performante en betaalbare oplossing voor het verpakken van hoogfrequente CMOS chips. De huidige technieken voor het verpakken van chips, in het bijzonder draad- en flip-chip verbindingen, hebben elk hun nadelen voor hoogfrequente toepassingen. Draadverbindingen zijn compatibel met de geringe afstand tussen de bondpaden op de chip, maar de lange draadverbindingen hebben een grote parasitaire inductantie, wat nefast is voor transmissie van hoogfrequent signalen. Het gebruik van flip-chip assemblage kan deze problemen verhelpen, maar heeft dan weer het nadeel dat het zware eisen stelt aan het substraat waarop de chip gemonteerd wordt. Dit substraat dient niet alleen rigide te zijn, maar de grootte van de structuren op het substraat moet overeenkomen met de afstand tussen de bondpaden op de chip. Gezien hoogfrequente chips gebruik maken van zeer geringe afstanden tussen de bondpaden, resulteert dit in zeer dure substraten en dus een hoge totale kost.

De hogervermelde tekortkomingen van de huidige verpakkingstechnieken kunnen vermeden worden door gebruik te maken van de ultradunne chip verpakking UTCP, welke ontwikkeld werd binnen CMST. Deze technologie maakt gebruik van silicium chips met een dikte van minder dan 30 µm, welke ingebed worden in lagen van uitgehard polyimide. De verbinding met de chip wordt gerealiseerd aan de hand van microvias doorheen de bovenste polyimide laag tot op de bondpaden van de chip. Deze op microvias gebaseerd verbinding is compatibel met de geringe afstand tussen de bondpaden op de chip. Daarenboven laat deze technologie toe om het verschil in grootte van de structuren op de chip t.o.v. het substraat te overbruggen. De ultradunne chip verpakking kan alleenstaand gebruikt worden of als tussenoplossingen ingebed worden in een al-dan-niet flexibele gedrukte schakeling. Door het uitspreiden van de contactpaden kan de chip voor het inbedden getest worden, wat niet mogelijk is bij naakte chips.

Tot nu toe werd de ultradunne chip verpakking steeds ontworpen en gerealiseerd voor laagfrequente toepassingen (<5 GHz). Het doel van dit doctoraatsonderzoek is om de prestaties van de ultradunne chip verpakkingen voor frequenties tot 60 GHz te evalueren. Hiertoe zullen specifieke ontwerpregels opgesteld worden die het mogelijk maken om sterk geminiaturiseerde systemen te bouwen voor de hoogfrequente toepassingen van de volgende generatie.

Teneinde de doelstellingen van dit doctoraatswerk te kunnen bereiken, werd het fabricageproces voor ultradunne chip verpakkingen herbekeken met het oog op productie in grote volumes. Alle processtappen voor het realiseren van de ultradunne chip verpakking worden in detail beschreven in hoofdstuk 2. Het diëlektrische materiaal PI-2611, wat oorspronkelijk gebruikt werd voor het realiseren van ultradunne chip verpakkingen, werd vervangen door het fotogevoelige polyimide HD-4110. Dankzij deze wijziging kunnen de microvias verwezenlijkt worden met behulp van een foto-lithografisch proces, welke betrouwbaarder is dan laser boren en goedkoper dan het gebruik van droge etstechnieken. Het losmaken van de ultradunne chip verpakking van de rigide drager wordt vergemakkelijkt door het opdampen van een kalium chloride (KCl) film voor het aanbrengen van de eerste polyimide laag.

Een bijkomende verbetering in het fabricageproces wordt beschreven in hoofdstuk 3. Een vlakke topografie van de verpakking is essentieel om meerlaagse structuren binnen de ultradunne chip verpakking te realiseren. Hiertoe werd een innovatie lithografie stap geïntroduceerd waarbij een caviteit rond de chip gerealiseerd wordt in het fotogevoelige polyimide. De totale dikte van de afgevlakte ultradunne chip verpakking blijft echter gelijk. De haalbaarheid en de betrouwbaarheid van het vernieuwde fabricageproces worden aangetoond aan de hand van elektrische testen. De gewenste betrouwbaarheid en flexibiliteit werden hierbij behaald.

Hoofdstuk 4 beschrijft de hoogfrequente materiaalkarakterisering van HD-4110. Een driedimensionale golfsimulatie wordt gebruikt voor het bepalen van de parameters. De diëlektrische constante en de verlieshoek warden berekend voor een frequentiebereik van 10 MHz tot 60 GHz. De gevonden waarden komen goed overeen met het opgestelde fysische model, welke voldoet aan de vereisten van causaliteit.

Twee types overgangen tussen de chip en de ultradunne verpakking warden ontworpen en gerealiseerd. Het ontwerp, de fabricage en de karakterisering worden beschreven in hoofdstuk 5. Het eerste type is een overgang van vlakke golfgeleider naar vlakke golfgeleider. Het andere type maakt gebruik van een tussenliggende microstrip golfgeleider. De transmissie- en reflectiecoëfficiënt werd voor beide overgangen bepaald in een bereik van 10GHz tot 60 GHz. Een goede aanpassing van de impedantie en lage verliezen kunnen met beide overgangen gerealiseerd worden. In vergelijking met overgangen gebruikt in andere hoogfrequent verpakkingstechnieken, presteert de ultradunne chip verpakking bovenmaats.

De dunne-filmtechnieken die gebruikt worden voor het realiseren van de verbindingen in de ultradunne chip verpakking kunnen eveneens toegepast worden voor het fabriceren van passieve elementen. In het kader van het Europees project SHIFT werden dergelijke passieve componenten gerealiseerd. Hoofdstuk 6 beschrijft de bijhorende processtappen en bespreekt de meetresultaten van de gerealiseerde weerstanden, spoelen en laagdoorlaatfilters. Gezien de toegepaste technologieën volledig compatible zijn met de ultradunne chip verpakking kunnen beide technieken op eenvoudige manier gecombineerd worden.

List of Acronyms

Acronym	Description
ACA	Anisotropic Conductive Adhesive
BCB	Benzocyclobutene
BEOL	Back End of Line
BGA	Ball grid array
BBUL	Bumpless Build-Up Layer
CiP	Chip in Polymer
COB	Chip-On-Board
COF	Chip-On-Flex
CSP	Chip Scale Package
CTE	Coefficient of Thermal Expansion
CPW	Coplanar Waveguide
DIP	Dual In-line Package
EBGA	Enhanced Ball Grid Array
ECG	Electrocardiogram
EEG	Electroencephalogram
EPC	Embedding Passive Component
ENIG	Electroless Nickel / Immersion Gold
EMG	Electromyogram
FBGA	Fine Pitch Ball Grid Array
FCB	Flexible Circuit Board
FCOB	Flip-Chip On Board
GSG	Ground Signal Ground
IC	Integrated Circuit
I/O	Input / Output

IMB	Integrated Module Board
ICA	Isotropic Conductive Adhesive
KGD	Known Good Die
LRM	Line-Reflection-Match
LCP	Liquid Crystal Polymer
MIM	Metal-Insulator-Metal
MSL	Microstrip Line
MCM	Multi-chip-module
PCB	Printed Circuit Board
PSPI	Photosensitive Polyimide
PVD	Physical Vapor Deposition
PI	Polyimide
PoP	Package on Package
QFP	Quad flat package
RIE	Reactive Ion Etching
SiP	System in Package
SMD	Surface Mount Technology
SoC	System on Chip
SOLT	Short-Open-Line-Thru
TAB	Tape Automated Bond
TFMSL	Thin Film Microstrip Line
TRL	Thru–Reflection-Line
TLine	Transmission line
TSV	Through Silicon Via
UBM	Under Bump Metallization
UTCP	Ultra Thin Chip Package
VNA	Vector Network Analyzer
WLP	Wafer Level Packaging

CHAPTER 1

General Introduction

1.1 Integrated circuit packaging

In electronic manufacturing, integrated circuit (IC) packaging is the final stage of device fabrication [1]. The main purpose of the IC packaging is to provide electrical connection between the chip and the external circuitry on the system board. Furthermore, the package should help for heat removal from on-chip transistors to the ambient air, and also protect the chip against environment contamination, such as dirt, finger prints, and moisture ingress. After the packaging step, device will be submitted to a functional test. So, in summary, IC packaging bridges the gap between the semiconductor chip manufacturing and the final product application [2], [3].

1.1.1 Requirements for IC packaging

The trend in semiconductor manufactorinng has significant impact on the evolution of IC packaging and interconnects [4-5]. According to Moores' law, the number of transistors on an integrated circuit will be doubled every 18 months [6]. This trend is first observed in 1965, and it is still valid today and expected to continue during the next decade. As a result of the Moores'

law, in the past century semiconductor chip technology has been improved continuesly in the following aspects [4],[7]:

1) The transistor dimensions are scaled down from sub-micrometer to around a few tens of nanometers. The current state-of-art lithography tool enables the minimum feature size in chip manufacturing to shrink from 0.8μm in 1990s to 22nm and even below;

2) Along with the increasing transistor density, more and more functionality can be integrated on a single chip. In the meanwhile, the number of chip input/output (I/O) counts needs to increase at the same pace to enable complex operations. For high end devices, the I/O counts increased from below 100 to over a few thousands by a rate of 50% (x1.5) every 18 months.

3) Although the supply voltage is reduced in every technology generation, the power density of the chip is increased almost exponentially with time from around 1 W/cm^2 to above 50 W/cm^2.

4) For the sake of faster computing speed, the operating clock frequency is also increased. In 1971, the first commercially available microprocessor Intel 4004 only works at 108 kHz [8], and the maximum record in 2011 has reached 5.2 GHz, which is 5000 times higher than the first one.

In the above discussed trend, the advances in semiconductor chips create great challenges to the packaging technology and reform the packaging method to adapt for new requirements in the following aspects:

1) The increasing I/O chip pin counts means that the same number of interconnect channels should be realized on package level. Assuming the chip area remains the same, which is normally the case, if more functionality is integrated, a tighter interconnect pitch is required. And correspondingly, the circuit on the package board should be more dense and fine.

2) When the dissipated power density becomes higher, the generated heat is also higher. If the heat cannot quickly spread to the ambient environment, it will be trapped around the chip, which may damage the chip functionality and cause some reliability problems. Thus packaging needs to improve interface materials, in order to obtain a better thermal conductivity. Sometimes, more complex cooling systems should be constructed in a package for better heat dissipation.

3) According to the microwave scaling rule, when the operating frequency becomes higher, all circuit dimensions should be scaled down proportionally to obtain the same performance. Therefore, the increasing chip clock rate requires the package circuit to have finer pitch and higher resolution. Low-k dielectric with low dielectric loss is preferred to reduce propagation delay time and signal power attenuation.

4) Apart from requirements driven by IC advances, one more need for packaging is miniaturization. For portable and mobile devices, it is important to control the weight and volume of the final product.

1.1.2 History of IC packaging

The requirements for IC packaging listed above are reflected on the package structures in its historic evolution. Fig. 1.1 shows different types of package during the past decades.

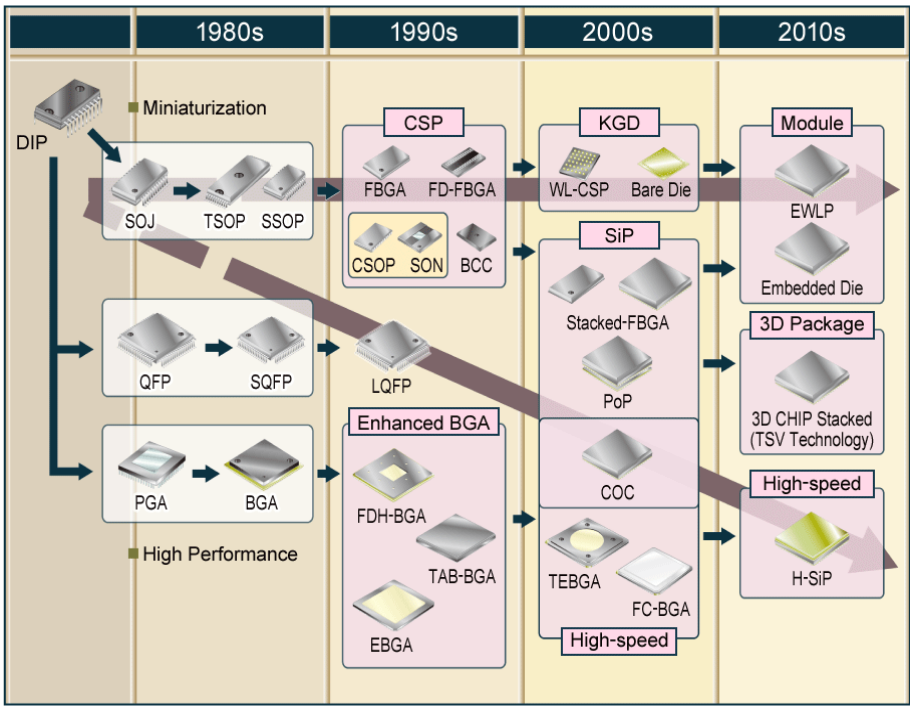

Figure 1.1 *The evolution of IC packaging*[9].

In the following context, we will briefly review some important packaging types, which are the most commonly used ones in the past and at present. The sequence of the description is mainly in chronological order starting from the 1970s up to now in steps of ten years.

1970s

Dual in-line Package (DIP) is the first to be discussed. DIP is a kind of through hole mounted package which was widely used in 1970s [10]. The above mentioned first commercial available microprocessor Intel 4004 was packaged in the standard DIP packaging [8]. As shown in Fig. 1.2, DIP packages are made of opaque molded plastic resin with plated lead frames. Inside the package, the IC chip is cemented in the center of a rectangular chamber and is connected to the outside through the lead frames. The package can be mounted by either through hole soldering to printed circuit board or inserting in sockets. DIP is a low cost and easy handling package with very robust attachment of lead in hole. However, the interconnect pitch is limited to about 2.5 mm and the number of I/O is limited to numbers below 64. Consequently, the circuit density on PCB board is also limited. The operating frequency of DIP is normally from 2 to 160 MHz.

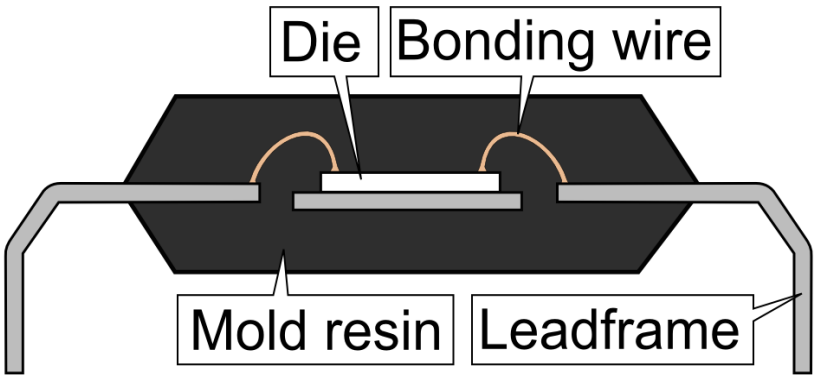

Figure 1.2 *Schematic cross section of DIP* [11]**.**

1980s

In order to avoid the cost of drilling holes in the PCB and to obtain a higher interconnect density, through hole technology was mostly replaced by surface mount technology (SMT) by the end of 1980s [12]. Two

representative types of SMT are quad flat package (QFP) [13] and the later invented ball grid array (BGA) package [14].

Although components in a QFP were first introduced in 1970s and already been used in Japanese consumer electronics since then, it became popular in the world until late eighties. QFP component is similar to DIP, which has four sides with leads extending from the component body to all four directions. But instead of through hole lead as DIP, QFP uses "gull wing" leads, as shown in Fig. 1.3, which can be mounted directly onto the surface of PCBs.

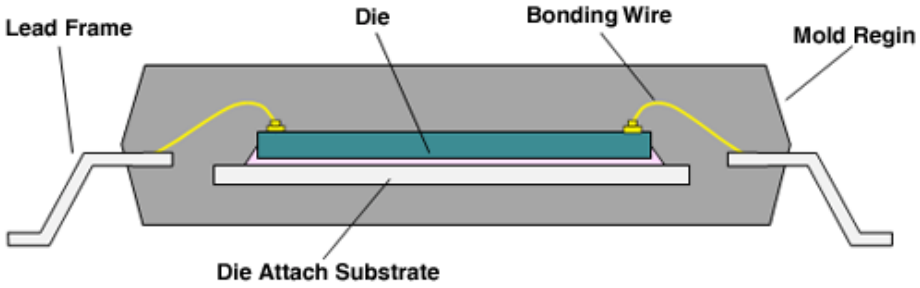

Figure 1.3 *Schematic cross section of QFP [15]*.

A QFP lead frame is normally made of iron/nickel alloy or copper alloy to guarantee good thermal and electrical performance. Because of its surface mount capability, compared to DIP component, QFP can achieve tighter lead pitch and higher I/O count. Different versions of QFP offer I/O counts ranging from 32 to 304 pins with a lead pitch from 0.4 to 1 mm. Therefore, QFP can allow increased circuit density on PCB.

However, QFP has connections only around the periphery of the package. In order to increase the number of pins, the interconnect pitch has to be reduced. This tight lead spacing may cause solder short problems and put higher demands on the soldering process with more advanced alignment of components. As a result, when tighter pitches are needed, the yield of QFP is relatively low and the overall cost becomes high. The later BGA package allows for high pin counts with similar package size, as well as alleviates the problem caused by close lead spacing.
BGA package utilizes laminated or ceramic multilayer interconnect substrate instead of metal lead frame. This multilayer interconnect substrate is also called as "interposer" of the package. The structure of BGA package is

shown in Fig. 1.4. In a BGA package, the chip is mounted on the multilayer substrate and interconnected through bonding wire. The area array connections from the package "interposer" to the PCB are realized using solder balls. These solder sphere can be placed manually or by automatic machine and held under the interposer with tacky flux until soldering begins. The BGA package is then placed on PCB contact pads, which has the same pattern of ball grid array. Normally, the soldering is carried out by heating the assembly in a reflow oven to melt the solder ball. Before solder balls cools down and hardens, surface tension aligns the package on PCB at correct separation distance.

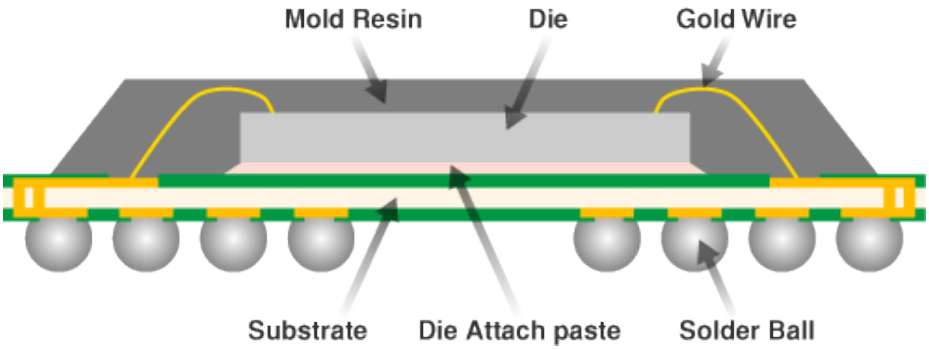

Figure 1.4 *Schematic cross section of BGA package[16].*

BGA package can alleviate the problem of producing a miniature IC package with hundreds of I/O counts. The ball pitch is normally of 1.00, 1.27 or 1.5mm, and the number of I/O can reach to 420. Besides the advantage of higher pin counts, the distance of solder ball connection between the package and PCB is shorter than leaded connection, which lowers the parasitic inductance and therefore minimizes the signal distortions in high speed application.

All package structures have their drawbacks, and BGA package is not an exception. There are mainly two problems in BGA package [17]. First, the thermal stress between the package interposer and PCB is accumulated at the solder joint, and becomes a reliability issue. So it's common to select a plastic material which more closely matches the thermal characteristic of PCB. Second problem is that it is hard to inspect the balls and joints for soldering defects, as the package is soldered down on the PCB. To overcome the second problem, various machines, were developed to look underneath the soldered package, such as x-ray machine, industrial CT scanning machine, as well as some special microscopes.

1990s

In the early 1990s, it becomes clear that the evolution of IC packaging proceeds toward two directions. One direction is developed for high-end electronic device, which has very high pin counts and high power consumption. The package for high-end devices needs to allocate more connect channel and has better thermal management. A couple of methods were proposed to meet the new requirements. Enhanced ball grid array (EBGA) is one of these methods, which has been widely used [18]. The other direction is to make miniature package for portable electronics. As the fast growing of mobile electronic market, there is a huge demand to make mobile devices smaller and lighter. Then it is necessary to shrink the size of IC packaging. The concept of chip scale package (CSP) was proposed and developed for portable devices [19]. A typical CSP is fine pitch ball grid array (FBGA) package. Next, we will describe the structures of EBGA and FBGA, and see what it the improvement in these two types of packaging.

EBGA is descended from traditional plastic BGA technology. With thermally and electrically enhancement, EBGA is capable to package chips for high-end devices. The configuration of an EBGA package is present in Fig. 1.5. As a descendant of BGA, connection between the package and the main board is still using solder balls. Inside EBGA, the chip is attached on a heat spreader in a face down cavity. The die attach material is a special compound with better thermal conductivity. So the heat generated from chip can quickly transfer to the spreader.

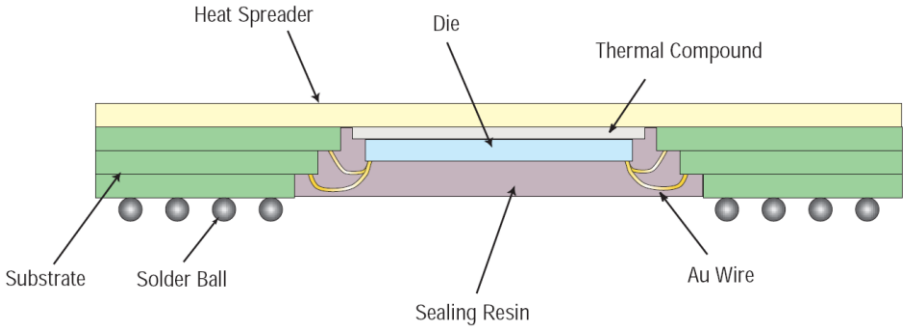

Figure 1.5 *Schematic cross section of a EBGA package [18].*

The connection of the chip to package is realized by wire bonding. Unlike normal BGA, two-tier substrate is offered in the EBGA for the wire bonding.

So, more I/O connections can be realized around the chip perimeter. Furthermore, the separation of power and ground planes in two-tie substrate can make electrical performance better. Normally, EBGA package can has total I/O counts up to 700.

Besides the direction for high-end electronics, CSP is the other package progress direction targeting for portable electronics. The definition of CSP is a single die surface mounted package with an area of no more than 1.2 times that of the original die area. The concept of CSP only put requirement on the package size without specific details in package structure. Various types of CSP were proposed, and flip chip CSP (fcCSP) is one of the main CSP solutions. The fcCSP is a miniature version of standard BGA, whose configuration is similar to the one shown in Fig. 1.4 except for the replacement of wire bonding by flip. However, fcCSP has a chip scale size, with lower profile and less weight than standard BGA. More importantly, fcCSP offers a finer solder ball pitch, ranging from 0.4 mm to 1 mm. The number of I/O is normally between 40 and 460. But the number of connection is not a stringent requirement for portable devices.

2000s

During the 21th century, package technology continues to develop towards two directions for high-end devices and portable devices. More advanced package methods were invented, such as wafer level packaging (WLP) [20]. The flip chip ball grid array (FCBGA) is another type of package, which already existed in 1990s and becomes popular in 21th century [21].

WLP is a true chip scale package technology, offering the smallest possible footprint of the same size of the die. The low profile and improved signal characteristic make WLP ideal for portable electronics. In addition, WLP has the ability to integrate package process in wafer fab, which provides a streamline from the silicon start to customer shipment. The WLP cross section and a close-up backside image are presented in Fig. 1.6.

As can be seen, WLP does not use an interposer, and the solder balls are realized on the chip by wafer level processing. The solder ball pad is routed within the chip outline from the chip perimeter contact pad, which is so called a “fan-in” design. The ball pitch can be as small as 0.3 mm. But, as the WLP is directly mounted on PCB, ball pitch larger than 0.4 mm is necessary to ensure high yield and reliability. Another limitation of WLP is

the number of I/O count. Since the package area and ball pitch are confined, the total number of I/O count is normally no more than 100.

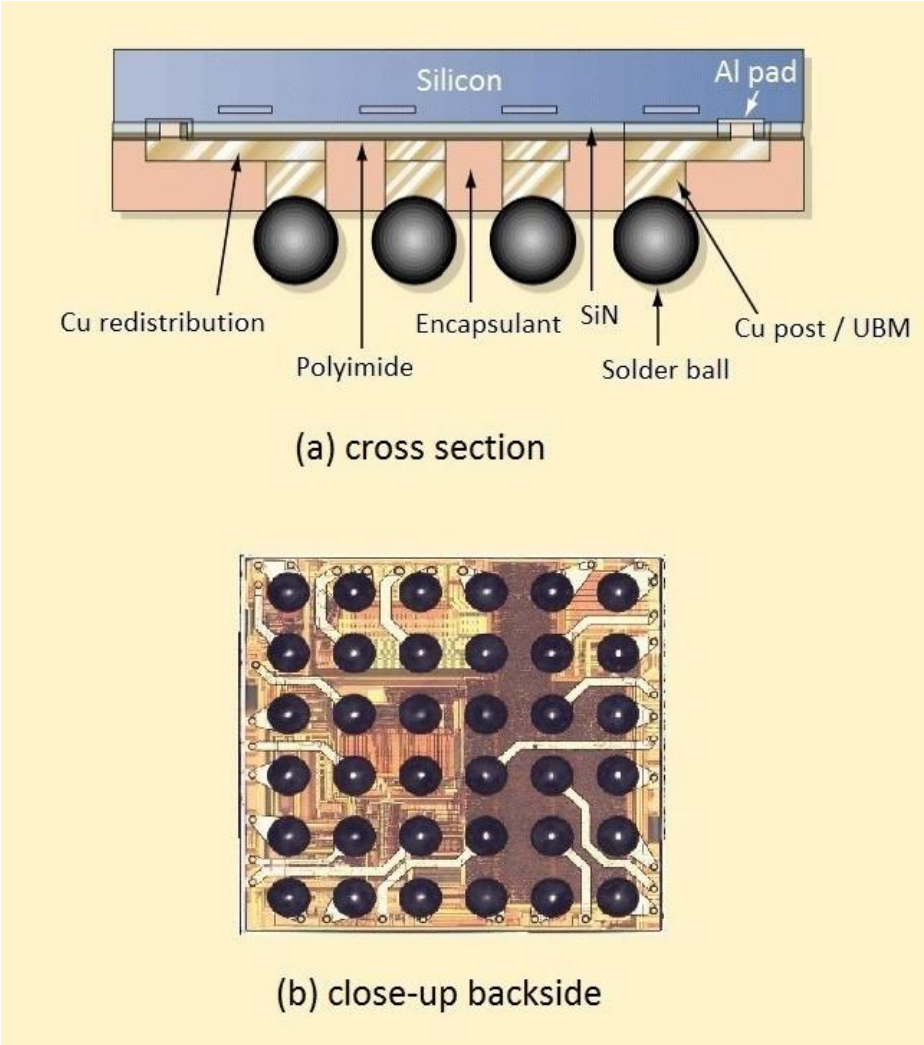

Figure 1.6 *WLP (a) Schematic cross section* [18] *and (b) backside photography* [22].

In parallel with the development for miniature package, FCBGA package is a technology designed for devices requiring extremely high pin count and high performance. In the past, the chip connection to the package interposer was realized by wire bonding. For the sake of higher pin count, which is the

same reason drive lead frame package to BGA, the chip connection to the interposer can move from wire bonding to area array bonding, primarily by flip chip solder bump. The configuration of FCBGA is shown in Fig. 1.7.

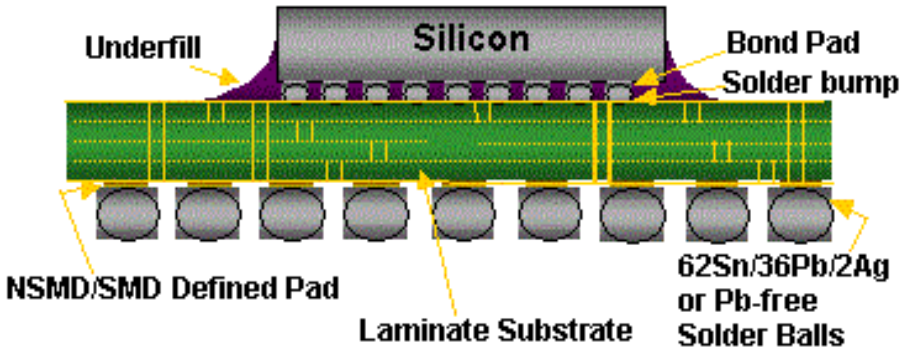

Figure 1.7 *Schematic cross section of FCBGA* [23]**.**

First, the solder bumps are deposited on the silicon chip. The bumped chip is then flipped over and placed face down onto the interposer. The bump pitch is 0.25 or 0.35 mm, which is much smaller than the ball pitch for package level connection. Due to the small bump pitch, the interposer material should provide equal pattern resolution, and reliable attachment. Co-fired ceramic was first used as interposer material because its coefficient of thermal expansion (CTE) is very close to that of silicon. Later, some high resolution organic substrates are also used to lower the total cost. But compared with ceramic substrate, the reliability of flip chip bonding on the organic substrates is still an issue needs further improvement [24]. Since the traditional wire bonding is replaced by flip chip bonding, the maximum I/O count could increase effectively up to more than 2000. Another benefit is better electrical performance, as the short connection length of flip chip bonding causes less parasitic inductance and resistance.

2010s-present

Some new technologies are emerging in the 21th century and their mass production was gradually launched around 2010s. These emerging technologies are the current state of the art and some of them are still the focus of research. Embedded chip package [25] and 3-dimension

(3D)packaging [26], [27] are two representatives of the new emerging technologies.

3D packaging exploits the third or Z height dimension to provide a compact miniature package solution for high end electronics. There are basically two approaches in 3D packaging, which are known as stacked packages and stacked dies. It's obvious that the vertical stack of elements is a highly space save configuration, which results in increasing functionality, density and performance of the final product. 3D packaging is very useful for high tech electronics, such as smart phone, tablet computer, ultrabook, etc.

Die Stacking is a process of mounting multiple chips on top of each other to form a single electronic package. There are numerous ways developed to make connection between the stacked chips. So far wire bonding is still the predominant 3D interconnect technology. But sometimes a hybrid of flip chip and wire bonding has been applied to improve warpage control and package integrity. Because multiple die were stacked together, it's important to limit the total pile height. Otherwise, the wire bonding length for top chips is too far to reach. So the chips are normally thinned down to about 30 μm before they are mounted together. Fig. 1.8 is a schematic cross section for a traditional 3D package of three stacked die using wire bonding as interconnection. The high density bonding wires have ultra fine pitch of 60μm or even below. Using the thinned chips and fine pitch wire bonding, a stack of 24 chips was realized and demonstrated by Amkor.

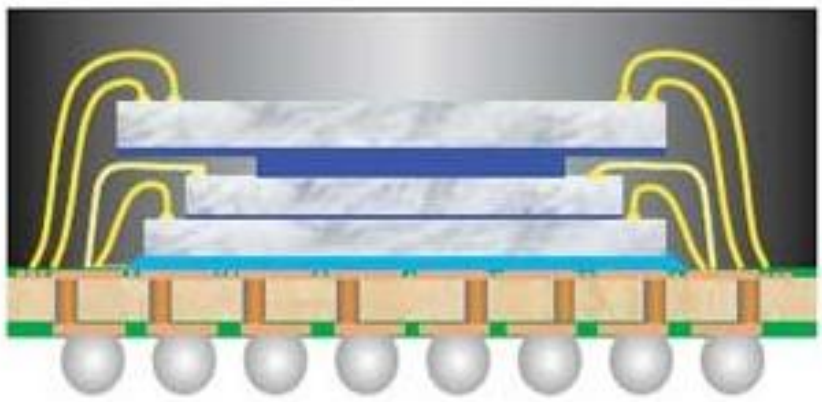

Figure 1.8 *Triple chip stacked cross section* [28].

Combined with mirco bump of flip chip bonding, through silicon via (TSV) technology is another way for stacked die connection. 3D die stacking based on TSV and micro bumping holds the promise of the highest integration density and performance, and it is currently a very hot research topic in IC packaging. TSV is a vertical electrical connection passing completely through a silicon die. The use of TSV is first found in IBM's Silicon Carrier Packaging Technology, where multiple chips are side-by-side flip bonded on a silicon interposer containing TSVs to route the chips to the bottom package level connection, as shown in Fig. 1.9. At present, the thinned silicon chip itself contains TSVs and can be directly bonded to another thinned chip with micro bumps, as present in Fig. 1.10.

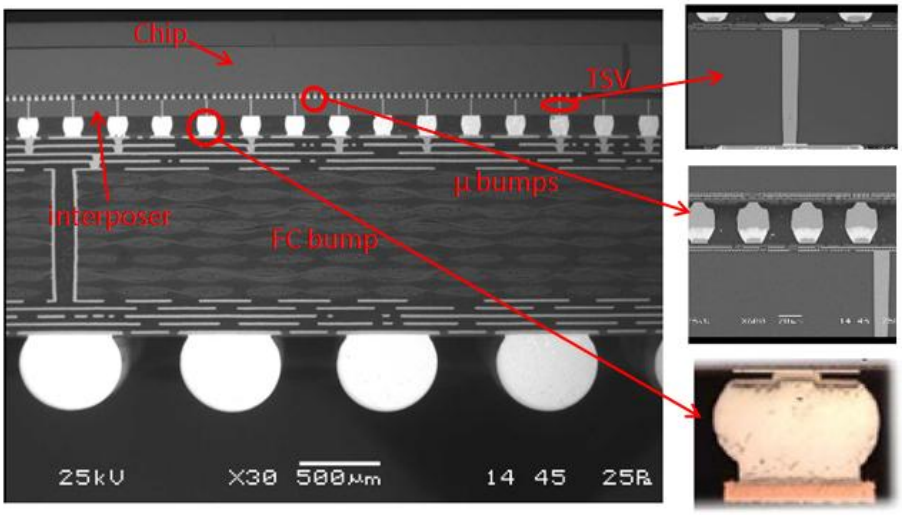

Figure 1.9 *Stacked silicon on TSV based interposer* [29].

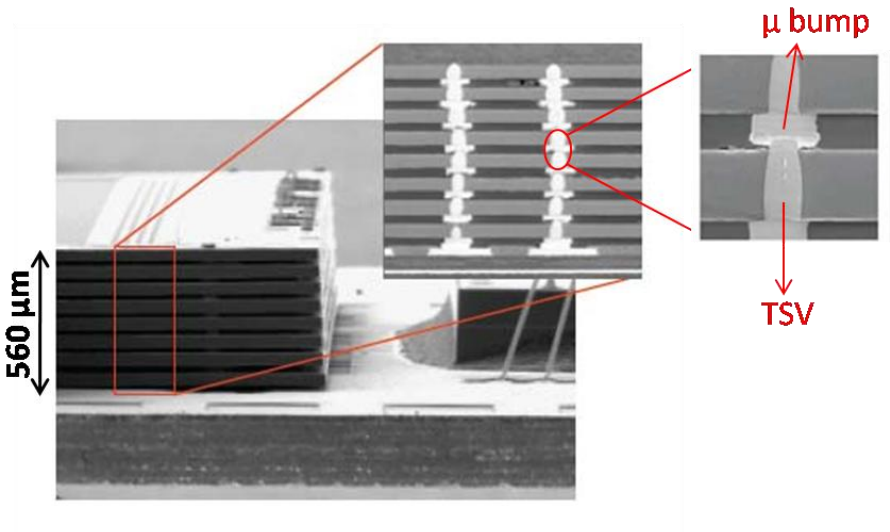

Figure 1.10 *Eight 2Gb NAND flash die stack. (Courtesy of Samsung Electronics Co., Ltd)*

Although 3D die stacking is a very promising technology, it suffers from problems of reliability and yield optimization. Thermal mechanical management is a key challenge for 3D stacked die due to its high power density and lack of thermal dissipation. At present, a lot of analysis is carrying to improve the reliability. "Known good die" (KGD) is another issue related to package yield. Since multiple die are used in one package, one nonfunctional die can result in failure of the package and yield loss. So it's important to know if the chip is good before placing it in the stack. However, functionality test on chip level is difficult, especially for thinned chip with TSVs.

As an alternative to die stacking, another 3D technology is package on package (PoP), whose sub-unit is an individual chip package after processing and test. PoP has the similar ability of high density integration and board footprints saving. Compared with die stacking, PoP can easily test the functionality of its sub unit and only choose the "known good" package to use. Besides, PoP brings some flexibility in sub-unit selection and replacement. On the other hand, additional connection length is required for interoperating parts in PoP, which leads to longer propagation delay than stacked die. Numerous PoP architectures have been developed. Some renowned types include µZ–ball stacked package, µPILR flash and DRAM PoP (both from Tessera [30], [31]) and SMAFTI package (from NEC [32],

[33]). Fig. 1.11 depicts a realized 3D packaging using Tessera's μPILR technology.

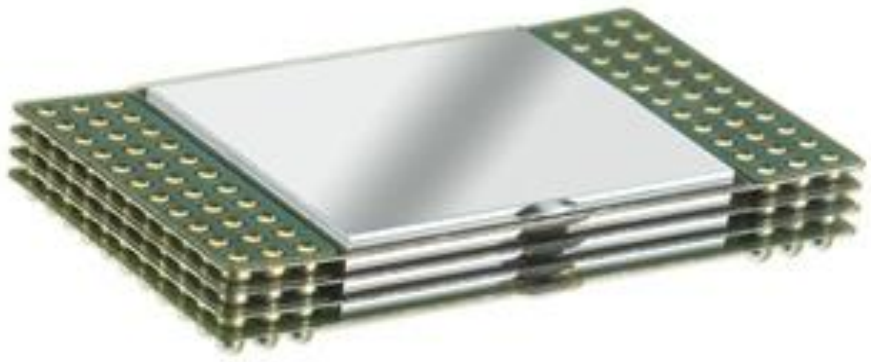

Figure 1.11 *Photography of μPILR™ PoP device* [31].

The last technology discussed here is embedded chip package. It's a new revolution for single die package to achieve the highest degree of miniaturization. The concept of embedded chip is first proposed as a continuation of WLP. Because WLP has limited surface area for solder ball arrangement, the chip can be embedded in a mold frame, which provides a "fan out" area. Then the concept is extended to integrate the bare dies directly inside PCB or other multilayer substrate, where passive components are incorporated on the top and bottom layers. A number of approaches for die embedding have been presented. One of the first was bare die assembly of chips on flex substrate, also known as Chip on Flex (COF) shown by General Electric [34]. Intel announced its Bumpless Build-Up Layer (BBUL) for their future microprocessors [35]. Helsinki University of Technology developed the so-called Integrated Module Board (IMB) technology, which was further industrialized by Imbera [36]. In the frame of European "Hiding Dies" project, the Chip in Polymer (CIP) is presented by joint institute of Fraunhofer IZM and the Technical University of Berlin [37].

All the above listed embedding methods use microvias on chip pad for electrical connection. The Chip embedded packaging can meet system requirements for signal frequencies in the order several GHz which could not be met by long bonding wires and interconnect path on a board. But it is

obvious that the KGD issue is still needs to be solved. At IMEC-CMST, an ultra thin chip package (UTCP) technology was developed as a solution of the KGD problem [38]. UTCP serves as an interposer, which can be tested before embedding in the main board. The main content of this PhD work is development and optimization of the UTCP technology and the use of UTCP's in high frequency applications.

1.1.3 Basic Elements of Package Structure

The last section reviewed some major types of IC packaging in historic evolution. Viewing from another perspective, we can examine an IC package by dividing its configuration into basic elements. Table 1.1 gives basic elements common to various package types and their existing approaches.

Table.1.1 *The basic elements in a package structure and their commom implementation approaches*

Basic elements	***Approaches***
Electrical connection from chip to package	*Wire bond *Micro bump *Microvia *Flip chip solder bump *Tape automated bond (TAB) [39] *Conductive adhesives: (ACA, ICA, ects. [40])
Electrical connection from package to circuit board	*Through hole *Leaded *Leadless *Array pads *BGA
Substrates	*Plastic *Ceramic *Metal *Glass
Encapsulation of chip	*Underfill [41] *Overmold [42] *transfer molding [43]

The structure of an IC package is defined by a combination of the listed four basic elements. For each structure element, the selection of implementation techniques depends on the specific application, system requirements and overall cost.

1.2 System on Chip (SoC) and System in Package (SiP)

The terminology SoC refers to a very large scale integration circuit, which integrate an electronic system on a single chip [44]. The embedded electronic system is able to combine all needed functions, including microprocessor, memory, optical, oscillator, and often radio-frequency, etc. SoC has a couple of advantages. Because everything is integrated on a single chip, the fabrication process can be well controlled, which leads to higher yields and higher system reliability. Normally the overall performance for SoC is better than SiP due to the compact connection. There are however some issues posed by SoC technology, such as very high design and prototyping cost, long development cycle time.

Given the high cost of SoC early development, SiP provides an alternative method to make up a complete electronic system [45]. In contrast to SoC, SiP incorporates multiple chips into a single package. Each incorporated chip handles a part of functions in the whole system, and the combined system can operate the same as if it was integrated by SoC. SiP is actually a broader sense of an old concept called multi-chip-module (MCM). MCM normally refers to assembly of multiple chips side-by-side on a single ceramic substrate using traditional connecting processes, such as wire bonding and flip chip. Regarded as the next level of MCM technology, SiP is designed with the ability to assembly multiple chips not only horizontally (on the same plane), but vertically as well. The above mentioned 3D die stacking and package stacking technology are encompassed in the concept of SiP. Sometimes, SiP even integrates several 3D structures on a single substrate in the same manner as MCM. With SiP technology, electronic companies can drastically reduce development time and risk, which overcomes the limitations of SoC development. But as mentioned before, the KGD issue is still an obstacle for successful SiP implement and high yield production.

SoC and SiP have their own pros and cons [44]. It’s believed that SoC is more suitable for high volume production of systems with low complexity. And SiP is a good choice for low volume production of high complex systems.

1.3 IC Packaging for RF Application

Due to the rapid growth of mobile marcket, there is an increasing demand for higher bandwidth and higher communication speed. As discussed in previous sections, IC packaging technology is developed to improve the system performance for a higher operating frequency.

The current packaging technologies mainly use wire bonding or flip chip to realize the interconnection for the RF chips. From the perspective of RF performance, the wire bonding technique is somehow obsolete. The long bonding wire introduces excessive parasitic inductance, which can not be easily compensated. A recent research reports that the insertion loss of a common wire bonding connection is as high as 2.2 dB at only 9.5 GHz [46]. On the other hand, the flip chip bonding is a more promising candidate for high frequency application. A lot of study has been carried out to improve the RF performance of flip chip bonding. Normally, chips with GSG contact pads are flipped and bonded to the coplanar waveguide on the package substrate to form a CPW to CPW transition. The final RF performance of the transition depends on the bonding pitch, the involved bonding material, as well as the compensation structures. In general, a compensated flip chip bonding with small pitch and low resistive material can significantly reduce the insertion and reflection losses. The state of art flip-chip bonding using micro bump technology presents an insertion loss of 0.2 dB up to 90 GHz [47].

1.4 Ultra Thin Chip Package (UTCP)

The UTCP technology is a kind of embedded chip package, which was developed by IMEC-CMST in the framework of EU funded SHIFT project. In this technology, a thinned silicon chip, with thickness below 30 μm, is encapsulated in organic substrates, consisting of cured spin-on polyimide film. Contacts of the chip to the outside world are realized using laser drilling or reactive ion etching (RIE) through the polyimide to the chip pads and thin film interconnection metallization. The result of UTCP is a very thin package with a total thickness of only 50-60 μm, which becomes even flexible and can be bent including the chip.

The UTCP technology is developed to meet an increasing demand of high frequency chip package. Since the current RF chips are realised by cmos technology, the chip size is shrinked as the scaling down of the transistors. But due to the strigent requirement of connection pitch, the chip bond pads can not be reduced as quickly as the chip size. Therefore the bond pads

cosume a considerably large area of the chip surface, which leads to a higher fabrication cost. It has been presented that the UTCP package with mirovia connection provides fine pitch capability and can further make the bond pads smaller. The fan out design provided by UTCP eliminates the need for precise placement and high density circuit board.

Although the wire bonding can also achieve connection pitch smaller than 60μm, the long wire introduces excessive parasitive inductance and degrades the transmission quality. Since the UTCP microvias mimic the solder bump in the case of flip chip bonding, which should show similar performances. The flip chip bonding is proved to have superior quality over the wire bonding [48], but is only in coarse pitch connection. Then it is expected that the UTCP can surpass the wire bonding in RF performance, and maintains the fine pitch capability.

The UTCP is albe to be used independently or serves as an interposer, which can be further embedded inside PCB or FCB (flexible circuit board) and replace the needs for directly embedding of bare die. The KGD problem is solved, because the functionality of UTCP can be easily tested before embedding it in the main board. Fig. 1.12 shows a functional electrocardiography (ECG) measurement circuit, where a TI microcontroller was packaged using UTCP technology and embedded inside FCB. The functionality of the microcontroller after thinning down to 25 μm has been proved by test of the UTCP.

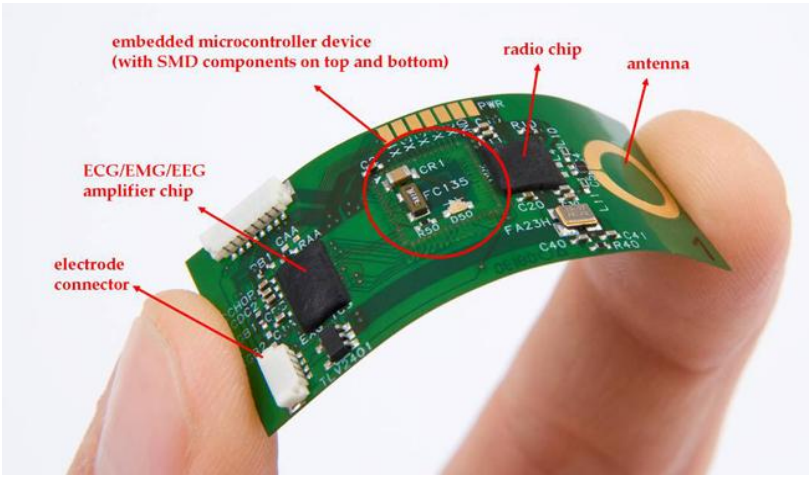

Figure 1.12 *Flexible wireless ECG monitoring circuit with embedded UTCP of TI microcontroller* [49].

1.5 Thesis Content Overview

This PhD research is a continuation study on the development of UTCP technology. The original UTCP is designed and fabricated as a single chip package for low frequency application (<5 GHz) only. In this PhD work, we exploit the use of UTCP to go beyond the current limitation and develop design strategies for embedded modules at radio frequency up to 60 GHz.

According to the main objective and scope discussed in previous section, this dissertation is organized as follows:

- Chapter 1 is a general introduction.
- Chapter 2 presents the design and optimization of microvia process for embedded chip interconnection (via size, shape, and generation method). A new process flow is estabilished for phtotosesitive polyimide.
- Chapter 3 presents another improvement in the UTCP fabrication process to achieve a flat UTCP topography. A flat surface is more suitable for multilayer build up and 3D PoP stacking.
- Chapter 4 demonstrates ultra-high frequency characterization of the dielectric material used in UTCP technology, especially for cured spin-on polyimide film.
- In Chapter 5, design, simulation and optimization of thin film structure is elaborated for high frequency interconnections to embedded chips. Two types of connection are built up. Their insertion and reflection properties were analyzed and compared with each other.
- Chapter 6 discussed passive devices which are realized by generic thin film technology in combination with the UTCP processing. A set of passive elements are designed and fabricated in EU SHIFT project. This chapter briefly explains the used process flow and mainly presents the RF characteristic of the realized passive devices.
- Finally, Chapter 7 summarizes the results presented in this dissertation and gives an outlook for future research.

Scientific Contributions in the PhD Period

Journal contributions

- L.Wang, T. Sterken, M. Cauwe, D. Cuypers, and J. Vanfleteren, "Fabrication and characterization of flexible ultrathin chip package using photosensitive polyimide," *IEEE Trans on Compon Packag and Manuf. Technol*, vol. 2, No. 7, pp 1099-1106, 2012.

- L.Wang, M. Cauwe, S. Brebels, W. D. Raedt and J. Vanfleteren, "Self-Aligned Flat Ultra-Thin Chip Package for Flexible Circuits," *Circuit World*, vol. 39, Iss: 4, 2013.

Conference contributions

- L. Wang, W. Christiaens, S. Brebels, W. De Raedt, and J. Vanfleteren,"A novel approach to embed off-chip RF passives in PCB based onthin film technology," in Proc. Electron. Syst.-Integr. Technol. Conf., Sep. 2010, pp. 1–4.

- T. Sterken, M. O. de Beeck, F. Vermeiren, T. Torfs, L. Wang, S.Priyabadini, K. Dhaenens, D. Cuypers, and J. Vanfleteren, "High yieldembedding of 30 μm thin chips in a flexible PCB using a photopatternable polyimide based ultra-thin chip package (UTCP)," in Proc. 45th Int. Symp. Microelectron., Sep. 2012, pp. 940–945.

- S. Priyabadini, T. Sterken, L. Wang, K. Dhaenens, B. Vandecasteele, S. Van Put, A. E. Petersen, and J. Vanfleteren, "An approach to produce a stack of photo definable polyimide based flat UTCPs," in 2012 4th Electronic System-Integration Technology Conference, 2012, pp. 1–4.

References

[1] William J. Greig, *Integrated circuit packaging, assembly and interconnections*. Springer, 2007.

[2] C. Harper, *Electronic Packaging and Interconnection Handbook 4/E*. McGraw-Hill Professional, 2004, p. 1000.

[3] W. Greig, *Integrated Circuit Packaging, Assembly and Interconnections (Springer Series in Advanced Microelectronics)*. Springer, 2007, p. 328.

[4] International Roadmap Committee, (2012), "The International Technology Roudmap for Semiconductor." [Online]. Available: http://www.itrs.net/home. html

[5] Association Connecting Electronics Industries, (2013), "Current industry trend." [Online]. Available: www.ipc.org/

[6] Gordon E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, pp. 114–117, April 19, 1965.

[7] ISSCC, (2013), "ISSCC 2013 Tech Trends." [Online]. Available: http://isscc.org/doc/2013/2013_Trends.pdf

[8] Intel, (2008), "The intel4004." [Online]. Available: http://www.intel4004.com/qa4004.htm

[9] Fujitsu Semiconductor Lt,(2011) "IC Package," [Online]. Available: http://www.fujitsu.com/downloads/MICRO/fma/pdf/a810000114e.pdf

[10] K. A. Jackson and W. Schröter, *Handbook of Semiconductor Technology: Electronic structures and properties of semiconductors*. Wiley-VCH, 2000, p. 842.

[11] Dummer, G.W.A. *Electronic Inventions and Discoveries*, 2nd ed. Pergamon Press, 1978, p.204.

[12] P. M. (editor), *Surface Mount Council; Surface Mount Technology; Status of the Technology; Indus*. EIA, 1990.

[13] A. Seth, E. Pope, and S. Gordon, “Plastic quad flat pack,” in *Proceedings. Japan IEMT Symposium, Sixth IEEE/CHMT International Electronic Manufacturing Technology Symposium*, pp. 90–100.

[14] B. Freyman and R. Marrs, “Ball Grid Array (BGA): The New Standard For High I/O Surface Mount Packages,” in *Proceedings of Japan International Electronic Manufacturing Technology Symposium*, pp. 41–45.

[15] Toshiba, (2013), “QFP Packages.” [Online]. Available: http://www.semicon.toshiba.co.jp/eng/product/asic/package/package2/lqfp.html

[16] Toshiba, (2013), “BGA Packages.” [Online]. Available: http://www.semicon.toshiba.co.jp/eng/product/asic/package/package2/pbga.html

[17] S. T. Rao, “Ball grid array assembly issues in manufacturing,” in *Proceedings of 16th IEEE/CPMT International Electronic Manufacturing Technology Symposium*, pp. 347–348.

[18] Fujitsu Semiconductor Ltd, (2002) “ASIC Packaging,” [Online]. Available: www.fujitsu.com/downloads/MICRO/fma/pdf/ASIC20PKG.pdf

[19] M. Yasunaga, S. Baba, M. Matsuo, R. Matsushima, S. Nakao, and T. Tachikawa, “Chip scale package (CSP) ‘a lightly dressed LSI chip’,” in *Proceedings of 16th IEEE/CPMT International Electronic Manufacturing Technology Symposium*, pp. 169–176.

[20] P. Elenius, “Ultra CSP/sup TM/: a wafer level package,” in *Proceedings International Symposium on Advanced Packaging Materials. Processes, Properties and Interfaces (IEEE Cat. No.99TH8405)*, pp. 241–245.

[21] Texas Instruments, (2005), “Flip Chip Ball Grid Array Package Reference Guide,” [Online]. Available: http://www.ti.com/lit/ug/spru811a/spru811a.pdf

[22] J. Jackson and A. O’Donnell, (2007), “MicroCSP^{TM} Wafer Level Chip Scale Package,” *Analog Devices*. [Online]. Available: www.analog.com/static/imported-files/application_notes/AN_617.pdf

[23]Freescale, (2013),"FCPBGA." [Online]. Available: http://www.freescale.com/webapp/sps/site/overview.jsp?code=CSIC_PACKAGING

[24] T. Y. Wu, Y. Tsukada, and W. T. Chen, "Materials and mechanics issues in flip-chip organic packaging," in *1996 Proceedings 46th Electronic Components and Technology Conference*, pp. 524–534.

[25] A. Ostmann, D. Manessis, J. Stahr, M. Beesley, M. Cauwe, and J. De Baets, "Industrial and technical aspects of chip embedding technology," in *2008 2nd Electronics System integration Technology Conference*, 2008, pp. 315–320.

[26] W. R. Davis, J. Wilson, S. Mick, C. Mineo, A. M. Sule, M. Steer, and P. D. Franzon, "Demystifying 3D ICs: The Pros and Cons of Going Vertical," *IEEE Design and Test of Computers*, vol. 22, no. 6, pp. 498–510, Jun. 2005.

[27] S. F. Al-Sarawi, D. Abbott, and P. D. Franzon, "A review of 3-D packaging technology," *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B*, vol. 21, no. 1, pp. 2–14, 1998.

[28] M. Kada and L. Smith, "Advancements in stacked chip scale packaging provides system in a package functionality for wireless and handheld applications," in *Proc. 5th Pan Pacific Microelectron. Symp.*, 2000, p. pp.246 –251.

[29] Amkor Technology, (2013). "Through Silicon Via (TSV) Wafer Finishing & Flip Chip Stacking." [Online]. Available: http://www.amkor.com/index.cfm?objectid=7478706F-E1C7-1A4D-E62795E72380FA68

[30] Tessera Inc, (2013). "μPILR Package-on-Package (PoP) interconnect solution" [Online]. Available: http://www.tessera.com/technologies/intellectualproperty/substrateinterconnect/Pages/uPILR-PoP.aspx

[31] V. Solberg, "μPILR trade package-on-package technology: development and reliability testing," in *2007 9th Electronics Packaging Technology Conference*, 2007, pp. 55–60.

[32] Y. Kurita, K. Soejima, K. Kikuchi, M. Takahashi, M. Tago, M. Koike, K. Shibuya, S. Yamamichi, and M. Kawano, "A Novel 'SMAFTI' Package for Inter-Chip Wide-Band Data Transfer," in *56th Electronic Components and Technology Conference 2006*, pp. 289–297.

[33] Y. Kurita, N. Motohashi, S. Matsui, K. Soejima, S. Amakawa, K. Masu, and M. Kawano, "SMAFTI packaging technology for new interconnect hierarchy," in *2009 IEEE International Interconnect Technology Conference*, 2009, pp. 220–222.

[34] R. Fillion, B. Burdick, D. Shaddock, and P. Piacente, "Chip scale packaging using chip-on-flex technology," in *1997 Proceedings 47th Electronic Components and Technology Conference*, pp. 638–642.

[35] H. Braunisch, S. N. Towle, R. D. Emery, and G. J. Vandentop, "Electrical performance of bumpless build-up layer packaging," in *52nd Electronic Components and Technology Conference 2002. (Cat. No.02CH37345)*, pp. 353–358.

[36] P. Palm, R. Tuominen, and A. Kivikero, "Integrated Module Board (IMB); an advanced manufacturing technology for embedding active components inside organic substrate," in *2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No.04CH37546)*, pp. 1227–1231.

[37] L. Boettcher, D. Manessis, A. Neumann, A. Ostmann, and H. Reichl, "Chip embedding by chip in polymer technology," in *Proc. Device Packaging Conference*.

[38] W. Christiaens, E. Bosman, and J. Vanfleteren, "UTCP: A Novel Polyimide-Based Ultra-Thin Chip Packaging Technology," *IEEE Transactions on Components and Packaging Technologies*, vol. 33, no. 4, pp. 754–760, Dec. 2010.

[39] S. M. Wentworth, D. P. Neikirk, and C. R. Brahce, "The high-frequency characteristics of tape automated bonding (TAB) interconnects," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 12, no. 3, pp. 340–347, 1989.

[40] H. Kristiansen and J. Liu, "Overview of conductive adhesive interconnection technologies for LCDs," *IEEE Transactions on Components,*

Packaging, and Manufacturing Technology: Part A, vol. 21, no. 2, pp. 208–214, Jun. 1998.

[41] K. K. Wang, "Analysis of the flow of encapsulant during underfill encapsulation of flip-chips," *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B*, vol. 20, no. 4, pp. 424–433, 1997.

[42] S. Ouimet and M.-C. Paquet, "Overmold technology applied to cavity down ultrafine pitch PBGA package," *IEEE Transactions on Advanced Packaging*, vol. 22, no. 2, pp. 123–128, May 1999.

[43] T. Braun, K.-F. Becker, M. Koch, V. Bader, U. Oestermann, D. Manessis, R. Aschenbrenner, and H. Reichl, "Wafer level encapsulation - a transfer molding approach to system in package generation," in *4th Electronics Packaging Technology Conference, 2002.*, 2002, pp. 235–244.

[44] R. Wilson, (2005)."The Great Debate: SOC vs. SIP." [Online]. Available: http://www.eetimes.com/electronics-news/4052047/The-Great-Debate-SOC-vs-SIP

[45] M. Romig and V. Gupta, (2012). "System-in-package provides viable integration solution." [Online]. Available: http://www.eetimes.com/design/eda-design/4236765/System-in-package-provides-viable-integration-solution-

[46] C. H. J. Poh, C. E. Patterson, S. K. Bhattacharya, S. D. Philips, N. E. Lourenco, J. D. Cressler, and J. Papapolymerou, "Packaging Effects of Multiple X-Band SiGe LNAs Embedded in an Organic LCP Substrate," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 2, no. 8, pp. 1351–1360, Aug. 2012.

[47] A. Jentzsch and W. Heinrich, "Theory and measurements of flip-chip interconnects for frequencies up to 100 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 5, pp. 871–878, May 2001.

[48] T. Krems, W. Haydl, H. Massler, and J. Rudiger, "Millimeter-wave performance of chip interconnections using wire bonding and flip chip," in *1996 IEEE MTT-S International Microwave Symposium Digest*, vol. 1, pp. 247–250.

[49] W. Christiaens, T. Torfs, W. Huwel, C. Van Hoof, and J. Vanfleteren, "3D integration of ultra-thin functional devices inside standard multilayer flex laminates." in *Microelectronics and Packaging Conference (EMPC)*, 2009, pp1-5.

CHAPTER 2

UTCP Technology Using Photosensitive Polyimide

This chapter describes an improved UTCP process flow with microvia formation by standard UV lithography through photosensitive polyimide (PSPI). Such microvia formation method proved to be more reliable than laser drilling techniques and simpler than a dry etching process. Since the used PSPI is self-priming, a thin layer of potassium chloride (KCl) was introduced as a release layer. In the end, the polyimide encapsulation of thinned die can be released from the carrier substrate and becomes a flexible chip package with a total thickness of around 50 μm. Daisy chain test dies were encapsulated inside spin-coated polyimide films. Excellent chip-to-package interconnection was demonstrated by electrical daisy chain and contact resistance measurements. Bending tests and thermal cycling tests were also performed on the daisy chain test vehicles. Desired flexibility and reliability of UTCP's was observed.

2.1 Introduction

The development of integrated circuits leads to an increase in components density, which requires chip packaging technologies to enable higher lead count, finer pitch, and smaller size. This trend is clear in the evolution of

packaging. In the evolution from DIP to BGA, typical pin count increases from 24 to 280, while the thickness decreases from 4 mm to 1 mm and the area is reduced from 32 mm x 14 mm to 9 mm x 9 mm [1, 2].

Recently, assembly of thinned die has become the focus of research to further lower the package profile [3-5]. A thinned silicon die is either flip bonded onto or embedded into thin film substrates [5-9]. The chip embedded approach is one promising candidate for the next generation System-in-Package (SiP) technology by reason of its high-density interconnection capability and superb electrical performance [10]. As described in chapter 1, one of the most prominent embedding approaches is Chip-in-Polymer (CiP) technology developed by Fraunhofer IZM in corporation with TU Berlin [11]. The basic concept of CiP is to laminate thinned die in dielectric resin and then make contact to chip bond pads by laser ablation and direct metallization [9-11]. In UTCP technology, thinned die was encapsulated inside spin-on polyimide layers [12]. The result of UTCP is a very thin and even flexible chip package, with a total thickness around 50 µm. This technology allows the fabrication of ultra thin flexible electronics, which have attracted a lot of attention because of their conformal property [13-15]. Flexible electronics create possibilities for many applications in portable electronics, sensor array systems and aerospace [16-18]. The flexibility of an end product is often limited by the rigid components mounted on the surface of the substrate. An introduction of ultra-thin chips, which are well bendable in contrast to bulk silicon chips, can further enhance the mechanical flexibility of the electronic circuitry.

This chapter presents an updated version of IMEC's UTCP technology. In previous work, via-holes connecting die contact pads were generated by laser drilling through a PI-2611 polyimide (from HD Microsystems) covering layer [12]. In doing so, besides the reported problem of laser beam misalignment, the high intensity power of the laser beam has the potential to damage the metal bump pad on the chip [19]. In today's high density PCB industry, laser drilling with either UV lasers or CO2 lasers is a well established and widely adopted method for microvia formation. If the drilling process is properly controlled, the damage to the bond pads can be eliminated or minimized to an acceptable level [11, 12]. Photo definition is another well known via formation process by introducing photosensitive material. In this work, photo definition is used as an alternative to laser drilling. Via formation using photosensitive polyimide (PSPI) is similar in process sequence to a generic photolithography technique, which is more reliable than laser ablation and is more cost-effective than dry etching based

via formation techniques. However, if PSPI is selected as the covering material, in order to avoid CTE mismatch between the top and base dielectric layer, the same PSPI should also be used as the base material. Since most of the PSPI is self-priming and cannot be easily released from the rigid carrier substrate, a new release method based on potassium chloride (KCl) evaporation is invented and discussed in this chapter.

2.2 Process Flow

The improved technique was developed to embed a thinned die into two PSPI films. The schematic process flow is depicted in Fig. 2.1. First, a 400nm layer of KCl is thermally evaporated on a rigid glass carrier substrate. Then the base PSPI is spin-coated on the KCl film and fully cured. The thinned die is glued on the base PSPI (face up) using benzocyclobutene (BCB) as adhesive. After the curing of BCB, the top PSPI layer is spin-coated, illuminated through a mask and developed to define the microvias to the chip contact pads. Finally, the top PSPI is cured and the metal pattern is realized on top. After the whole process, the multilayer assembly of thinned die can be released from the glass carrier, and becomes a flexible ultrathin chip package (UTCP).

2.3 Test Design

PTCE chips from IMEC are selected as test dies for the embedding trials. The PTCE chip is a 5 mm × 5 mm daisy chain silicon chip which has been thinned down from 675 µm to 20 µm on wafer level. Wafer thinning and separation by coarse grinding and sawing are no longer feasible when the thickness is below 150 µm, due to large stress and deep cracks in silicon [20].

For the purpose of fabricating the ultra-thin chips, an additive process technology, Chipfilm, is developed at IMS [21,22]. The main feature of Chipfilm is the precise control of chip thickness and uniformity. Such technology can provide good mechanical stability of ultra-thin chips with high yield, which paves the way for future flexible electronic applications. However Chipfilm technology is not available at our facility. In contrast to Chipfilm, wafer backside grinding is used for this work. Wafer thinning down to 50 µm or less is common for 3D integration. But wafer dicing by use of a conventional sawing machine can generate deep cracks in the silicon

which is detrimental for ICs' reliability especially in case of thinned chips. Therefore, instead of dicing a thinned wafer, the Dicing-by-Thinning concept was employed to accomplish this task [23].

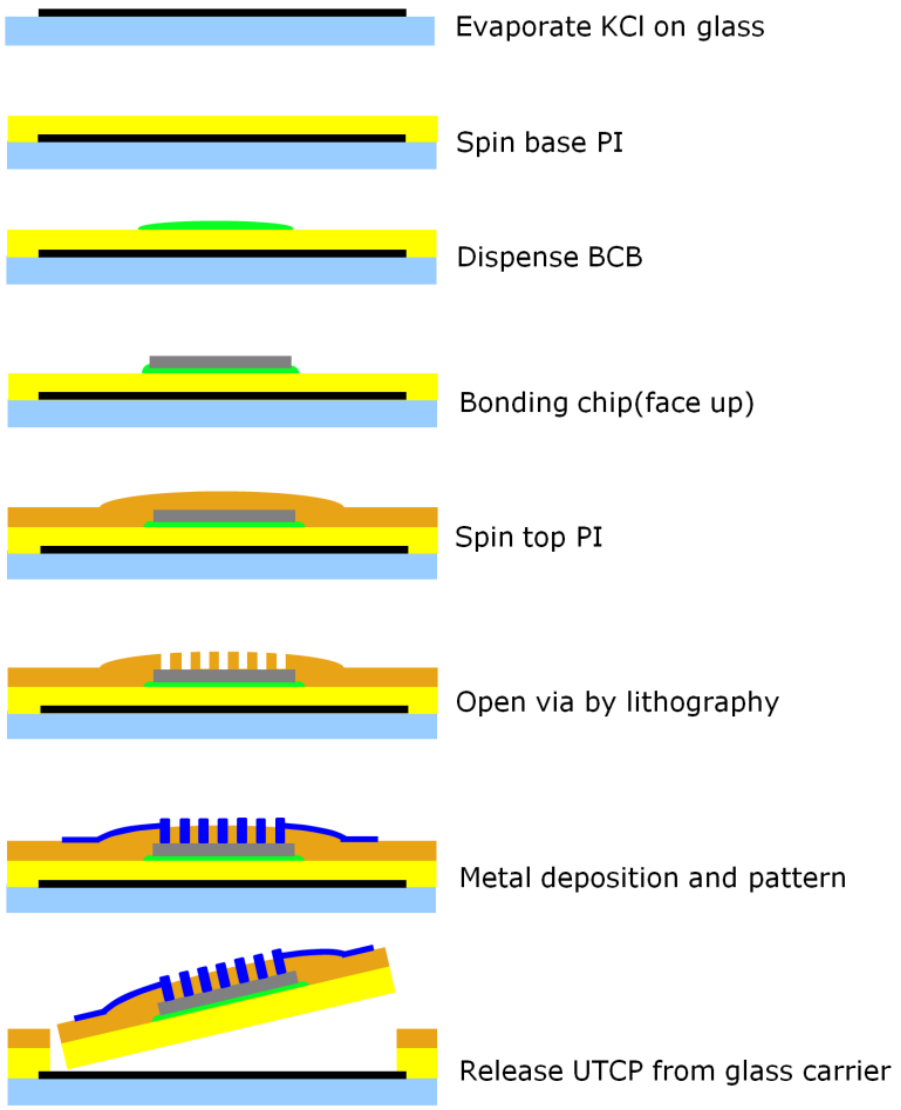

Figure 2.1 *Process flow to produce UTCP using PSPI.*

There are three types of daisy chains around the chip edge with different pitches (60, 100 and 200 μm). The trials in this work only use the coarsest

pitch which has 90μm × 90μm × 1μm (length × width × thickness) aluminum contact pads and 110 μm wide space in between (Fig. 2.2). In order to characterize the feasibility of the technology, a metallization pattern is designed to interconnect the bond pads. The layout of the metallization is shown in Fig. 3 together with the chip layout. This design includes four short daisy chains (DC1-4) along the edges, each connecting 20 peripheral bond pads. A series link from DC1 to DC4 forms a long daisy chain DCT. Four four-point Kelvin structures (FP1-4) are also fabricated at corners of the chip for contact resistance measurements.

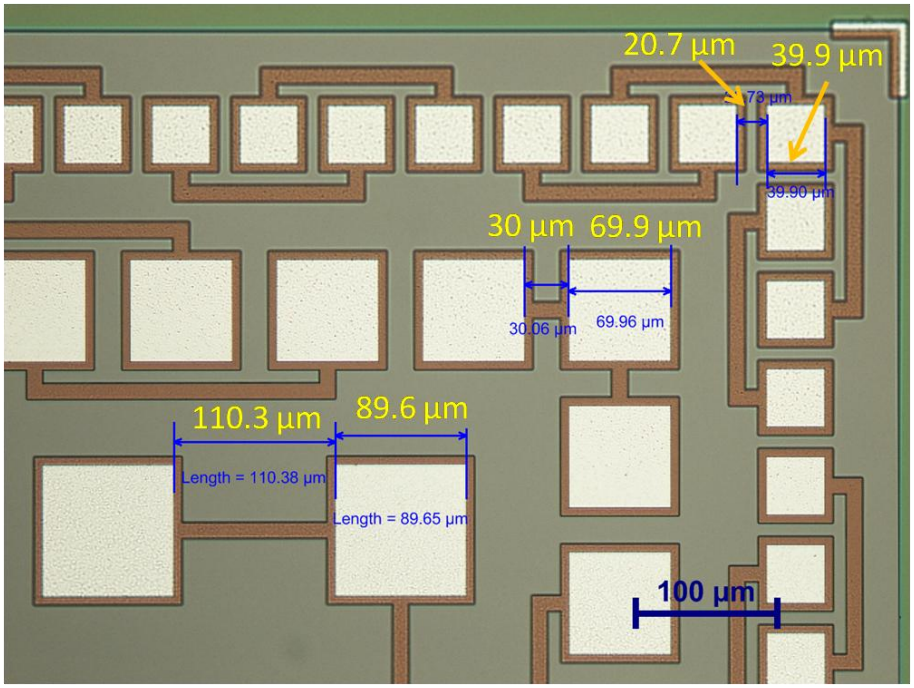

Figure 2.2 *Peripheral bond pads with different pitch on PTCE chip.*

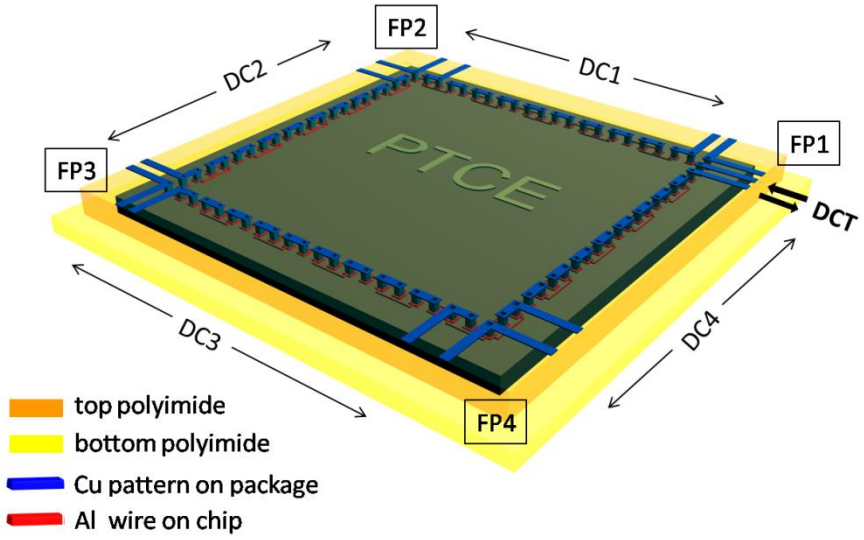

Figure 2.3 *Schematic graph showing UTCP of PTCE chip and its interconnect layout.*

2.4 Fabrication Process And Optimization

2.4.1 Substrate Preparation

The assembly of thinned die was built up on a 5 cm × 5 cm rigid glass carrier purchased from Praezisions Glas and Optik. The glass should be thoroughly cleaned in RBS, IPA and DI water in sequence to remove dust and grease from manufacturing and transport. Next, a 400 nm thick KCl layer was thermally evaporated on the glass, the edges of which were covered by aluminum foil. Since the PSPI is self-priming and becomes hard to peel off after curing when directly deposited on glass, such KCl film, which can be easily dissolved in water, serves as a release layer between the base PSPI and the glass carrier. Moreover, the base PSPI on the edge of the glass can protect KCl from any solvent during the whole process. A major concern

about the use of KCl is that K+ and Cl- ions are common contaminants which can have detrimental impact on a semiconductor processing line especially with the high temperature diffusion. But the fabrication of UTCP is carried out in a thin film package environment which does not need to meet the high purity level for semiconductor production. Additionally, the evaporation of KCl is performed in a confined physical vapor deposition (PVD) chamber under high vacuum condition to avoid exposure to ambient air. Due to the presence of KCl in PVD, it is not recommended to process other materials by the same machine. By doing this, KCl contamination can be reduced to an acceptable level.

HD-4110 from HD Microsystems was used for both the base and top PSPI in order to avoid CTE mismatch [24]. The first PSPI layer was then spin-coated at 1000 rpm for 10 s, followed by a final speed of 1800 rpm for 1 min. The lower starting speed is used to spread the highly viscous HD-4110 in order to form a more uniform layer. After the spinning, the substrate was cured in a vacuum oven for 6 hours with 5 sccm nitrogen flow. The curing temperature profile was as follows: increase from 20 °C (room temperature) to 200 °C with a ramp rate of 4°C/min; hold the temperature of 200 °C for 30 min; increase to the final curing temperature of 375 °C with a ramp rate of 2.5°C/min; and maintain the elevated temperature for an hour; then let it cool down naturally. The thickness of base PSPI after curing is 15 μm.

In order to improve the adhesion to the bonding material and the top PSPI, an increase in surface roughness of the base PSPI is preferred by a plasma etching treatment. This was done by Reactive Ion Etching (RIE), first using a CHF3/O2 mixture gas with a flow rate of 5/20 sccm for 2 min, and another 2 min using pure O2 with a flow rate of 25 sccm, both at a fixed power of 150 W and a pressure of 100 mTorr. Fig. 2.4 shows a substrate after RIE which is ready for the next chip bonding step. The dashed line in the graph encloses the area where the KCl film was deposited.

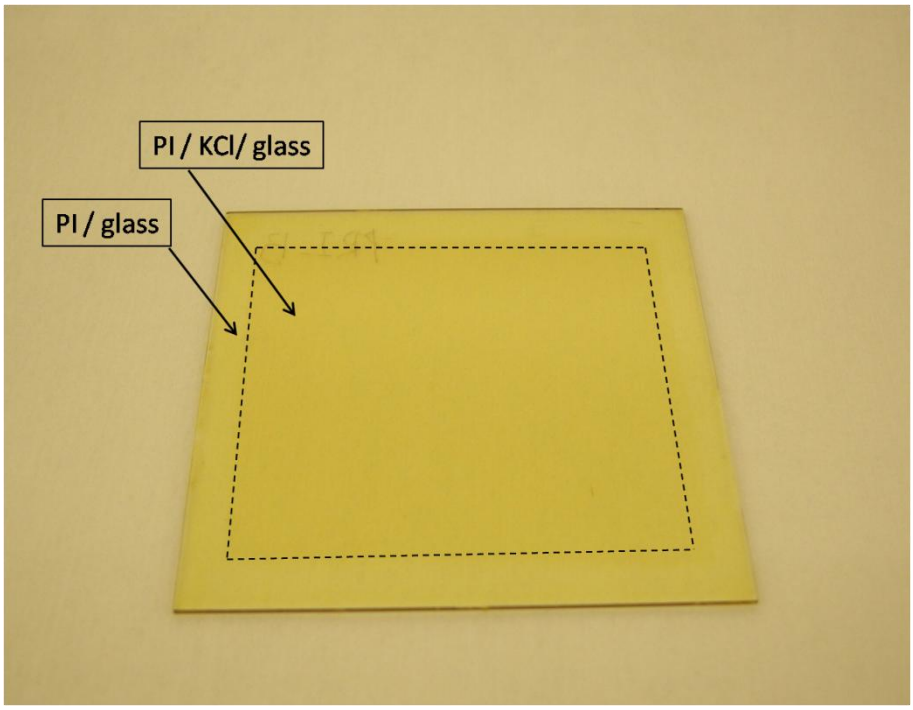

Figure 2.4 *Graph of a prepared substrate on glass carrier.*

2.4.2 Chip Placement

The PTCE chip tends to curl after thinning to 20 μm thick due to its internal stress. The chip warpage can cause multiple reflections of the light during exposure, which leads to unsuccessful opening of the microvias. Therefore, bonding the thinned chip in a flat plane on the substrate is of vital importance.

BCB of the Cyclotene 3000 Series from Dow Chemical Co. was selected as an adhesive material. A droplet of BCB (about 50 nL) was put on the substrate and was subjected to a soft bake on a hot plate at 60 °C for 5 min. The purpose of the soft bake is to evaporate solvent in the BCB and to dehydrate the base PSPI layer. Without performing this step, some air bubbles could be trapped underneath the chip during the BCB curing. The thinned chip was then manually placed face-up on the BCB and a release film ACC-3 (from Holders Technology PLC) was put on the top of the chip.

The release film, which has resistance against different chemicals, was used to prevent BCB from sticking to the press plate in the next bonding process.

The bonding of the die was accomplished in two steps. The preliminary bonding was done in a Logitech wafer bonder at an elevated temperature of 150 °C for 1 hour under a pressure of 500 mBar and followed by a quick cooling down to room temperature. After preliminary bonding, the BCB was only partially cured. In case a small amount of BCB overflowed between the chip and the ACC-3 film, it still can be removed by acetone. IPA and DI water was used to clean the residual acetone and the sample was dried in the air. Afterwards, the final BCB curing was carried out in a nitrogen oven with 1kg weights applied to enhance the bonding strength. The BCB hard curing profile was the following: heat from 20 °C to 150 °C with a ramp rate of 4 °C/min followed by an increase to 250 °C with a ramp rate of 2.5 °C/min, and maintain the temperature of 250 °C for 1 hour before cooling down.

The die surface topography was scanned by a Wyko optical profilometer as shown in Fig. 2.5. Compared to the chip profile before bonding, the radius of curvature increases from about 100 mm to more than 5 meters, showing a virtually flat chip assembly as desired.

2.4.3 Via Formation

A new via formation technique using PSPI HD-4110 was developed in this work. HD-4110 was spin-coated at the same speed as the base polyimide layer for a target thickness of 10 μm on the chip after curing. After spinning, the sample should be baked on a hot plate at 110 °C for 4 min for a tack free top surface, otherwise it can stick to the mask during exposure. The thickness of top polyimide layer is about 15 μm after prebake. Since HD-4110 is a photosensitive dielectric, the via-holes to the chip contact pad can be defined by a photolithography process. The corresponding mask with 70 μm × 70 μm via size is shown in Fig. 2.6. Thanks to the transparent polyimide layer, the mask can be aligned according to the position of contact pads on the chip. The accuracy of the alignment depends on the carefulness and experience of the operator. In our case, the misalignment is around 5μm.

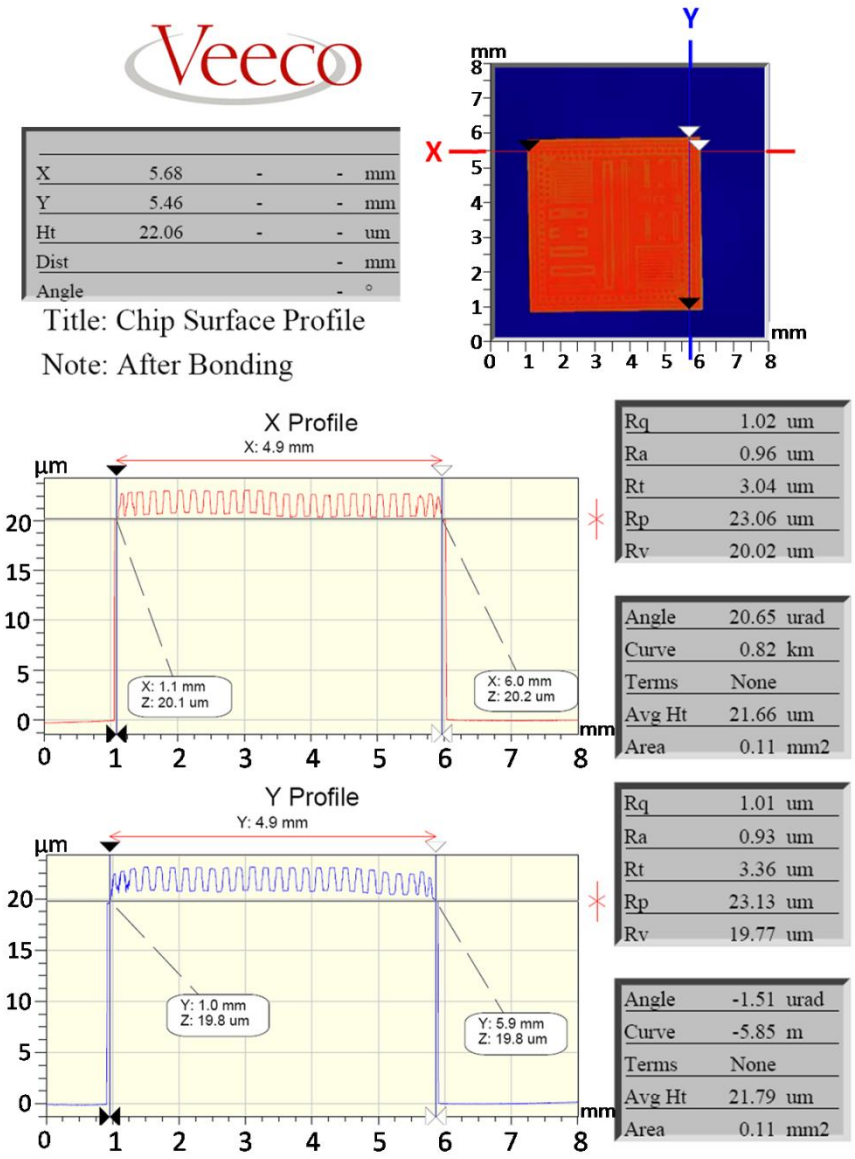

Figure 2.5 *Surface profile of PTCE chip after bonding on the substrate.*

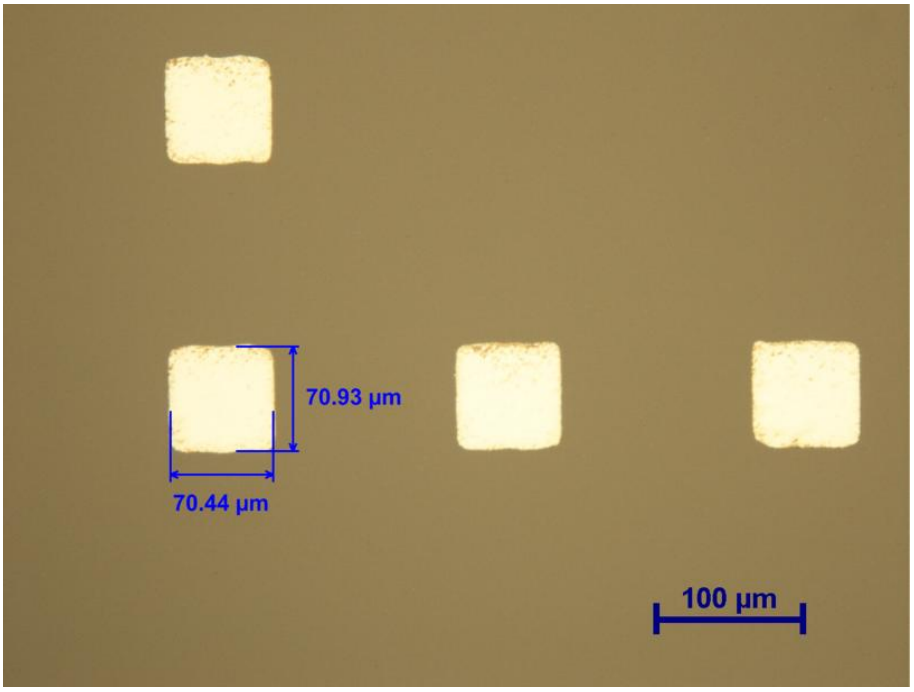

Figure 2.6 *Graph of microvia mask for PTCE chip.*

Illumination was done using a broadband stepper with light intensity of 9 mW/cm2. The exposure time was tested by changing it from 10 to 40 s in steps of 5 s. If the light dose is not sufficient, the top polyimide layer becomes easy to peel off after the development. In contrast, excessive light cannot open the bottom of the via-holes, as HD-4110 is a negative tone polyimide. The test result indicates a broad process window between 20 to 30 s with an optimal value of 25 s, which is equal to a total light energy of 225 mJ/cm2.

After the exposure, holding the sample for a minimum of 10 min prior to development is required to complete the corresponding chemical reaction. The development was then carried out by immersing the sample in a beaker filled with PA400D for 40 s with the assistance of ultrasonic agitation. This is followed by two 30 s consecutive rinses: first in a 1:1 mixture of PA400D and PA400R and secondly in pure PA400R. Both PA400D and PA400R solvents were purchased from HD Microsystems. After a nitrogen blow dry, the via-holes were easily observed under a microscope.

In the next step, the sample was again cured in a vacuum oven using the same curing parameters as the base polyimide layer. Fig. 2.7 demonstrates a detailed view of the microvias on chip contact pads after curing. It can be seen that the top of the microvias had a dimension of 85 µm × 85 µm, which is larger than its bottom dimension (71 µm × 71 µm). The corresponding 3D plot using a Wyko profilometer is shown in Fig. 2.8. It should be noted that smaller via sizes can also be achieved by using this method. In our experiments, microvias down to 30 µm in diameter (bottom dimension) can be generated on the chip contact pads with 100% yield using the same process sequence (Fig. 2.9). This gives the possibility to reduce the interconnect pitch to 60 µm or even below.

Photo definition offers an alternative to laser drilling technique. Via formation using PSPI is a multistep process, whereas laser drilling is an essentially single step operation. The photo definition method can produce a a massive number of vias at one time, in contrast to the sequential nature of laser drilling. However the modern laser can now reach very high drilling speed of up to 1500 holes/s and it still has room for improvement in the future [9]. Compared to the current high drilling speed, the photo definition method can not show any throughput advantage over laser drilling. Another limitation of photo definition is that this process restricts material selection to spin-on photosensitive material and precludes the use of other material with better electrical and mechanical properties, such as liquid crystal polymer (LCP). When such roll-to-roll material is desired for embedding chips, lamination combined with laser ablation as CiP technology provides a suitable solution.

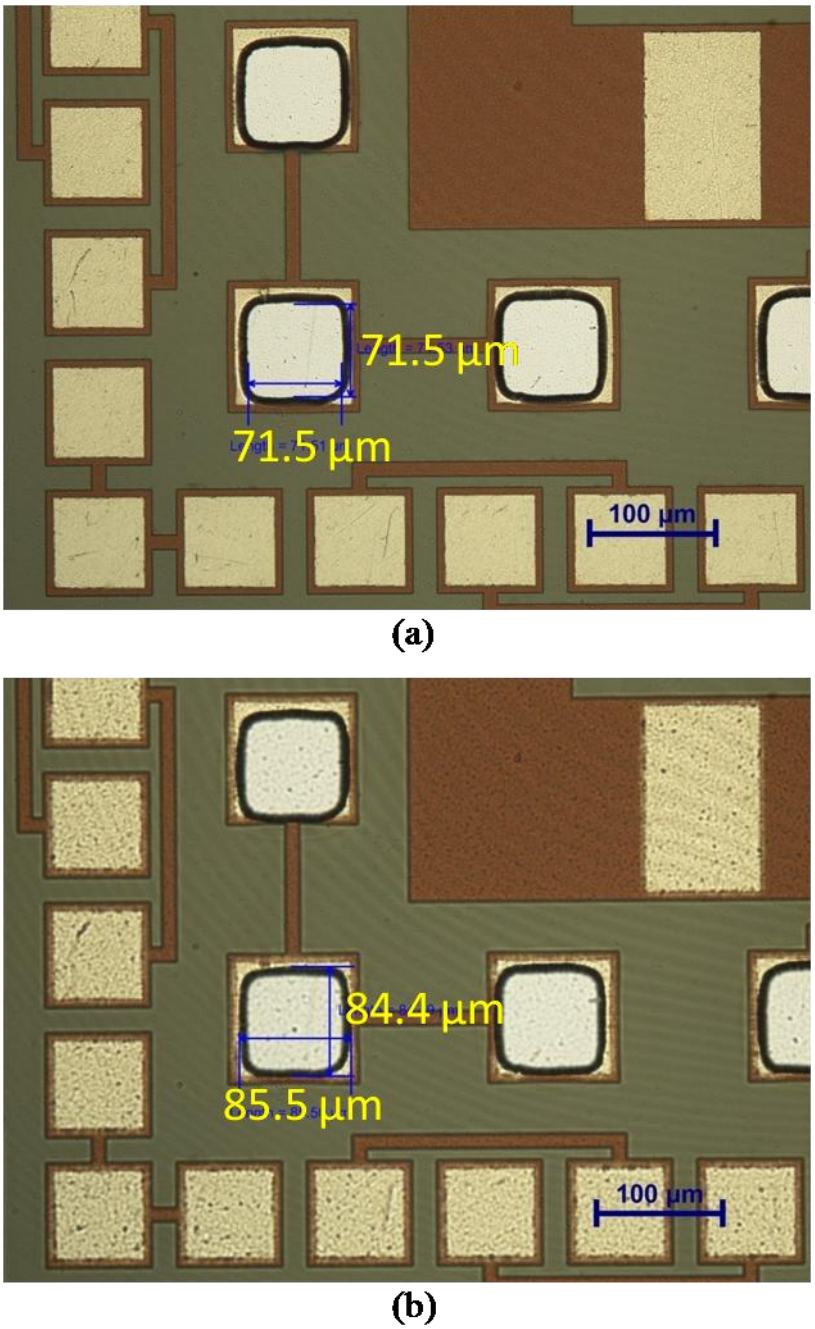

Figure 2.7 *Comparison of microvia size focus on (a) top of the via (b) bottom of the via.*

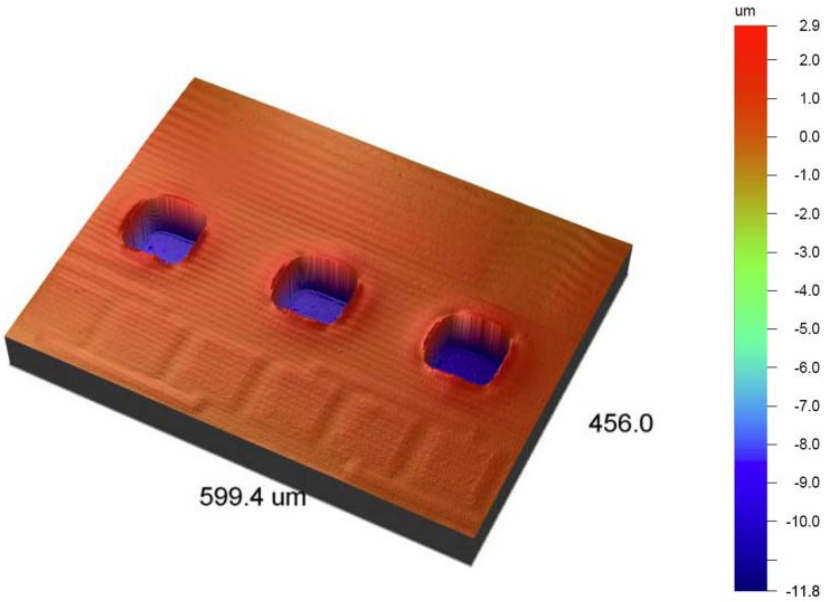

Figure 2.8 *Profile of the developed microvias after curing of polyimide.*

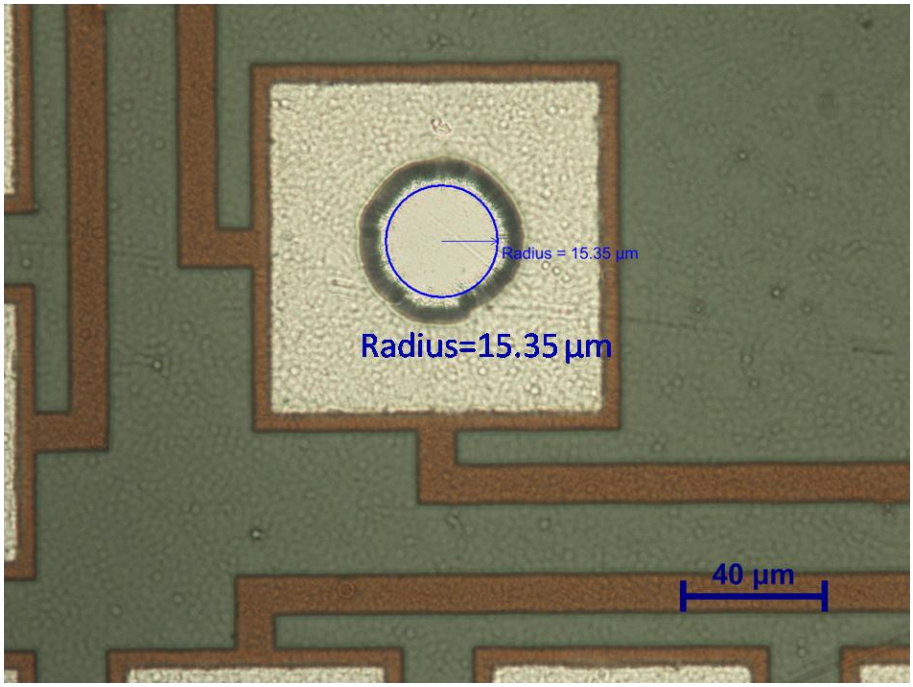

Figure 2.9 *Top view of developed microvia with 30 µm diameter.*

2.4.4 Metallization and Circuit Interconnect

The next task is to make electrical connections to the chip pads. Two pre-treatments need to be done before the metal deposition. First, oxygen RIE was again employed to increase the surface roughness using the same parameters described in above section, since it proved to be helpful to enhance the adhesion of conductor films on polyimide [25]. Second, electroless Ni/Au bumping was applied to remove aluminum oxidation on the chip pads and to lower the contact resistance. This was done by immersing the sample in a sequence of commercially available plating baths (from Enthone Inc.), followed by rinsing in DI water and N2 blow drying. As the chip was covered by the polyimide, the bumping can only happen in the photodefined microvias as shown in Fig. 2.10. The typical bump height is 4 μm Ni / flash (about 100 nm) Au. Then the sample should be dehydrated on a hot plate at 200 °C for 30 min to minimize contamination induced by degassing of the polyimide in the sputtering system.

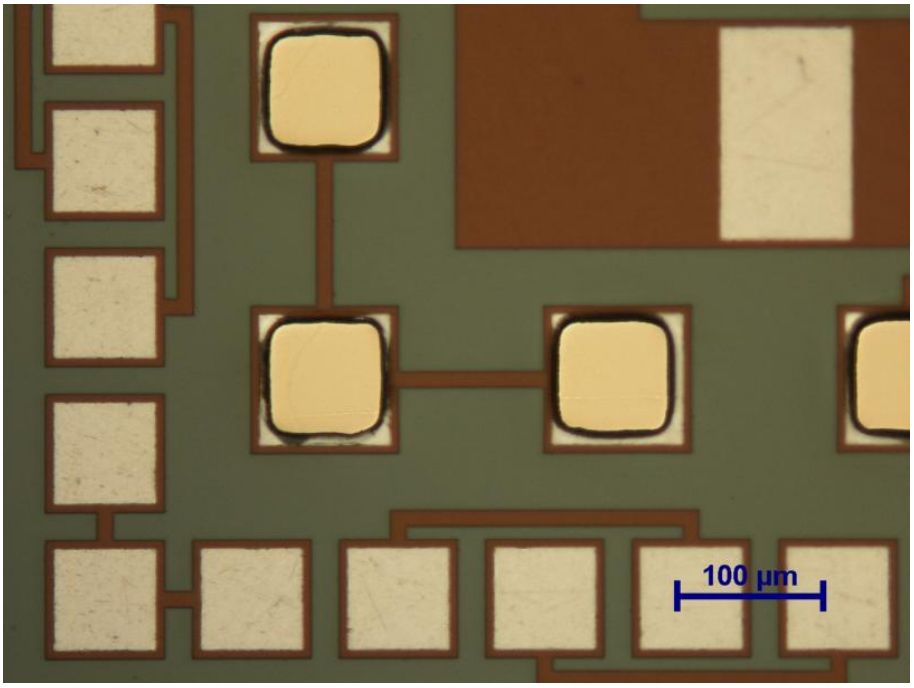

Figure 2.10 *Graph of microvia filled with Ni/Au bumping.*

After the preparation, a seed layer consisting of a 50 nm thick TiW and 1 μm thick Cu was sputtered over the whole top surface, followed by a standard copper electroplating to increase the copper sheet thickness to 6 μm. The multilayer metal stack was annealed at 120 °C for 1 hour in an air convection oven to relieve stress.

In the end, the interconnect pattern was formed using a conventional lithography and wet etching method. The top view of the sample after etching is shown in Fig. 2.11. Moreover, cross sections of the samples were made to inspect the step coverage of the metal in the microvia. An example of such a cross section is presented in Fig. 2.12. Smooth sidewall profiles and desirable metal contacts are observed from the picture.

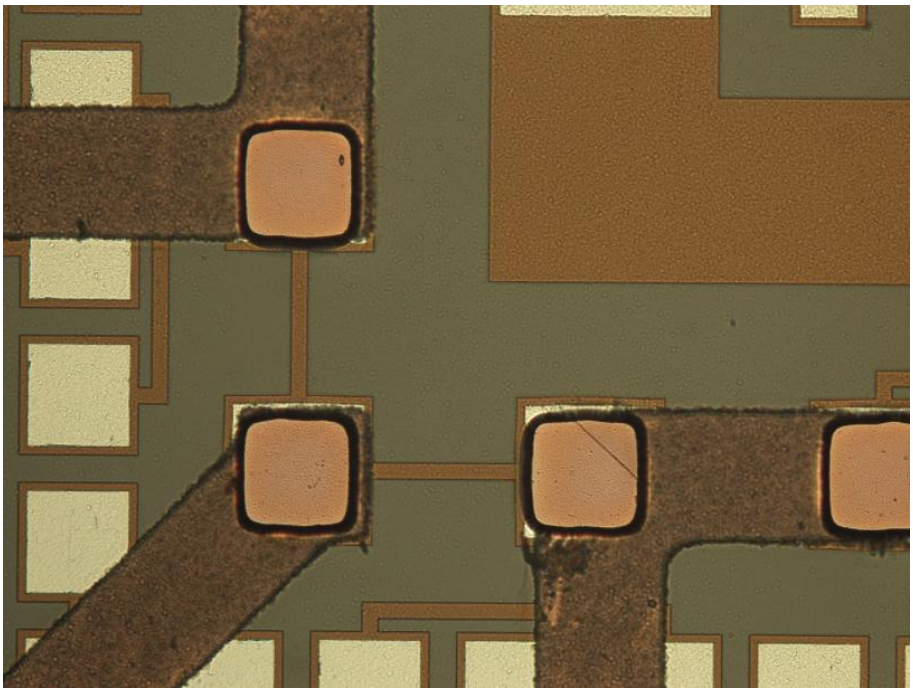

Figure 2.11 *Graph of pattern metallization on top polyimide.*

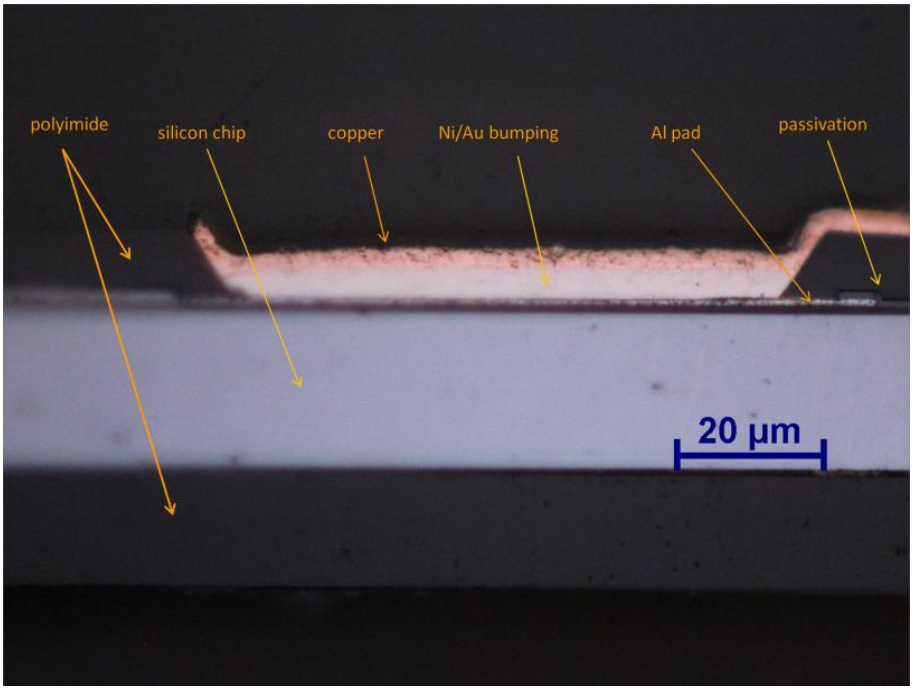

Figure 2.12 *Cross section of UTCP microvia with thinned die.*

2.4.5 Package Release

After the above processes, the assembly of thinned die was ready for release from the glass carrier. But, in order to prevent Cu from oxidation in the following reliability test, a solder mask and a Ni/Au surface finish were applied on the UTCP package. Then, by making a cut in the PI layers, water can reach the underlying KCl film and dissolve it. Therefore, the UTCP package easily comes off the glass carrier. The final result is a flexible chip package with a total thickness of about 50 μm. Fig. 2.13 shows a realized chip UTCP package bending around a pen. The package green look outer surface is the solder mask.

Figure 2.13 *A realized UTCP bending around a pen to show its flexibility.*

2.5 UTCP Characterization

2.5.1 Electrical Measurement

The feasibility of the technology was verified by electrical measurements. 12 samples were produced in a single process run. For each sample, both contact resistance and daisy chain resistance were extracted from the measurements of test structures. It should be mentioned that, all the measurements were done before releasing the samples from their glass carriers.

The contact resistance of the sputtered and plated metal on the chip contact pads was obtained from four-point Kelvin measurements (FP1-4), of which the typical configuration is shown in Fig. 2.14. In this configuration the measured voltage V divided by the imposed current A is the contact

resistance of the metallization on the corner pad. A linear relationship was found between the detected voltage and the current source in the range from -100 mA to +100 mA as shown in Fig. 2.15. On the basis of 48 measurements, we conclude that the contact resistance ranges from 0.2 to 2 mΩ with an average value of 0.83 mΩ. Further analysis reveals that the variation in contact resistance is mainly due to slight differences in four-point configurations of test sites (FP1-4) and different locations of FP1-4 along the daisy chain DCT (refer to Fig. 3). Table 2.1 gives the summary statistics obtained from 12 measurements for each test site. As can be seen in the table, the variation at each test site is below 0.65 mΩ which is almost one third of the overall variation of 1.8 mΩ. Among all sites, FP4 records the lowest average value of 0.34 mΩ, which is reduced as compared with that of our early work [19]. In addition to contact resistance, an average resistance of 12.88 Ω can be deduced from the short daisy chains (DC1-4) measurements of all the samples. Taking account of about 12 Ω Al-on-chip wiring (in total 4.5 mm long, 1 μm thick and 10 μm width) resistance in each daisy chain, the sum resistance of 20 microvia connections is lower than 1 Ω, which is in a good agreement with the contact resistance results. The obtained values are acceptable for chip packaging and prove the success of chip-to-package interconnection.

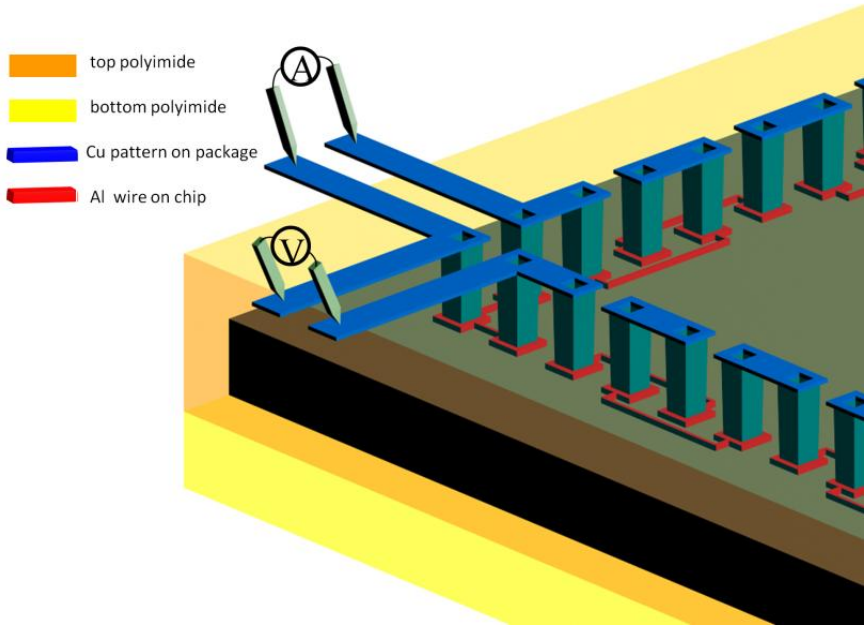

Figure 2.14 *Schematic graph of four-point Kelvin configuration.*

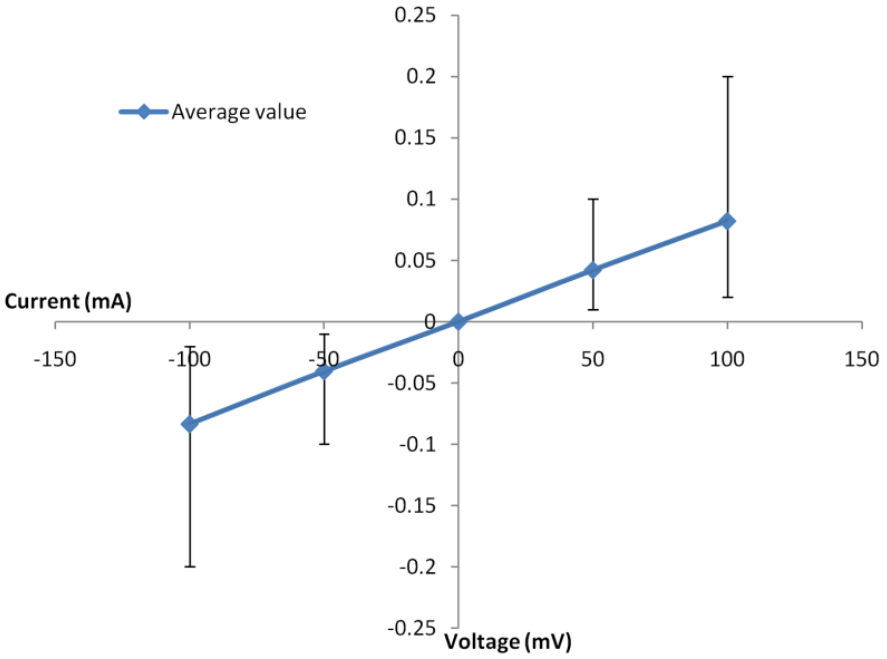

Figure 2.15 *The detected voltage as a function of applied current for four-point Kelvin measurements.*

Test Site	Min	Max	Variation	Average
FP1	1.35	2	0.65	1.6
FP2	0.2	0.65	0.45	0.35
FP3	0.85	1.3	0.45	1.05
FP4	0.2	0.45	0.25	0.34

Table 2.1 *Summary of contact resistance at each test site [mΩ]*

2.5.2 Bending Test

The UTCP mechanical flexibility property was examined by bending tests, which were carried out on 3 samples. Each sample was taped on different cylinders with diameter ranging from 20 to 4 mm as shown in Fig. 2.16. Thus, the embedded silicon chip was bent outwards with its interconnection on the outside. The long daisy chain DCT was measured to check the connection while the sample was bent over the different cylinders. The

obtained DCT resistance at each diameter was shown in Fig. 2.17. All the samples work well when the bending diameter is larger than 6 mm, but the connection is lost due to chip fracture when the bending diameter is lowered to 4 mm. It should be mentioned that only passive structures have been measured under one test condition. More work with more methods is needed to determine the influence of bending on basic active components like CMOS transistors or diodes.

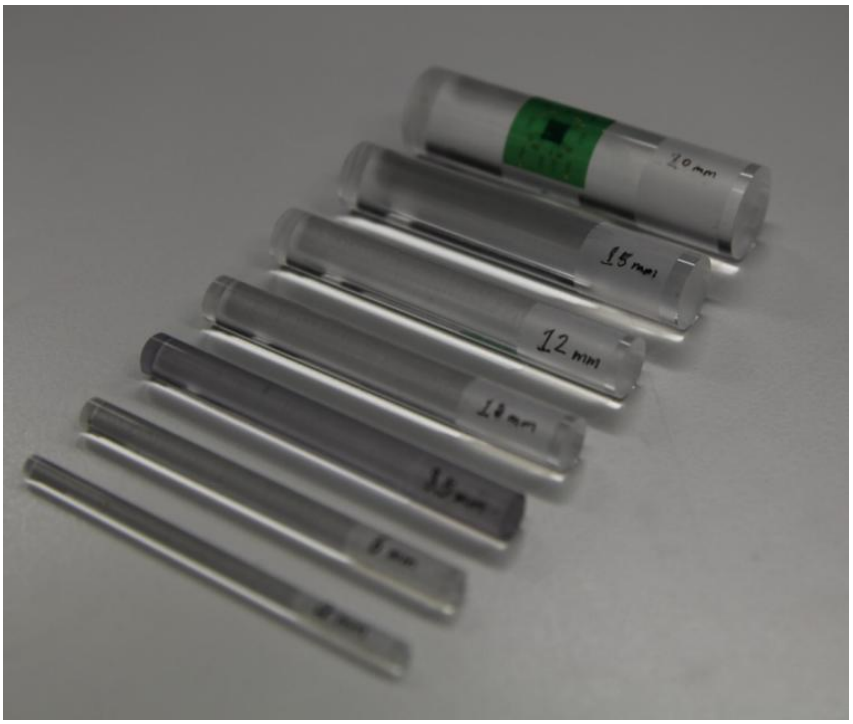

Figure 2.16, *A UTCP is bent over on the surface of cylinders with diameter from 20 to 4 mm for mechanical flexibility test.*

2.5.3 Reliability Test

A thermal cycling test was conducted according to JESD22-A104C standard (-40 °C to 125 °C). Eight samples were taped on ceramic substrates and put in a chamber. Their DCT resistances were measured every 200 cycles as plotted in Fig. 2.18. All the samples survived 1000 cycles without any failure. Furthermore, the contact resistance was monitored for four samples during the reliability test. The average contact resistance (obtained from FP1

to FP4) of each sample is depicted in Fig. 2.19 for each period. All the values remain almost constant up to 1000 cycles, which indicates no degradation of chip-to-package interconnection takes place.

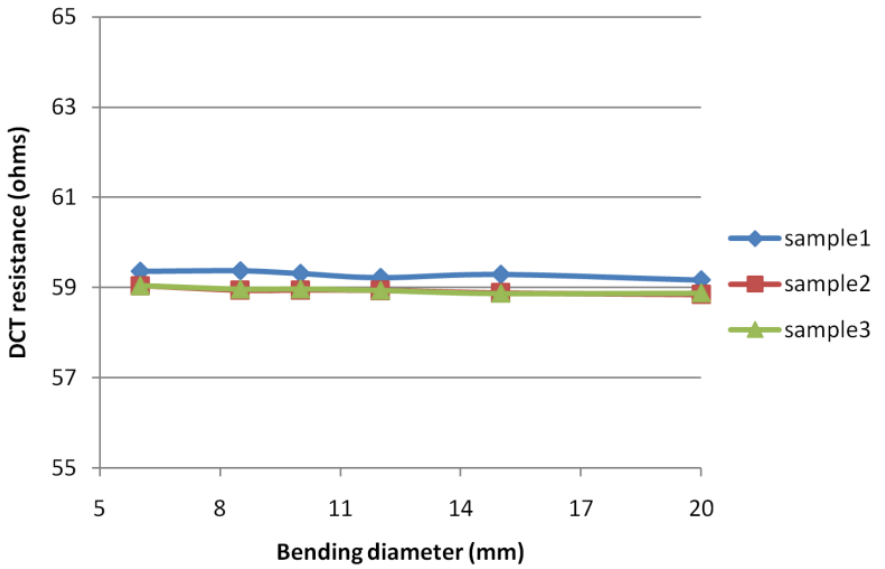

Figure 2.17 *Daisy chain (DCT) resistance as a function of bending diameter.*

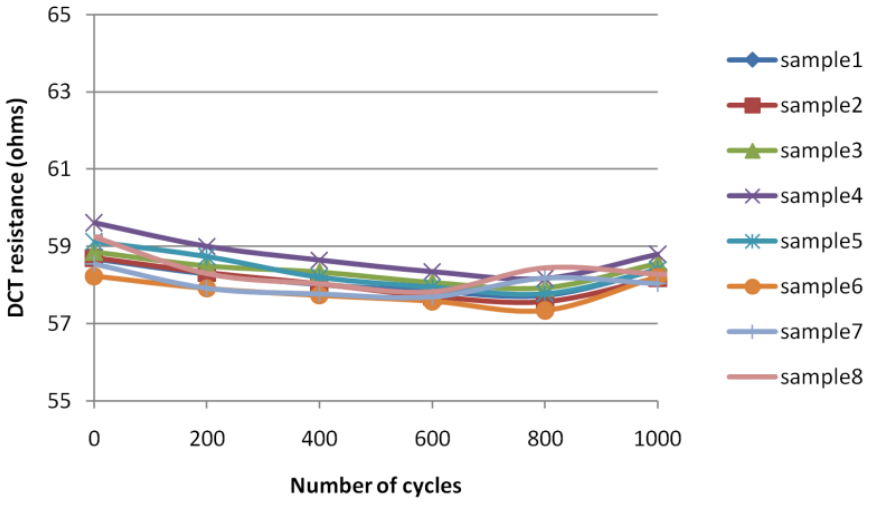

Figure 2.18 *Daisy chain (DCT) resistance under thermal cycling test.*

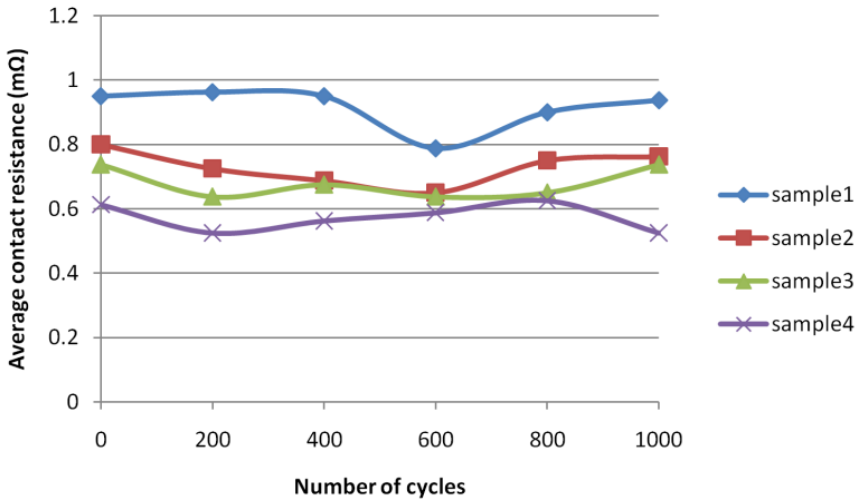

Figure 2.19 *Average contact resistance under thermal cycling test.*

2.6 Conclusion

A new process flow has been developed to embed thinned die (thickness: 20 µm) inside two PSPI layers. In this process, an evaporated KCl film was introduced to release the self-priming PSPI base layer from its rigid carrier substrate. The bonding of the ultra-thin die was improved in order to achieve a planar chip surface. The microvias to the chip contact pads were generated by standard UV lithography, which is a more reliable technique than laser ablation and is a more cost-effective alternative compared to dry etching. The final thickness of the flexible ultra-thin chip package is about 50 µm. Daisy chain test dies were embedded for the first trial. The average contact resistance between chip and package is 0.83 mΩ. The mechanical flexibility property of UTCP was verified by bending the package around the surface of a 6 mm diameter cylinder without any failure of passive resistance structures. A Thermal cycling test (-40 oC to +125 oC) shows that the UTCP is still reliable after 1000 cycles. The present process flow is developed for packageing single chip per carrier and it is easy to transfer to a manufacturing environment without using expensive facilities. If multiple chips are intented to process on one carrier, precise placement of the chips is necessary. The UTCP process allows fine lead pitch (60 µm) ultra-thin chip packaging.

References

[1] C. A. Harper, *Electronic Packaging and Interconnection Handbook*, 4th ed. New York: McGraw-Hill, 2005.

[2] B. Keser, C. Amrine, T. Duong, S. Hayes, G. Leal, W. Lytle, D. Mitchell, and R. Wenzel, "Advanced Packaging: The Redistributed Chip Package," *IEEE Trans. Adv. Packag*, vol. 31, pp.39-43, 2008.

[3] J. W. Balde, *Foldable Flex and Thinned Silicon Multichip Packaging Technology*, Norwell, MA: Kluwer, 2003.

[4] M. Feil, C. D. Adler,M.H. Konig, and K. Bock, "The challenge of ultra thin chip assembly," in *Proc. 54th Electron. Compon. Technol. (ECTC'04)*, Jun. 2004, vol. 1, pp. 35–40.

[5] J. N. Burghartz, *Ultra-thin Chip Technology and Applications*, 1st ed., New York: Springer, 2011.

[6] K. Y. Chen, R. L. D. Zenner,M. Arneson, and D. Mountain, "Ultra-thin electronic device package," *IEEE Trans. Adv. Packag.*, vol. 23, no. 1, pp. 22–26, Feb. 2000.

[7] T. Zhang, Z. Hou, R. W. Johnson, L. Del Castillo, A. Moussessian, R. Greenwell and B. J. Blalock, "Flexile Electronics: Thin Silion Die on Flexilbe Substrates," *IEEE Trans. Electron. Packag. Manuf.*, vol. 32, no. 4, pp.291-300, Oct. 2009.

[8] J. Govaerts, W. Christiaens, E. Bosman and J. Vanfleteren, "Fabrication Processes for Embedding Thin Chips in Flat Flexible Substrates," *IEEE Trans. Adv. Packag*, vol. 32, no. 1, pp.77-83, Feb. 2009.

[9] L. Boettcher, D. Manessis, A. Ostmann, S. Karaszkiewicz, and H. Reichl, "Embedding of Chips for System in Package realization-Technology and Applications," in *Proc. 3rd IMPACT*, 2008, pp. 383-386.

[10] L. Boettcher, D. Manessis, S. Karaszkiewicz, A. Ostmann, and H. Reichl, "Next Generation System in a Package Manufacturing by Embedded Chip Technologies," *Journal of Microelectronics and Electronic Packaging*, vol. 7, pp. 131-137, 2010.

[11] L. Boettcher, D. Manessis, A. Neumann, A. Ostmann, and H. Reichl, "Chip embedding by chip in polymer technology," in *Proc. Device Packaging Conference*, Mar 19-22, 2007.

[12] W. Christiaens, E. Bosman, and J. Vanfleteren, "UTCP: A Novel Polyimide-Based Ultra-Thin Chip Packaging Technology," *IEEE Trans on Compon and Packag* Technol, Vol. 33, No. 4, pp 754-760, 2010.

[13] Chin-Chin Tsai, "Recent development in Flexible Electronics." pp. 370–371, 2011.

[14] J. Hu, "Overview of flexible electronics from ITRI's viewpoint," in *2010 28th VLSI Test Symposium (VTS)*, 2010, pp. 84–84.

[15] A. Nathan, A. Ahnood, M. T. Cole, Y. Suzuki, P. Hiralal, F. Bonaccorso, T. Hasan, L. Garcia-Gancedo, A. Dyadyusha, S. Haque, P. Andrew, S. Hofmann, J. Moultrie, A. J. Flewitt, A. C. Ferrari, M. J. Kelly, J. Robertson, G. A. J. Amaratunga, and W. I. Milne, "Flexible Electronics: The Next Ubiquitous Platform," *Proceedings of the IEEE*, vol. 100, no. Special Centennial Issue, pp. 1486–1517, May 2012.

[16] W.-Y. Chang, T.-H. Fang, H.-J. Lin, Y.-T. Shen, and Y.-C. Lin, "A Large Area Flexible Array Sensors Using Screen Printing Technology," *Journal of Display Technology*, vol. 5, no. 6, pp. 178–183, Jun. 2009.

[17] K. Jain, M. Klosner, M. Zemel, and S. Raghunandan, "Flexible Electronics and Displays: High-Resolution, Roll-to-Roll, Projection Lithography and Photoablation Processing Technologies for High-Throughput Production," *Proceedings of the IEEE*, vol. 93, no. 8, pp. 1500–1510, Aug. 2005.

[18] L. Del Ca, A. Moussessian, R. McPherson, R. Dean, and R. Wayne Johnson, "Flexible electronic assemblies for space applications," *IEEE Aerospace and Electronic Systems Magazine*, vol. 25, no. 6, pp. 25–29, Jun. 2010.

[19] J. Govaerts, E. Bosman, W. Christiaens, and J. Vanfleteren, "Fine-Pitch Capabilities of the Flat Ultra-Thin Chip Packaging," *IEEE Trans. Adv. Packag*, vol. 33, no.1 , pp.72-78, Feb. 2010.

[20] K. Bock, M. Feil, and C. Landesberger, "Thin chips for flexible and 3D-integrated electronic systems," in *Foldable Flex and Thinned Silicon Multichip Packaging Technology*, J. W. Balde , Ed. Norwell, MA: Kluwer, 2003, pp. 101-148.

[21] J.N. Burghartz, C. Harendt, Tu Hoang, A. Kiss, and M. Zimmermann, "A New Fabrication and Assembly Process for Ultrathin Chips," IEEE Trans.on El. Devices, vol.56, pp.321-327, 2009.

[22] E.A. Angelopoulos, M. Zimmermann, W. Appel, S. Endler, S. Ferwana, C. Harendt, T. Hoang, A. Prümm, and J.N. Burghartz, "Ultra-Thin Chip Technology for System-in-Foil Applications", Digest Tech. Papers, IEDM'10, San Francisco, USA, Dec. 6-8, 2010, pp.2.5.1-2.5.4.

[23] M. Feil, C.Adler, G. Klink, M. König, C. Landesberger, S. Scherbaum, G. Schwinn, and H. Spöhrle, "Ultra thin ICs and MEMS elements: techniques for wafer thinning, stress-free separation, assembly and interconnection," *Microsystem Technologies*, vol. 9, pp. 176-182, 2003.

[24] W.J. Lee, Yoon B. Kim, W.Y. Lee, S.H. Han, J.H. Han, and K.K. Jee, "Adhesion Properties of Copper/Polyimide Film Modified by Reactive Ion Etching(RIE)," *Solid State Phenomena*, vol. 124-126, pp1593-1596, Jun. 2007.

[25] HD Microsystems. Product information: Pyralin® HD-4110. http:// www.hdmicrosystems.com

CHAPTER 3

Self Aligned Flat UTCP

Assembly of thinned die allows for making flexible electronics. It is a fast expanding field with numerous applications both in research and industry. UTCP is one of the flexible assembly technologies, by which thinned dies are encapsulated inside spin-coated dielectric films. For sake of higher density integration and bending stress suppression, two UTCPs can be stacked vertically by lamination. This chapter describes further improved UTCP process flow to embed thinned chip in a symmetric dielectric sandwich to achieve a flat topography. The UTCP flat top surface is suitable for metallization and further 3D stacking. In the new process, a central polyimide film is introduced, in which a cavity is made for the embedded chip. The cavity is defined by lithography using the chip itself as a photo-mask. In this way, the cavity size and position is self-aligned to the chip, excluding additional gap filling and polishing steps. The chip thickness is compensated by the surrounding central layer, and a UTCP with flat topography (flat UTCP) is realized after top dielectric deposition. A batch of daisy chain test vehicles was produced. The feasibility of the process flow is verified by optical and electrical measurements. A thermal humidity test was performed and showed no significant degradation of the UTCP after 1000 hours.

3.1 Introduction

On the basis of previous work, an interesting further development of UTCP is to stack individual packages vertically. A stack of two UTCPs can not only increase the functional density, but can also minimize mechanical bending stress in ultra-thin chips [1]. However, in the fabrication of UTCP, the top spin coated polyimide film follows the shape of the embedded chips and creates a non-flat surface. The non-flat topography, in turn, leads to high pressure on embedded chips during stack lamination process, which results in die cracking and yield loss [2]. Thus UTCP with flat top surface (flat UTCP) is a key to reduce pressure on the dies for stacking application.

The first trial of flat UTCP fabrication is presented in [3]. A central photosensitive polyimide (PSPI) layer was introduced, in which a cavity was made by lithography to compensate for the thickness of the embedded chip. Then the chip was placed inside the cavity and the top layer was spin-coated in the end. However, due to inevitable die placement misalignment, the size of the cavity should be slightly larger than the size of the chip. Consequently there is always a gap between the chip and the cavity sidewall. The gap at the chip-cavity interface generates difficulties for lithography and metallization, resulting in a number of opens in the metal tracks that cross the gap.

Therefore, an improved process flow, which can achieve a flat topography and in the meantime solve chip-cavity bridge issue, is proposed and investigated in this PhD research. In the current approach, a cavity is defined through backside illumination by using the chip as a photo-mask. In this way, the size and position of the cavity is self aligned to the chip and no additional gap filling step or chemical mechanical polishing (CMP) are required. Thus, this approach of using the chip as a photo-mask is expected to be more cost effective. The details of fabrication are described in the following sections.

3.2 Process Flow

The technique was developed to embed a thinned die in symmetrical polyimide sandwich films. The schematic process flow is depicted in Fig. 3.1.

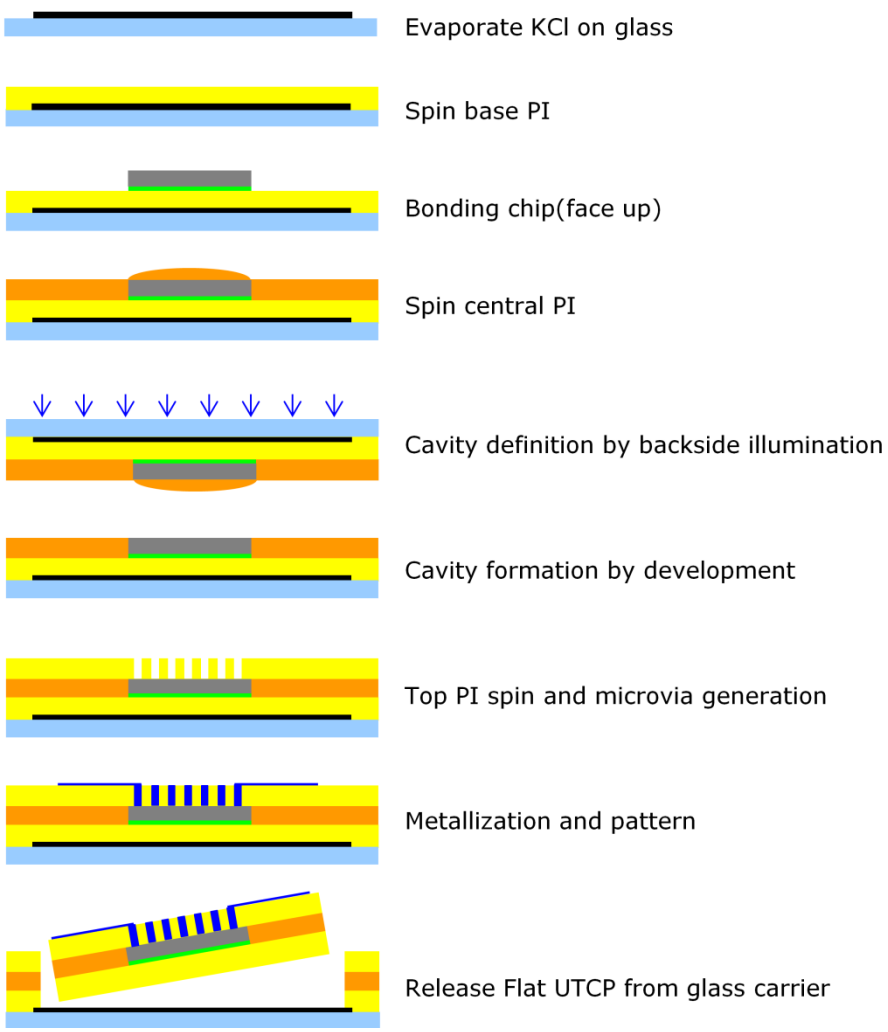

Figure 3.1 *Process flow for fabrication of flat UTCP.*

Firstly, a 400 nm potassium chloride (KCl) layer is thermally evaporated on a rigid glass carrier. Then the base polyimide is spin-coated on the KCl film and fully cured. The thinned die is glued on the base polyimide (face up) by using benzocyclobutene (BCB) as adhesive. A central PSPI layer is spin-coated on top of the chip. After that, UV light is used to illuminate this PSPI layer from the backside of the glass. The illumination is followed by developing the central PSPI film to define the cavity. As a last step, the top polyimide is applied and microvias are generated on chip contact pads for later electrical connections. The multilayer encapsulation of the thinned die

has a flat topography and can be released from the glass carrier. The realized flat UTCP package is flexible and suitable for further stacking applications.

3.3 Test Die and Design

PTCE chips from IMEC are still selected as test dies for the embedding trials. In the first trial of flat UTCP fabrication, reported in [3], the interconnect pitch of 100 µm was explored. However, due to the open metallization problem at the chip-cavity interface, the yield is low (about 50%). In this study, the 100 µm pitch daisy chain remains selected so as to enable comparison to the first trial. The daisy chain with 100 µm pitch contains 180 aluminum contact pads with dimension of 70 µm × 70 µm × 0.8 µm (length × width × thickness) and 30 µm wide space in between. A metallization pattern is designed to connect the bond pads, as shown together with the chip layout in Fig. 3.2. Since the interconnection problem occurred at the chip-cavity interface in previous work, the interconnect traces between two adjacent pads were designed intentionally to protrude across the interface towards the outside of the cavity, in order to demonstrate the feasibility and reliability of the improved process flow. The layout of the metallization consists of four short daisy chains (DC1-4) along the edges. A series link from DC1 to DC4 forms a long daisy chain DCT, in which the total length of copper traces on the package (60 µm width) and aluminum wiring on the chip (10 µm width) are 10.38 cm and 2.03 cm, respectively. In addition, 4 four-point Kelvin structures (FP1-4) were also fabricated at corners of the chip for precise contact resistance measurements.

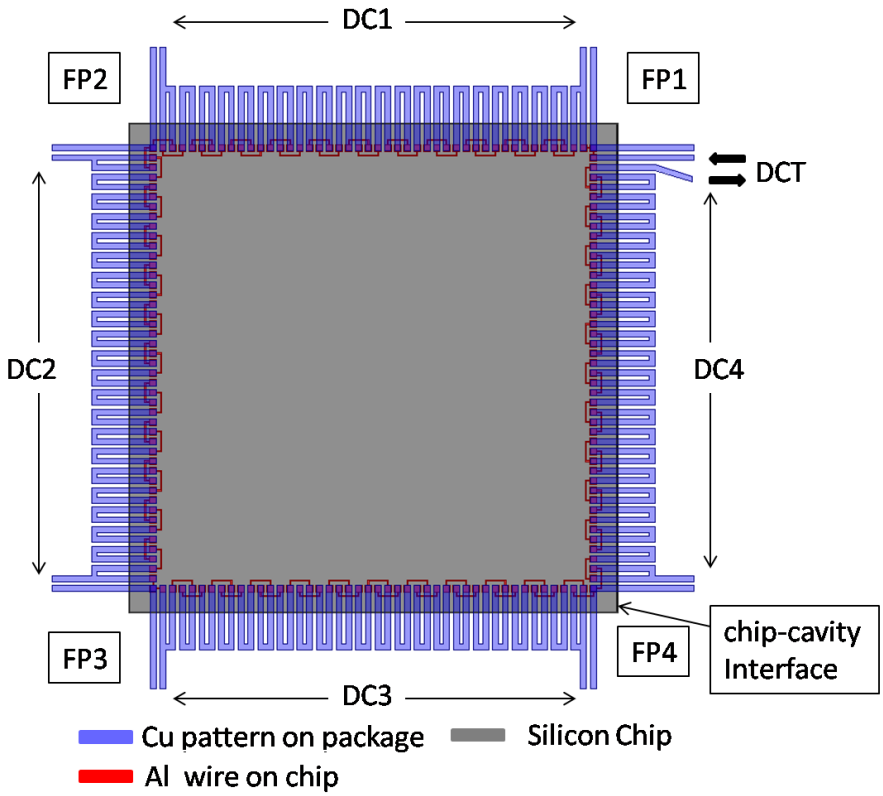

Figure 3.2 *Schematic layout of PTCE chip and its UTCP interconnection. (The chip-cavity interface is indicated by the outline of the gray square.)*

3.4 Fabrication Process and Optimization

The details of substrate preparation, chip placement and microvia generation were thoroughly discussed in [4,5]. This section focuses on the use of a central polyimide layer to make a cavity for chip thickness compensation.

The chip assembly was built up on a 5 cm × 5 cm rigid glass carrier purchased from Praezisions Glas and Optik. A 400 nm thick KCl layer was thermally evaporated on the glass. The ultra-thin PTCE chip was then embedded in a polyimide sandwich structure on the prepared glass carrier. This multilayer structure needs to be a symmetrical buildup to avoid coefficient of thermal expansion (CTE) mismatch problem. That is to say,

the top and bottom polyimide should be the same material, such as PI-2611 series or HD-4100 series polyimide (both are from HD Microsystems). In this case, the top and bottom layer can exert equal stress on the central layer but in opposite directions, and the entire stack will remain flat after release from the carrier as shown in Fig. 3.3 (a) and (b). In comparison, Fig. 3.3 (c) presents an asymmetric stack composed of 10 µm PI-2611 / 20 µm HD-4110/ 10 µm HD-4110. The CTE mismatch between PI-2611 (3x10^-6/°C) and HD-4110 (35x10^-6/°C) causes high intrinsic stress and results in excessive curling of the stack. For simplicity, in this entire work, we limit ourselves to the use of HD-4110 polyimide for all three layers, like in Fig. 3.3 (b). It should be mentioned that all layers were cured at a maximum temperature of 350 °C in a vacuum oven. In addition, an oxygen plasma treatment was applied before each deposition step for adhesion enhancement.

After the bottom layer was spin-coated and fully cured, the chip was permanently attached on top of it using BCB as adhesive. Fig. 3.4 is a view from the sample backside. It can be seen that over the whole substrate, only the chip area was opaque whereas the other surface area was almost transparent in the visible light range. As a guide for later exposure assessment, the optical transmittance of the substrate was measured by using UV-VIS spectrophotometer (Shimadzu Corp.) over the wavelength range from 200 to 1100 nm in a 1 nm increment, and is plotted in Fig. 3.5. High light absorption (>95%) is observed in the ultraviolet regime, and with a sharp increase in transmission at about 400 nm, the light transmittance becomes stable around 80% beyond 500 nm.

The central PSPI film was then applied, wherein a cavity was to be made for chip accommodation. It is important to match the film thickness to the chip thickness, so that the final top layer can be deposited on a relatively flat base.

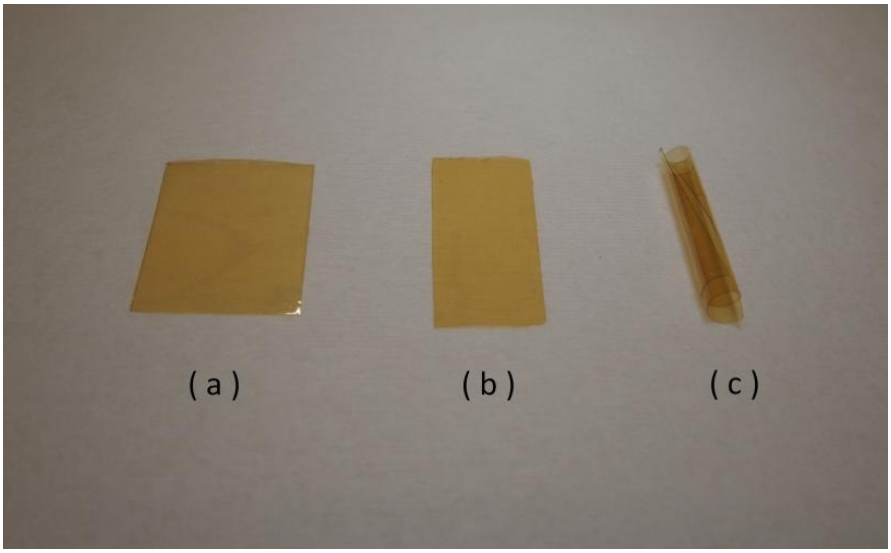

Figure 3.3 *Graph of freestanding polyimide multilayer structure. a) PI-2611/ HD-4110/ PI-2611symmetrical stack. b) A homogeneous stack of three HD-4110 films. c) PI-2611/ HD-4110/ HD-4110 asymmetrical stack.*

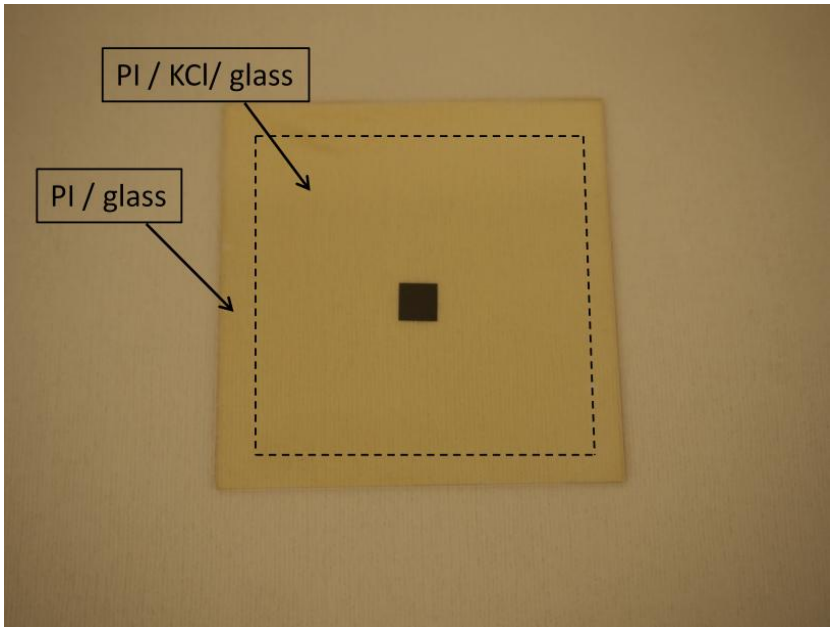

Figure 3.4 *Rear view of PTCE chip attached on prepared substrate (dashed lines show boundary between PI/glass and PI/KCl/glass zones).*

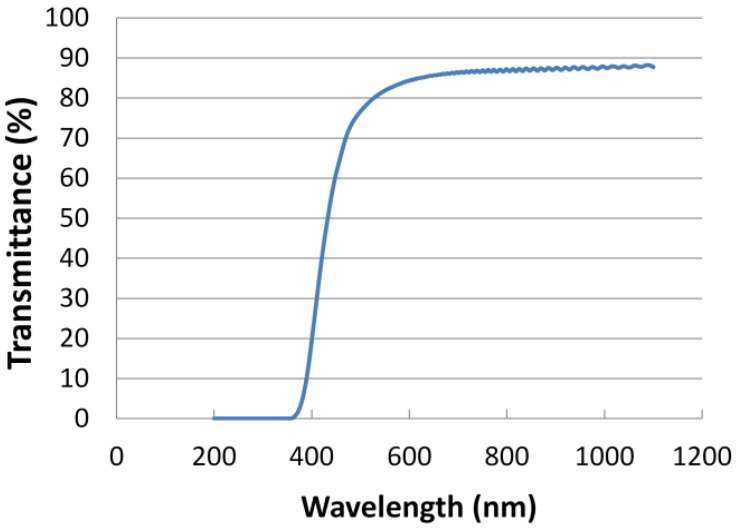

Figure 3.5 *Optical transmittance of 15 μm HD-4110 film on KCL evaporated glass carrier.*

The thickness of central PSPI film can be adjusted in a certain range by controlling the spin speed. The spin curve for HD-4110 was obtained experimentally and is plotted in Fig. 3.6. According to the solid line in Fig. 3.6, spinning at a speed of 1400 rpm for 1 min results in about 20 μm thick central PSPI film after curing, which is equal to the chip thickness. In case a thicker chip (more than 30 μm) needs to be embedded, a second central layer is required to be coated.

After spinning, the sample should be baked on a hot plate at 110 °C for 4 min for obtaining a tack-free top surface. Up to this processing step, the substrate is blank except for the placed chip. This provides a good condition for the subsequent exposure step. The sample was flipped over and the substrate is illuminated from the back. Therefore the portion of central polyimide film on top of the chip was blocked from exposure. Since the HD-4110 is a negative tone photosensitive material, the unexposed portion of the central coating will be removed by developer and a cavity is then realized. Because the chip itself was used as a photo-mask for cavity formation, the cavity dimension can perfectly fit the chip size without any gap in between. It should be mentioned that this self aligned process can be directly applied to multiple chips on a single substrate in future development.

Illumination was done using a broadband light source with an output intensity of 9 mW/cm2. Although HD-4110 is the most sensitive to I-line radiation (365 nm), broadband light is also capable to drive photochemical reaction and reduce the amount of I-line energy used. According to the transmittance spectrum depicted in Fig. 3.5, I-line spectrum was totally absorbed by the base substrate. So it is logical to prolong the exposure time to reach the required energy level. If the light dose is not sufficient, there is a risk of delamination of the coating layer. In contrast, excessive time will limit overall throughput. The threshold was determined by gradually decreasing exposure time from 4 min until delamination occurred. This test result indicates a minimum time of 1 min.

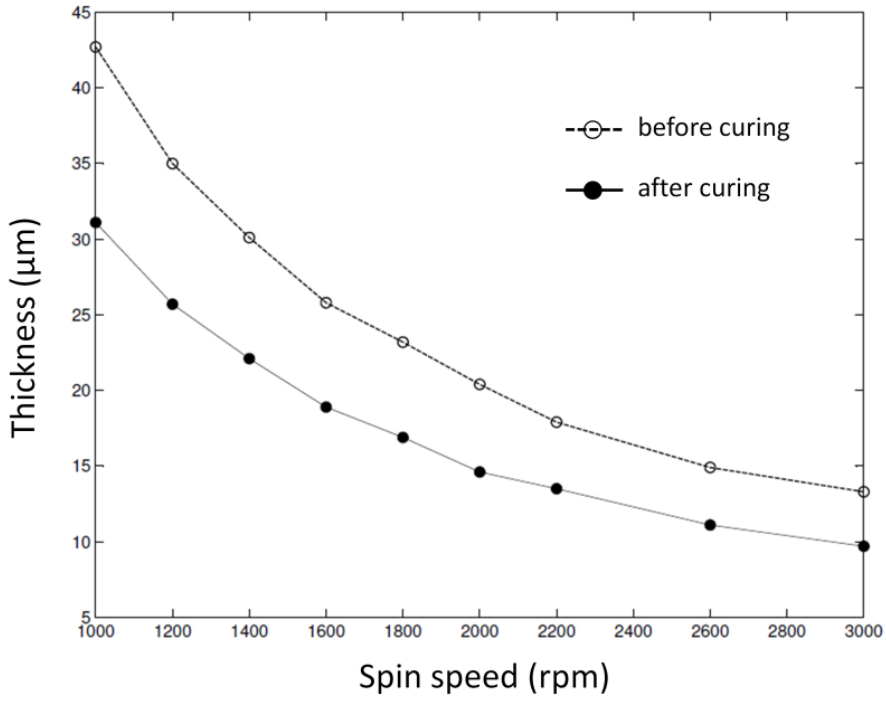

Figure 3.6 *Spin curve of polyimide HD-4110.*

After exposure, the sample needs to be held at room temperature for a minimum of 10 min prior to development for optimal resolution. The development was then carried out by immersing the sample in a beaker filled with PA400D for 40 s with the assistance of ultrasonic agitation. This is followed by two 30 s consecutive rinses: firstly in a 1:1 mixture of PA400D and PA400R and secondly in pure PA400R.. Fig. 3.7 is an optical surface profile (Veeco system) at the interface between chip and cavity after curing.

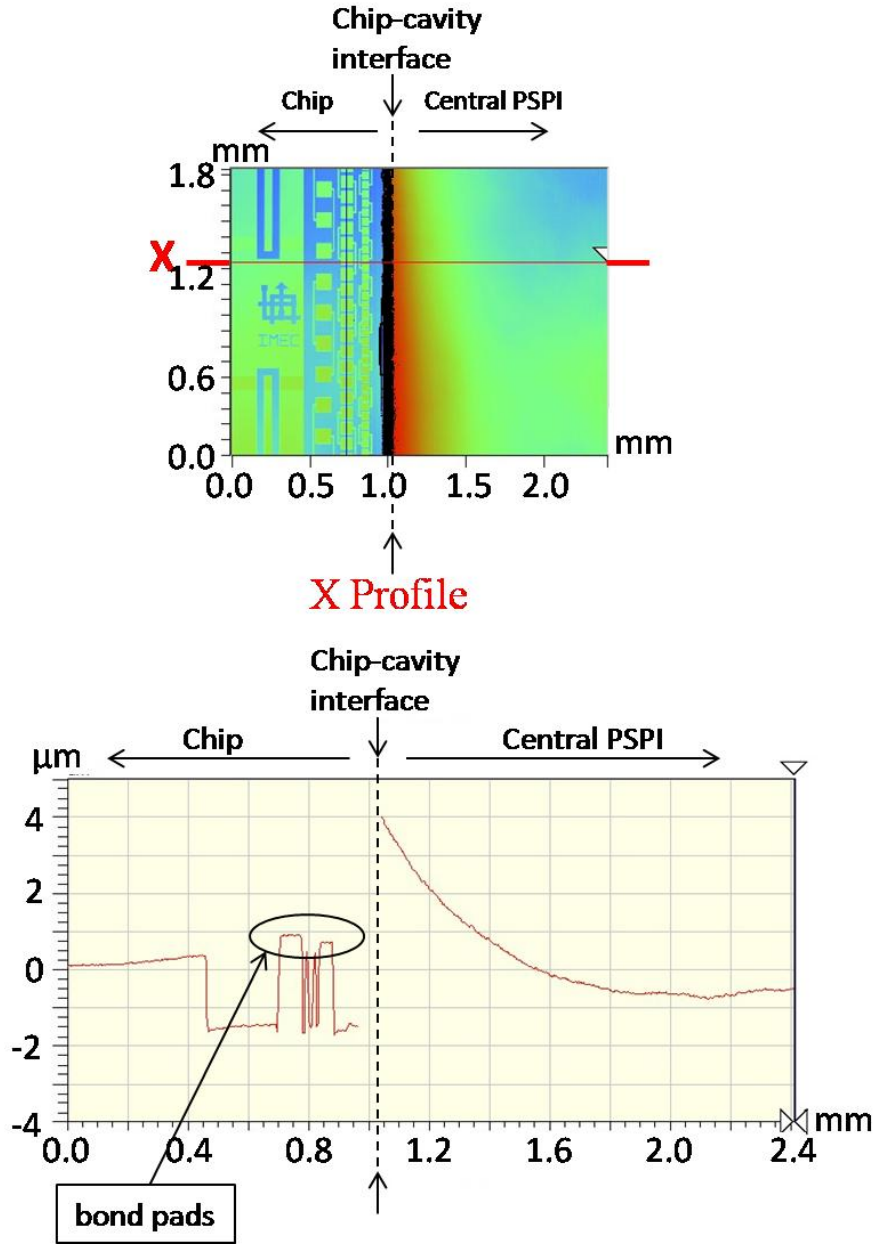

Figure 3.7 *Surface profile of attached PTCE chip and its surrounding thickness compensation layer.*

It can be seen that the chip thickness was compensated by the surrounding central film and no gap is observed at the interface. At this point of the processing a 4µm step height of the PI at the edge of the chip is measured. As will become clear, the subsequent top PI easily planarises this topography.

In the next step, the top layer was spin coated for a thickness of 15 µm to cover the chip. Microvias to the embedded chip were generated for electrical connection. Both laser drilling and photo imaging are feasible for microvia formation. In this work, a photo imaging process was performed. Fig. 3.8 presents a top view of microvias on contact pads after curing of the top layer. The circular via bottoms with diameters of 53 µm are clear of any visual obstruction. The corresponding surface topography was examined, whose 3D plot is presented in Fig. 3.9. Fig. 3.10 shows the thickness variation along the indicated plane A-A of Fig. 3.9. As can be seen from the two figures, a flat top surface profile with thickness variation smaller than 1 µm (except for the via depth) was realized. The flat topography eliminates the chip-cavity bridge issue, which makes the package suitable for pattern definition and future 3D package stacking.

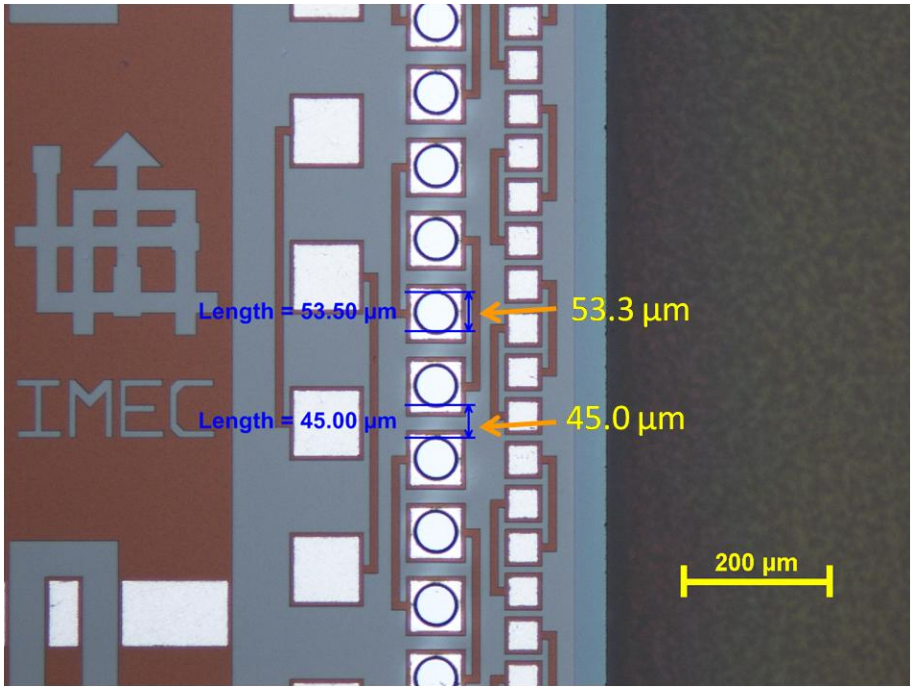

Figure 3.8 *Top view of developed microvias with 50 µm diameter.*

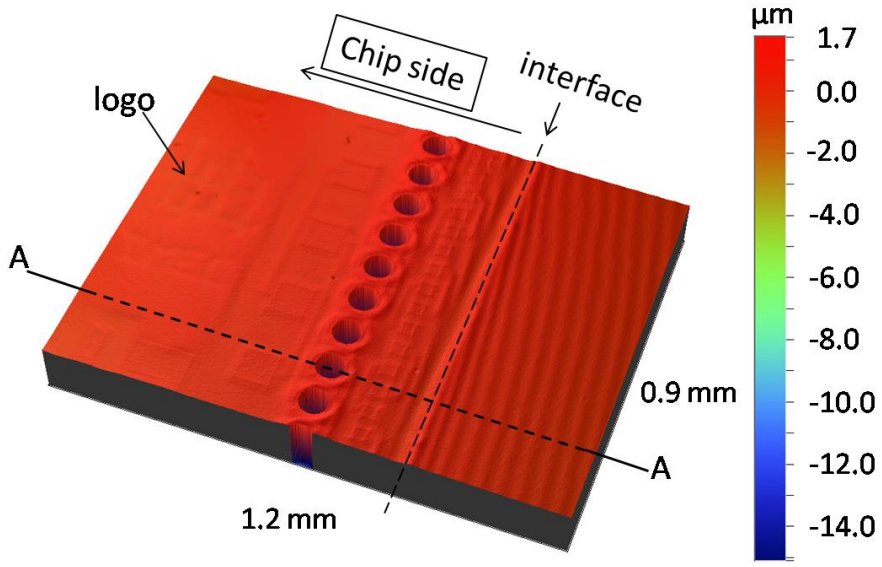

Figure 3.9 *3D image of flat UTCP with embedded PTCE chip.*

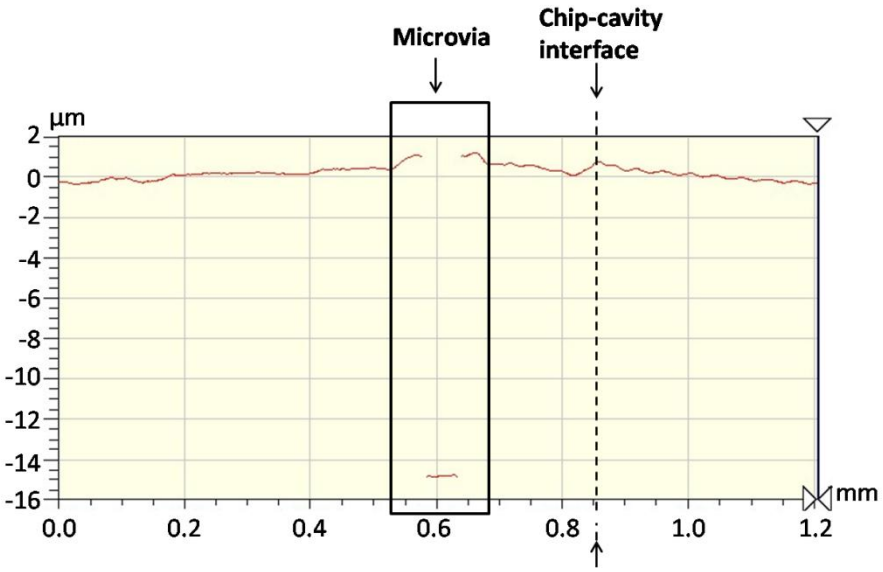

Figure 3.10 *Thickness variation along plane A-A in Fig. 3.9.*

In the end, electrical connections were made. A metal seed layer consisting of 50 nm TiW and 1 µm Cu was sputtered after a standard electroless Ni/Au under bump metallization (UBM) process of the Al chip bond pads. Copper was electroplated uniformly over the substrate up to a thickness of 4 µm. Finally, the metal layers were patterned by subtractive etching. The top view of the sample after etching is given in Fig. 3.11. The metal traces were routed from the chip region to the external region without any failure.

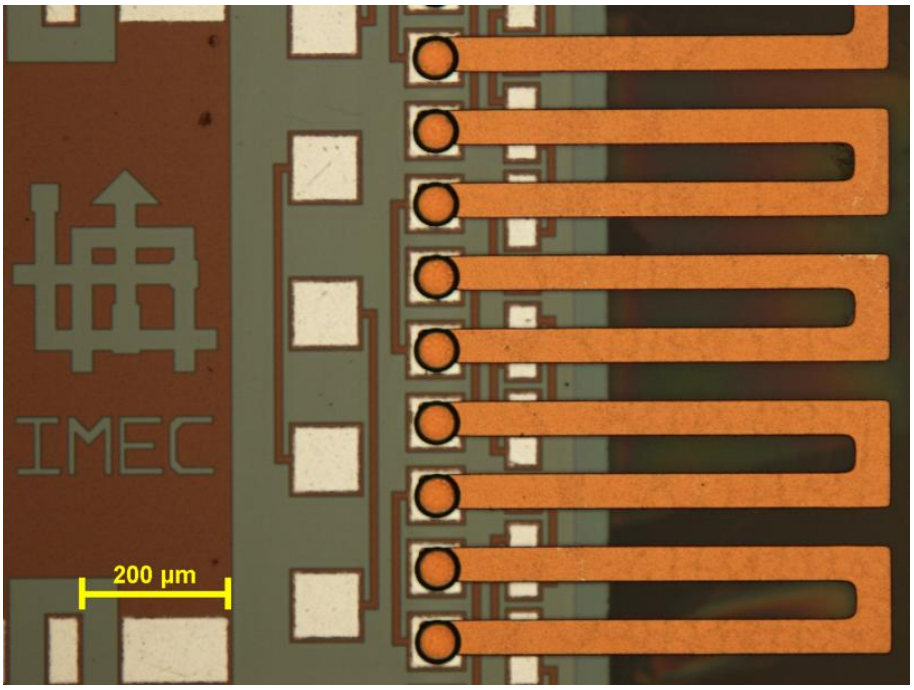

Figure 3.11 *Graph of metallization pattern on top polyimide.*

The flat assembly of thinned die with a total thickness of about 50 µm was now ready for release from the glass carrier, thus obtaining a flexible chip package suitable for 3D stacking. The release was done by providing an access to the KCl release layer by cutting through the PI stack, followed by dissolving the KCl in water, thus releasing the package from the glass substrate. However, for the following reliability test, a solder mask and a Ni/Au surface finish were also applied on the UTCP package before release.

3.5 Characterization

3.5.1 Electrical Measurements

Daisy chain and contact resistance measurements were performed on the first batch of 9 samples to verify the electrical connection. Calculated from 36 measurements, the contact resistance varies from 1.65 to 7.6 mΩ with an average of 4.28 mΩ. The obatained value shows a higher resistance compared to the results in Chapter 2. The higher contact resistance is because of the reduced contact area in smaller microvia.This is also observed in our previous work [3], which shows a similar result. Anyway, the contact resistance is low enough for a good electrical connection. The long daisy chain (DCT) resistance amounts to a mean value of 79.78 Ω. This value is composed of 71.5 Ω of Al wiring on chip, 7.4 Ω of Cu trace on package, and about 1 Ω of 180 microvia connections, which is in a good agreement with the contact resistance results. The daisy chain resistance implies 100% yield, showing a clear improvement compared to our previous Flat UTCP experiments [4].

3.5.2 Reliability Test

In the previous section, a thermal cycling test was conducted on samples made of PSPI and showed no degradation after 1000 cycles. Due to the moisture absorption property of polyimide, in this work, realized samples were stored in an environment at 85 °C and 85% RH for thermal humidity test, which thus can be considered as a severe reliability test. DCT resistances were measured every few days until 1000 hours, as plotted in Fig.3.12. Furthermore, the contact resistance was monitored for four samples during the reliability test. The average contact resistance of each sample is depicted in Fig.3.13. Both DCT resistances and contact resistance of each sample remain almost constant after 1000 hours, which indicates that interconnect degradation is negligible and the UTCP package has a high resistance to moisture intrusion.

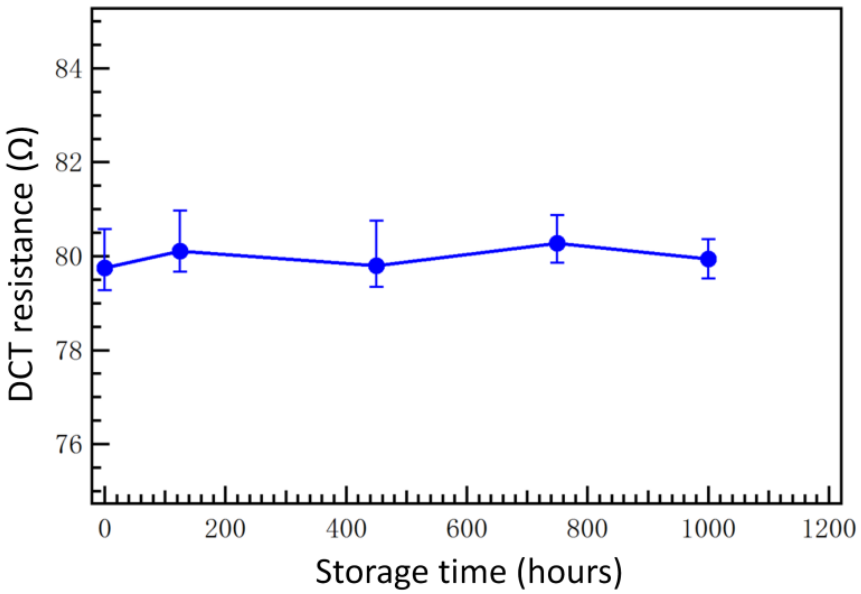

Figure 3.12 *Daisy chain (DCT) resistance under thermal humidity test.*

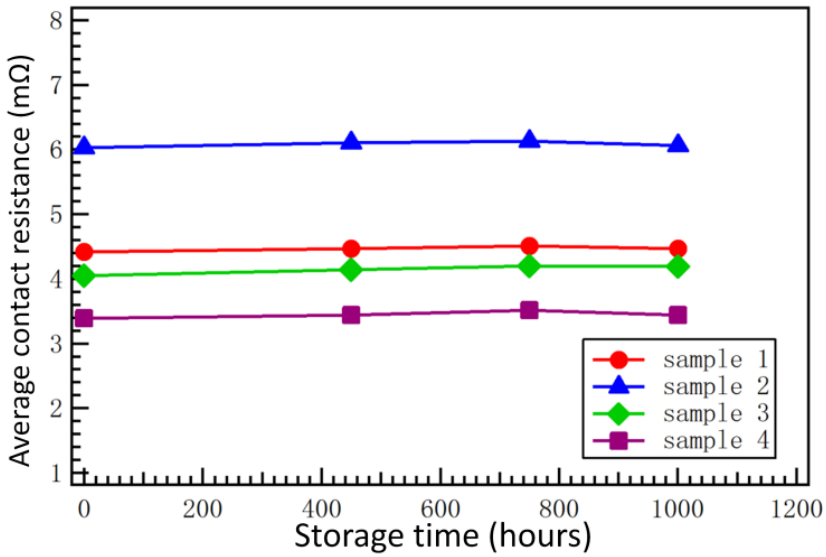

Figure 3.13 *Average contact resistance under thermal humidity test.*

3.6 Conclusion

3D Stacking of individual UTCPs allows for higher density integration and bending stress suppression. A key to achieving this is the fabrication of a flat topography on UTCPs to alleviate lamination pressure on the embedded dies. An improved process flow has been developed to embed thinned die (thickness: 20 µm) in a symmetric polyimide sandwich. The top and bottom layer should be made of the same material to avoid CTE mismatch problems. For thickness compensation a central layer was introduced in which a cavity was made to accommodate the embedded chip. The cavity was defined by a self aligned method using the chip as a photo-mask. A UTCP with flat topography (flat UTCP) is realized after top dielectric deposition. The flat UTCP can be released from its carrier, resulting in a flexible chip assembly with a total thickness of about 50 µm. A batch of daisy chain test vehicles was produced. Compared to previously published flat UTCP trials, the improved process shows a significant yield increase. A thermal humidity test was performed on the test vehicles and showed no significant degradation after 1000 hours storage at 85 °C and 85% RH.

References

[1] S. Endler, H. Rempp, C. Harendt, and J.N. Burghartz , "Compensation of externally applied mechanical stress by stacking of ultra-thin chips," in Proc. 41st Eur. Solid-State Device Res. Conf., Helsinki, Finland, 2011, pp. 279–282.

[2] S. Priyabadini, A. Gielen, K. Dhaenens, W. Christiaens, S. Van Put, J. Vanfleteren, G. Kunkel, A.E. Petersen, "3D-Stacking of UTCPs as a Module Miniaturization Technology," in Proc. 44th. Int. Symp. On Microelectronics (IMAPS 2012), Long Beach, CA, Oct9-13, 2011.

[3] J. Govaerts, W. Christiaens, E. Bosman and J. Vanfleteren, "Fabrication Processes for Embedding Thin Chips in Flat Flexible Substrates," *IEEE Trans. Adv. Packag*, vol. 32, no. 1, pp.77-83, Feb. 2009.

[4] W. Christiaens, E. Bosman, and J. Vanfleteren, "UTCP: A Novel Polyimide-Based Ultra-Thin Chip Packaging Technology," IEEE Trans on Compon and Packag Technol, vol. 33, No. 4, pp 754-760, 2010.

[5] L.Wang, T. Sterken, M. Cauwe, D. Cuypers, and J. Vanfleteren, "Fabrication and characterization of flexible ultrathin chip package using photosensitive polyimide," IEEE Trans on Compon Packag and Manuf. Technol, vol. 2, No. 7, pp 1099-1106, 2012.

CHAPTER 4

Characterization of Thin Film Dielectric Material

This chapter describes a method to determine the complex permittivity of a dielectric material from microstrip line measurements. The transmission line equivalent circuit model is adapted for the case of an air-filled line and a lossless line, whose distributed elements can be obtained by simulations. The technique includes a simple way to separate the dielectric loss from the measured total loss using the propagation constant. A rational dielectric model is employed to fit the extracted complex permittivity, which ensures causality of the final solution. A good agreement is shown between the experimental and the simulated results. The proposed method is demonstrated on a thin film polyimide material, and it can also apply to materials with high surface roughness.

4.1 Introduction

The current electromagnetic simulation tools can achieve very high accuracy and provide valuable insight into circuit behavior. This helps circuit design engineers to build up models for signal analysis and performance prediction. An accurate simulation model requires precise input data on the complex

permittivity of substrate materials. As the transmission speed increases, it's desirable to obtain the broadband high frequency dielectric property instead of using the single point low-frequency information given by manufactures. In the past decades, extraction of dielectric permittivity was accomplished by numerous measurement schemes, which mainly fall into three categories: parallel plate capacitor [1], resonators [2,3] and transmission line (TLine) measurements [4-7]. The parallel plate method only works at low frequencies and the resonator measurement is reliable at a few discrete frequency points. The TLine measurements, on the other hand, give repeatable results and showed capability of determining frequency dependent material parameters. Based on TLine measurements, some recent researches relate the imaginary part of the permittivity to the real part of it using dielectric relaxation models [8,9]. The obtained permittivity is physically consistent with the Kramers-Kronig relation. However the algorithm for optimizing dielectric model parameters is somehow complex and normally returns multiple solutions, which need to be further determined by numerous simulations. In contrast, we first calculate the complex permittivity with aid of simulation and design equations. A simple way is proposed in this work to separate the dielectric loss of the substrate from the measured total loss. And then a rational dielectric model is used to fit the calculated raw data, which ensures the causality constraint.

4.2 Experiment

Polyimide dielectric HD-4110 (from HD Microsystems) is selected as specimen material. And the thin film microstrip line (TFMSL) is used as test structure. The TFMSL, as depicted in Fig. 4.1, consists of two metal layers and one dielectric layer. In this work, both the signal trace and ground plane are copper films deposited using magnetron sputtering.

Multiple TFMSLs were fabricated on a single substrate. First the ground metal layer was deposited directly on the glass carrier and then patterned by wet etching method. Next, the central polyimide film HD-4110 was spin coated. In order to make electrical connection from probe pads to the microstrip ground plane, via holes were generated through the central polyimide by the lithography technique as explained in previous chapters. The sample was then cured in a vacuum oven. After the curing, a brief RIE treatment was applied on the polyimide surface, and the top metal layer was deposited and patterned. Fig. 4.2 presents a graph of the realized sample including a set of TFMSLs with different length from 400 μm to 7000 μm.

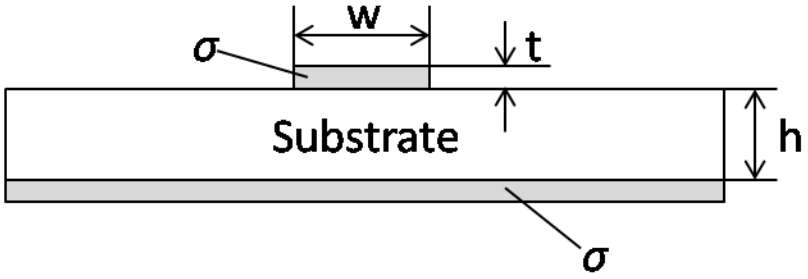

Figure 4.1 *Microstrip line cross section with dimensions and conductivity, where w = 38.3, t = 1, h = 14.2 (all in micrometers) and σ = 5.8×10^7 S/m.*

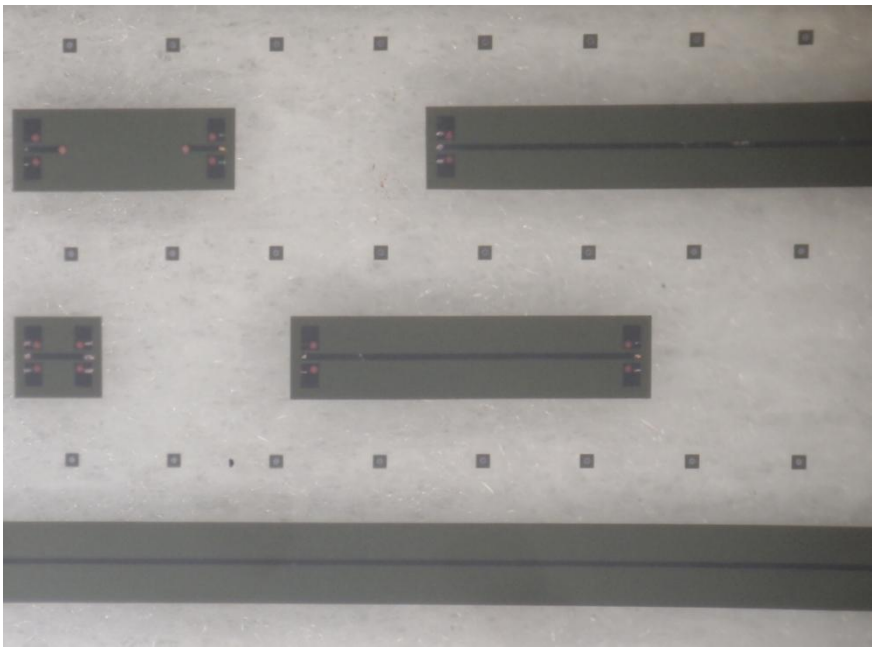

Figure 4.2 *The realized TFMSLs for extraction of polyimide permittivity. The first structure from the left is a short reflection element and the rest of the structures are TFMSLs with line length from 400 to 7000 µm.*

All the lines, in addition to connecting with the same Ground-Signal-Ground (GSG) probe pads, have the same line width of 38.3 µm. A linear taper transition is made from the central probe pad to the microstrip width. The thickness of polyimide is measured to be 14.2(±0.15) µm across the whole surface area. After the fabrication, the surface roughness of both polyimide

and top metal trace were inspected by means of a Wyko optical profilemeter. The calculated root-mean-square roughness for both polyimide and metal surface is below 20 nm, which is low enough so that it can be neglected in the following analysis.

The microwave measurements on the TFMSLs were carried out by using a vector network analyzer (VNA) AGT E8361C (from Aglient Technologies). A total number of 401 frequency points were measured over the frequency range from 10 MHz to 60 GHz. A pair of GSG probes with pitch of 150 μm was connected to the VNA through coaxial cables. After an initial probe tip thru-reflection-line (TRL) calibration, the probes were directly placed on the TFMSL contact pads to start measurements. The temperature of laboratory during measurement is 20°C.

The propagation constant can be determined from the scattering parameter measurements of transmission lines using multiline method [10]. If two measured microstrip lines have the same line width and dielectric thickness, a larger difference in their line length can minimize the error in calculating the propagation constant. However it is difficult to control the dimension uniformity for an extremely long line. Any variation in the dimension will deteriorate the accuracy of the method. In this work, we use only two TFMSLs with length of 400 and 7000 μm, which are the shortest and longest line amongst the realized structures.

4.3 Methodology

The central dielectric of the TFMSLs is spin-coated polyimide film, which was cured in a vacuum oven. The complex permittivity of the dielectric is defined as

$$\varepsilon = \varepsilon_0 \varepsilon_r (1 - \mathrm{j} \tan\delta) \tag{1}$$

where ε_0 is the free space permittivity, ε_r is the relative permittivity and $\tan\delta$ is the loss tangent.

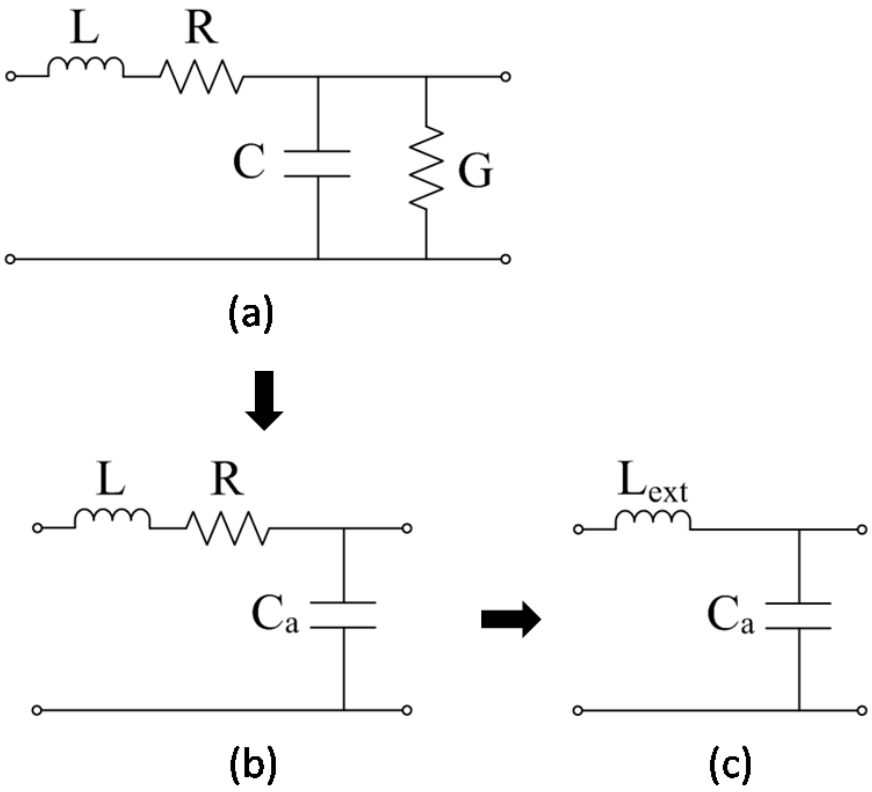

Figure4.3 *Distributed equivalent circuit model of the microstrip line in the following cases (a) dielectric-filled line, (b) air-filled line, (c) air-filled lossless line.*

When the TFMSL operates in the quasi-TEM region, a well known distributed equivalent circuit model can describe its transmission behavior, as shown in Fig. 4.3a [11].

The TLine characteristic impedance Z and propagation constant γ can be written in terms of the distributed elements,

$$Z = \sqrt{\frac{(R+j\omega L)}{(G+j\omega C)}} \tag{2}$$

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{3}$$

The resistance and inductance per unit length are independent on the central dielectric property [12]. Thus, in case of an air-filled line, the equivalent circuit model can be simplified by removing the shunt conductance while retaining the series impedance elements such as shown in Fig. 4.3b. It is also of note that the air-filled capacitance per unit length is represented by Ca. The total inductance is a sum of its internal and external part. The internal inductance, which stems from the magnetic field inside the conductors, is further excluded in the model of Fig. 4.3c for an air-filled lossless line. The expressions of characteristic impedance and propagation constant in Eq. 2 and 3 also hold for the models of Fig. 4.3b and c, and their value can be calculated by a full wave simulation of the TLine. Then combining Eq. 2 and 3, the value of the distributed elements are also determined. Ansoft HFSS is employed to perform the simulation. An air-filled microstrip model is built up with the same geometry as shown in Fig. 4.1. Since the surface roughness of the TFMSL is measured within tens of nanometer, its influence on transmission is not incorporated in the simulation. According to Fig. 4.3, the total inductance and resistance are obtained through simulation of the model with finite conductivity. Similarly, the external inductance is calculated through simulation of the model with perfect conductor.

4.4 Dielectric Permittivity Extraction

The propagation constant of the TFMSL is able to be extracted using two lines with different length. For both lines, the measured two port scattering parameters can transfer to a form of cascading matrix **M**, which is considered as a product of three parts,

$$[M_1] = [X] \bullet [T_1] \bullet [Y] \quad (4)$$

$$[M_2] = [X] \bullet [T_2] \bullet [Y] \quad (5)$$

where the input transition from probe tip to microstrip line is included in the input matrix **X**, the wave propagation along an impedance matched transmission line is represented by matrix **T**, and the output transition from microstrip line to probe tip is included in an output matrix **Y**. The matrix **X**, **T** and **Y** are all in cascading form. When multiplying the matrix $\mathbf{M_1}$ with the inverse of the matrix $\mathbf{M_2}$, the result is an eigenvalue equation

$$[M_{12}] \bullet [X] = [X] \bullet [T_{12}] \quad (6)$$

$$[M_{12}]=[M_1]\cdot[M_2]^{-1} \quad (7)$$

$$[T_{12}]=[T_1]\cdot[T_2]^{-1} \quad (8)$$

The diagonal elements of the matrix $\mathbf{T_{12}}$ are the eigenvalues of $\mathbf{M_{12}}$, and the columns of **X** are the eigenvectors of $\mathbf{M_{12}}$. Using the fact that the trace is invariant under cyclic permutation in matrix calculation, the propagation constant can be derived from the relation

$$Tr([M_1]\cdot[M_2]^{-1}) = Tr([T_1]\cdot[T_2]^{-1}) = 2\cosh(\gamma\Delta l) \quad (9)$$

where Δl is the length difference between the two transmission lines.

Once the propagation constant γ is determined, we can separate it into real part and imaginary part. The real part α is called attenuation constant, which reflects the loss of propagation; the imaginary part β is called phase constant, which represents the speed of transmission. When the electromagnetic wave propagates in a microstrip transmission line, most of energy is contained in the dielectric substrate, but a part of the energy exists in the ambient air. So the complex effective permittivity ε_{eff} and permeability μ_{eff} of transmission line takes this into account. Therefore, the propagation constant can be defined as a function of ε_{eff} and μ_{eff} as given in [13]

$$\gamma = \alpha + j\beta = j\frac{\omega}{c}\sqrt{\mu_{eff}\varepsilon_{eff}} \quad (10)$$

where c is the speed of light, ω is the angular frequency. Combining Eq. 10 and Eq. 3, we can deduce the expression of ε_{eff} and μ_{eff} in terms of the lumped elements

$$\mu_{eff} = \frac{R+j\omega L}{j\omega L_{ext}} \quad (11)$$

$$\varepsilon_{eff} = \frac{G+j\omega C}{j\omega C_a} = \varepsilon'_{eff} - j\varepsilon''_{eff} \quad (12)$$

Then in order to separate ε'_{eff} and ε''_{eff}, we can combine Eq.10-12 and get

$$\beta^2 - \alpha^2 + j2\alpha\beta = \frac{\omega^2}{c^2}\left(1 + \frac{L_{int}}{L_{ext}}\right)\varepsilon'_{eff} + j\frac{\omega^2}{c^2}\left(\frac{L}{L_{ext}}\frac{G}{\omega C_a} + \frac{\varepsilon'_{eff}\,R}{\omega L_{ext}}\right) \quad (13)$$

The first step is to find the relative permittivity ε_r. By taking the real part of Eq. 13, we can calculate the relative effective permittivity ε'_{eff} as,

$$\varepsilon'_{eff} = \frac{c^2}{\omega^2}\frac{\beta^2 - \alpha^2}{\left(1 + \frac{L_{int}}{L_{ext}}\right)} \quad (14)$$

Since both the L_{int} and L_{ext} are already known from the simulations, ε'_{eff} then can be determined. There is a one-to-one correspondence between ε'_{eff} and the relative permittivity ε_r. If the microstrip line width w is larger than dielectric thickness h, which is true for our test structures, ε_r can be found through the relation given in [8],

$$\varepsilon'_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{12h}{w}\right)^{-1/2} - 0.217(\varepsilon_r - 1)\frac{t}{\sqrt{wh}} \quad (15)$$

The next step is to calculate the dielectric loss tangent $\tan\delta$. The imaginary part of Eq. 13 can be written as

$$2\alpha\beta = \frac{\omega^2}{c^2}\left(\frac{L}{L_{ext}}\frac{G}{\omega C_a} + \frac{\varepsilon'_{eff}R}{\omega L_{ext}}\right) \quad (16)$$

As the wave energy propagates in a microstrip line, the attenuation caused by dielectric loss is modeled by the shunt conductance G. On the other hand, the energy stored in dielectric material results in shunt capacitance C, which can be further expressed by substrate permittivity and air-filled capacitance C_a. According to [11, p.155], the relation between conductance G and C_a is

$$\frac{G}{\omega C_a} = \frac{(\varepsilon'_{eff} - 1)\varepsilon_r}{\varepsilon_r - 1}\tan\delta \quad (17)$$

and substitute it in Eq. 16, one has

$$\alpha = \frac{\omega^2}{2\beta c^2}\frac{L}{L_{ext}}\frac{(\varepsilon'_{eff} - 1)\varepsilon_r}{\varepsilon_r - 1}\tan\delta + \frac{\omega^2}{2\beta c^2}\frac{\varepsilon'_{eff}R}{\omega L_{ext}} \quad (18)$$

The first term on the right hand of the Eq. 18 is related to the dielectric loss, and the second term represents the conductor loss. It is now possible to calculate the value of the loss tangent, since all the other parameters in Eq.18 are already known. The solid lines in Fig. 4.4 and 4.5 show the extracted high frequency relative permittivity and loss tangent. The result of a simulation with the extracted permittivity should guarantee a good agreement with the experimental result.

The data below 4.2 GHz is suppressed, because strong slow wave effect is dominant for this frequency range. The slow wave effect, which is caused by small ratio of the metal thickness to the skin depth, results in large variation in extracted permittivity [7]. At 4.2 GHz, the metal thickness is about equal to the skin depth. We can assume that result is accurate beyond this threshold.

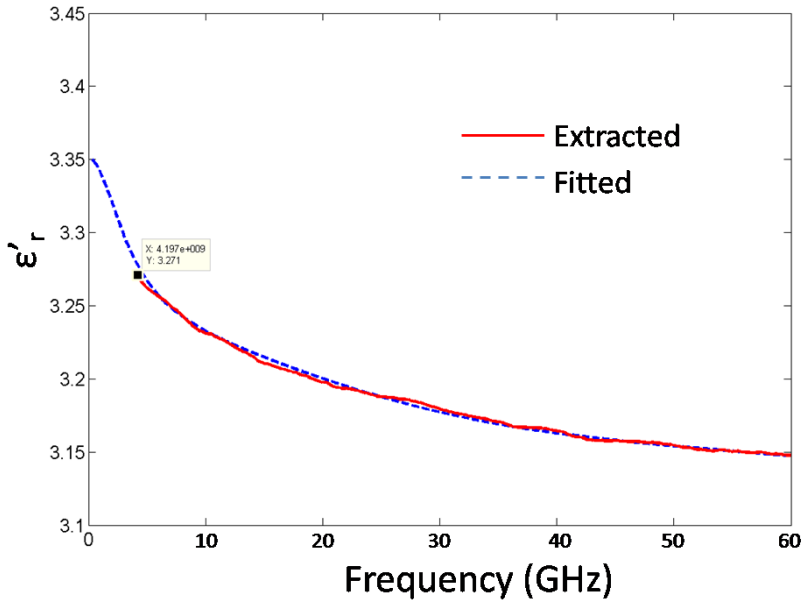

Figure4.4 *The extracted relative permittivity of polyimide HD-4110 from measurements of TFMSL and the corresponding dielectric model fitted curve. The dimensions of used TFMSL are w = 38.3, t = 1, h = 14.2 (all in micrometers) and* $\sigma = 5.8\times10^{7}$ *S/m.*

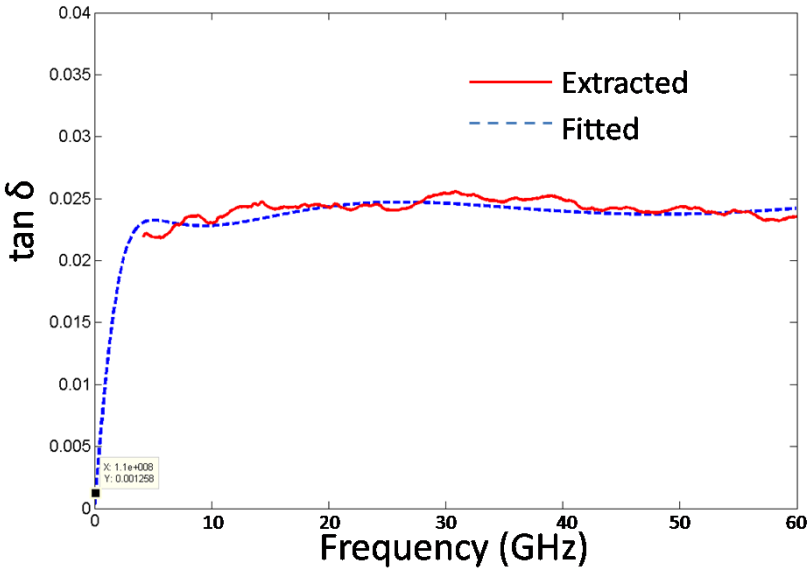

Figure4.5 *The extracted loss tangent tan δ of polyimide HD-4110 from measurements of TFMSLs and the corresponding dielectric model fitted curve. The dimensions of used TFMSL are w = 38.3, t = 1, h = 14.2 (all in micrometers) and σ = 5.8×10^7 S/m.*

4.5 Dielectric Model Fitting

A rational dielectric model is given in [9, Eq.2] which consists of a discrete sum of dipole moments,

$$\varepsilon(s) = \varepsilon_{\infty} + \sum_{n=1}^{N} \frac{c_n}{s - a_n} \tag{19}$$

where ε_∞ denotes the infinite frequency limit, s is equal to $j2\pi f$, a_n are the poles and c_n are the residues. For the sake of stability, the real part of a_n must be negative. This dielectric model is employed to fit the extracted permittivity using Matlab rational fitting function. The fitted data set automatically satisfies the Kramers-Kronig relation, which ensures the causality constraints. The number of poles in the dielectric model should be kept small while it still maintains a best fit. For the concerned bandwidth in this work, four-pole equation is sufficient to express the dielectric function. It should be mentioned that when the fitting is required for a broader

bandwidth, the number of dipoles may need to be increased accordingly and the rational fitting technique can be used to determine the multi-pole model parameters [14]. The result of the fitting is plotted in Fig. 4.4 and 4.5 by the dash lines.

It can be seen that the extracted permittivity can be well reproduced by the model. Moreover, the fitted model can extrapolate the permittivity value below 4.2 GHz. At the lowest frequency of 10 MHz, the model predicted relative permittivity is 3.35, which is very close to 3.36 provided by the manufacture. The same thing is also found for the loss tangent. The fitted loss tangent at 10 and 110 MHz are 1×10^{-4} and 1.3×10^{-3} respectively. And the loss tangent provided by the manufacture is 1×10^{-3} at 10 MHz, which is right in between the predicted values. This is a strong indication that the method we proposed to extract material property is valid.

As an evaluation of the accuracy, another pair of TFMSLs are produced using the same thin film technology. But the new TFMSLs have a different thickness of 7.1 μm and a different line width of 25.5 μm. A simulation of the new TFMSL model is performed with the fitted data set to calculate the propagation constant. The simulated propagation constant is compared to the one obtained from measurements. Fig. 4.6 shows that a good agreement is achieved between the measurement and HFSS simulation.

4.6 Accuracy Analysis

Although the above technique shows promising results, some uncontrolled factors can influence the accuracy of the method. The fitted data used in the final simulation relies on the accuracy of the raw data, which is originally calculated from simulations. Therefore, some errors in the simulation model may cause a deviation of results from true values. The errors mainly come from the variation of dimensions and the uncertainty in conductivity. But these factors can be minimized by measurements at multiple sites along the TLines and take their average value. Furthermore, the surface roughness introduces a higher conductor losses, which should be accounted for in assessing the dielectric loss tangent. It is proved that HFSS can precisely predict the TLine performance incorporating the effect of surface roughness [14]. So if the surface roughness is large compared with the skin depth, one can include it in the simulation model in the course of distributed elements calculation. In this case the effect due to surface roughness is compensated.

And it means that the procedure described in this chapter is also applicable for high roughness substrate.

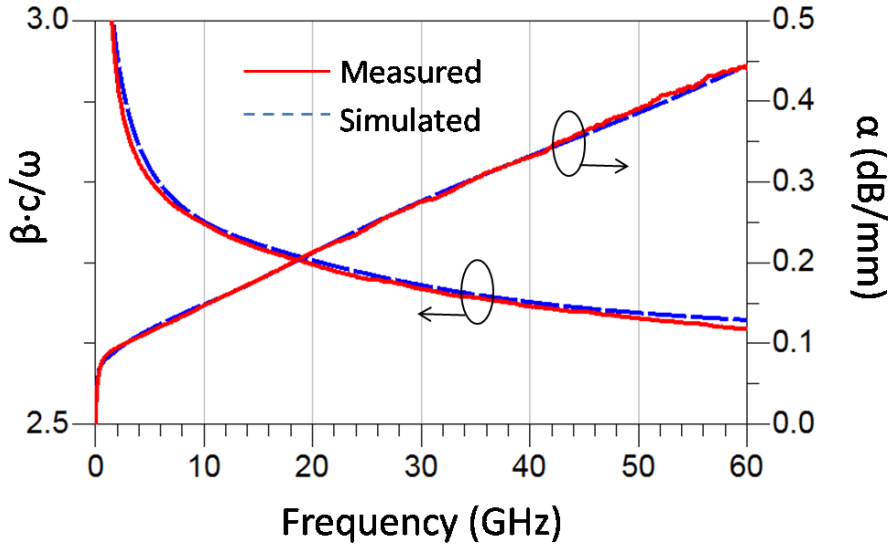

Figure4.6 *Comparison of measured and simulated propagation constant for TFMSL with dimension of w = 25.5, t = 1, h = 7.1 (all in micrometers) and σ = 5.8×10^7 S/m.*

4.7 Conclusion

The proposed method can be used to determine complex permittivity of dielectric materials up to mm-wave frequency. Knowing the geometry of the microstrip lines, distributed elements in the equivalent circuit model are obtained by merely two simulations. Based on the obtained distributed elements and propagation constant, the dielectric loss is very simply separated from the measured total loss. The extracted permittivity is well fitted by a rational dielectric model and the fitted solution satisfies the causality constraints. The result of simulation with the fitted data shows good agreement with the experimental result. Although the accuracy of this method is limited by some uncertainty in physical dimensions and conductivity, it is possible to account for and eliminate the influence of surface roughness.

References

[1] R. H. Voelker, G.-T. L. G.-T. Lei, G.-W. P. G.-W. Pan, and B. K. Gilbert, "Determination of complex permittivity of low-loss dielectrics," IEEE Transactions on Microwave Theory And Techniques, vol. 45, no. 10, pp. 1955–1960, 1997.

[2] A. Kaczkowski and A. Milewski, "High-Accuracy Wide-Range Measurement Method for Determination of Complex Permittivity in Reentrant Cavity: Part A --- Theoretical Analysis of the Method," IEEE Transactions on Microwave Theory and Techniques, vol. 28, no. 3, pp. 225–228, Mar. 1980.

[3] J. R. Bray and L. Roy, "Microwave characterization of a microstrip line using a two-port ring resonator with an improved lumped-element model," IEEE Transactions on Microwave Theory and Techniques, vol. 51, no. 5, pp. 1540–1547, 2003.

[4] M. Cauwe and J. De Baets, "Broadband Material Parameter Characterization for Practical High-Speed Interconnects on Printed Circuit Board," IEEE Transactions on Advanced Packaging, vol. 31, no. 3, pp. 649–656, Aug. 2008.

[5] M. D. Janezic, D. F. Williams, V. Blaschke, and A. Karamcheti, "Permittivity characterization of low-k thin films from transmission-line measurements," IEEE Transactions on Microwave Theory and Techniques, vol. 51, no. 1, pp. 132–136, Jan. 2003.

[6] M. D. Janezic and J. A. Jargon, "Complex permittivity determination from propagation constant measurements," IEEE Microwave and Guided Wave Letters, vol. 9, no. 2, pp. 76–78, 1999.

[7] G. E. Ponchak and A. N. Downey, "Characterization of thin film microstrip lines on polyimide," IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B, vol. 21, no. 2, pp. 171–176, May 1998.

[8] Z. Zhen and K. L. Melde, A Comprehensive Technique to Determine the Broadband Physically Consistent Material Characteristics of Microstrip Lines, IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 1. 2010, pp. 185–194.

[9] T. Demeester, M. Cauwe, and D. De Zutter, "Frequency-Dependent Substrate Characterization via an Iterative Pole Search Algorithm," IEEE Microwave and Wireless Components Letters, vol. 21, no. 4, pp. 173–175, Apr. 2011.

[10] R. B. Marks, "A multiline method of network analyzer calibration," IEEE Transactions on Microwave Theory and Techniques, vol. 39, no. 7, pp. 1205–1215, Jul. 1991

[11] R. E. Collin, Foundations for Microwave Engineering. Wiley-IEEE Press, 2000.

[12] A. R. Djordjevic and T. K. Sarkar, "Closed-form formulas for frequency-dependent resistance and inductance per unit length of microstrip and strip transmission lines," IEEE Transactions on Microwave Theory and Techniques, vol. 42, no. 2, pp. 241–248, 1994.

[13] R. B. Marks, D. F. Williams, and M. B. Steer, "Accurate experimental characterization of interconnects: a discussion of 'Experimental electrical characterization of interconnects and discontinuities in high-speed digital systems'," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. 15, no. 4, pp. 601–604, 1992.

[14] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting," IEEE Transactions on Power Delivery, vol. 14, no. 3, pp. 1052–1061, 1999.

[15] X. Chen, EM Modeling of Microstrip Conductor Losses Including Surface Roughness Effect, IEEE Microwave and Wireless Components Letters, vol. 17, no. 2. 2007, pp. 94–96.

.

CHAPTER 5

High Frequency Properties of UTCP Interconnection

The UTCP technology with fine pitch capability is a potential candidate for high frequency chip packaging. This chapter explores the high frequency properties of interconnections to the UTCP embedded chips. Thinned silicon chips, on which coplanar waveguide (CPW) transmission lines are patterned, were embedded in polyimide as test chips using the Flat-UTCP process sequence. Two types of structures were fabricated for electrical connection between the test chip and its package. One structure is CPW to CPW connection, and the other one is microstrip line (MSL) to CPW connection. The transmission and reflection coefficients were derived up to 60 GHz for the two types of connections. Pros and cons of the two structures are discussed, which leads to basic design principles for high frequency application.

5.1 Introduction

The scaling down of CMOS circuits to 45 nm and below opens the possibility for realizing electronic systems operating up to 60 GHz [1], [2]. In the meanwhile, since the bond pads consume an increasing part of chip

area, new technology tends to reduce the bond pad area and pitch. Along with the higher operating frequency and smaller pitch, the package of RF chips appears to be a significant challenge, which can not be easily overcome by traditional packaging methods, such as wire bonding or flip chip technologies [3], [4].Although the wire bonding technique can achieve a fairly small pitch connection, it also introduces excessive parasitic inductance, which can not be well compensated [5], [6]. The flip chip connection, on the other hand, is more suitable for high frequency application. A great deal of study has been done on flip chip bonding with CPW transmission line in the form of CPW to CPW transition[7], [8], [9], [10]. Good electrical performance has been shown for the flip chip technologies compared with a conventional wire bonding technique and its capability for high frequency application was verified. However, due to the limitation of the circuit substrate and bonding accuracy, the pitch of bond pad for flip chip technique is generally larger than 150 μm [11]. If the chip wants to be directly bonded on main board without an interposer, the required pitch can be as large as 200 μm or even more.

In order to overcome the current limitation of conventional chip packaging, an increasing number of research focuses on developing direct embedding techniques and fan-out wafer level packaging (WLP), such as CiP and RCP technologies mentioned before. The UTCP technology developed at IMEC-CMST makes use of embedded thinned chip. A layer of organic resin based membrane is coated on top of the embedded chip surface. The interconnection to the chip is realized by forming micro-via through the coated resin film to chip bond pads. The micro-via based connection is able to meet the fine pitch requirement for the chip connection. Moreover, a fan out design on the package level can bridge the pitch mismatch between the chip and coarse substrate. So the UTCP technology can fall into the scope of fan-out WLP and also can take advantage of direct embedding techniques.

Excellent mechanical and thermal reliability has already been demonstrated for the UTCP package as described in previous chapters. Although some research indicates that the micro-via based connection result in the lowest electrical parasitics and is superior over the traditional approaches, there is still very little work to characterize the embedded chip interconnection for real application in millimeter wave frequencies [12]. The work in this chapter explores the high frequency properties of interconnections to the UTCP embedded chips up to 60 GHz. Two types of structures were fabricated for electrical connection between the test chip and its package. One structure is CPW to CPW connection and the other one is microstrip

line (MSL) to CPW connection. By using Thru–Reflection-Line (TRL) algorithm, the reflection and transmission characteristics of the two proposed connections are derived and compared with each other [13].

5.2 Test Die and Design

The PTCE chips from IMEC are still used as test dies for the high frequency characterization. Besides the daisy chain test structure, the PTCE chip also integrates multiple CPW transmission lines and reflection structures, which can be used for TRL de-embedding of UTCP transition characteristics and on-chip CPW transmission behavior. The layout of the chip is present in Fig. 5.1.

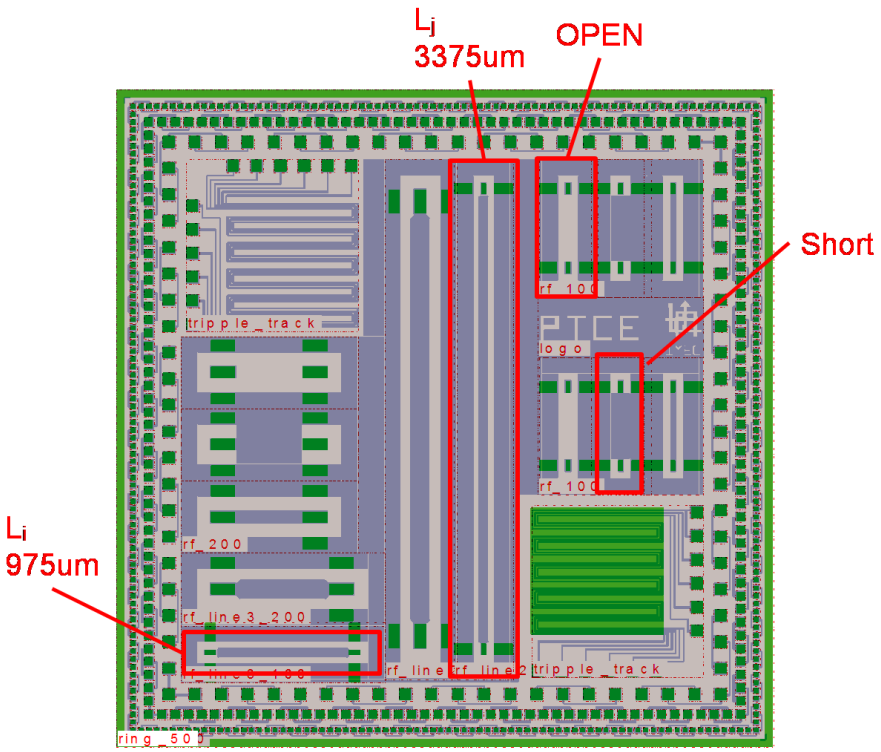

Figure 5.1 *Layout of the PTCE chip.*

Two CPW lines with different length are used. The long line L_j has a length of 3375 μm and the short line L_i has 975 μm long. Except for the length difference, the other dimensions of the CPW lines are the same, which are designed for a target characteristic impedance of 50 Ω. The gap is 37.5 μm wide and the central width is 75 μm. The pads to connect to the CPW line are Ground-Signal-Ground (GSG) pads with a minimum pitch of 100 μm. Since the ground pads are designed as wide as 145 μm, RF probes with pitch larger than 100 μm can also be placed on the pads for direct measurements.

The reflection structures include open stubs and short stubs. Either of the reflection structure can be used for TRL de-embedding. In this work, we only use the open stubs. As required by the TRL de-embedding algorithm, the pads of the reflection are designed exactly the same as that of the CPW line.

All the metal films on the chip are realized in 0.8 μm aluminum. The silicon chips are thinned down to 30 μm by grinding and attached on polyimide coated glass carrier which has 0.7 mm thickness. Since the CPW line is originally designed for 6 inch wafer of 675 μm thick, the characteristic impedance of CPW may have been changed after thinning. Detuning is another effect that influences the value of CPW characteristic impedance. When doing the measurement, the glass carrier is directly placed on probe stage chuck. Since the glass thickness is not large, the metal chuck acts as a ground plane and the on-chip CPW line becomes conductor backed CPW, whose characteristic impedance is quite different from the target value. The effect of detuning is more pronounced at lower frequencies. A full wave simulation is employed to estimate the actual CPW characteristic impedance. The model for the simulation is shown in Fig 5.2 and its result is presented in Fig. 5.3. It can be seen that the characteristic impedance first drops rapidly at lower frequency and then becomes relatively stable at 50 Ω after 5 GHz. It means that at higher frequency the influence from the chip thinning and detuning is almost negligible. In the following analysis, we mainly consider the bandwidth above 10 GHz, where the performance is only caused by transition structures.

The PTCE chip is embedded in polyimide thin films using the Flat-UTCP process sequence as described in Chapter 3. First the central polyimide is coated to compensate the chip thickness. Then the aluminum bond pads are Ni/Au bumped for good electrical contact. Multilayer structures are built up on the embedded chip for high frequency connection.

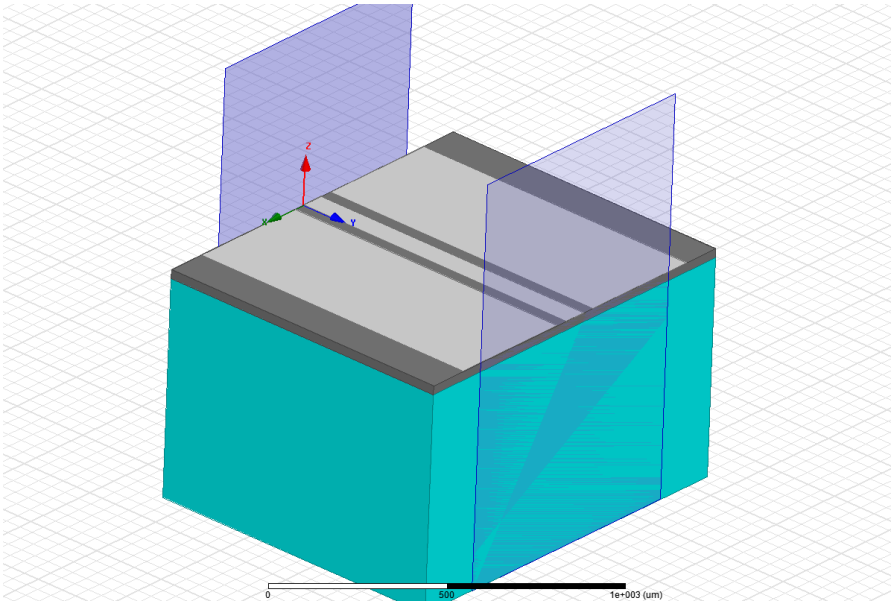

Figure 5.2 *Schematic model of on-chip CPW transmission line.*

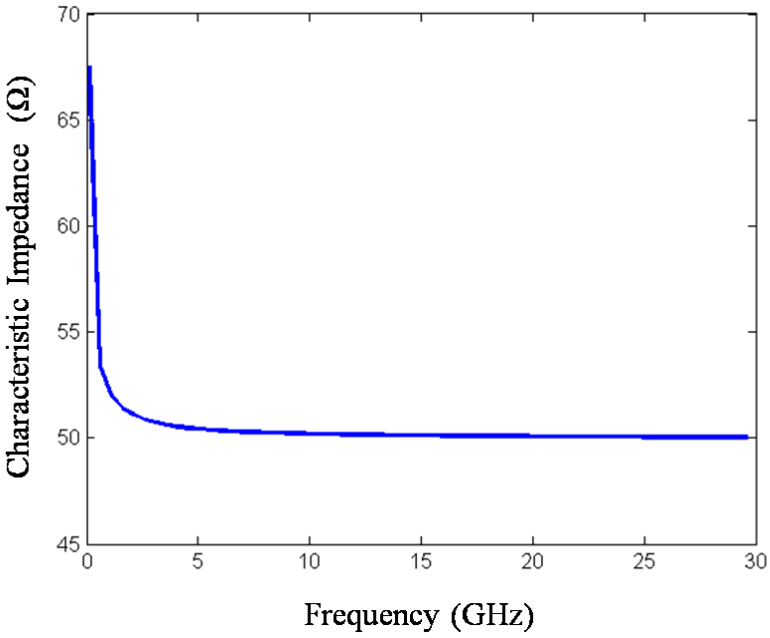

Figure 5.3 Calculated *characteristic impedance of of on-chip CPW transmission line.*

Two types of high frequency transition structures are fabricated for the embedded PTCE chip. The first type is CPW to CPW transition, as shown in Fig. 5.4. The ground and signal trace of CPW transmission line on the package is directly connected to the chip bond pads by microvia technology through the top polyimide film. The size of microvias is about 60 μm in diameter with a pitch of 100 μm. The CPW traces on package completely cover the microvias and can build up a route for signal transition outwards the chip area, which is also known as a fan-out design. Since the width of the CPW ground trace can be much larger than the chip bond pads, the pitch requirement for package level connection is not as stringent as the chip level requirement, which solves the pitch mismatch problem. The RF probes can be directly place on the CPW traces for measurement. As indicated in the figure, the position of the probe is very close to the microvias (about 150 μm), because we want to extract the performance of the transition itself without the transition of the CPW line. For such a short length, the CPW on the package acts as a GSG probe pads. So in this case, the line width and space of the CPW line is not very critical. In between the CPW on package and chip, the thickness of top polyimide is designed to be 15 μm after curing.

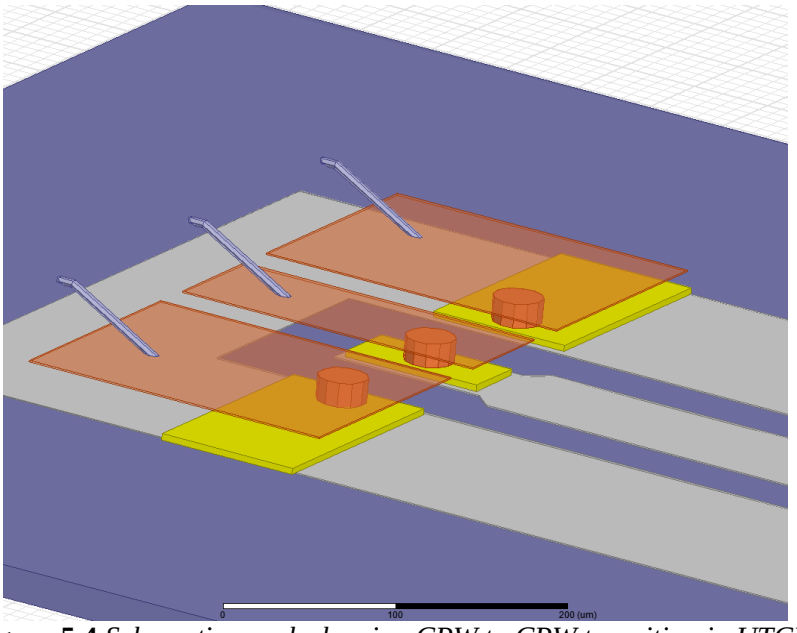

Figure 5.4 *Schematic graph showing CPW to CPW transition in UTCP.*

The CPW transition has a simple configuration which is easy to fabricate. But the CPW line is very sensitive to the underling silicon chip, especially

for the UTCP with thin top dielectric film. Moreover, when the CPW crosses the chip edge, its transmission property should change due to difference of the underlying material property. All these issues make difficulties in designing an impedance matching network by CPW transmission. To avoid these problems, another transition structure is proposed, which is denoted as MSL to CPW transition.

Compared with the CPW to CPW transition, the MSL transition is more complex and needs a build-up of two metallization layers. A schematic drawing of the structure is presented in Fig. 5.5. The first layer is deposited as the ground plane of the MSL. The ground plane is connected to the chip ground bond pads the same way as CPW transition. But unlike the finite width CPW ground, the microstrip ground is a blank plane that shields the underlying chip surface. In this case, the characteristic impedance of the MSL should be consistent and independent on the chip metallization even around the chip edge area. The shielding ground plane provides simplicity for matching network design, but it may affect the chip functionality. When the bond pads are close to the center of the chip, the ground plane has to cover most of the chip surface to build the MSL transmission. So it behaves like an extra ground plane for the back end of line (BEOL) structures and may disturb the performance of the chip. The distance between the ground and the chip is made the same as the CPW to CPW connection of 15 μm. The microstrip signal trace is realized in the second metal layer on top of the ground plane. And it is connected to the central chip bond pads through two layers of polyimide. So the central microvia is higher than the microvia on the ground pads. The microstrip signal trace can be separated into three parts. The first part is a square pad of 80 μm × 80 μm, which captures the central microvia. Then the capture pad gradually narrow down to next part, the strip line, which is made for a characteristic impedance of 50 Ω. The value of the microstrip characteristic impedance is important, as will be explained in the section. In this work, we design a strip line width of 23 μm which implies 10 μm thickness of the polyimide layer in between the strip and ground plane. Since we can not directly do measurement on microstrip line, GSG pads, as the third part, are made in connection with strip line for the final RF probe placement.

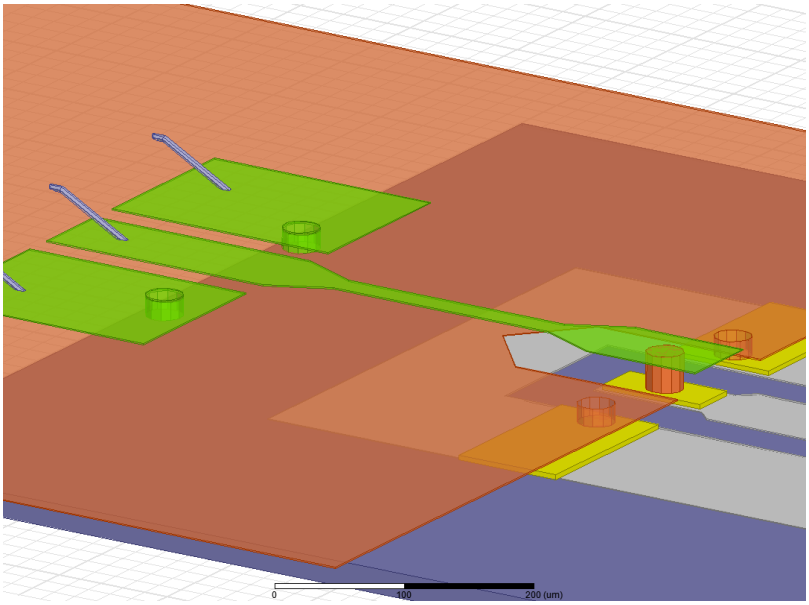

Figure 5.5 *Schematic graph showing MSL to CPW transition in UTCP.*

5.3 Fabrication Process

The fabrication of the high frequency interconnections is quite similar to the conventional Flat-UTCP process sequence. But there are some difficulties that need to be taken into account during the processing.

5.3.1 Fine Line Patterning

The first difficulty is the patterning of circuit trace. For thin film structure, high resolution pattern definition of metallization is very critical. Because the trace feature size is very small, a little variation even in micrometer range from original design can result in quite different performance. Copper is a material commonly used in IC packaging and RF circuitry, because copper can be easily deposited by evaporation or sputtering and the conductivity of it is much higher than all the other metal material except silver. Table 5.1 lists an overview of properties of some common thin film metals. However, pattern of copper film in high accuracy is not an easy task. In IC packaging processing, there are mainly three ways for patterning materials, which are known as dry etching, wet etching and semi-additive

plating. Dry etching process exposes the unwanted material area to bombardment of ions, which remove the exposed material by producing reactant compound gas. It is a method commonly applied in semiconductor manufacturing for etching dielectric material and thin film metal. The dry etching method can achieve high resolution normally within 1 μm. But since most of copper compound is not in vapor phase, dry etching of copper still at research stage and is not quite reliable. So it is not a good option for our work.

Metal Material	Symbol	Electrical cond. ($\times 10^7$ S/m)	CTE ppm/°C	Termal cond. W/m.K
silver	Ag	6.1	18.0	429
copper	Cu	5.8	19.7	418
gold	Au	4.1	14.2	297
aluminum	Al	3.7	23.0	240
titanium	Ti	1.82	8.9	22
tungsten	W	1.82	4.5	200
nichel	Ni	1.45	13.3	92
iron	Fe	1.03	11.8	80.4

Table 5.1 *Overview of material properties of typical thin film metals* [14].

Semi-additive plating, also known as pattern plating, is another alternative method to produce fine line and space interconnects, which is widely used in packaging manufacture. The basic process sequence of semi-additive plating of copper is shown in Fig. 5.6. First, titanium (or titanium tungsten) and copper metal were deposited in situ by evaporation or sputtering on rigid substrate with a total thickness of about a few hundreds of nm to form a very thin seed layer for the following plating. Ti (or TiW) is used as an adhesion layer. Next, photoresist layer was spin-coated on the seed layer and patterned by photo lithography. The portion of the photoresist is developed from the area, where the final copper pattern is intent to create. Next the sample is electroplated in the bath to the final desired thickness. Since the resist shields the seed layer from bath solution, only the open area will be plated. After that, the resist is striped and the seed layer is flash etched away.

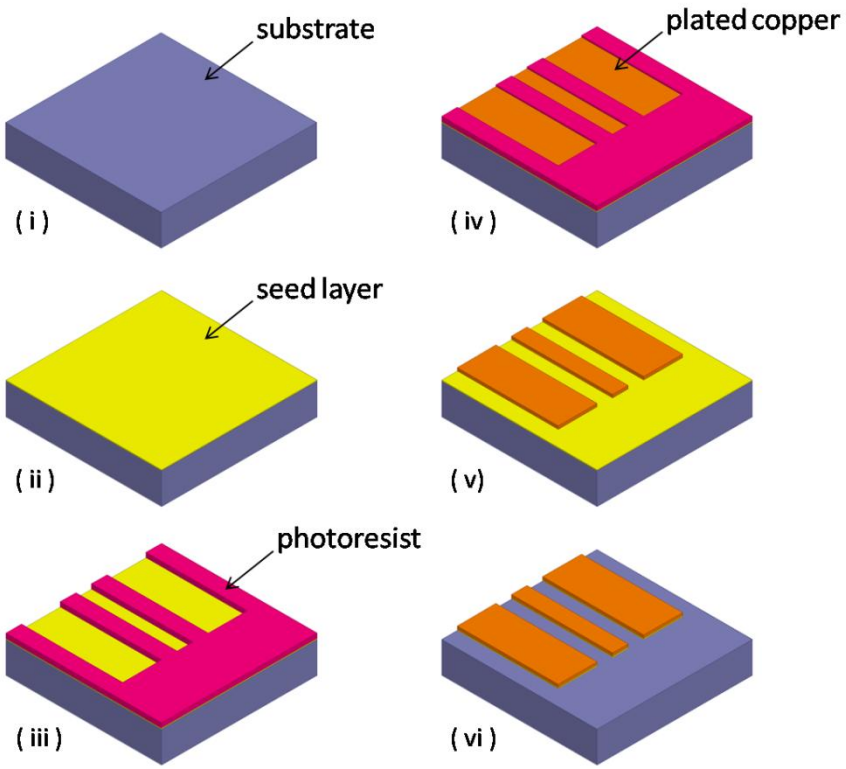

Figure 5.6 *Process sequence of semi-additive plating.*

In theory, the resolution of semi-additive plating is defined by the resolution of photo lithography process and the resolution of the mask, which is normally within 1 μm. But in practical, there are some concerns needs to be take account. Because the copper plating bath consists of high percentage of sulfuric acid, the selected resist should be able to withstand and have good adhesion on the seed layer. Otherwise, undesired plating could start under the photoresist, i.e. under plating, and deteriorate the final resolution. In addition, the plating uniformity and surface roughness are very important issues and difficult to achieve. To obtain smooth surface and high uniformity, we need to optimize the plating parameters, such as current density and plating time. At the time of this PhD research, the semi-additive plating is not well prepared in our facility and it would cost a long time to build up such technology.

Based on the above considerations, subtractive wet etching is the only choice to continue our work. Wet etching uses corrosive etchant to remove part of the copper sheet, while the final copper pattern is preserved by photoresist. In order to obtain smooth surface roughness and consistent final line width, all metallization layers in the device fabrication are restrict to 1 μm thick sputtered copper sheet. Cupric chloride (CuCl2) and ferric chloride (FeCl3) based etchants are the two most used candidates for copper wet etching. Since the etching rate of CuCl2is slower and better for control, it is applied in this work. The etching of sample is carried out in a spray etching machine. The concentrate of the etchant is optimized for 18 μm thick rolled copper on normal PCB substrate for the minimum under-etching. The concentration consists of 0.2 mol of hydrochloric acid and 2.5 mol of CuCl2. At work temperature of 30 °C, etching of 18 μm thick rolled copper needs 7 passes. But for the thin sputtered copper sheet, it is found that even one pass is enough and can have generate large under-etching around 3 μm per side on average (± 1.5 μm max deviation). Fig. 5.7 is a graph of substrate after spray etching, showing severe under-etching of copper sheet. The value of under-etching is taken accounted during the design of RF transition structure.

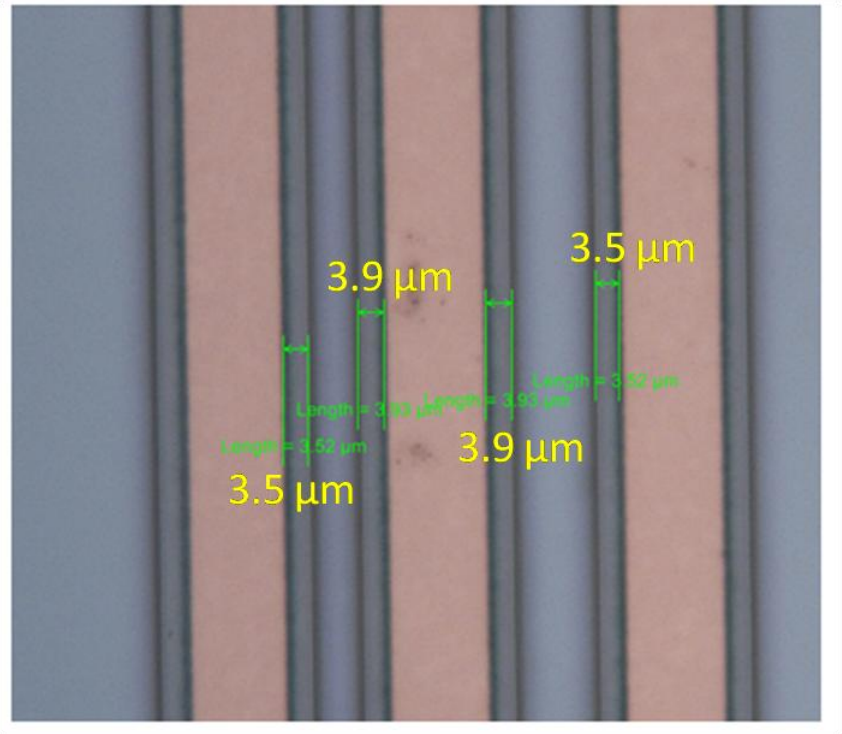

Figure 5.7 *Graph of thin film copper after spray etching.*

5.3.2 Microvia formation for MSL

The above section describes the solution for making fine feature pattern of metallization, which is the first problem we encountered in the fabrication. Microvia formation is another problem found during making the MSL to CPW transition. The MSL to CPW transition is comprised of two layer of buildup, and the signal trace is required to connect through two dielectric layers to the bottom chip signal bond pad. The microvia generation can be achieved by laser drilling or photo lithography. Photosensitive polyimide is selected as basic dielectric material, and the lithography parameter have already been optimized in the Flat-UTCP process. So it's a simple choice to continue working with the photovia technique. For making the two-layer build up, the first layer of polyimide is spin-coated and developed to generate microvias to all chip bonds pads. Then the MSL ground metallization is deposited on the whole surface, and patterned by wet etching. In this step, the metal on the central chip bond pads will be etched away, leaving only the Ni/Au bumping. Next, the second polyimide is coated. To make connection for the MSL signal trace, microvias are made on top of the microvias in the first layer, i.e via on via. In the end, signal trace is deposited. Fig. 5.8 shows the realized structure of both CPW to CPW transition (a) and MSL to CPW transition (b). In the graph of Fig. 5.8, the RF probe launch position is indicated by the plane P-P' and the transition structures are marked as area from A-A' to B-B'. For the CPW transition, the position of probe coincides with the starting reference plane of transition area A-A'. The subscript number indicates the number of port.

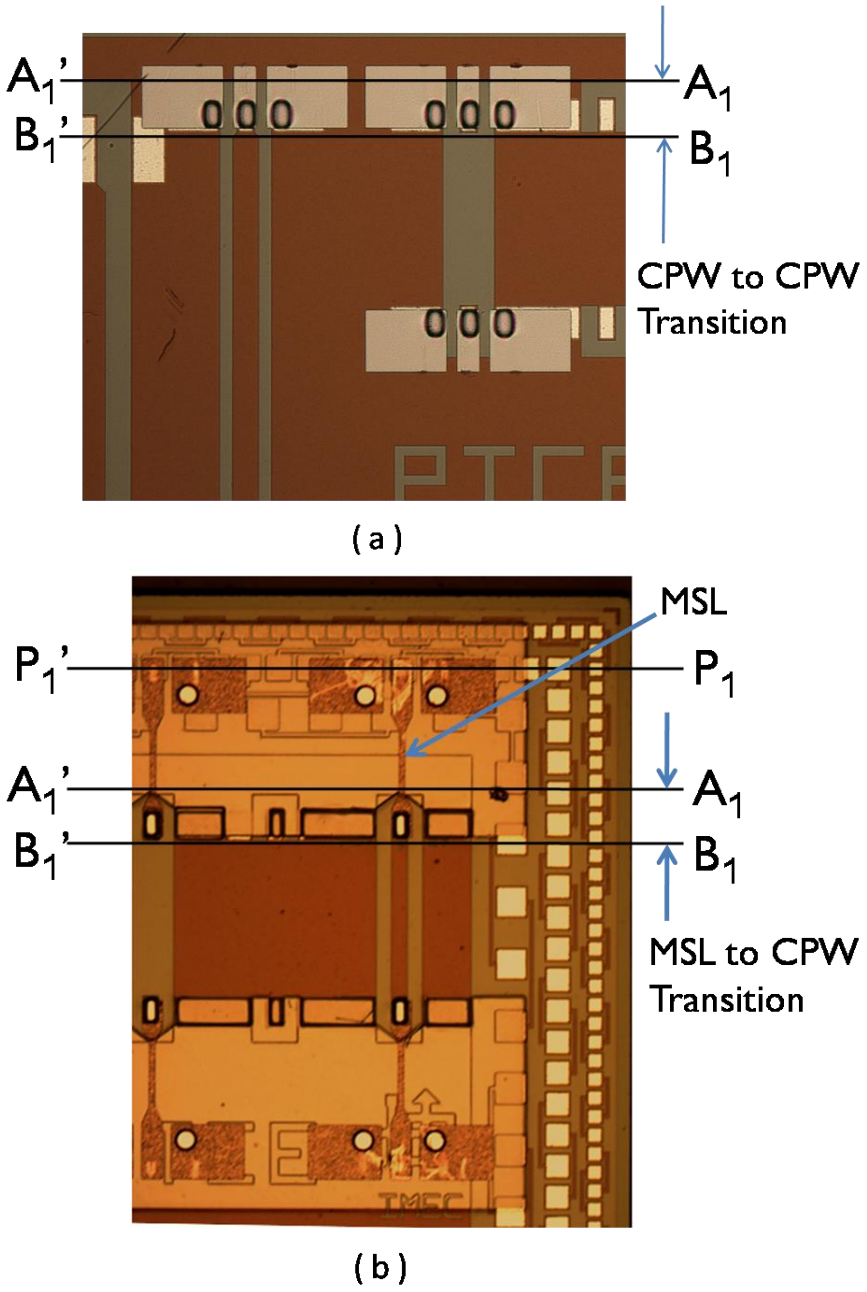

Figure 5.8 *Graph of realized RF transition structures in UTCP package: (a) CPW to CPW transition, (b)MSL to CPW transition.*

5.4 High Frequency Analysis

In this section we will characterize the high frequency properties of the above fabricated UTCP interconnections. The two kinds of transition are compared with each other based on extracted transmission and reflection parameters.

The samples were measured up to 60 GHz by a vector network analyzer (VNA) AGT E8361C (from Agilent Technologies). A pair of GSG probes with pitch of 150 μm is connected to the ports of the VNA at one end, and placed on the probe pads of structures on the other end. Before the real measurement, probe tip calibration was first carried out by following Line-Reflection-Match (LRM) calibration procedure. After the probe tip calibration, the reference impedances of both ports change to the value of resistors integrated in the match element, which is equal to 50 Ω. Then, S parameters were measured for each transition structure and also for Ni/Au bumped bare PTCE chip.

For a measured transmission line i, the obtained two port S matrix can be converted to a cascade matrix M_i, which can be further divided into sub-matrixes. Fig. 5.9 shows the diagram of the measured cascade matrix M_i for model extraction. The reference planes indicated in the diagram of Fig. 5.9are consistence with the reference planes marked in Fig. 5.8.

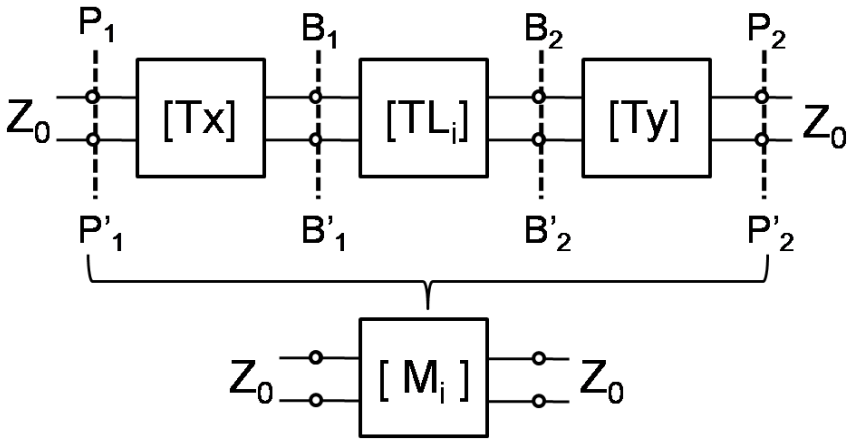

Figure 5.9 *Diagram of the S parameters for model extraction.*

In the diagram, Zo represents 50 Ω reference impedance connectedto the ports. The measured matrix M_i is composed of three cascade-parameter matrices Tx, TL_i and Ty. The TL_i matrix represents the transmission characteristic of the on-chip CPW line. And the Tx and Ty are denoted as the matrix for two port network describing the behavior between the probe and the start of the CPW line. Since our measurement is done after a pre-calibration, the matrix of Tx and Ty not only includes the influence of probe contacts, transition structure, but also the impedance transformation from reference impedance to the characteristic impedance of the line. Actually, due to the symmetry of the system, in theory Ty at port 2 is close to a symmetrical matrix of Tx at port 1. However, because the structures at both sides may have some differences introduced by misalignment or calibration uncertainty, it is not a very safe solution to directly apply the symmetrical property in the analysis. From the diagram, we can have the relation of:

$$[M_i] = [Tx] \bullet [TL_i] \bullet [Ty] \tag{5.1}$$

For a normal matched transmission line, its cascade-parameter matrix can be written as:

$$[TL_i] = \begin{bmatrix} e^{-\gamma l_i} & 0 \\ 0 & e^{\gamma l_i} \end{bmatrix} \tag{5.2}$$

where γ is the propagation constant of the transmission line, and l_i is its corresponding length[15]. By combing the measured matrix of both short line (L_i) and long line (L_j) on the chip, we can reduce the number of unknown parameters and extract the matrix of Eq. 5.2[16].

$$[M_{ij}] \bullet [Tx] = [Tx] \bullet [TL_{ij}] \tag{5.3}$$

$$[M_{ij}] = [M_j] \bullet [M_i]^{-1} \tag{5.4}$$

$$[TL_{ij}] = [TL_j] \bullet [TL_i]^{-1} \tag{5.5}$$

Because the impedance transformation is incorporated in the error box of Tx and Ty, the matched line expression of Eq. 5.2 can be substituted into Eq. 5.5. Then, we can further get an eigenvalue problem from Eq. 5.3. The diagonal elements of matrix TL_{ij} are the eigenvalues of M_{ij}, and the columns of Tx are the eigenvectors of M_{ij}. We can derive that the diagonal elements of TL_{ij} are determined by the eigenvalues of M_{ij}. Then by using a pair of line

with different line length, the propagation constant γ can be determined. This approach is similar to the standard TRL algorithm, but the elements of error boxes of Tx and Ty are not needed to be known to extract the transmission line propagation constant. The extracted line cascade-parameter matrix can be converted to S-parameter matrix. We first compare the transmission coefficient (S12) of the long line L_j in extracted S matrix for Ni/Au bumped bare die and UTCP embedded chips, which are shown in Fig. 5.9. The blue curve represents value extracted from UTCP embedded chip with MSL to CPW transition, while the red curve is with CPW to CPW transition.

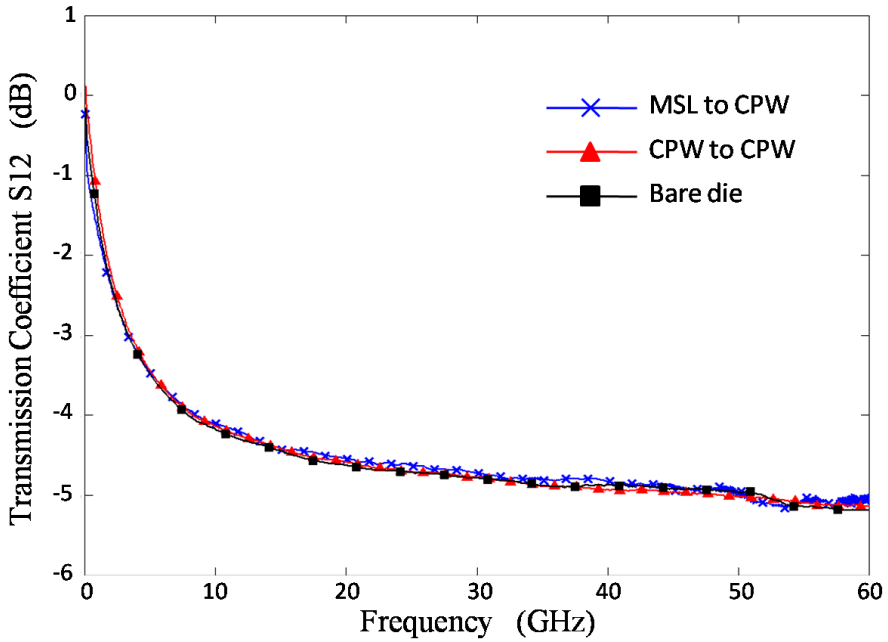

Figure 5.9 *De-embedded transmission coefficient of on-chip CPW line L_j.*

Due to intrinsic high dispersion property of silicon and the finite conductivity of thin film metal, the extracted short length CPW line shows a transmission loss as large as -5 dB. It can be seen that at any frequency point the maximum difference between the curves is about 0.1 dB, which is a very small value and shows good consistence of the results within the whole bandwidth. It means that, although the UTCP embedded chips have a thin layer of polyimide on top of it, the propagation constant of their on-chip CPW line does not change greatly compared to the bared die. So we can conclude that the top polyimide layer with limited thickness of 10 to 20 μm

has little influence to the embedded chip. It's not surprising that all on-chip CPW lines have the same transmission characteristics, because they have the same pattern and taped out from the same wafer. So in the following analysis, we can assume that any differences in connection properties of UTCP packaged chips are not correlated with the performance variations among on-chip CPW lines.

The Ni/Au bumped PTCE chips patterned with 50 Ω CPW transmission lines were embedded using UTCP technology. Before extracting the matrix for package transition structure, we can look at the overall performance. Fig 5.10 shows the back to back transmission and reflection measurement results. As mentioned above, we only consider frequency band beyond 10 GHz.

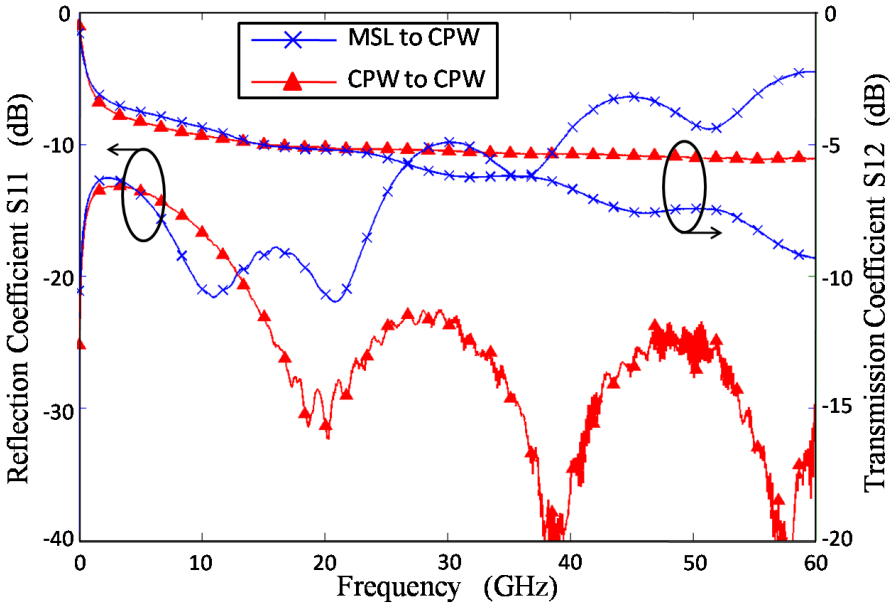

Figure 5.10 *Back to back measurement results of UTCP embedded CPW line L_j.*

For the CPW to CPW transition, the insertion loss S12 is almost constant around 5 dB, and its return loss S11 is well below 15 dB. It's clear that the reference impedance at the probe matches to characteristic impedance of the line. Considering the loss from the on-chip CPW line as depicted in Fig 5.9, it seems the CPW to CPW transition structure introduces only very small insertion loss. On the other hand, the sample with MSL to CPW transition

shows similar results as the one with CPW transition up to 20 GHz, and beyond this point it's the insertion loss starts to degrade until the end of the measurement. The measured S12 is about9.3 dB at 60GHz, which is about 4 dB worse than the sample with CPW transition structure. Correspondingly, the measured S11 increases as increasing of frequency from -20 dB to -4.5 dB at 60GHz.

We can see that the back to back measurement data for the sample with MSL transition has more insertion and reflection losses compared to the sample with CPW transition. But it should be noted that the poor performance does not reflect the performance of the transition structure, but also includes the impact of GSG probe contact pads.

In order to extract and compare the matrixes of only the transition structures, we first need to define the start and stop reference plane of them. For both configurations, as marked in Fig. 5.8, the transition area is between plane A-A' and B-B'.

In case of the CPW transition, the start plane coincides with the probe launch position. So the error box of Tx in Fig 5.9 is actually the matrix which can represent the CPW transition behavior. Following the Eq. 5.3, the content of Tx (and Ty) can be derived if we incorporate measurement result of a reflection structure (open or short stub). A detailed analysis of the TRL de-embedding algorithm can be found in [13, 15]. After de-embedding, the error box Tx is extracted as a two port matrix, whose reference impedances are Zo for the input port and Z_L for the output port. Z_L is the characteristic impedance of the on-chip CPW line. As discussed above, the value of both Z_L and Zo are close to 50 Ω beyond 10 GHz.

For the MSL transition, the Tx matrix can be divided into two parts as shown in Fig. 5.11. The first part is denoted as Tx_{11}, which includes the section from plane P_1-P_1' to A_1-A_1' as indicated in Fig 5.8. So the matrix $Tx_{11}$is composed of probe contact pads as well as a short length of MSL. And the second part $Tx_{12}$is the matrix representing the transition from MSL to CPW in UTCP package.

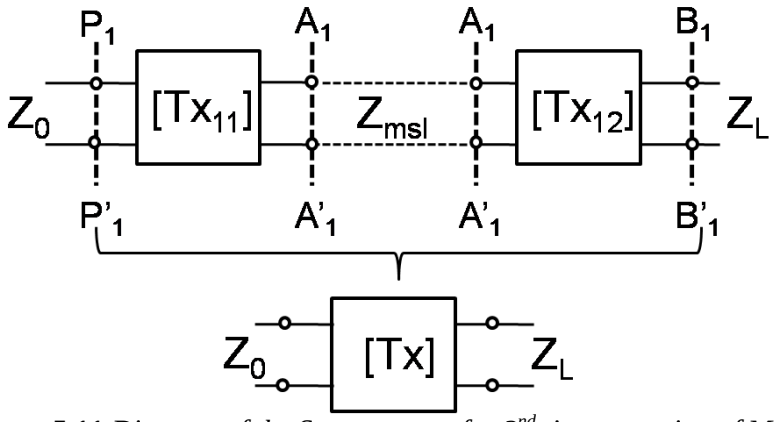

Figure 5.11 *Diagram of the S parameters for 2nd tier extraction of MSL transition.*

Since $Tx_{11}$and $Tx_{12}$are in cascade with each other to form the error box Tx, we can have the relation:

$$[Tx_{12}] = [Tx_{11}]^{-1} \bullet [Tx] \tag{5.6}$$

It is obvious that a second tier de-embedding is needed to remove the impact of Tx_{11}. This issue is considered in the original design. We have incorporated a set of structures for the 2nd tier de-embedding, which include several MSLs and a corresponding short stub. Both the line and the stub are designed with the same contact pads the one connected to the UTCP MSL transition structure. These de-embedding structures are fabricated together with the UTCP on the same glass carrier, which minimizes the variations in polyimide thickness and other process parameters. Similarly as above, by applying the TRL algorithm on the measurement data of de-embedding structures, we can get the content of Tx_{11}. Since the matrix Tx is already known after the 1stdeembedding, Tx_{12} can be derived if Tx and Tx_{11} are substituted into Eq. 5.6. The extracted Tx_{12} is equivalent to a two port network with reference impedances of Z_L and Z_{msl} at double sides. Z_{msl} is denoted as the characteristic impedance of the connected MSL. So in the original deisgn, we make the MSL to have characteristic impedance of 50 Ω. Z_{msl} is verified by by Agilent ADS Linecalcas. The MSL polyimide thickness is measured to be 10 μm and the signal trace has a line width of 23 μm. The material property of polyimide is already extracted in chapter 4. By applying all the above data in Linecalcas, Z_{msl} is calculated to be 49.98 Ω.

Then it is that the extracted Tx_{12} is directly comparable to the Tx matrix of the UTCP CPW transition.

Fig 5.11 presents the S11 and S12 of both CPW and MSL transition structures realized in UTCP. It can be seen thatS11 curves are well below 15dB in target bandwidth, which means that the input and output ports are well matched. So the impact of impedance mismatch is negligible for the transition performance. The transmission curves S12 of both transitions are compared with each other.

For the CPW transition, S12 is almost constant around -0.25 dB (± 0.1 dB) within the whole frequency bandwidth up to 60 GHz. It is well known that the capacitive property dominates in circuit model of the CPW to CPW transition in flip chip package. Its capacitance mainly comes from the overlap between chip bond pads and the package CPW line. But for the UTCP package, the constant reflection shows a resistive property. This is because bond pad area is very small thanks to the UTCP fine pitch interconnecting capability. On the other hand the resistance is higher than flip chip bonding due to the small microvia and thin metallization.

For the MSL transition, the S12 curve starts at almost the same point as the S12 of CPW transition, and then it starts to going slowly down as the increasing of frequency. At about 43 GHz, reflection curve is reversed and starts to increase rapidly. The increase in reflection loss leads to a faster degradation of S12. This is probably because for the MSL transition, the central microvia with a longer depth generates higher inductance than that of the microvias in CPW transition. And beyond 43 GHz, the behavior of MSL transition shifts to an inductive region, whose impedance is proportionally increased with the frequency. However the degradation of MSL transition is very limited. At 60GHz, its value is recorded at -0.78 dB, which is only 0.5 dB lower than the value of CPW transition. It should be noted that, the peak and valley in the curve is because error introduced by the 2^{nd} de-embedding, since the result of TRL algorithm becomes not stable and collapse at integer multiple of CPW propagation wavelength corresponding to 13.7 GHz in this case. From Fig. 5.12, we can conclude that the performance of MSL transition is slightly worse than that of the CPW transition. For the MSL transition, the high inductance together with the resistive loss degrades the overall performance.

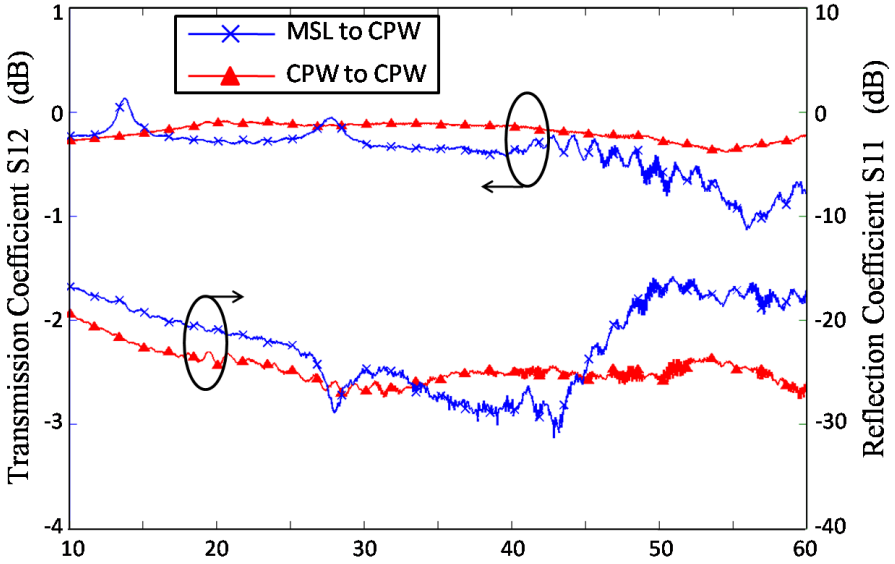

Figure 5.12 *Extracted transmission and reflection coefficients of RF transitions realized in UTCP.*

The high frequency performance of UTCP package is compared with other IC package methods. Table 5.2 listed insertion loss presented in some literatures for flip chip or wire bonding based connection. It should be mentioned that the RF performance of each connection is very much dependent on dimension parameters and the incorporated material composition. For example, the ACA joint in [20] normally has a high contact resistance and results in a higher insertion loss. Table 5.2 just gives a rough performance range of some commonly used conjunctions.

Ref no.	Insertion loss	Frequency	Transition type
[17]	0.3 dB	optimized for 35 GHz	Flip chip without underfill
	0.8 dB	optimized for 35 GHz	Flip chip with underfill
[18]	below 0.5 dB	below 50 GHz	Flip chip
[19]	0.2 dB	up to 90 GHz	Flip chip compensated
	0.3 dB	up to 90 GHz	Flip chip not compensated
[20]	2 dB	below 30 GHz	ACA flip chip
[21]	4 dB	40 GHz	Flip chip
[22]	0.4 dB	9.5 GHz	Flip chip
	2.2 dB	9.5 GHz	Wire bond

Table 5.2 *Insertion losses reported in literaturesof package methods.*

We can see that, except [19] is with values at the same level as UTCP losses, the results from all the other references show higher losses. In summary, we can conclude that the UTCP package presents one of the best performances amongst the current package methods. Both the CPW and MSL transition realized in UTCP package show acceptable insertion loss and impedance matched reflection coefficient, which indicates suitability for high frequency application up to 60GHz.

In addition to the superb RF performance, UTCP package has the finest pitch capability compared to the normal package methods. Connection pitch of 60 μm or even below has been demonstrated. Normally CPW or MSL is connected to the chip and route the signal to the UTCP I/O port. The UTCP package can be used standing alone. Another possibility is to use it as an interposer which can be further attached on or embedded in a system main board. In this way, a fan-out design is realized to bridge the pitch mismatch between the embedded chip and the main board.

As mentioned above, CPW and MSL are two main types of transmission line, which can be fabricated on UTCP for signal routing. It is necessary to investigate their transmission property. Fig. 5.13 shows the attenuation coefficient of the CPW and MSL with conductor thickness of 1, 3 and 5 μm. The attenuation results are calculated at 60 GHz by Agilent ADS Linecalcas and are plotted as a function of the transmission line central conductor widths from 20 to 100 μm. Polyimide HD 4110 is applied as dielectric material in the calculation, whose property has been extracted and presented in Chapter 4. The characteristic impedances of the lines were set to 50 Ω by adjusting the other line dimension parameters.

From the figure, we can see that the CPW line shows higher losses compared with the MSL. It means that, although the loss of CPW transition is lower than the MSL transition, the overall losses may be quite opposite if the routing length is long. In addition to the higher losses, another drawback of CPW is sensitive to the detuning from the on-chip metallization. On the other hand, the MSL ground plane provides shield for the signal trace. In case of both CPW and MSL, the attenuation is always reduced as the increasing of the line width. This is because of the reduction of the line resistance. But, for the CPW line, the conductor width is limited by the minimum pitch in chip connection. For the MSL, the thickness of dielectric needs to increase as the increasing of line width to maintain 50 Ω impedance.

Then the deeper microvia through the MSL dielectric can generate higher inductance and in the end degrades MSL transition performance.

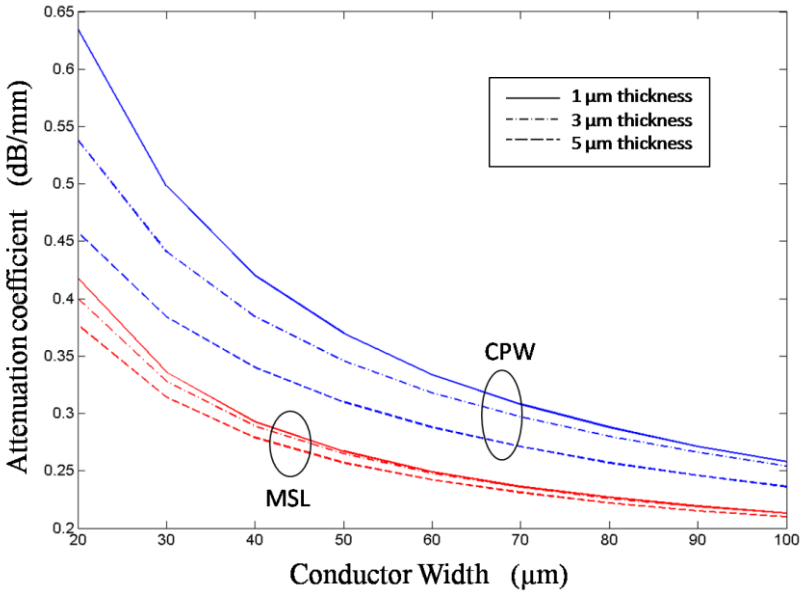

Figure 5.13 *Calculated attenuation of CPW and MSL transmission line made in thin film polyimide.*

5.5 Conclusion

In this chapter, we studied the high frequency property of UTCP transition structures. Two types of transition structure were fabricated by following UTCP process sequence. One type is CPW to CPW transition and the other type is MSL to CPW transition. The MSL transition requires two layer of dielectric buildup instead of single layer in CPW transition structure. The transmission and reflection coefficient is extracted for both transition structures from 10 GHz up to 60 GHz. The reflection coefficients are all well below -15 dB, indicating good impedance match. The CPW transition shows a more or less constant insertion loss at around 0.25 dB. It can be interpreted by resistive loss of small microvias. The loss of MSL transition starts at -0.2 dB at 10 GHz and gradually degrades to -0.78 dB at 60 GHz. The worse performance of MSL transition is probably due to the extra inductance introduced by central deep microvia. Compared with the results of the

current package methods in literatures, we can concludes that UTCP package shows one of the best performance for high frequency application.

References

[1] J. Essing, R. Mahmoudi, Y. Pei, and A. van Roermund, "A fully integrated 60GHz distributed transformer power amplifier in bulky CMOS 45nm," in *2011 IEEE Radio Frequency Integrated Circuits Symposium*, 2011, pp. 1–4.

[2] E. Cohen, S. Ravid, and D. Ritter, "60GHz 45nm PA for linear OFDM signal with predistortion correction achieving 6.1% PAE and −28dB EVM," in *2009 IEEE Radio Frequency Integrated Circuits Symposium*, 2009, pp. 35–38.

[3] M. Wojnowski, K. Pressel, G. Sommer, and M. Engl, "Package Trends for Today's and Future mm-Wave Applications," in *38th European Microwave Conference*, 2008.

[4] W. Heinrich, "The flip-chip approach for millimeter wave packaging," *IEEE Microwave Magazine*, vol. 6, no. 3, pp. 36–45, Sep. 2005.

[5] A. Sutono, N. G. Cafaro, J. Laskar, and M. M. Tentzeris, "Experimental modeling, repeatability investigation and optimization of microwave bond wire interconnects," *IEEE Transactions on Advanced Packaging*, vol. 24, no. 2, pp. 595–603, 2001.

[6] L. Gu, W. Feng, W. Che, and Y. L. Chow, "Investigations on bonding wire array for interconnect of RFICs," in *2012 International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, 2012, vol. 5, pp. 1–4.

[7] W. Heinrich, A. Jentzsch, and G. Baumann, "Millimeter-wave characteristics of flip-chip interconnects for multichip modules," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 12, pp. 2264–2268, 1998.

[8] Y. Arai, M. Sato, H. T. Yamada, T. Hamada, K. Nagai, and H. Fujishiro, "60-GHz flip-chip assembled MIC design considering chip-substrate effect," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 12, pp. 2261–2266, 1997.

[9] L.-H. Hsu, C.-W. Oh, W.-C. Wu, E. Y. Chang, H. Zirath, C.-T. Wang, S.-P. Tsai, W.-C. Lim, and Y.-C. Lin, "Design, Fabrication, and Reliability of Low-Cost Flip-Chip-On-Board Package for Commercial Applications up to 50 GHz," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 2, no. 3, pp. 402–409, Mar. 2012.

[10] Y. K. Song and C. C. Lee, "RF modeling and design of flip-chip configurations of microwave devices on PCBs," in *2004 Proceedings. 54th Electronic Components and Technology Conference (IEEE Cat. No.04CH37546)*, 2004, vol. 2, pp. 1837–1842.

[11] S. Yamamichi, K. Mori, K. Kikuchi, H. Murai, D. Ohshima, Y. Nakashima, K. Soejima, M. Kawano, and T. Murakami, "Chip-level and package-level seamless interconnect technologies for advanced packaging," in *2009 IEEE International Electron Devices Meeting (IEDM)*, 2009, pp. 1–4.

[12] R. Fillion, C. Woychik, T. Zhang, and D. Bitting, "Embedded Chip Build-Up Using Fine Line Interconnect," in *2007 Proceedings 57th Electronic Components and Technology Conference*, 2007, pp. 49–53.

[13] G. F. Engen and C. A. Hoer, "Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 27, no. 12, pp. 987–993, Dec. 1979.

[14] G. P. Zhigal'skii and B. K. Jones, *The Physical Properties of Thin Metal Films. CRC Press. 2003.* CRC Press, 2003.

[15] D. M. Pozar, *Microwave Engineering*. Wiley, 2011, p. 752.

[16] M. Cauwe and J. De Baets, "Broadband Material Parameter Characterization for Practical High-Speed Interconnects on Printed Circuit Board," *IEEE Transactions on Advanced Packaging*, vol. 31, no. 3, pp. 649–656, Aug. 2008.

[17] K. C. Gupta and Y. C. Lee, "RF and mechanical characterization of flip-chip interconnects in CPW circuits with underfill," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 12, pp. 2269–2275, 1998.

[18] W. Heinrich, K. Hirche, W. Scholz, M. Warth, and W. Ehrlinger, "Optimized flip-chip interconnect for 38 GHz thin-film microstrip multichip modules," in *2000 IEEE MTT-S International Microwave Symposium Digest (Cat. No.00CH37017)*, 2000, vol. 1, pp. 69–72.

[19] A. Jentzsch and W. Heinrich, "Theory and measurements of flip-chip interconnects for frequencies up to 100 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 5, pp. 871–878, May 2001.

[20] G. Zou, H. Gronqvist, and J. Liu, "Theoretical Analysis of RF Performance of Anisotropic Conductive Adhesive Flip-Chip Joints," *IEEE Transactions on Components and Packaging Technologies*, vol. 27, no. 3, pp. 546–550, Sep. 2004.

[21] U. R. Pfeiffer and A. Chandrasekhar, "Characterization of flip-chip interconnects up to millimeter-wave frequencies based on a nondestructive in situ approach," *IEEE Transactions on Advanced Packaging*, vol. 28, no. 2, pp. 160–167, May 2005.

[22] C. H. J. Poh, C. E. Patterson, S. K. Bhattacharya, S. D. Philips, N. E. Lourenco, J. D. Cressler, and J. Papapolymerou, "Packaging Effects of Multiple X-Band SiGe LNAs Embedded in an Organic LCP Substrate," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 2, no. 8, pp. 1351–1360, Aug. 2012.

CHAPTER 6

Embedded Passive Compoments

Embedding passive components (EPCs) is known as a promising technology to provide high electrical performance. In the frame of EU SHIFT project, off-chip RF passives are produced based on thin film technology. Multilayer structures are built-up on temporary glass carrier substrates by repetitive application of spin-coated polyimide layers and sputtered metal layers. After processing and testing the structures can easily be released from the carrier and embedded inside PCB or FCB. This chapter briefly describes the fabrication process and shows measurement results of the realized passive elements.

6.1 Introduction

Passive components are of great importance for the overall characteristics of the RF circuits [1]. High-performance and low-cost can hardly be achieved by integrating passives into RF chips since the large area consumed by the passives on silicon substrate leads to a higher cost and higher loss [2]. System in a package technology is an interesting alternative which is widely used in wireless communication systems [3], [4]. Amongst all packaging and

assembly technologies, embedded passive components (EPCs) hold the promise of fine pitch interconnect and cost effective solution. However the embedded devices put rather strict requirements on their final geometry and often need complex processing [5].

In order to retain the good electrical behavior of EPCs and to relieve geometry restrictions, off-chip RF passives can be produced based on thin film stack which is developed in EU funded SHIFT project [6]. The proposed fabrication technique is compatable with the UTCP processing. In this case, the passive elements and the UTCP can be integrated together to work as a complete system. Fig. 6.1 shows the principle of this technology, including assembled components. EPCs which have multilayer thin film structure can be laminated inside FCB and interconnected by through hole via and Cu track.

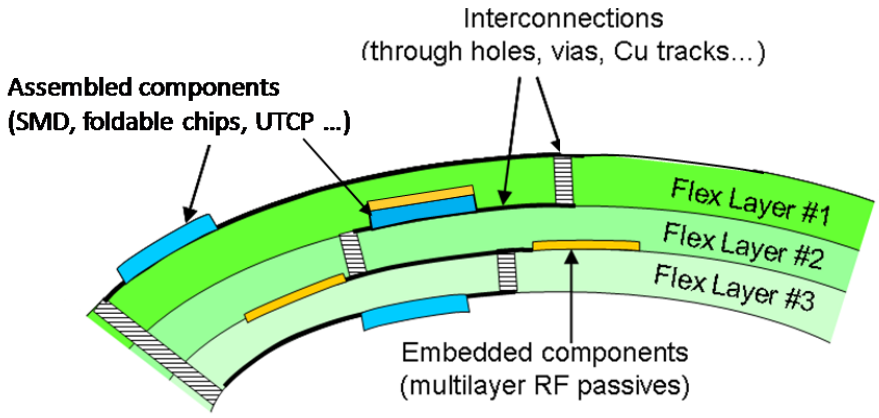

Figure 6.1 *Principle of embedded off-chip RF passives.*

In section 2, the process flow to fabricate the EPCs based on thin film technology is discussed briefly. In Section 3, characterization and analysis of the test structures are presented. In Section 4, an electromagnetic simulation is introduced by using ADS Momentum (2.5D simulator). A comparison between experimental and simulated results is demonstrated for an inductor.

6.2 Process Description

Inductors, capacitors, resistors (RLC) and transmission lines are realized on glass substrates, based on thin film technologies. A suitable process flow is

proposed and established in SHIFT project for building up multilayer RF elements through repetitive application of polyimide layers by a spin-on process and metal layers by sputtering (Fig. 6.2).

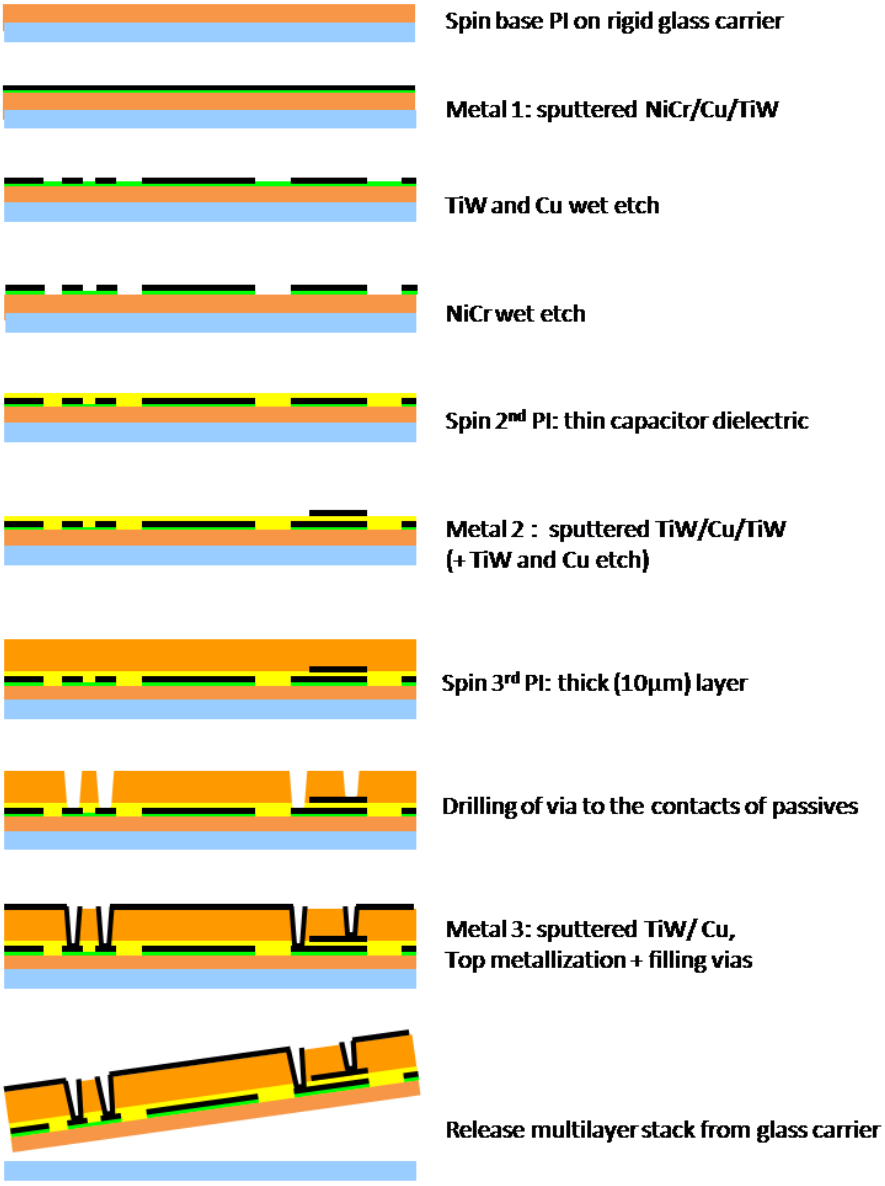

Figure 6.2 *Process flow for multilayer RF passive elements*

In the SHIFT project, only non-photosensitive polyimide PI-2611 is used as dielectric material. But if photo via technology is preferred, polyimide HD-4110 is a suitable candidate and can replace the PI-2611 in the process sequence without siginificant adaptation. White Float glass is selected as carrier substrate.

Before applying the first polyimide layer, the 4 edges of the glass carrier are coated with adhesion promoter VM652. Thus, the first polyimide layer only sticks to the edge of the substrate. In contrast, the center area does not have good adhesion. After the whole processing (and testing), the polyimide structures can be easily cut out and released from the substrate. The build-up of multilayer thin film structures consists of 3 polyimide layers and 3 metal layers. A schematic cross section is shown in Fig. 6.3. The first metal layer is NiCr/Cu/TiW (20nm/1um/50nm) layer, where NiCr is chosen as resistor material and the copper layer on top of the NiCr provides the connection for the NiCr resistors. An additional TiW layer can protect the Cu layer from oxidation and ensure a good contact to other metal layers. Resistors, inductors and the bottom electrode of capacitors can be defined in the first metal layer. PI2 is a very thin polyimide layer, which is used as dielectric for the capacitors. Metal 2 is TiW/Cu/TiW layer for top electrode definition. Metal 3 is another TiW/Cu layer which provides the contact to the test structure, and also can define inductors and striplines. Vias between the metal layers are opened by CO2 laser ablation and a following RIE cleaning to remove residual polyimide at the bottom of the vias.

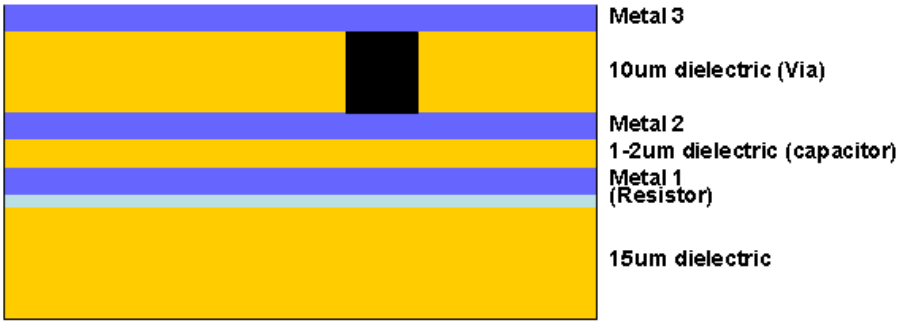

Figure 6.3 *Schematic cross section of the multilayer structure*

In the first prototype, several test elements were made based on the thin film technology. All elements are connected with Ground-Signal-Ground (GSG) contact pads for direct RF measurements. The test structures include integrated resistors with a nominal value of 50 Ω. A library of spiral inductors was also designed on the sample. The value of inductance was

adjusted by changing the number of spiral turns. In addition, a low pass filter was designed by cascading MIM capacitors and the spiral inductors. For each test element, its performance was measured by a VNA AGT E8361C with GSG probes. The measurement set-up was first calibrated up to the probe tips using a TRL calibration substrate (from Cascade Microtech). During the measurement, an air spacer was put between the sample and the wafer vacuum chuck to avoid detuning effect. And finally, the insertion and reflection coefficients of each element were obtained.

After the whole processing and characterization, the multilayer RF structures can be easily released from the glass carrier (see Fig. 6.4), resulting in extremely thin foils which are suitable for embedding inside conventional PCB or FCB stacks.

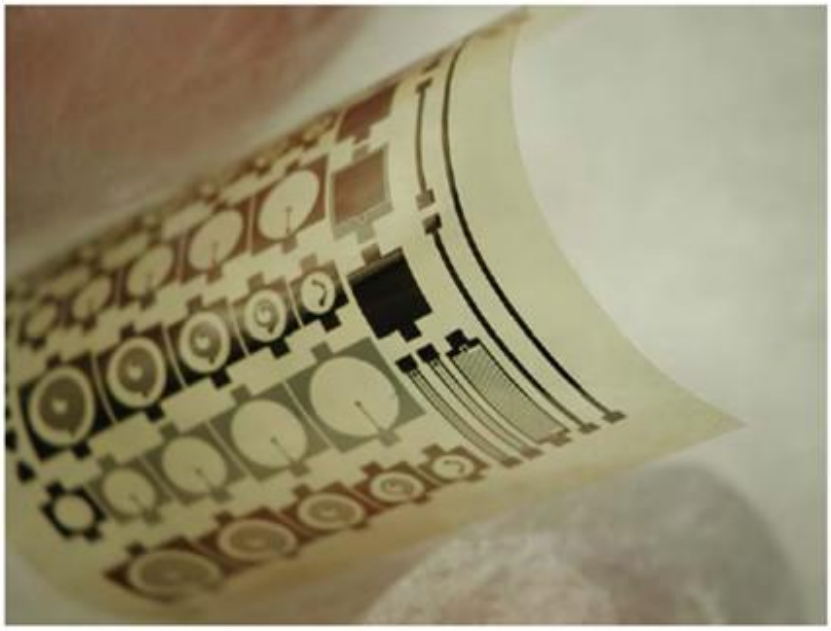

Figure 6.4 *Multilayer RF structures after re lease from the glass carrier*

6.3 Characterization and Analysis

6.3.1 Spiral Inductors

Spiral inductors are realized on metal 3, which are separated from the ground plane of metal 2 by 10um PI3. The number of turns N is changed from 0.5 to 4.5 in steps of 1 turn. Fig. 6.5 shows a typical spiral inductor with 3.5 turns. The inner trace can cross over the spirals through the groud plane. For each structure, GSG contact pads are designed for use with the same type of probe. In this work, all the inductors have a distance of L = 300um between spiral inductor and ground plane, and an internal diameter r of 450um. The width of the metal traces t and the space between metal traces S are both 50um for each inductor. The above mentioned geometry parameters are summarized in Table 6.1

Fig. 6.6 shows the well known lumped element model of a spiral inductor [7]. The series inductance L and series resistance R represents the inductance and resistance of the spiral inductor. The coupling capacitance between the spiral and the ground plane is modeled as parallel capacitances C1 and C2.

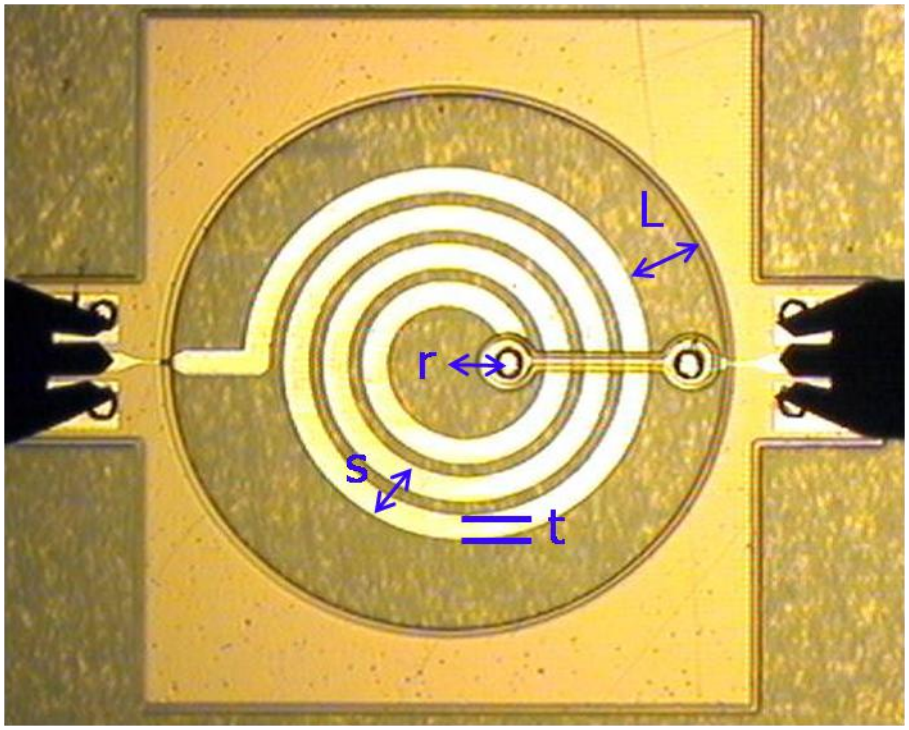

Figure 6.5 *Top view of a realized spiral inductor with 3.5 turn*

Geometry	r	S	t	L
Length (μm)	450	50	50	300

Table 6.1 *Summary of geometry parameters for spiral inductors*

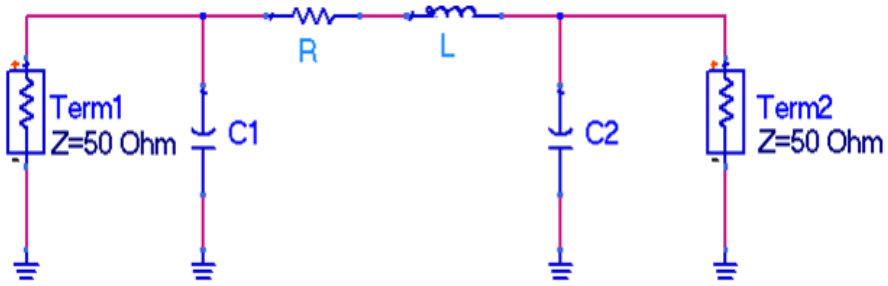

Figure 6.6 *Lumped element model of a spiral inductor on glass substrate*.

The series inductance L and Q-factor can be calculated from the measured datasets. The Q-factor is defined as a ratio of the stored energy to the dissipated energy. In practical, Q and the inductance L can be calculated based on the following equations,

$$Q = \frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \tag{6.1}$$

$$L = \frac{-\mathrm{Im}(1/Y_{21})}{2\pi f} \tag{6.2}$$

where Y is the converted admittance matrix from the measured S matrix.

The extracted inductance L and Q-factor for different spiral inductors (N=0.5 to 4.5) is plotted in Fig. 6.7 and Fig. 6.8. An increase of the inductance value from 1.5 nH to 25 nH is observed, with an increasing number of turns, while the value of the Q factor ranges between 10 and 12.5. It should be noted that Eq. 6.2 is valid for analyzing only up to first resonance frequency of a spiral inductor. Beyond this threshold, an inductor works in capacitive region and we can not use Eq. 6.2 to calculate its inductance. This can explain why there is a steep drop-off of the inductance value for the two largest inductors. The degradation of Q factor is common for large inductance, because the longer trace for realizing higher number of spiral turns causes higher resistive loss and result in a smaller Q factor.

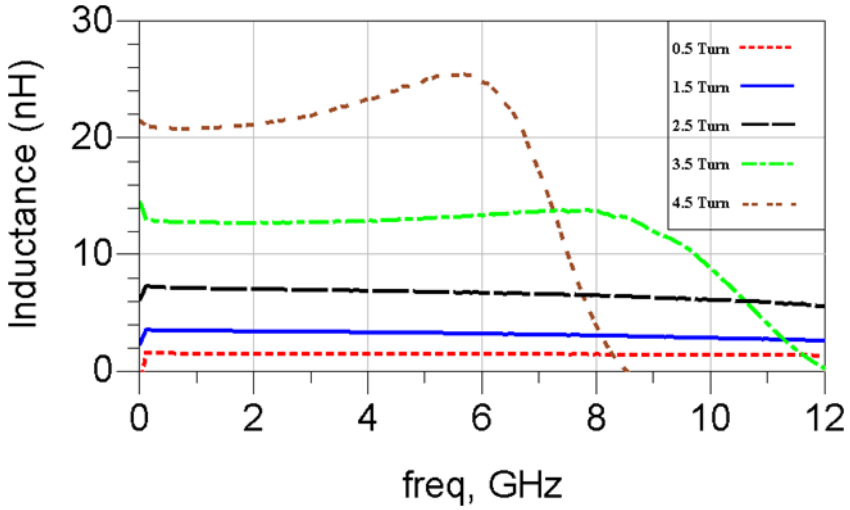

Figure 6.7 *Extracted inductance L from measurement for different spiral inductors (N=0.5 to 4.5)*

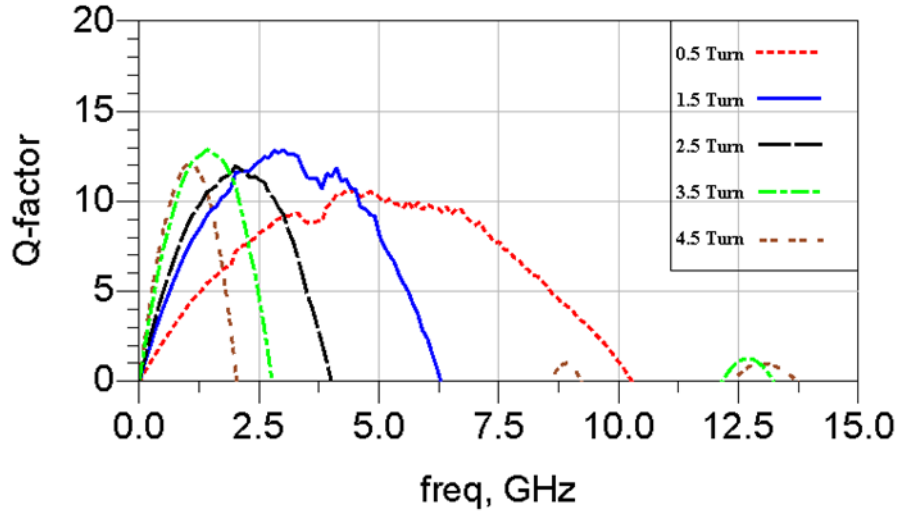

Figure 6.8 *Measured Q-factor for different spiral inductors (N=0.5 to 4.5)*

6.3.2 Resistors

Integrated resistors are defined in the 20nm NiCr layer which is designed to have a sheet resistance of 100Ω/square. Fig. 6.9 shows a 50Ω LOAD structure including a design of 50Ω integrated NiCr resistor. The input

impedance can be calculated from the reflection coefficients according to the following equation:

$$Z_{in} = \frac{Z_0 \times (1+S_{11})}{1-S_{11}} \quad (1)$$

Where Z_0 is the characteristic impedance of the cable, which is 50 Ω in our case. The real part of Z_{in} is shown in Fig. 6.10, and a value of 54 Ω is measured @ 45 MHz which is very close to the nominal value of the NiCr resistor. The difference between the measured value and the nominal value may be attributed to the underetching of routing the layer of metal 1. This can be improved by a more strict control over the etching process.

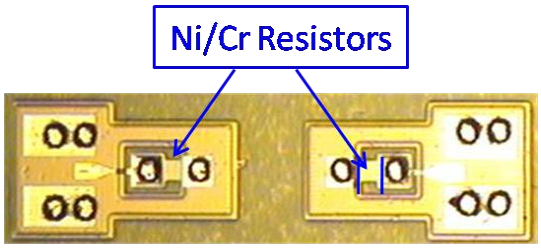

Figure 6.9 *Top view of a realized LOAD structure including 50ohm NiCr resistors as indicated by blue arrow.*

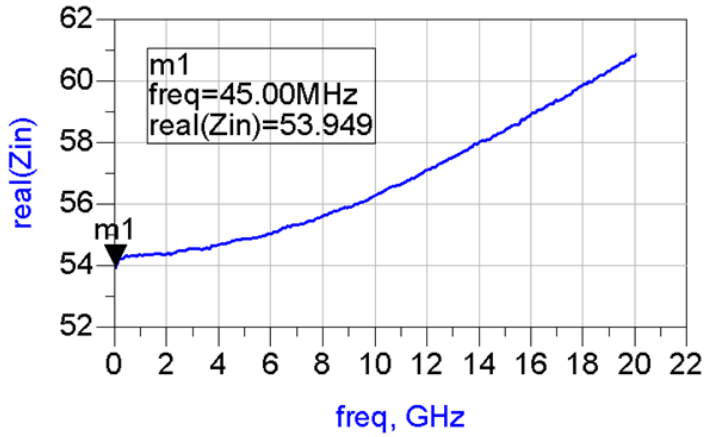

Figure 6.10 *The real part of input impedance Z_{in} of a LOAD structure*

6.3.3 Low Pass filter

A filter has been realized by cascading spiral inductors and metal-insulator-metal (MIM) capacitors. The filter is designed as a maximally flat low pass

filter with a cut off frequency of 1 GHz. The insertion at 1.5 GHz should be at least 15 dB. To meet the design requirements, the filter needs to have a five stage symmetric layout (Fig. 6.11), and so does its equivalent circuit. Spiral inductors with 3.5 turn are integrated for the filter. The expected value of the inductance L is 12.8 nH, which is actually verified in previous section. Correspondingly, by adjusting the parallel plate overlap surface area, the value of capacitance for C_1 and C_2 are set to 1.95 pF and 6.36 pF respectively. More detail about the fabrication and the design specifications can be found in [8-10], and they are not covered in this PhD dissertation.

The filter measured S parameters are plotted in Fig. 6.12. S12 shows a sharp drop from -2.75 dB to -15dB between 0.99 GHz and 1.5 GHz, which basically fulfills the design requirements.

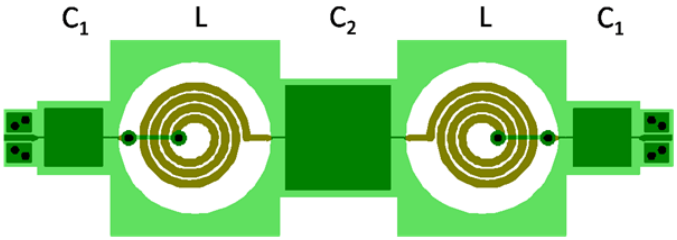

Figure 6.11 Layout of a 1GHz low pass filter

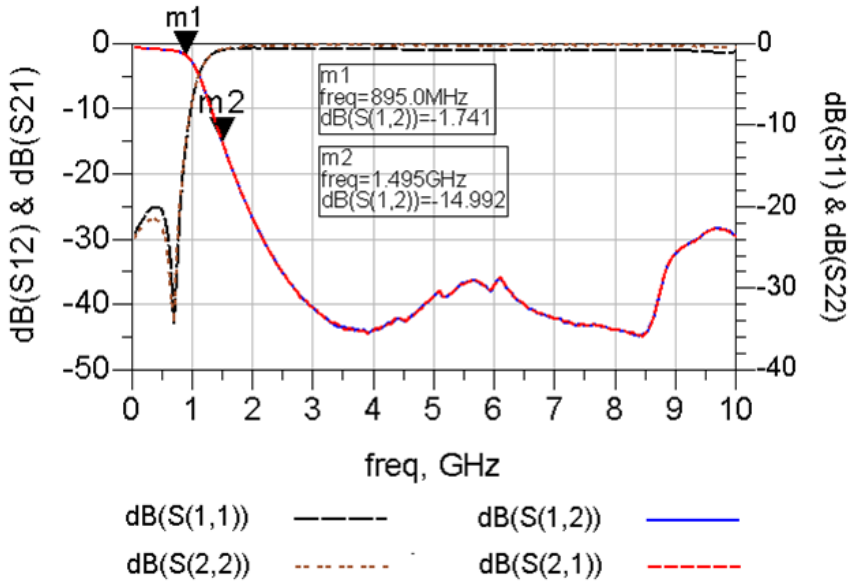

Figure 6.12 *S parameters of a 1GHz low pass filter.*

6.4 Electromagnetic Simulation

Electromagnetic simulation is useful to predict the performance of the RF circuit. The spiral inductor with 0.5 turn is simulated in ADS Momentum. The ADS Momentum is a 2.5D wave simulation tool. In the created model, the layout of two conducting planes (signal and ground) as well as the microvia holes was created in three different layers. The dielectric between the two conducting layers was defined as polyimide in the simulator "substrate property". The permittivity of polyimide is set to its nominal value of 2.9. The microvia layout is selected as model VIA layer and defined as a 3D distributed model so as to include both vertical and horizontal currents. On each inductor contact pad, three ports, with two ground reference ports and one central internal port are created. Then, the model is simulated from 10 MHz up to 40 GHz.

The measured and simulated S parameters are plot together in Fig. 6.13 and show a good agreement up to 30GHz. The spiral inductance is extracted based on the lump element model in Fig. 6.6. The comparison between the measured and simulated inductance is given in Fig. 6.14. A good agreement is shown up to the first resonant frequency.

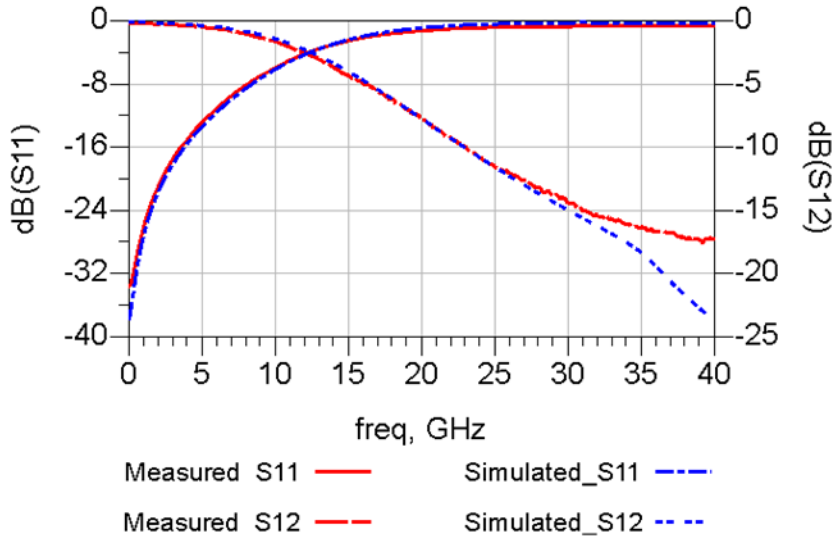

Figure 6.13 *Measured and simulated S parameters for a spiral inductor with 0.5 turn*

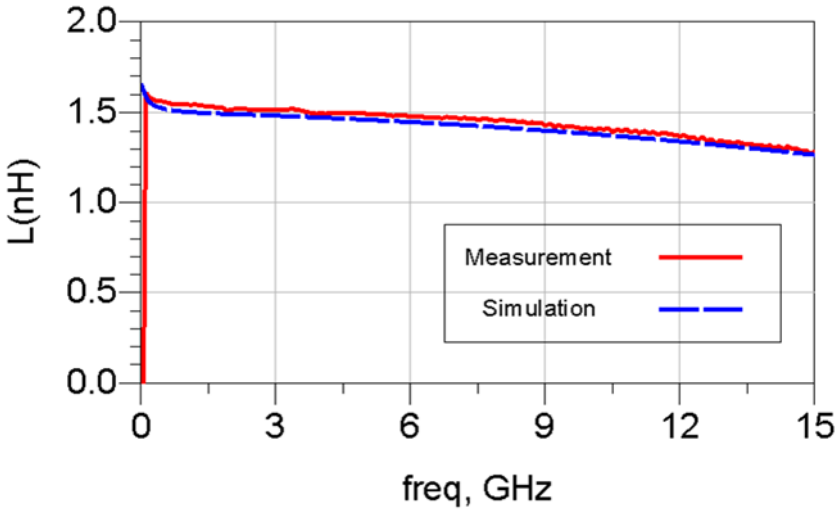

Figure 6.14 *Extracted L from measurement and simulation for a spiral inductor with 0.5 turn.*

6.5 Conclusion

In this chapter, a novel approach to fabricate EPCs based on thin film technology is presented. A process flow for polyimide based multilayer structures (having 3 metal layers) has been established and first test structures have been realized. After processing (and before release from their rigid carrier), different structures have been characterized and analyzed: the inductance of the spiral coil increases from 1.5 nH to 25 nH as the number of turns increases from 0.5 to 4.5. A 50 Ω resistor and a 1 GHz low pass filter are both successfully fabricated. In the end, an electromagnetic analysis has been completed by using ADS momentum. A comparison between experimental and simulated results is demonstrated for an inductor. A good agreement is obtained.

References

[1] Davis M.F., "RF-Microwave Multi-band Design Solution for Multilayer Organic System on Package Integrated Passives," IEEE MTT-S Int. Microwave Symp. Dig, Vol. 3(2002), pp. 2217-2220

[2] A. Ali, "Design and comparison of various passive components of a 5 GHz wireless LAN applications," Proc.Nat. Conf. Emerging Technol, 2004, pp. 17–23.

[3] Martin, M. "System-in-package (SiP) modules for wireless multiradio," ECTC 56th, 2006

[4] Shamim, A. "Wireless Dosimeter: System-on-Chip Versus System-in-Package for Biomedical and Space Applications," IEEE Trans. Circuits Syst. II, Exp. Briefs, Vol 55, No.7(2008), pp. 1549-7747

[5] W. Jillek, "Embedded components in printed circuit boards: a processing technology review," Int J Adv Manuf Technol, Vol. 25, No.3-4 (2005), pp. 350-360

[6] Smart High Integration Flexible Technology. http://www.shift-project.org.

[7] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May 1998.

[8] W. Christiaens, "Active and passive component integration in polyimide interconnection substrates," Ph.D dissertation, Dept. of Electro. & Inform. Syst., Ghent Univ., Ghent, Belgium, 2009.

[9] W. Christiaens, et al, "Polyimide Based Embedding Technology for RF Structures and Active Components," Proc. 12th Pan Pacific Microelectronics Symposium, Maui, HI, Jan. 2007.

[10] W. Christiaens, H. Burkard, J. Link, J. Vanfleteren, "Integration of Thin Flexible RF Structures into Flexible PCB", EMPC 2007, Oulu, Finland, June 17-20.

CHAPTER 7

Conclusion and Outlook

7.1 Main Achievements

In the framework of this PhD study, the UTCP technology has been further developed and optimized to explore its capability for high frequency application up to 60 GHz.

The UTCP process flow is optimized to make it more suitable for high volumn manufacturing. The original dielectric material is replaced by a photosensitive polyimide HD-4110. In order to release the self-priming PSPI base layer from its rigid carrier substrate, an evaporated KCl film was introduced in the new process. The bonding of the ultra-thin die was improved in order to achieve a planar chip surface. The microvias to the chip contact pads were generated by standard UV lithography, which is a more reliable technique than laser ablation and is a more cost-effective alternative compared to dry etching. The final thickness of the flexible ultra-thin chip package is about 50 µm.

Another further improment of UTCP is to make the package top surface very flat. The flat topography is a key to achieve 3D Stacking of individual UTCPs, which allows for higher density integration and bending stress

suppression. An innovative self-alignment lithography step is introduced to make a cavity in dielectric for chip thickness compensation by using the chip itself as a photo-mask. The thinned die is then embedded in a symmetrical polyimide sandwich. The realized flat UTCP does not increase its total thickness and still can be released from the carrier to further stack vertically.

Some electrical and mechanical characterizations have been carrier out on the normal UTCP and flat UTCP. Daisy chain test dies were embedded for the study. The connection pitch of 100 µm is feasible for the UTCP process with 100% yield. It shows a significant yield increase compared to the previous work. The average contact resistance between chip and package is 4.5 mΩ for microvias in diameter of 50 µm. The mechanical flexibility property of UTCP was verified by bending the package around the surface of a 6 mm diameter cylinder without any failure of passive resistance structures. But the connection is lost due to chip fracture when the bending diameter is lowered to 4 mm.

The UTCP daisy chain test vehicles were subject a couple of reliability tests. A thermal cycling test was conducted on eight samples according to JESD22-A104C standard (-40 °C to 125 °C). No failure was found after 1000 cycles for all the samples. Another batch of 10 samples was stored in an environment at 85 °C and 85% RH for thermal humidity test. All the samples were survived after 1000 hours storage without any siginificant degradation.

In spite of DC electrical verification, a systematic study was carried out to investigate the high frequency property of UTCP package. First the dielectric material HD 4110 is characterized aiming to extract its dielectric constant and loss tangent factor. A 3D full wave simulation is employed for modeling and parameter extraction. We found that the dielectric constant of HD 4110 is about 3.1 from 10 to 60 GHz and its loss tangent increases from 0.005 to 0.012 chromologically. The extracted material property is well fitted by a rational dielectric model, which satisfies the causality constraints.

Two types of transition structure were fabricated for high frequency connection of UTCP embedded chips. One type is CPW to CPW transition and the other type is MSL to CPW transition. The MSL transition requires two layer of dielectric buildup instead of single layer in CPW transition structure. The transmition and reflection coefficient is extracted for both transition structures from 10 GHz up to 60 GHz. The reflection coefficients are all well below -15 dB, indicating good impedance match. The CPW

transition shows a more or less constant insertion loss at around 0.25 dB. It can be interpreted by resistive loss of small microvias. The loss of MSL transition starts at -0.2 dB at 10 GHz and gradually degrades to -0.78 dB at 60 GHz. The worse performance of MSL transition is probably due to the extra inductance introduced by central deep microvia. Compared with the results of the current package methods in liturratures, we can conclude that UTCP package shows one of the best performances for high frequency application.

In the end, a couple of passive devices, including resistor, spiral inductors and capacitors, were fabricated based on thin film technology and their test results were demonstrated. The inductance of the spiral coil increases from 1.5 nH to 25 nH as the number of turn increases from 0.5 to 4.5. A 50 Ω resistor and a 1 GHz low pass filter are both successfully fabricated as expected in original desgin.

7.2 Future work

The technology developed in this PhD study provides base foundation for further development of high frequency package. As the UTCP shows very promising performance on passive test die, a next step would be embedding active chips in UTCP for real application. The embedded die can be integrated along with passive components to realize a full functional system.

The Flat UTCP technology is also introduced in other (parallel running) projects. In the frame of European FP7-STRP-TIPs project, the individual flat-UTCPs are stacked together. 3D stack of UTCP is an alternative to TSV (through-silicon) based chip stacking and can achieve the compact level. The development of UTCP stacking is a subject of on-going PhD study of Swarnakamal Priyabadini, Ghent University.