

From IP Over WDM to All-Optical Packet Switching: Economical View

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Abstract—In this paper, a technoeconomical study of several (optical) packet-switching node architectures is described. Therefore, different architectures proposed in IST-WASPNET and IST-LASAGNE projects as well as a standard optical circuit switching approach are considered, and their economical impact is estimated by means of cost comparisons between the different technologies. The switching architectures all use optical fiber as a transport medium, but each of them uses a different technology to process switching. Their cost is evaluated as a function of most characteristic parameters for each technology. In the all-optical approaches, the main cost is that related to the fiber assembly, whereas for electronic processing, the most expensive cost is related to the optical-electronic-optical (OEO) conversions. The results show that the integration of optical components is crucial to make all-optical packet-switching nodes feasible.

Index Terms—Cost functions, economics, optical networks, optical node, packet-switching architectures.

I. INTRODUCTION

AS AN INITIAL step, the main node functionalities are implemented by using electronics, reducing the all-optical technology to the transport segment. However, because the traffic demand increases dramatically, mainly due to Internet applications, the electronic data processing in the network nodes imposes a severe bottleneck and all-optical processing techniques will be required [1]. However, the current optical technology still lacks of mature components, and architectures to manage the required network-node functionalities in an efficient manner still require a deep study. In addition, there is not yet an adequate all-optical alternative for electronic RAM. During the last years, great efforts in the field of optical packet-switched networks have been devoted to achieve ultrahigh speeds, not only for fiber transmission, but also for data processing in the network nodes [2], [3].

Manuscript received March 14, 2005; revised December 19, 2005. This work was supported in part by the European Commission through the project(s) LASAGNE/Information Society Technologies (IST)-ePhoton/ONe and FP6-IST-LASAGNE project (507509), and by the Flemish Government through the project(s) Institute for Encouragement of Innovation through Science and Technology in Flanders (IWT)-GBOU ONNA. The work of R. Van Caenegem was supported by the IWT through a Ph.D. grant.

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Digital Object Identifier 10.1109/JLT.2006.871012

Optical packet-routing approaches based on label swapping [4] allow for a simplification of this problem, as the high-speed data packets can be routed all optically and the electronic processing is reduced to simply reading a lower bit rate (BR) optical label containing the routing information. The label is transmitted within each data packet. For the generation and transmission of this optical label, modulation techniques different to those of data packets are usually employed such as subcarrier multiplexing (SCM) [5] and optical phase or frequency modulation [6], as well as the aforementioned different BRs. However, these approaches increase the complexity of the signals transmitted through the network, and homogeneous data packets with the same BR (40, 80, or even 160 Gb/s) for both intensity-modulated payload and label would be desirable [7]. In fact, this is the first step towards a transparent terabit-per-second photonic router where ultrahigh-speed data packets are forwarded with very low latencies. Within this latter field, the FP6 LASAGNE project [8] aims at studying and proposing an all-optical node architecture based on optical logic gates and optical flip-flops to perform all-optical label swapping (AOLS) and packet routing at high speeds. The main drawback of an all-optical node architecture, however, is its associated cost. Although the cost of optical components has been reduced with the penetration of the optical technology into the telecommunications market, it is still too high to make the all-optical packet-switched network a fact. The advantages of optics over electronics are clear, but the main drawback in this field is the current economical difference between both technologies.

This paper reports a study of different node architectures from an economical point of view. Optical packet-switching (OPS) nodes are presented, as well as the conditions to be matched in forthcoming economic trends so that the idea of an all-optical network node becomes a reality. Buffering techniques are beyond this study and were not considered. Nevertheless, this functionality can be implemented by means of optical delay lines and other passive elements and should not dramatically increase the costs in this kind of architectures.

Many papers about the technoeconomics of (optical) networks have been written. In [9], a cost model for IP/Optical Transport Networks (OTN) networks is deployed. It defines a framework for calculating the cost of the equipment and infrastructure of a whole network, whereas this paper tries to compare node costs, using the packaging cost of an optical component as a reference for the total component cost.

The paper is organized as follows. In Section II, an overview of the different OPS architectures is presented, describing their

benefits and main drawbacks. The architectures described in this section are a fully electronic configuration, an OPS node with optical–electronic–optical (OEO) conversion of the packet label, an all-optical approach with label swapping, and an all-optical approach with label stripping. A study comparing how the costs of the different architectures relate to one another is performed in Section III. Finally, the main conclusions of this study are summarized in Section IV, showing some cost figures and the design rules for which the cost of an all-optical approach could be affordable.

II. NODE ARCHITECTURES

Optical packet-switched networks route data on a packet-by-packet basis. Therefore, many different photonic packet-switching architectures have been proposed and demonstrated [6], [7]. The key functional blocks include packet routing, contention resolution, packet-label replacement, packet synchronization, and timing recovery [10]. Truly photonic switches require an all-optical implementation for these functions. The packet-label replacement function is necessary to read and change the contents of the packet label as it passes through each switching node to perform the packet-forwarding procedure. In optically transparent packet switching [11], it is necessary to carry out the label-replacement function all optically [12]. The buffering function is essential to prevent packet contention [13]. In packet-switched networks, it is extremely important to ensure a low packet-loss probability, while achieving a relatively high throughput [14]. This requires a large buffering capacity, depending on the switch architecture. Furthermore, the synchronization between the optical node subsystems and the timing information of the incoming packets is of crucial importance for the proper operation of the network node.

The remainder of this section describes four different node architectures: a fully electronic configuration, an OPS node with OEO conversion of the packet labels, and two all-optical approaches, one based on label swapping and one based on label stripping.

A. Fully Electronic Configuration:

IP-Over-Wavelength-Division-Multiplexing (WDM) Approach

The first step in the evolution of optical packet networks towards all-optical processing was the adoption of the optical fiber as the transmission medium. While getting profit of the high bandwidth provided by the optical fiber, the signal processing is still performed by electronics. In this kind of network, the optical signal that arrives at a network node (in IP networks, a network node is commonly referred to as a “router”) is converted into an electronic signal by using optical–electrical (O/E) converters. It is processed inside the node and then converted again into an optical signal using an electrical–optical (E/O) converter before it is transmitted through the optical fiber.

The IP-over-WDM approach allows increasing the flexibility and manageability of these kinds of networks. IP data packets are wavelength multiplexed on different optical carriers and transmitted through the optical fiber. Therefore, the WDM signal is wavelength demultiplexed and electronically converted by a set of O/E converters (one device per wavelength) at the

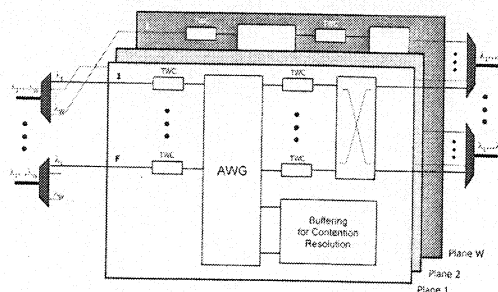


Fig. 1. Architecture of the AWG-based switch proposed in WASPNET.

input of the network node. The IP data packets on different wavelengths are extracted and, after processing in the electronic network layer, switched to another wavelength. At this point, the IP packets are again optically wavelength multiplexed into the optical fiber and forwarded towards the next network node.

B. OPS Node With OEO Packet Header Processing: WASPNET Approach

An example of an OPS node with OEO treatment of the packet label is proposed in the WASPNET project [15]. The OPS node consists of an F-fiber multiplane architecture, as shown in Fig. 1. Each plane performs the routing and buffering tasks for packets arriving on a particular wavelength. Fig. 1 also shows the detailed architecture of each wavelength plane. It broadly comprises two stages of processing. In the first stage, the input ports are connected through wavelength converters to an $F \times F$ arrayed-waveguide grating (AWG) that provides contention resolution and routes the packet payload to the correct output port. The second stage comprises wavelength converters followed by an $F \times F$ space switch that ensures that each packet is switched to the correct output fiber at the proper wavelength. In the remainder of this paper, this node will be referred to as the node with electronic header processing (NEHP).

The incoming optical packets are first wavelength demultiplexed and then fed to the corresponding plane to be processed. As an optical packet enters the plane, its label is separated and processed electronically. The routing information inside the label controls the fast-tuneable input wavelength converter, which then assigns an appropriate wavelength to the packet payload. The payload entering the AWG is passively routed to the appropriate output port according to its wavelength. At the output, a further stage of wavelength conversion ensures that the output packet wavelength matches the external network requirements. The new address label is inserted in the output wavelength converter through modulation of the optical carrier prior to the payload. The optical header is implemented by using the SCM technique and placed in time before the payload to facilitate the header removal by simply activating an optical gate [16].

C. All-Optical Approach With Label Swapping: LASAGNE Approach I

The main functionalities required by this node—label swapping and packet routing—are based on the use of all-optical logic gates. The input interface comprises wavelength demultiplexers that feed each all-optical label swapper with a specific

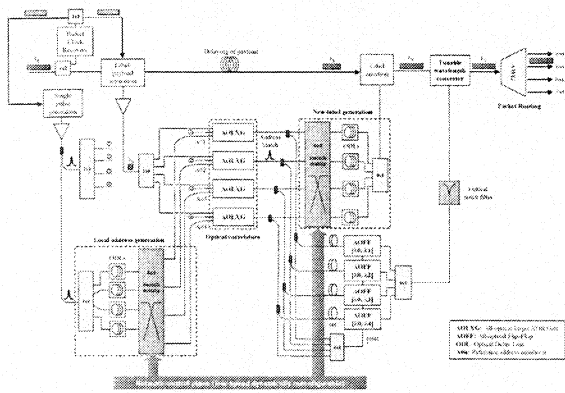


Fig. 2. LASAGNE swapping approach switching architecture.

wavelength. Each incoming packet is processed by a specific swapper (depending on its wavelength and input fiber). At the output of the AOLS block, the packet is wavelength converted and routed to the appropriate output fiber using an AWG. Finally, the packets are buffered if needed to solve contention-resolution problems.

Fig. 2 depicts the AOLS subsystem proposed in LASAGNE. The subsystem processes the incoming packets. First, the packet payload and the label are separated using the scheme proposed in [16]. The extracted optical label is fed to a bank of optical correlators that are based on all-optical logic XOR gates (AOLXGs) [17], where the label is compared to a set of local addresses. After the comparison, a single high-intensity pulse will appear at the output of the AOLXG matching the locally generated address. This pulse feeds a control block, which drives a tuneable wavelength converter. This control block is made up of all-optical flip-flops (AOFFs) [3]. Depending on the matching address (indicated by the correlator output pulse), the appropriate flip-flop will emit a continuous wave (CW) signal at a certain wavelength. Meanwhile, a new label is generated and inserted in front of the payload. Both the payload and the new label are now converted to the wavelength generated by the flip-flop. The packet is routed in an AWG, and therefore, the wavelength on which the packet leaves the AOLS block determines its outgoing port. Two switches provide the flexibility to configure the assignments between the incoming labels and the outgoing labels and wavelengths. Finally, the packets go through a contention-resolution subsystem before exiting the node. The size of the packet router (for example, number of optical correlators and flip-flops) is very dependent on the number of local addresses used in the routing table. The AOLS subsystem of Fig. 2 is depicted for the specific case of four different locally generated addresses (2-bit optical labels).

The AOLS node requires timing extraction on a packet-by-packet basis and a packet-arrival detection scheme. These functionalities are performed by a clock recovery circuit [18] and a single pulse generator. The first is placed at the beginning of the router and it is capable to handle high-bit-rate burst-mode optical packets. The latter generates an optical pulse as a packet arrives at the AOLS block. The switches used to provide flexibility in labeling are controlled by a low-speed dynamically reconfigurable network control plane. The main advantage of this architecture is that all-optical label processing is possible,

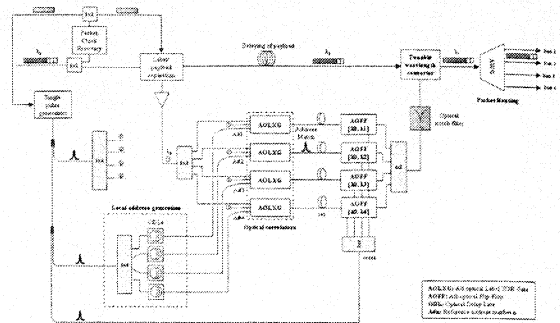


Fig. 3. Header-processing part in the label-stripping approach switching architecture.

becoming the first step towards an ultrahigh-speed all-optical packet switch.

D. All-Optical Approach With Label Stripping: LASAGNE Approach II

The use of AOLS in an OPS network creates some challenges and opportunities from the networking point of view. To lower the cost of the AOLS node, it is beneficial to reduce the number of different labels used throughout the network, and hence the number of bits occupied by the label. To this purpose, a new label-switching strategy [19] is also investigated in the LASAGNE project. A packet is switched through the network based on an end-to-end label. This label is a concatenation of multiple local labels. In each intermediate node, the AOLS subsystem strips off the first bits of the end-to-end label (this is the local label) and makes a switching decision (i.e., the stripped label points to which output port the packet has to be forwarded).

The main difference for the architectures between Figs. 2 and 3 lies in the number of correlators needed and the absence of a new label-generation block. In the stripping case, the label/payload separation block extracts only the first local label to process it at the current node, while the rest of the local labels and the payload are passed through the delay line. The packet, which is comprised by the payload and the remaining local labels, is wavelength converted at the tuneable wavelength converter in order to be properly routed to the appropriate output port of the node through the AWG. It is worth noting that by using this approach, because a local label refers to one of the node's output ports, the number of correlators is reduced (i.e., it is equal to the number of output ports), and therefore, the size of the router is also reduced [19].

III. ECONOMICAL STUDY

The above section described several node architectures. In this section, their building costs are summarized. Because all architectures intend to switch at a packet-by-packet level, but each of them uses a different technology, the cost comparison is dependent on those parameters that are characteristic for each of the technologies. The total cost makes a distinction between the optical cost and the electronic cost. The optical cost of a node is the sum of component costs of the all-optical

TABLE I
COMPONENTS TO BUILD THE OPTICAL COST FUNCTION

Function	Description: Cost for a...	Number of FCC
$C_D(W)$	Demultiplexer with W channels	$W+1$
$C_T(W)$	TWC with output range W wavelengths	4
$C_{AWG}(W)$	$W \times W$ AWG	$2 \cdot W$
$C_{CO}(W)$	Coupler of W channels into 1	$W+1$
$C_M(W)$	Multiplexer with W input channels	$W+1$
$C_S(W)$	Splitter into W channels	$W+1$
C_{HP}	Header/ Payload Separation Circuit	4
C_L	Label Insertion Circuit	5
C_C	Clock recovery Circuit	6
$C_{LAG}(B)$	Local Address Generation for addresses with B bits	$3(B-1)+B(2^{B-1}+1)$
$C_{NLG}(B)$	New Label Generation for labels with B bits	$3(B-1+2^{B-1}-1)+6(B-1)(2^{B-1}-1)+3B$
$C_{AOLXG}(B)$	All-optical Comparator for B bits	$7B-3$
C_{FF}	All-optical Flip flop	7
$C_{Switch}(I,O)$	Switch with I inputs and O outputs	$I+O$
C_P	Single pulse generator	6
C_N	Optical Notch Filter	2
C_{amp}	Amplifier	2

TABLE II
PARAMETERS DESCRIBING THE COST FUNCTIONS

Name	Description
F	The number of fibers
W	The number of wavelengths in one fiber
P	The ratio between the optical cost for an FCC and the electronic cost for an OEO, thus $P = \text{Cost}_{\text{OEO}} / \text{Cost}_{\text{FCC}}$
B	The number of bits in a label
BR	Header bit rate

components to build the node. The electronic cost is the cost to do an OEO conversion. Both costs are calculated for each of the node architectures, but first, some necessary notations are introduced.

A. Notations

Before calculating costs, and more interestingly comparing them, all the individual used components need be defined (see the first two columns in Table I). Their optical cost will be expressed as a function of the parameters of Table II. The meaning of these parameters will become clear in the next section.

B. Optical Cost

To compare the optical cost of different node architectures, the number of fiber-to-chip couplings (FCCs) for each of the optical components in the node architectures is defined. The FCC is considered to be the assembly and packaging tasks. This choice is based on the assumption that packaging and, more specifically, the number of interconnections to the outer world dominate the cost of optical components. Due to that, cost improvement is possible by way of integration. A sum over all the components in the architecture gives the total number of FCCs for the specified architecture. Going into detail for the FCC counting would lead us far beyond the scope of this paper,

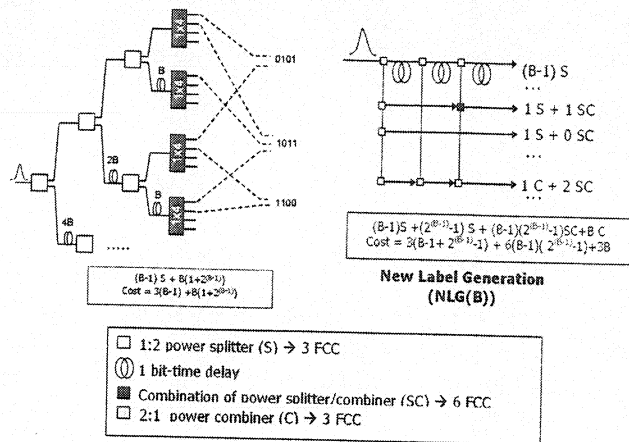


Fig. 4. Schematic of the LAG and NLG.

but the last column of Table I summarizes the cost functions (i.e., the cost as a function of the parameters of Table II).

For the all-optical nodes, the FCC counting for the new label generation (NLG), the local address generation (LAG) [$C_{NLG}(B)$ and $C_{LAG}(B)$], and the all-optical correlators ($C_{AOLXG}(B)$) are not clear at first glance. For the $C_{NLG}(B)$ and $C_{LAG}(B)$, the scheme from Fig. 4 is used. To count the number of FCCs for the $C_{NLG}(B)$, the number of couplers and splitters is counted. The number of splitters is defined by the number of bit sequences starting with a one (this is $2^{(B-1)}$ sequences for a B -bit pattern), which are the splitters counted in the vertical direction, increased by $B - 1$ splitters to split the original pulse (the splitters on the first row in the horizontal direction). The number of splitters, including a combiner to form the resulting label, is defined by the total number of ones in the 2^B sequences, of which each sequence is formed out of $B - 1$ bits [$(B - 1)2^{(B-1)}$ splitter/combiner combinations]. Fig. 4 shows that the last one in a column never needs a splitter because the pulse is not needed any lower, but it needs a combiner. This makes a total of $(B - 1) + 2^{(B-1)} - 1$ splitters, B combiners, and $(B - 1)(2^{(B-1)} - 1)$ splitter/combiner combinations.

The $C_{LAG}(B)$ is clarified as follows: The number of FCCs is again defined by the number of splitters and their size in this network of delay lines and splitters. At first, $B - 1$ 2:1 splitters are needed to form the B branches of the tree. Each edge has the appropriate delay to one of the bit positions in the final B -bit sequence. At the end of each edge, a 1:2 ($B-1$) splitter is needed. The size of this splitter is defined by the number of ones that can appear on this position (as there are 2^B sequences to be formed on half of the sequences, a one will be needed in this certain position).

To count the number of FCCs for the $C_{AOLXG}(B)$ in the nodes C and D, the scheme of Fig. 5 is used. The bits from the local addresses are directly coming from the LAG (see Fig. 2). For each bit to compare, a Mach-Zehnder interferometer (MZI), counting four FCCs, is needed. To bring on the bits from the incoming label, the label needs splitting. The component to do this requires $B - 1$ splitters. This makes a total of $7B - 3$ FCCs.

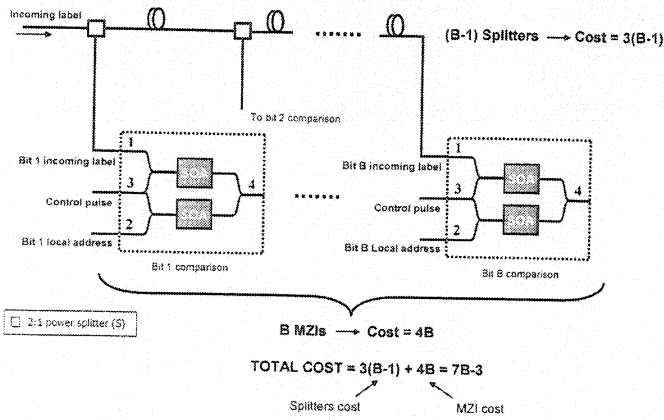


Fig. 5. Schematic of the AOLXG.

TABLE III
DIFFERENT COST FUNCTIONS FOR THE STUDIED NODE STRUCTURES

Node architecture	Optical Cost in number of FCC
All-optical label swapping node	$F \cdot C_M(W) + F \cdot W [C_C + C_{HP} + 3 \cdot C_S(2) + C_P + 3 \cdot C_S(2^B) + C_{Amp} + C_{LAG}(B) + C_{Switch}(2^B \cdot 2^B) + 2^B \cdot C_{AOLXG}(B) + 2 \cdot 2^B \cdot C_S(2) + C_{Switch}(2^B \cdot 2^B) + C_{NLG}(B) + C_{Co}(2^B) + C_L + C_T(W) + C_N + 2^B \cdot C_{FF} + C_{Co}(2^B)] + F \cdot C_{AWG}(W) + F \cdot C_D(W)$
All-optical label stripping node	$F \cdot C_M(W) + F \cdot W [C_C + C_{HP} + C_P + 4 \cdot C_S(2^B) + C_{Amp} + C_{LAG}(B) + 2^B \cdot C_{AOLXG}(B) + C_S(3) + 2 \cdot C_S(2) + C_T(W) + C_N + 2^B \cdot C_{FF} + C_{Co}(2^B)] + F \cdot C_{AWG}(W) + F \cdot C_D(W)$
NEHP	$F \cdot C_D(W) + F \cdot W \cdot C_T(W) + W \cdot C_{AWG}(F) - F \cdot C_{Co}(W) + W \cdot C_{Switch}(F \cdot F) + F \cdot W \cdot C_S(2) + F \cdot W \cdot C_L$

Starting from the individual cost functions, the optical cost functions of the (all-) optical nodes can be built. This technique is also used in [20]. Going through the architecture figures (Figs. 1–3) from left to right, the number of components is counted. Additionally, the values of the parameters used in the cost function are defined. For example, the all-optical swapping node (Fig. 2) has, from right to left, F demultiplexers with W wavelengths [$F \cdot C_M(W)$] and then, $F \cdot W$ AOLXG blocks, each comprising one clock recovery circuit (C_C), and one header/payload separation circuit (C_{HP}) etc. The complete results are noted in Table III. The optical cost function of the NEHP includes more than the components depicted in Fig. 1; it also has a label-insertion block for all wavelengths and a 1:2 splitter to split the incoming packet power to the electronic part of the node where the header is examined and to the optical plane, which is depicted in the figure.

C. Electronic Cost

The electronic cost of a node counts the number of OEO conversion circuits necessary in the node. A reference of one is assumed to be set to the cost of one OEO conversion at a BR of 155 Mb/s (i.e., one OEO costs P with the definition of Table II). For higher BRs, the cost is defined according to the following relation [9]:

$$\text{Bit rate} \times 4 \rightarrow \text{Cost} \times 2.5. \quad (1)$$

TABLE IV
TOTAL COST FUNCTIONS FOR THE DIFFERENT NODES

Node	Cost Function (in number of FCC)
IP over WDM	$P \cdot F \cdot W \cdot C_{BR}$
NEHP	$2 \cdot F + 15 \cdot F \cdot W + W \cdot F^2 + P \cdot F \cdot W \cdot C_{BR}$
Label swapping node	$F(2 + 48 \cdot W + 21 \cdot W \cdot 2^{(B-1)} \cdot B + 27 \cdot W \cdot 2^{(B-1)} + 4 \cdot W \cdot B)$
Label stripping node	$F(2 + 42 \cdot W + 15 \cdot W \cdot B \cdot 2^{(B-1)} + 9 \cdot W \cdot 2^B + 4 \cdot W \cdot B)$

D. Total Cost

The total cost for the different nodes comprises an optical part and an electronic part. Entering the expressions of Table I in the above cost functions, we find the cost functions in terms of the parameters from Table II. The results are collected in Table IV.

E. Costs Comparison

1) *Parameter P*: A comparison of the general cost functions from Table IV shows that the share taken by the optical cost in the total cost depends heavily on the node architecture. It changes from 100% in the all-optical approaches to 0% in the IP-over-WDM nodes. For the NEHP, the percentage of the optical cost is influenced by the parameter P . P is used to count the optical and electronic cost together. At 155 Mb/s, $1/P$ is the cost for one FCC so that two cost functions of two compared nodes have the same value. The percentage of the optical cost in the NEHP can be expressed as follows:

Percentage of the optical cost

$$= \frac{2 \cdot F + 15 \cdot F \cdot W + W \cdot F^2}{2 \cdot F + 15 \cdot F \cdot W + W \cdot F^2 + P \cdot F \cdot W \cdot C_{BR}} \quad (2)$$

2) *General Trends*: The major drawback of all-optical architectures is that for each possible incoming label, a separated hardware component is needed, resulting in hardly scalable switches. According to Van Caenegem *et al.* [19], label stripping could bring in a solution because the dimensions of the AOLXG switch are exponentially dependent on the parameter B . Routing by the use of label stripping decreases the number of bits in a label and, thus, the number of components needed. The results from [19] are confirmed by the cost functions in Table IV. Fig. 6 depicts a comparison of the cost for all-optical nodes to the NEHP and the IP-over-WDM node.

Fig. 6 represents the costs as a function of the parameter P . Of most importance in these graphs are the intersections of the cost for the all-optical nodes with the NEHP or the cost for IP-over-WDM architectures. They will be discussed further in this paper. In Fig. 6, $F = 4$, and $W = 32$. In each of the graphs, the cost function for the NEHP and the IP-over-WDM nodes are set out for different values of BR. Note that for the label stripping, the label length is only 3 bits, whereas for label swapping, it should be 8 bits.

The intersection values of P are different for all kinds of node combinations. As the BR increases, the OEO conversions become more costly, and it is thus no coincidence seeing the intersection value of P increase with decreasing BR. Although

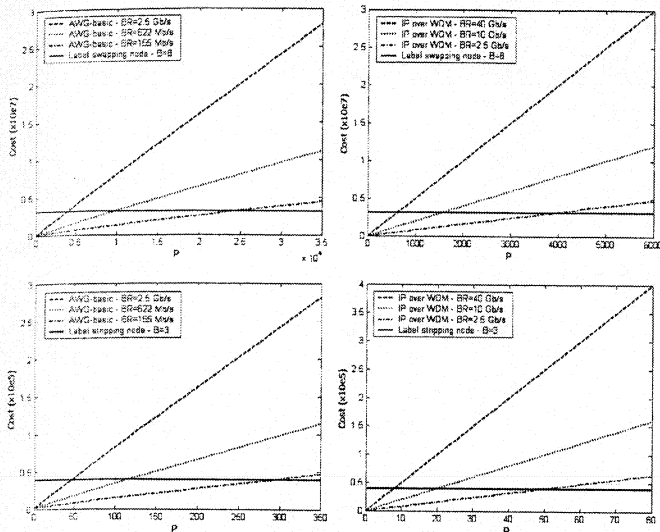


Fig. 6. Cost comparison of all-optical nodes and the NEHP and IP-over-WDM architecture for the parameters $F = 4$, $W = 32$, B , and BR dependent on the situation.

TABLE V
INTERSECTION VALUES p FOR P IN THE CASE STUDY [$F = 4$, $W = 32$, $B = 8$ (LABEL SWAPPING), $B = 3$ (LABEL STRIPPING)]

F=4, W=32	BR=155 Mb/s	BR=622 Mb/s	BR=2.5 Gb/s	BR=10 Gb/s	BR=40 Gb/s
Label swapping – IP over WDM			4006.4	1602.5	641.02
Label stripping – IP over WDM			48.97	19.58	7.83
Label swapping – NEHP	25021	10008	4003		
Label stripping – NEHP	287	114.8	45.9		

the label-length difference is very important in the final cost value of an all-optical node, also, the smaller nature of the label-stripping cost function (no need for an NLG and insertion circuit in the node architecture) contributes to the smaller intersection values of P , which is called p .

The intersection values of P are of most importance for the interpretation of the cost functions and especially the comparison of the cost for different nodes. The intersection points refer to the value of P for which the optical cost of the all-optical node becomes equal to the optical + electronic cost of the NEHP or the IP-over-WDM node. For values of P lower than the value p ($P < p$), the NEHP, or IP-over-WDM node is more beneficial in terms of FCC. For P bigger than the value p ($P > p$), the all-optical approaches become beneficial.

In Table V, the intersection values for P are collected. The values for IP-over-WDM nodes with BRs at 155 and 622 Mb/s are not calculated because this is not in use. It is the same for the NEHP. A 2.5-Gb/s header BR is already very fast. These intersection values clearly show the influence of the relation (1), which was for the OEO cost, e.g., the ratio between the intersection points of BR = 155 Mb/s and BR = 622 Mb/s for the label swapping and NEHP is $25\,021/10\,008 = 2.5$.

TABLE VI
INTERSECTION PERCENTAGES IN THE CASE STUDY [$F = 4$, $W = 32$, $B = 8$ (LABEL SWAPPING), $B = 3$ (LABEL STRIPPING)]

F=4, W=32	BR=155 Mb/s	BR=622 Mb/s	BR=2.5 Gb/s
Label swapping – NEHP	0.03221%	0.03221%	0.03222%
Label stripping – NEHP	2.73247%	2.73247%	2.73363%

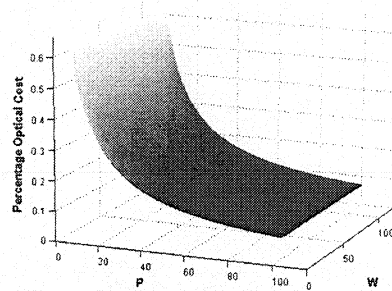


Fig. 7. W and P dependence of the percentage.

With (2) and the value ranges for P , the percentage the optical cost takes from the total cost in the cost function for the NEHP can be defined. By the use of the values from Table V, it is also possible to calculate the turning point, i.e., the value of the percentage from which the all-optical approaches become cost beneficial.

Table VI shows that the intersection percentages are quite small and independent of the header BR. These small percentages indicate that the all-optical approaches only are beneficial if the cost for optical components becomes very cheap compared to the cost for electronic components with the same functionality. In fact, they say that, from the point the optical cost in the total cost of NEHP becomes only 2.7% of the total cost, it is more beneficial to use an all-optical node based on label stripping, assuming that this node is made out of the same optical technology. In fact, the percentages show the ratio between the optical cost in the NEHP and the all-optical cost of the all-optical nodes.

Equation (2) shows that the percentage in optical cost is independent of the header BR and only slightly dependent on the number of fibers (F). Fig. 7 shows hardly any W dependence in the percentage using (2). Over and over, the main influencing parameter is the parameter P . Thus, to get any grip on all-optical nodes and their relation to other OPS nodes, a good understanding of the optical technology is needed so that a cost reduction of the components can be targeted.

F. Integration Evolution Impact on the Node Cost

The evolution and improvement of the integration degree of optical components is a key factor in the total cost of an all-optical node. If it would be possible to integrate a number of components while reducing the number of FCCs, the intersection value p will decrease. This issue has a special importance in the LASAGNE node architecture, which uses a semiconductor optical amplifier (SOA) MZI as the main building block to implement the label-switching functionalities.

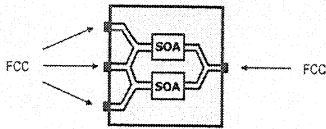


Fig. 8. Number of FCCs in an SOA MZI device.

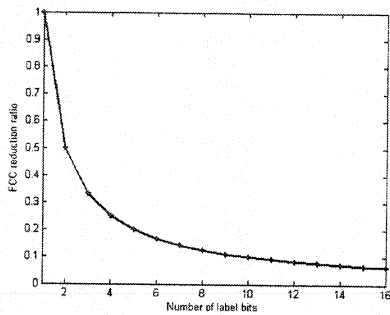


Fig. 9. Impact of integration on the cost in the LASAGNE node.

An example enlightens how the integration impacts on the cost of a node. It focuses on the label comparison block of the LASAGNE node. This entity is composed by L branches of B -cascaded SOA MZIs (i.e., one AOLXG per branch). B is the number of label bits and $L = 2^B$ the number of possible labels using B bits. For example, in the case of a 2-bit label, two SOA MZIs per branch are required, and the total number of branches is four.

Taking into account that the FCC cost for a single SOA MZI is four (see Fig. 8), the total number of FCCs for the AOLXGs without any further integration is

$$\text{FCCs (low integration)} = (B \times 4) \times L = 32. \quad (3)$$

In the case of a high integration level, all the cascaded SOA MZIs are collected into one single chip, and the total cost of one AOLXG would only be four FCCs (i.e., this is the cost per branch); then, the total number of FCCs of all the AOLXGs would be

$$\text{FCCs (high integration)} = 4 \times L = 16. \quad (4)$$

The ratio between low and high integration costs is

$$\text{Ratio} = \frac{\text{FCCs (high integration)}}{\text{FCCs (low integration)}} = \frac{1}{B} = \frac{16}{32} = 0.5. \quad (5)$$

The cost in number of FCCs is reduced to half. Fig. 9 shows that the cost-reduction evolution is inversely proportional to the number of label bits. These results make clear how improvements on the integration degree of SOA MZIs on a single chip would result in huge reduction in the optical cost of active components, bringing closer the all-optical concept.

Generally, signals are routed based on wavelength, intensity, or polarization. AWGs and power splitters are examples of components with passive functions. It is well known that (even without integration) the cost of active components is higher than those of passive components.

Recent developments [21] provide a preview of how optics can be less expensive: through miniaturization and integration. Those approaches make it easier to mass produce the optical

devices themselves, reducing the cost of packaging, which is often the most expensive aspect of an optical component, and, at the same time, improving unit-to-unit uniformity. Monolithic as well as hybrid integration of passive and active optical components are being deeply investigated (e.g., FP6 IST-MUFINS project and FP6 NoE ePIXnet, respectively) and have become a crucial point to reduce costs.

IV. CONCLUSION

This paper assessed the cost of different OPS node architectures. The optical cost functions were based on the hypothesis that packaging and, more specifically, the number of interconnections to the outer world dominate the cost of optical components. The study compared the optical cost to the number of OEO conversions as a measure for the electronic cost. Although the need for all-optical routers increases because of the increasing chasm between the fiber data speed and the current electronic router speed, this paper shows that the introduction of all-optical nodes will not take place in the very near future. Not only does the node suffer from the lack of all-optical memory, making it hardly scalable, but it also needs a huge reduction of the cost for optical components to make it competitive with the current OPS nodes. Packet routing based on label stripping forms a good solution to accelerate the possible introduction of all-optical nodes, although higher integration levels will also be crucial.

ACKNOWLEDGMENT

The authors would like to thank all the people involved in the LASAGNE project.

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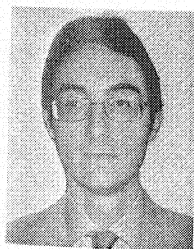
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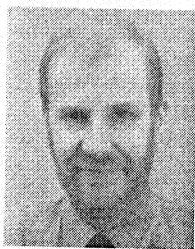


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