Design of a low-voltage op-amp-less ASDM to linearise VCO-ADC

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REFERENCES

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Design of a low-voltage op-amp-less ASDM to linearise VCO-ADC

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We present a very simple ASDM design for linearization of VCO ADC's. The circuit only consists of a passive feedback filter and a schmitt trigger. By proper sizing, the nonlinearity error can be reduced to well below 0.12% for input signals that go almost rail-to-rail. The design has been manufactured in the low power version of TSMC 65nm technology and was measured at a 1V power supply.

Introduction: VCO based Analog to Digital conversion allows easy implementation of noise shaping A/D conversion [1–6]. However, in a straightforward implementation of such a VCO ADC, the overall linearity will be limited by the linearity of the VCO, which typically will not be good enough. A potential solution is to convert the input voltage into a two-level signal where the information is stored in the duty cycle of the resulting square-wave using an Asynchronous Sigma Delta Modulator (ASDM) or a Pulse Width Modulator (PWM). This method is known as 'PWM pre-coding' [4–6]. Untill now all reported implementations either require an op-amp, a highly linear ramp source, or a linear gm cell [5–7]. In practice such high-performance analog circuits are difficult to implement at today's low supply voltages (of the order of 1 Volt) and hence are to be avoided. An alternative would be an ASDM with a passive RC loop filter [4, 8, 9]. However, it is not obvious how such a passive ASDM should be designed as to achieve simultaneously high bandwidth and good good linearity. For this reason, untill now, such a circuit has not yet been demonstrated in practice. In this letter, we explain how such a passive ASDM linearization of a VCO can be designed to achieve good overall performance. The validity is confirmed by measurements on a protoype implemented in a 65nm technology.

Passive ASDM: The structure of the passive ASDM, is shown in Fig. 1.a. The key element is that the linear loop filter $F(j\omega)$ should be passive. A potential implementation is shown in Fig. 1.b. Here, the linear loop filter $F(j\omega)$ equals $F(j\omega) = 1/[2(1 + j\omega\tau)]$ with $\tau = RC/2$.

The input signal V in the diagram of Fig. 1.a is symmetrical around 0 and is also normalized toward the full scale amplitude. Hence, the input signal V_{in} of the circuit of Fig. 1.b is related to the signal V in Fig. 1.a by the following relationship: $V = 2V_{in}/V_{dd} - 1$

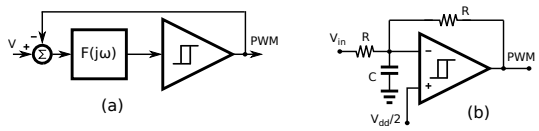

Fig. 1. Passive ASDM: (a) block diagram and (b) circuit.

By proper sizing of the Schmitt Trigger's delay and/or hysteresis width, the ASDM can be forced to oscillate at a desired oscillation frequency $f_P = \omega_P/(2\pi)$. This oscillation frequency should always be sufficiently higher than the relevant system bandwidth.

To obtain good performance both τ and ω_P should be carefully chosen. A first consideration is the nonlinear distortion, for which expressions were derived in [8, 9]. A complication here, is that this distortion depends on the gain of the filter F and hence might vary over the signal band. However, the problem can be greatly simplified by observing that the input referred noise of the Schmitt Trigger is also inversely proportional to the gain of the filter F. This means that the effect of comparator noise spectral components that are above the filter cut off frequency $(1/(2\pi\tau))$ will be significantly increased. Since this is not tolerable in the usefull signal band, this implies that the filter cut off frequency should not be smaller than the usefull signal bandwidth. When we take this into account, the filter F must have a flat gain over the signal band and the expressions of [8, 9] are significantly simplified. In particular the expression for the signal band component PWM_{LF} of the PWM signal simplifies into:

$$PWM_{LF} \approx v - \frac{\pi^2}{6}\frac{v}{1-v^2}\frac{1}{1+(\tau\,\omega_P)^2} \qquad (1)$$

For the case that the input signal is a sine, the expression for the distortion [8, eq.23] (dominated by the 3rd harmonic) becomes:

$$THD \approx -20\log\left(\frac{\pi^2}{6A^4(1+(\tau\,\omega_P)^2)}\left(2A^2 - 8 - \frac{6A^2-8}{\sqrt{1-A^2}}\right)\right) \qquad (2)$$

From this equation, it is clear that the ASDM performance is a strong function of the desired input range and of the ASDM oscillation frequency ω_P. Based on these considerations, we come to the following design flow. First, size the filter time constant τ such that it corresponds to the desired signal bandwidth. Second, decide the input signal range. And third, decide the desired self-oscillation frequency based on the nonlinearity by evaluating Eq. (2). In the circuit that we implemented, we aimed for a 10MHz bandwidth, and a usefull signal range of 750mV$_{pp}$ at a 1V supply voltage. Then we need an oscillation frequency of about 300 MHz to achieve a distortion performance of 65dB.

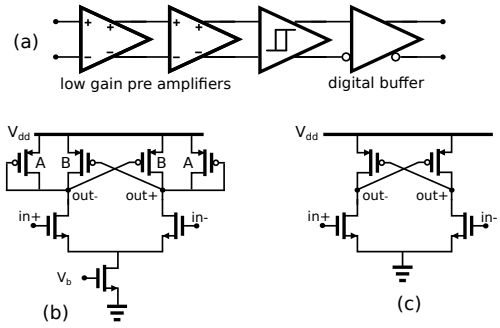

Fig. 2 *(a) Overall Schmitt Trigger structure, (b) schematic of the Pre amplifier, which (apart from the sizing) is identical to the Schmitt Trigger's schematic and (c) the digital buffer circuit*

Circuit design: We implemented a differential version of the conceptual circuit of Fig. 1. If we assume that the circuit's delay is negligible, the Schmitt Trigger hysteresis width should be as low as 46mV (differentially), to achieve an oscillation frequency of 300MHz at a 1V supply voltage and a filter bandwidth of 10MHz. To obtain such a low hysteresis width in a controlled way, we added two pre-amplifier stages with a controlled gain to the actual Schmitt Trigger (as shown in Fig. 2.a). The pre amplifier schematic is shown in Fig. 2.b. It consists of a simple NMOS differential pair with a combination of diode-connected and cross-coupled PMOS load transistors. Here, the weight A of the diode-connected PMOS is larger than the the weight B of the cross-coupled PMOS. The ratio A/B then sets the gain. The actual Schmitt trigger schematic is identical to Fig. 2.b, except that now the weight B of the cross-coupled PMOS is larger than the weight A of the diode-connected PMOS load transistors. In this case, the ratio A/B sets the hysteresis width. Finally a digital buffer (Fig. 2.c) is added to drive the resistors. All these stages consist of maximum three stacked transistors, and hence are suitable for low voltage designs.

After the first design iteration, it turned out that the circuit's delay (mostly due to the schmitt trigger) was not negligible and resulted in a too low oscillation frequency. It was also shown in [9] that loop delay will not ruin the performance of the ASDM, as long as it is (roughly) estimated, taken into account, and eventually compensated by choosing a hysteresis width of the schmitt trigger. In this case the actual circuit was implemented with a hysteresis width of 20mV and a delay of about 0.4ns.

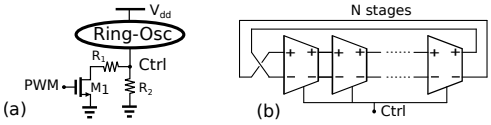

Fig. 3. Two-level Ring oscillator: (a) input circuit, (b) actual ring.

Two level ring VCO: The VCO only has to operate at the two PWM levels. This is implemented by the circuit of Fig. 3a. The two-level PWM signal drives a switch, M_1 in series with a resistor, R_1. The two resistors, R_1 and R_2, allow to control the two frequencies at which the VCO will oscillate. For the actual ring, any form of current starved Ring Oscillator

(see Fig. 3.b) could be used. In this work we used a design with the same delay cell as in [1]. By turning the transistor M_1 off and on, the VCO oscillates at a low frequency, f_1 and a high frequency f_2 respectively. The average of the two, and their difference, determine the carrier frequency f_c and tuning range f_{tune} of the VCO. In theory, the best VCO ADC performance is achieved by setting the f_1 equal to zero [2]. However, it was found that this extreme gives additional switching noise [5]. Therefore in this work we set f_1 to approximately half f_2.

If the ASDM is implemented differentially, the two ASDM outputs can drive two pseudo differential VCOs. But unlike [1], the proposed technique is also effective in the single-ended configuration of Fig. 1.

Measurement Results: The proposed circuit was implemented for a 1V supply in the low power (high threshold) flavour of a 65nm CMOS technology (on a die with other test circuitry). The ASDM was sized with a filter bandwith of 10MHz and an oscillation frequency of 300MHz. The VCO was a RO (Fig. 3) with 18 stages. In the input network, the resistor R_2 was sized $2k\Omega$ and the series connection of R_1 and M_1 was sized for the same value. The corresponding 2 VCO frequencies are around 350MHz and 175MHz. The test chip was actually differential (i.e. a fully differential ASDM with 2 VCO's in a pseudo differential configuration). However, due to limitations on the test chip the output of only 1 of the VCOs was accessible. Moreover of this single VCO, only one of the 18 phases was accessible. Due to this, the measurement results are read out single-ended and are also reported as a single-ended measurement. For quantitative evaluation, the available VCO output signal was sampled with a 10GS/s sampling oscilloscope, converted into a bitstream and differentiated digitally. This way, we obtain a configuration that is similar to an actual (single-ended) linearized VCO-ADC with first order noise shaping (only with reduced performance because we are only using 1 out of the 18 phases) [2]. With this set-up, the proposed ASDM is measured together with the VCO, and hence, both the linearity of the PWM can be determined, and the effectiveness of this linearisation method.

In a first experiment, the (static) voltage to frequency conversion curve of the ASDM-VCO was measured and is shown in Fig. 4(left) Bear in mind that in reality the VCO is switching between two frequencies (around 175MHz and 350MHz) and the plot actually shows the average frequency of the VCO (averaged over a long time). Clearly, the curve is visually linear. The deviation of this curve from a best fit line (the nonlinearity error) is shown in Fig. 4(right), where also the prediction of the nonlinearity according to Eq. (1) is shown. It is clear that the measured curve resembles the prediction. However, some even distortion is visible. This is attributed to unequal rise and fall times in the PWM signal, and would probably disappear in a fully differential setup. Still, over a near rail-to-rail signal range (50mV-950mV) the nonlinearity is well within ± 0.2MHz, corresponding to 0.12% of the full scale (of 175MHz).

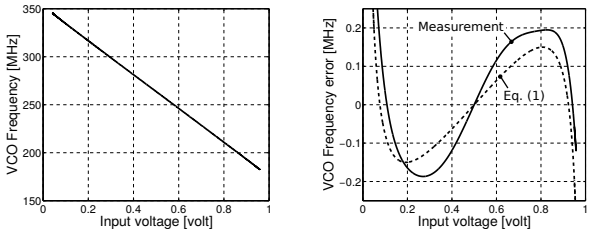

Fig. 4. I/O and nonlinearity plots.

In another measurement, the circuit was driven with a 550mV_{pp}, 100kHz input sine wave. The corresponding output spectrum is shown in Fig. 5. This is about -5dB below the absolute maximum signal level which whould be 1V_{pp}. The dominant harmonic is the third at -63dBc, which is adequate for several applications. The high frequency noise roll off of 6dB/octave corresponds to the expected first order noise shaping. In this measurement, this noise contribution already dominates above a few MHz, but as explained above, this is due to the fact that only 1 of the 18 VCO phases is used here. Finally, there is a white noise floor (related to circuit's thermal noise). For this case, the SNR and SNDR over a bandwidth of 2MHz were equal to 69dB and 61dB respectively.

The measurement of Fig. 5 was repeated for a range of input amplitudes and based on that a SNR-SNDR plot was drawn, for the case of a bandwidth of 2MHz. The theoretical prediction of the SNDR based on the expression for the distortion of Eq. (2) is shown as well. It is clear

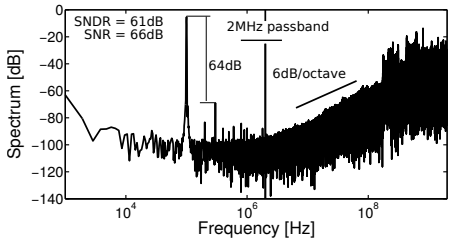

Fig. 5 *Output spectrum of the linearized VCO for a 550mV_{pp} 100kHz input signal.*

that the circuit is only limited by the inherent ASDM distortion only at very high signal levels.

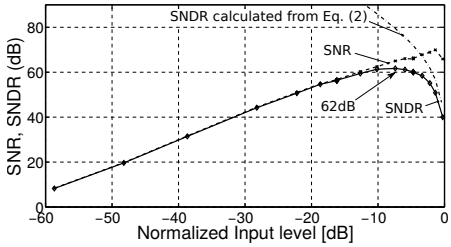

Fig. 6. SNR and SNDR vs. the normalized rail to rail input level (of 1 Vpp).

The entire (fully differential) ASDM consumes only $240\mu W$. The power consumption of 1 VCO channel is $500\mu W$. Hence, in a fully differential configuration the power overhead of the ASDM is modest. On the other hand there is a noise penalty (e.g. compared to [1], which comes from two sources: first the ASDM adds noise, and second the VCO full swing is reduced. The silicon area occupied by the PWM is $50\mu m \times 130\mu m$ and $60\mu m \times 25\mu m$ for a single VCO channel.

Conclusion: We present the design of a passive ASDM to linearize VCO ADC's. The key elements are a suitable selection of the filter time constant and the oscillation frequency. The approach is illustrated by a prototype design in 65nm CMOS which demonstrates a nonlinearity error which is below 0.12% for a near rail-to-rail input signal.

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