Deep Level Transient Spectroscopy measurements on Mo/Cu(In,Ga)Se_2/metal structure

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Abstract

In thin-film Cu(In,Ga)Se_2 (CIGS) solar cells a large number of intrinsic defect types are possible in the chalcopyrite structure and can influence the efficiency of the solar cell. Defect characterization is therefore essential. In this study Deep Level Transient Spectroscopy (DLTS) is used as an electrical defect characterization technique. The detection of defect related signals might be hindered by signals originating from barriers caused by the multi-layer structure and by a possible type inversion layer at the interface. To investigate to which extent the DLTS signals effectively arise from the CIGS absorber, solar cells are simplified to a metal/semiconductor/metal structures. This was done by etching away the buffer and window layer and subsequent metal evaporation. In this way structures closer to those normally measured in DLTS are obtained. Additional etches targeted at thinning the absorber layer and/or removing oxidation layers are also performed. In general very similar DLTS signals are recorded for complete cells and M/S/M structures before and after additional etches.

Keywords: CIGS thin-film solar cells, capacitance spectroscopy, Schottky contacts, deep-level defects

1. Introduction

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In (thin-film) solar cells recombination via (deep-level) defects will limit the conversion efficiency by reduction of V_{OC}. Therefore defect analysis is crucial to further improve the cell efficiency [1]. Information on the characteristics of deep level defects in a semiconductor can be obtained via Deep Level Transient Spectroscopy (DLTS). The interpretation of the DLTS signals on a $Cu(In,Ga)Se_2$ (CIGS) thin-film hetero junction solar cell is, however, not straightforward because of three reasons.

First, the defect structure is complex because a large number of intrinsic point defects and, complexes of these, are possible. Many of these defects have low formation energy [1, 2].

Second, as the ZnO/CdS/CIGS/Mo thin-film solar cell is a multilayer structure, the system is far more complicated than the 'ordinary' metal-semiconductor contacts on which the DLTS spectroscopy technique is normally applied. That the interpretation of the DLTS signals becomes therefore non straightforward, is demonstrated by the discussion about the origin of the two signals generally seen in the DLTS spectra of CIGS solar cells. The first signal, often labelled N1, appears at low temperature (T $<$ 150 K) and its DTLS signal after pulses with V_r, $V_p < 0$ (V_r reverse bias, V_p pulse bias) appears with a sign opposite to that expected for majority carrier traps in a bulk semiconductor. Its peculiar properties in DLTS and admittance spectroscopy have been the source of a long debate about its origin [3, 4, 5, 6, 7, 8, 9]. The signal has been interpreted as a bulk acceptor, interface defects, hopping conduction freeze out and non-ideality at the back contact. Concerning the latter assignation, we recently showed that the DLTS signal of a non-ideal Ohmic contact exhibits certain characteristics which allows to distinguish it from that of defects. In this paper the discussion on the origin of the N1 signal will not be pursued. We merely mention that in all spectra presented the low temperature signals have been checked to exhibit the characteristics of a non-ideal contact. For some of the cells taken up in this study, this has been discussed in more detail in reference [9].

Near room temperature (250-350 K), a second signal is commonly observed in the DLTS spectra. This signal is often labelled N2 and does have the sign expected for emission from a majority carrier trap. For this reason it has been most often assigned to bulk defects in the CIGS layer [1]. A third complication in the interpretation of DLTS measurements that the band diagram at the absorber surface can be altered by a type inversion layer or by an thin oxide layer between absorber and buffer. Different models exist for the type inversion layer; it can be formed by a Cu depleted surface which leads to a $CuIn_3Se_5$ phase [10] or by a Se depleted surface [11]. In alternative models Cu^+ ions diffuse towards the bulk and V_{Se} surface states cause a band bending [12] or Cd-diffusion during the chemical bath deposition (CBD) of CdS causes the n-type layer at the surface [13, 14]. The exact nature of the electronic junction remains under debate.

In this work we aim to eliminate the mentioned problems for the interpretation of the DLTS signals. The first problem cannot be overcome as the defect structure is intrinsic and can not be changed. However the other reasons can, at least in a part, be avoided or altered.

First, to get rid of the multiple layer structure a simplification to a metal/semiconductor/metal (M/S/M) structure was performed. Second to asses the effect of a type inversion layer or oxidation layer near the absorber/buffer interface, additional Br and HF etches were performed. Different metals on cells with originally different buffer layers (CdS and In_2S_3) were tested.

Similar M/S/M structures have been studied before using admittance spectroscopy [7]. It was found that the admittance responses of cells with different buffer layers and M/S/M structures were similar, despite the strongly modified interface properties. Based on these results the N1 response was attributed to a non-ideality of the back contact by these authors. The DLTS investigations presented here yields remarkably similar results, not only for the low temperature part of the spectrum, but also for the signals(s) near room temperature.

2. Experimental

The CIGS solar cells were fabricated at EMPA (Swiss Federal Laboratories for Materials Science and Technology). The absorber layers were produced by a three stage co-evaporation process on Mo coated soda lime glass substrates. The In_2S_3 buffer layer was deposited by ultrasonic spray pyrolysis [15], the CdS buffer by CBD [16]. On top of the buffer layer an i-ZnO/ZnO:Al window layer and Ni/Al grid were deposited.

To remove the grid, window and buffer layer a short HCl (10 % in H_2O) etch was performed, after which the samples were rinsed with methanol and deionized water. No traces of Cd or S could be detected by Energy Dispersive X-ray (EDX) measurements after the etch. On the bare absorber layer three different metals (Au, Al and In) were vacuum evaporated to form a Schottky contact with the p-type absorber. The area of the circular rectifying contacts was 3.14 $\cdot 10^{-2}$ cm^2. Complete cells with In_2S_3 and CdS buffer are labelled as $\text{cell}_{In_2S_3}$ and cell_{CdS} respectively. The etched cells with different metal contact (metal= Au, Al, In) are labeled as $\text{metal}_{In_2S_3}$ or metal_{CdS}. To thin the absorber layer in the Mo/CIGS structure an etching from the top was performed using a 0.1 vol% bromine in methanol solution during 35 minutes. After the metal (Au or Al) evaporation, the samples are labelled as $\text{metal}_{BR\text{-}CdS}$. To remove a possible oxide layer, an HF etch ($HF/HNO_3/H_2O$ (1:1:4)) was performed (20 s) after the HCl etch.

Temperature dependent DLTS measurements were performed using a Phystech Fourier Transform-DLTS setup (Phystech FT1030) in combination with a Boonton 72B capacitance bridge. The a. c. test signal has a fixed frequency of 1 MHz. Temperature scans were made between 10 K or 70 K and 300 K. Before starting the DLTS measurements, the solar cells were kept in the dark during at least 1 h at room temperature in order to bring them into the relaxed state.

In DLTS the capacitance is measured at a bias of V_r during a time t_w (window time) after a bias pulse of V_p was applied during t_p (filling time). Conventional pulses ($V_r < V_p < 0$), which measure the emission transient for majority carrier traps, and complementary pulses ($V_p < V_r < 0$) which measure their capture transients, were applied. We adopt as convention that an increasing capacitance transient ΔC (emission from majority carrier trap) is labelled as positive: $C(t) = C_r - \Delta C \exp(-t/\tau)$, with τ the time constant.

For Scanning Electron Microscopy measurements (SEM) a FEI Quanta 200F FEG-SEM was used. For EDX analysis a FEI Quanta 200 instrument, equipped with EDAX Genesys 4000 setup was used. The acceleration voltage was 15 kV. The characteristic X-rays of Cu_K, Se_L, In_L and Ga_L were monitored.

3. Results and discussion

3.1. Barrier height and shunt resistance

According to the Schottky model [17], the electronic transport across the metal semiconductor interface is controlled by the Schottky barrier height (ϕ_B). As this height is dependent on the work function of the metal (ϕ_M), several metals (Au, Al, In) with different work functions were evaporated on the CIGS surface in order to alter it. Reported work function values in the literature often cover a considerable range depending on the measurement method and surface cleanliness. This makes the calculation of the barrier height not unambiguous. Typical values for the work functions of the metals used here are: ϕ_{Au}: 5.10 - 5.47 eV, ϕ_{Al}: 4.06 - 4.26 and $\phi_{In} \sim 4.1$ eV [17, 18, 19]. Moreover in practice it appears difficult to alter the barrier height by using metals of varying work functions. Indeed, it turned out that imperfections at the semiconductor surface play an important role during the contact formation and influence the barrier height by Fermi level pinning [19, 20]. The latter appears to be confirmed in this work.

The I-V relationship for a Schottky contact, based on the thermionic emission current theory by Bethe, is given by [17] ($q\phi_B >> kT$)

$$I = I_s \left[\exp\left(\frac{qV}{nkT} \right) - 1 \right]$$

$$\text{with } I_s = A^* T^2 S^2 \exp\left(\frac{-q\phi_B}{kT}\right) \quad (1)$$

In the above equations q is the elementary charge, k is the Boltzmann constant, n the ideality factor, T is the absolute temperature, I_s is the saturation current, A^* the effective Richardson constant and S the diode area. The straight line intercept of the forward bias ln(I) vs V curve at zero bias gives the value of I_s, from which the barrier height can be calculated. Although the metal work functions vary by $\sim$ 1 eV, a barrier height between 650 and 800 meV was found for all samples. No further correlation between the barrier heights could be deduced, they appear to be sample dependent.

To determine the quality of the Schottky devices, the shunt resistance is determined by a linear fit for low (negative) voltages (figure 1, red solid line). The shunt resistance for Schottky device and cell are similar (in the order of 10^5 - 10^6 Ω): this shows that decent Shottky devices were obtained.

3.2. DLTS spectra

Figure 2 shows the DLTS spectra of $\text{cell}_{In_2S_3}$ and $\text{metal}_{In_2S_3}$ (metal= Au, Al, In). Experiment showed that the main features of the DLTS signals were not affected by the bias region (not shown here). In all spectra the low temperature (N1) signal appears around 120 K. At higher temperature (above 250K), the broad onset of a peak is seen in the spectra of $\text{In}_{In_2S_3}$, $\text{Au}_{In_2S_3}$ and $\text{cell}_{In_2S_3}$, exhibiting essentially the same characteristics for these three samples. A detailed analysis and interpretation of the high temperature signals for these cells and those with CdS buffer is difficult to make at this moment. Indeed, the maximum of the DLTS spectra does not appear in the measured temperature range. Moreover, in reference [21] it is demonstrated that correct interpretation of the transients with large time constants observed for CIGS cells at high temperature requires lengthy measurements since reproducibility can only be attained in a steady state regime. Such measurements are outside the scope of this paper. Therefore, we restrict ourselves here to comparing the qualitative features of the DLTS spectra of cells and Schottky diodes with different metals.

With this in mind, we found that only the $Al_{In_2S_3}$ sample yields deviant results (figure 2(b)): an extra component arises which exhibits a clear maximum in the range 250-300 K. It is tempting to relate this extra signal with Al diffusion in the absorber, but, as for identification of the other signals at high temperature, further investigation is necessary.

To test the effect of the buffer layer type and deposition technique, similar experiments were performed on a CIGS cell with CdS buffer layer. The spectra of $cell_{CdS}$ and Al_{CdS} look very similar (figure 3(a) and 3(b)): a signal at low temperature and the intense signal at high temperatures exhibits substructure for both samples. The results for Au_{CdS} were similar (not shown here). Hence, the intense high temperature DLTS signals cannot be directly related to the window and buffer layers (i. e. defects in these layers or at their interfaces).

The influence of a type-inversion layer near the surface was investigated by thinning the absorber further with a Br-methanol solution. SEM images in figure 4(a) confirm the thinning: the initial absorber layer thickness after HCl etch was 2.02 μm, the thickness after additional Br etching 1.58 μm. The surface of the Br etched sample is less rough. Such surface smoothening has been reported before [22] and it was shown that Br etching leads to a superficial Se^0 film formation on the CIGS surface. EDX measurements on a sample after HCl and Br etching cannot unambiguously confirm the small increase of the Se concentration at the surface (figure 4(b), left, blue curves). The measurements do however confirm an important qualitative change of the the Ga profile near the surface by the thinning: the double-graded Ga profile is no longer present. The composition changes near the surface hardly affect the DLTS spectra: the spectra after an additional Br etch (figure 3(c)) look very similar to those of the other samples (figures 3(a) and 3(b)). Essentially the same results are found for samples with Au contacts made from this cell and for thinning of M/S/M structures on cells with an In_2S_3 buffer layer. These experiments seem to rule out a possible influence a type inverted layer created by Cd diffusion on the

DLTS spectra, as Cd diffusion is expected to be limited to the first 10 nm [14].

In order to test whether an oxide layer on top of the absorber layer could influence DLTS signals, an HF etch after the HCl etch was performed. As the DLTS spectra of the cell and sample with additional HF etch again yield very similar spectra, also oxidation does not seem to have a strong effect on the DLTS signals.

4. Conclusion

Thin-film solar cells were simplified to M/S/M structures by chemical etching of the buffer and window layer, and vacuum evaporation of different metals on the CIGS absorber. In almost all cases the DLTS spectra of complete cells and of M/S/M samples are strikingly similar, even if the surface modification is enhanced by thinning the absorber layer - eliminating type inverted layers near the surface (Cd doping or ordered vacancy compounds) - or when an etching is performed targeted at removing surface oxide layers. All spectra exhibit one signal below 150 K and a signal at high temperature, possibly with substructure. For understanding the high temperature signals, further investigation will be necessary. Nonetheless, the present experiments already seem to exclude direct influences of the window and buffer layers, and of the special defect state of the absorber near its interface with the buffer. The results do not contradict an attribution to defects in the CIGS absorber bulk but also not conclusively confirm such identification. Understanding the reasons for the Fermi level pinning in the metal-CIGS Schottky diodes might be an element in the interpretation of these high temperature features.

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Figures

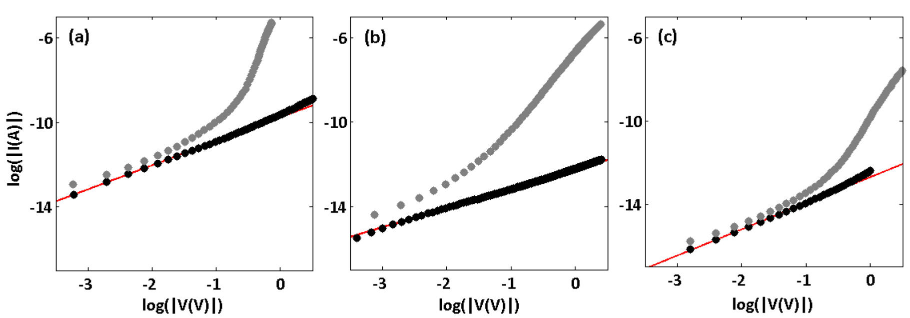
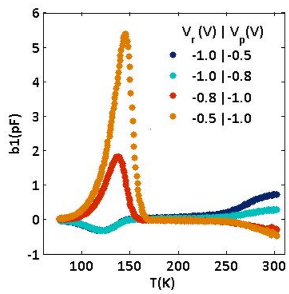
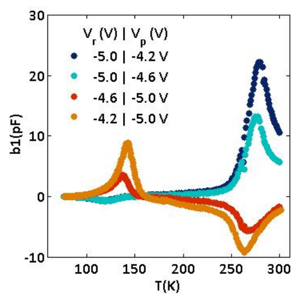


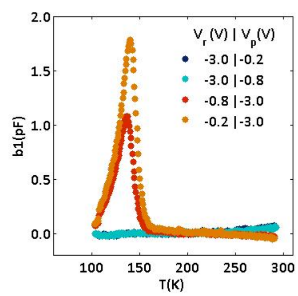
Figure 1: Shunt resistance determination of (a) $cell_{CdS}$, (b) Au_{CdS} and (c) $Al_{Br\text{-}CdS}$. Grey: forward bias, black: reverse bias, red: linear fit.



(a) $Au_{In_2S_3}$

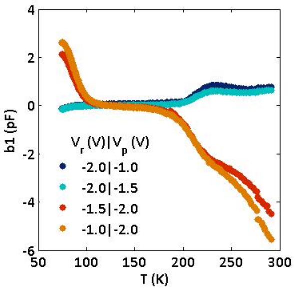


(b) $Al_{In_2S_3}$

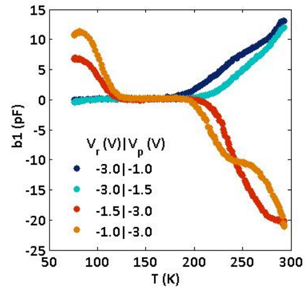


(c) $In_{In_2S_3}$

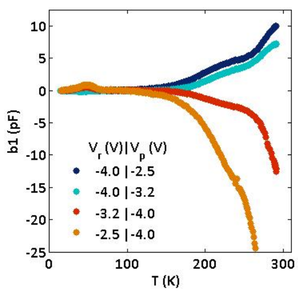
Figure 2: DLTS spectra t_w= 0.005 s, t_p= 0.050 s



(a) cell_{CdS}

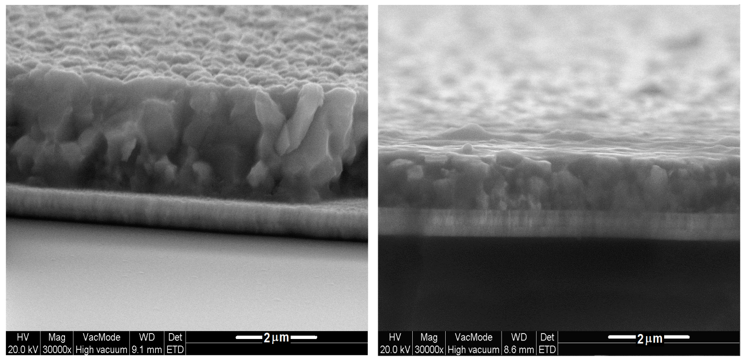


(b) Al_{CdS}

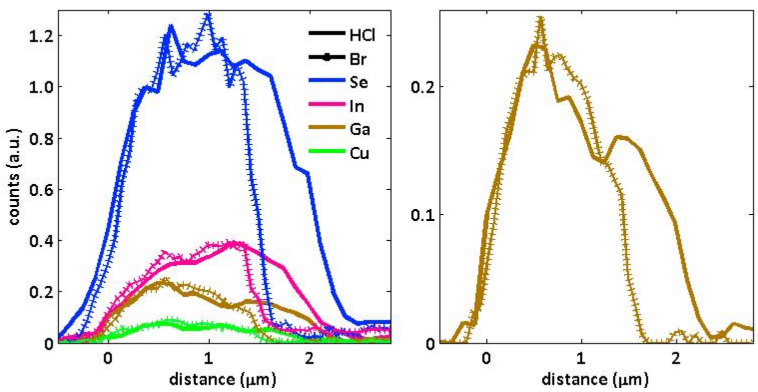


(c) $\text{Al}_{\text{Br-CdS}}$

Figure 3: DLTS spectra t_w= 0.005 s, t_p= 0.050 s



(a) SEM cross sections left: $cell_{CdS}$, right: $Au_{BR\text{-}CdS}$.



(b) EDX measurements of HCl (solid line) and Br etched (crossed line) samples.

Left: Cu, In, Ga and Se profiles. Right: Ga profiles

Figure 4