## Impact of firing on surface passivation of p-Si by $SiO_2/AI$ and $SiO_2/SiN_x/AI$ stacks

J. Chen<sup>\*,1,2</sup>, E. Cornagliotti <sup>3</sup>, X. Loozen <sup>3</sup>, E. Simoen <sup>3</sup>, J. Vanhellemont <sup>1</sup>, J. Lauwaert <sup>1</sup>, H. Vrielinck <sup>\*\*,1</sup> and J. Poortmans <sup>3</sup>

<sup>1</sup> Department of Solid State Sciences, Ghent University, Krijgslaan 281-S1, B-9000 Ghent, Belgium

<sup>2</sup> Institute of Applied Physics, Technische Universität Dresden, D-01062 Dresden, Germany

<sup>3</sup> Imec, Kapeldreef 75, B-3001 Leuven, Belgium

## Abstract

Firing impacts on surface passivation provided by SiO<sub>2</sub> and SiO<sub>2</sub>/SiN<sub>x</sub> stack with evaporated Al films are studied by capacitance-based techniques on MIS capacitors. For devices with insulator layers consisting solely of as-deposited SiO<sub>2</sub>, the densities of either interface states ( $D_{it}$ ) or fixed charges ( $Q_{fc}$ ) are hardly influenced by firing. Capping the SiO<sub>2</sub> layer with SiN<sub>x</sub> layer results in a shift of the peak activation energy of  $D_{it}$  towards the valence band ( $E_v$ ) of Si. Firing this SiO<sub>2</sub>/SiN<sub>x</sub> stack leads to an increase of  $Q_{fc}$ , a reduction of  $D_{it}$  and a moderate shift of peak activation energy of  $D_{it}$ towards  $E_v$ . And, co-firing with the Al film on top significantly reduces the  $Q_{fc}$ ,  $D_{it}$ and  $D_{it}$  peak activation energy, which is resulting from the atomic hydrogen passivation. These results are of particular interest for the development of solar cells with rear surface passivation and local contacts.

PACS 61.72.Mm; 72.20.-i; 72.80.Cw

Keywords crystalline silicon, surface passivation, firing, interface states

\* Corresponding author: e-mail jiahe\_chen@hotmail.com, Phone: +49 351 463 32459, Fax: +49 351 463 37060, currently with RENA Singapore and RENA China.

<sup>\*\*</sup> Postdoctoral Fellow of the Research Foundation Flanders (FWO-Vlaanderen)

Thermal SiO<sub>2</sub> is one of the obvious candidates for the surface passivation of both *n*- and *p*-type silicon of arbitrary doping level and is used in the record-efficiency passivated emitter and rear locally-diffused (PERL) crystalline silicon solar cell<sup>2</sup>. However, the use of a high quality thermal oxide would lead to a high cost of ownership, and the high oxidation temperature may degrade the crystalline silicon bulk quality. Many alternatives based on low-temperature processes therefore receive currently strong research interest, including plasma-enhanced chemical vapor deposition (PECVD)<sup>3</sup>, rapid thermal oxidation<sup>4</sup> and electrochemical oxidation<sup>5</sup>. Meanwhile, alternative novel dielectric materials, such as SiN<sub>x</sub>, SiC<sub>x</sub>, SiON and Al<sub>2</sub>O<sub>3</sub>  $^{6-9}$ , are being investigated. Bi-layer schemes like SiO<sub>2</sub> capped with SiN<sub>x</sub>  $^{10}$  have also been explored. Due to the potentially high throughput, SiO<sub>2</sub> thin films deposited via atmospheric pressure chemical vapor deposition (APCVD) are highlighted for industrial applications. Our recent research shows that capping an APCVD grown  $SiO_2$  layer with a PECVD grown  $SiN_x$  layer can improve cell quality significantly. The rear contact of a passivated emitter and rear cell (PERC) or PERL-type cell is typically achieved by local laser ablation of the dielectric stack, followed by deposition of an Al film, which is then co-fired in a belt furnace together with screen printed front contacts. However, the impact of firing in the presence of a capping Al film on the rear surface passivation quality of a  $SiO_2/SiN_x$  stack is not yet clear. This is among other due to the difficulty to investigate passivation layers covered by a metal film with minority carrier lifetime measurement techniques, such as microwave photoconductance decay ( $\mu$ w-PCD). In this communication, the impact of firing on the surface passivation provided by  $SiO_2$  and a  $SiO_2/SiN_x$  stack will be studied by the capacitance-based technique.

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Boron doped *p*-type (100) float zone (FZ) Si wafers with resistivity of 0.5 ohm.cm were submitted to a piranha clean (H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>=4:1), followed by an RCA clean and an HF dip. On the front side, they were coated by a  $SiO_2$  film with thickness of 100 nm grown by APCVD using silane and oxygen as precursor gases. Half of the wafers were then capped with an 80nm thick  $SiN_x$  film deposited by PECVD using silane and ammonia as precursor gases to generate the double layer passivation stack. Subsequently, 1 mm thick Al contact dots were e-beam evaporated on the passivation layers using a shadow mask with holes of 0.5-3mm diameter. A full Al film was evaporated on the back surface of the Si wafers to create a back contact for the electrical measurement of the generated Metal-Insulator-Semiconductor (MIS) capacitors. Either before or after the Al contact evaporation on both sides, part of the samples were subjected to a firing step, consisting of a rapid thermal processing with a peak temperature of 845°C in a belt furnace. The MIS capacitors were then measured using a 1 MHz Capacitance meter and a Fourier-Transform deep level transient spectroscopy (DLTS) system. The current-voltage curves were also monitored in order to determine the MIS capacitor leakage.

Figure 1 shows the C-V plots for the studied MIS capacitors. There is a systematic shift of the flat-band voltage ( $V_{FB}$ ) towards more negative values for the bi-layer samples compared to the single layer samples, in line with the increased thickness of the dielectric stack.  $Q_{fc}$  in the range of  $2.1 \times 10^{12}$  cm<sup>-2</sup> and  $3.8 \times 10^{12}$  cm<sup>-2</sup> for non-fired Si/SiO<sub>2</sub>/Al and Si/SiO<sub>2</sub>/SiN<sub>x</sub>/Al devices, respectively, have been derived from the V<sub>FB</sub> shifts with Al work function of  $4.1 \text{eV}^{11}$ . Slight hysteresis of V<sub>FB</sub> shift about 0.3V and 1.5V is found for non-fired Si/SiO<sub>2</sub>/Al and Si/SiO<sub>2</sub>/SiN<sub>x</sub>/Al devices, respectively. The higher hysteresis for the as-deposited bi-layer stacks is ascribed to more removable charge traps, which are probably induced by hydrogen in the SiN<sub>x</sub>

layer. For dielectric layers fired before Al deposition, the insulator capacitances decrease and  $V_{FB}$  slightly shifts towards more negative values in both cases: in comparison with the non-fired devices, the higher  $Q_{fc}$  of about  $2.3 \times 10^{12} \text{cm}^{-2}$  for Si/SiO<sub>2</sub>/Al device and  $4.6 \times 10^{12} \text{cm}^{-2}$  for Si/SiO<sub>2</sub>/SiN<sub>x</sub>/Al device is derived. However, after the co-firing of dielectric layers with an Al contact,  $V_{FB}$  shifts towards a much more positive value and a  $Q_{fc}$  of about  $-1.5 \times 10^{11} \text{cm}^{-2}$  is derived. No detectable hysteresis is recorded for such fired devices, indicative of fewer removable charge traps after the co-firing step. Note that the current-voltage test indicates an extremely leaky behavior for the fired Si/SiO<sub>2</sub>/Al capacitors which therefore have been omitted in this study.

Figure 2 shows the effective  $D_{it}$  spectra derived from the DLTS frequency scan measurements following the approach proposed by Simoen *et al.*<sup>12, 13</sup>. These spectra are obtained using the pulse bias sweeping from the depletion region to the accumulation region. The as-deposited Si/SiO<sub>2</sub>/SiN<sub>x</sub>/Al device has comparable  $D_{it}$  but peak activation energy of  $D_{it}$  closer to the valance band ( $E_v$ ) of Si compared with the as-deposited Si/SiO<sub>2</sub>/Al device. This is probably also accompanied by a reduction of the minority capture cross section, given the trend reported in Ref. 12 for example. Firing solely the as-deposited SiO<sub>2</sub> layer hardly alters the  $D_{it}$  distribution, whereas firing the as-deposited SiO<sub>2</sub>/SiN<sub>x</sub> stack leads to lower  $D_{it}$  and a shallower  $D_{it}$  peak activation energy, closer to  $E_v$ . After co-firing of the dielectric layers and the Al contact, the  $D_{it}$  is reduced significantly and the  $D_{it}$  peak activation energy shifts towards  $E_v$  dramatically at the same time.

Figure 3 shows the trap filling kinetics derived from the DLTS filling pulse duration scans. Typically, the fast capture initial stage is corresponding to the filling of fast interface states while the slow capture tail may be induced by the de-trapping of holes from the oxide defect traps to the Si substrate <sup>14, 15</sup>. In the Si/SiO<sub>2</sub>/Al devices fired before Al deposition, both interface states and deep oxide traps are pronounced. Contrarily, firing the Si/SiO<sub>2</sub>/SiN<sub>x</sub>/ Al devices before Al deposition results in an almost complete suppression of both interface states and deep oxide traps, indicating fewer interface states at the fired Si-SiO<sub>2</sub> interface. Interestingly, the de-trapping of holes from oxide defect traps to the Si substrate can be further suppressed by the co-firing with Al contact. The evolution of interface states coincides well with the D<sub>it</sub> spectra shown in Fig. 2.

The observations herein are also in line with the available minority carrier lifetime measurements. Photoluminescence lifetime image mappings on similarly processed wafers show that the non-fired  $SiO_2$  layer itself does not provide good surface passivation, coating with a  $SiN_x$  layer improves the surface passivation quality significantly and the firing treatment of bilayers and Al contact improves the passivation further.

The surface passivation quality is the combined result from both the deactivation of dangling bonds at wafer surface<sup>16</sup> and the field effect induced by the fixed charge traps in dielectric layers. High density of pinholes is presented in the amorphous SiO<sub>2</sub> layer deposited by APCVD. The high temperature firing process leads to the reconstruction of Si-O bridge bonds and the reduction of pinhole density, which probably induces the variations of the accumulation capacitance and of the Q<sub>fc</sub> in MIS capacitors. After capping the SiO<sub>2</sub> layer with SiN<sub>x</sub>, the additional positive charge contained in SiN<sub>x</sub> layer contributes to the induced electric field. The shallower D<sub>it</sub> in this case is due to the formation of stable Si-H bonds at the wafer surface during PECVD processing. When firing the as-deposited bilayers, hydrogen in the SiN<sub>x</sub> layer diffuses to the Si-SiO<sub>2</sub> interface and passivates more dangling bonds <sup>17, 18</sup> leading to

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reduction and shift of the maximum of  $D_{it}$  to lower energies. Firing solely a SiO<sub>2</sub> layer does not alter the  $D_{it}$ , which is ascribed to the absence of hydrogen source. During cofiring of the bilayer with Al film, atomic hydrogen can be released from the molecular hydrogen coming from SiN<sub>x</sub>. The oxide defect traps in SiO<sub>2</sub> and more dangling bonds at the Si-SiO<sub>2</sub> interface can be passivated by the hydrogen ions<sup>19</sup>. Similar defects and interactions with hydrogen in MOSFET studies showed up the excellent atomic hydrogen passivation effects by cracking of hydrogen molecular <sup>20, 21</sup>.

In conclusion, firing solely the SiO<sub>2</sub> layer as-deposited by APCVD hardly alters the distribution of interface states. Capping the SiO<sub>2</sub> layer with PECVD deposited SiN<sub>x</sub> layer already causes a shift of peak activation energy of D<sub>it</sub> towards  $E_v$ of Si. Firing the bilayers leads to a moderate increase of Q<sub>fc</sub>, a reduction of D<sub>it</sub> and a shallower peak activation energy of D<sub>it</sub>. Moreover, co-firing the bilayers with Al film results in significant reductions of the Q<sub>fc</sub>, D<sub>it</sub> and the D<sub>it</sub> peak activation energy, which is indicative of passivation by atomic hydrogen.

Acknowledgements M. Allardt and J. Weber are thanked for their useful discussions. The Alexander von Humboldt Foundation, Research Foundation Flanders and Natural Science Foundation of China (No. 60906001) are thanked for financial support.

## **Figure caption**

- Figure 1 CV plots at 1MHz and 295K for the studied Si/SiO<sub>2</sub>/Al and Si/SiO<sub>2</sub>/SiN<sub>x</sub>/Al MIS capacitors. Measurements were carried out in both directions while only the data from forward direction are plotted herein for clarity. The thickness of deposited SiO<sub>2</sub> layer is estimated to be around 100nm. *F* and *nF* refer to fired and non-fired layers respectively, and +Al to layers fired when already coated with Al.
- Figure 2  $D_{it}$  spectra for the Si/SiO<sub>2</sub>/Al and Si/SiO<sub>2</sub>/SiN<sub>x</sub>/Al MIS capacitors derived from DLTS frequency scans. The hole capture cross section of  $s_p \sim 3x10^{-17}$  cm<sup>2</sup> is used in the transformations, extracted from the boron doping level in Si bulk, a filling pulse time of 10<sup>-7</sup>s and the thermal velocity at room temperature of 10<sup>7</sup> cm/s.
- Figure 3 Normalized DLTS signals against filling pulse duration for the Si/SiO<sub>2</sub>/Al and Si/SiO<sub>2</sub>/SiN<sub>x</sub>/Al MIS capacitors during the measurements. The recorded DLTS amplitudes are normalized by the steady state capacitance corresponding with reverse bias and Al contact area.

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