Fast synchronisation algorithms of burst-mode 16QAM receiver for video-on-demand applications

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ABSTRACT

This paper describes a novel TDMA/FDMA combined 16 QAM receiver architecture developed for video-on-demand applications. A burst-operated rapid synchronisation scheme is proposed which employs an efficient training preamble for overlapped operation of automatic gain control, carrier phase acquisition and symbol timing alignment. All the dedicated synchronisation algorithms are digitally implemented, using field programmable gate arrays (FPGA), for a data rate of 10.8Mbit/s. Several analytic relationships for control accuracy, acquisition time and signal to noise ratio (S/N) are derived. Experimental results demonstrate that the proposed method significantly decreases the required preamble length to 23 symbols, together with a dynamic range of 11dB and a sensitivity of -56dBm for a bit-error-rate (BER) of $5*10^{-9}$. The BER performance with frequency offset and input power variation is also investigated.

Keywords : burst mode modem, carrier recovery, symbol timing, automatic gain control, QAM

1. INTRODUCTION

The increasing demand for providing high speed interactive data transport services has led to the development of modems which allow for duplex transmission over the existing CATV networks. Since the lower frequency band of the existing CATV channel (5-50MHz) is assigned for return path transmission, a lot of effort is done to investigate the upstream network characteristics, modulation and multiplexing methods and transceiver prototype implementations for achieving a bandwidth efficient, reliable and flexible transmission.

So far three categories of multiple access techniques can be applied for upstream transmission : code division multiple access (CDMA), time division multiple access (TDMA) and frequency division multiple access (FDMA). As CDMA is based on the spread spectrum technique, it is robust to all types of interference but at a cost of low spectral efficiency [1]. A combined TDMA/FDMA system is considered for providing a high upstream traffic efficiency. The reason is that burst-mode transmission is much more efficient than CW-mode to obtain a larger system capacity and support a variable data rate. Moreover, TDMA provides a greater immunity against the impulse noise in the network by using error correcting codes, while FDMA offers some protection from narrow band interference and each sub-channel distortion can be handled with a simple equaliser. To yield a net spectral efficiency of 3bits/s/Hz, a 16 QAM modem with a data filter roll off factor of 33% is considered. The essential requirements for these kind of burst mode modems are fast acquisition, i.e. quick burst envelope detection, fast timing recovery and carrier phase synchronisation, while other system specifications like large dynamic range, high sensitivity and low BER have to be met.

This paper presents the design principles and experimental results for a 2-channel multiplexed 16 QAM/TDMA transceiver with a data rate of 10.8Mb/s developed for upstream transmission over CATV networks. The main emphasis lays on the receiver fast synchronisation algorithms and efficient digital implementations for burst envelope detection (BED), automatic gain control (AGC), carrier phase acquisition (CPA) and symbol timing alignment (STA). These algorithms are based on an efficient training preamble which allows for overlapped operation of AGC, CPA and STA to reduce significantly the acquisition time. Several analytic relationships for control accuracy, acquisition time and S/N are derived and compromises among these factors are made to satisfy the system specifications. Measurement results demonstrate a receiver dynamic range

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of 11dB, a sensitivity of -56dBm and a run-in time of 23 symbols for a BER of $5*10^{-9}$ without forward error correction. The BER with frequency offset and input power variation are also investigated.

2. RECEIVER CONFIGURATION

The burst-mode 16QAM receiver is implemented with a hybrid analogue/digital architecture, as illustrated in Fig. 1.

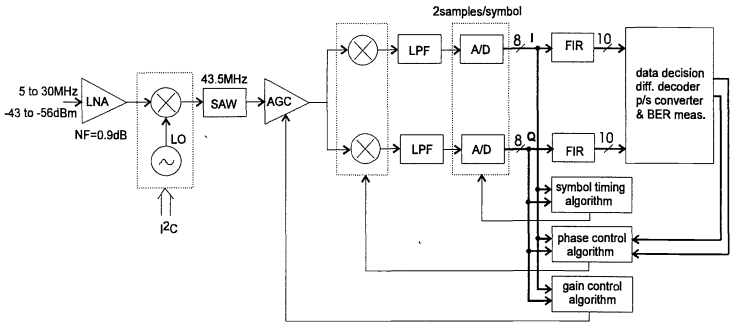

Fig.1 Burst mode 16 QAM receiver

The input signal is amplified using low noise active components and up converted to IF. A SAW filter is used as a channel selector followed by an amplifier with variable gain. The IF-signal is down mixed to base band using a quadrature local oscillator. The resulting in phase (I) and in quadrature (Q) signals are digitised with 8 bit wide AD converters. Both channels are further processed with digital technology realised in FPGA's. The main building blocks are the synchronisation algorithms (AGC, CPA, STA), two root raised cosine data FIR filters and the data decision and decoding logic. A rapid synchronisation scheme is developed based on a particular training preamble consisting of a balanced string of 1's and 0's with maximum vector amplitude in the constellation. Such an efficient preamble is chosen for fast and partly parallel operation of the AGC, CPA and STA without overcomplicating the digital implementations. The timing sequence for performing these algorithms is given in Fig. 2, where a coarse acquisition is performed during preamble and a fine tracking (FT) can be done during data transmission by using the values obtained in the acquisition phase as initial references.

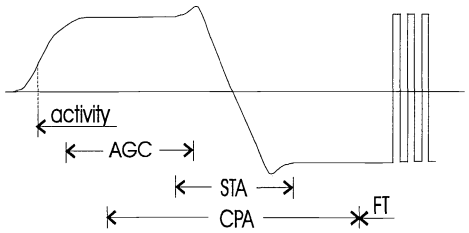

Fig.2 Timing sequences for synchronisation

Thus a considerable run-in time reduction is achieved. A short and balanced preamble has several advantages. It causes little penalty on the power efficiency at the transmitter output, i.e. peaking in the spectrum is minimised. Moreover, if the data content of each burst is DC-balanced, no charge-discharge effects of coupling capacitors after the demodulator occur, resulting in a low burst to burst crosstalk.

3. BURST ENVELOPE DETECTION AND AUTOMATIC GAIN CONTROL

For TDMA transmission over CATV networks, a large dynamic range is required since all bursts may suffer different attenuation over the network depending on the geographical location of the transmitters. Part of this dynamic range can be

realised at the transmitter side by setting an appropriate transmission level. However, AGC at the receiver side remains necessary. Hence, a fast and accurate amplitude measurement should be performed to detect the presence of a burst and adjust the gain of the receiver to set the input signals to an optimised level. At reset, the gain of the amplifier is set such that the received burst with maximum expected amplitude is within the linear range of the A/D converter. Since the AGC is active when the transmitted preamble has a constant amplitude, and the I and Q digital data are available, the signal amplitude can be calculated by the function $\sqrt{I^2+Q^2}$. This calculated amplitude is compared with a pre-determined threshold for BED. The activity threshold is determined by the noise floor of the A/D output noted as V_{noise} and the voltage V_{min} applied to the A/D converter corresponding to the lowest expected signal level. The relation between the parameters involved is given in formula (1)

$$\text{activity threshold} = \sqrt{V_{min} \cdot V_{noise}} \tag{1}$$

and

$$V_{min} = \text{Full-scale(A/D)} / 10^{\text{Dynamic-range}/20} \tag{2}$$

A similar algorithm is used for the end of burst detection but the threshold is determined by the smallest vector amplitude before data decision. At the end of the burst the gain of the receiver is again set to minimum to be prepared to process the following burst.

The square root function can be calculated using the Cordic transform, which has a fast convergence behaviour and requires no complex digital hardware [2-4]. To implement the Cordic transform with two's complement representation, only add and subtract functions are necessary. The idea is to rotate the vector (I,Q) such that it is in parallel with the I-axis. The rotation is done in different steps with increasing accuracy. The calculation result is then translated to a control word represented in dB via a table for adjusting the gain of the variable gain amplifier. The overall accuracy of the AGC is determined by the A/D effective number of bits N_{eff}, the total required dynamic range D (dB), the gain setting accuracy of the AGC amplifier S (dB) and the number of Cordic rotations n. The accuracy as a function of all these parameters is given in (3), the unit is dB.

$$ACC(n, Neff, D, S) = 20\,LOG\sqrt{\frac{1+2^{-2(n-1)}}{1-\frac{\sqrt{2}}{10^{-\frac{D}{20}}.2^{Neff-1}}}} + S \tag{3}$$

A further increase of the control accuracy can be made by performing iterative AGC cycles. After each iteration the dynamic range to be processed by the following stage is reduced, resulting in an overall accuracy improvement. A trade off between accuracy and preamble length can be made. For an initial dynamic range D=15dB, n=4 and S=0.5dB, the calculated control accuracy versus the A/D effective bits and the number of iterations is illustrated in Fig. 3. It can be seen that when $N_{eff} = 5$, three iterations are necessary to obtain an accuracy of 1dB. An additional iteration would not improve the accuracy significantly.

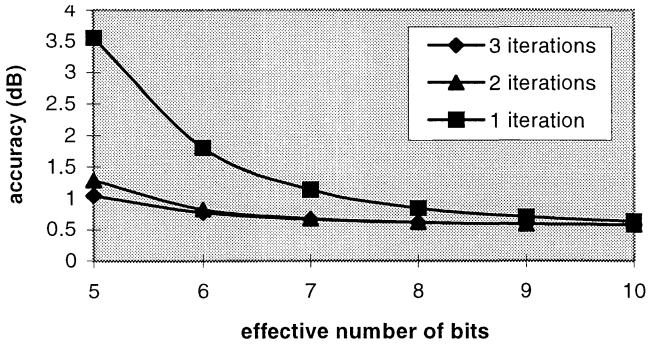

Fig. 3 AGC accuracy as a function of effective number of bits

4. SYMBOL TIMING ALIGNMENT

A fast symbol timing recovery scheme is proposed and developed which uses a single shot timing estimator and a programmable divider as a timing controller. The basic building block is shown in Fig. 4. The main advantage over other estimators[5-6], using a maximum likelihood function, is its simplicity and the possibility of simultaneous operation with the coarse carrier phase recovery. The architecture is extremely suited to be realised in FPGA technology. The input data is taken before the FIR data filter which decreases the acquisition time by avoiding the latency of this filter. However, a penalty in noise immunity needs to be taken into account.

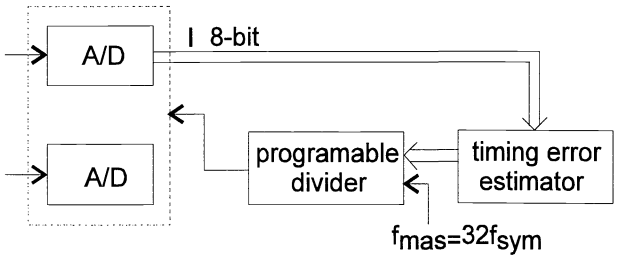

Fig. 4 Block diagram of symbol timing alignment

The timing error estimator accepts samples from the I channel at two samples in one symbol period. The exact sample moment is derived from a master clock running at a high frequency. The master clock divides the symbol period in discrete sub intervals. The sampling moment can be set at any transition from one sub interval to another. The required hardware for this function can be as simple as a programmable divider. If the master clock frequency is 32 times the symbol rate, a resolution of Tsym/32 is obtained, Tsym being the symbol period.

The method for timing error estimation is depicted in Fig. 5 and is based on the recognition of a symbol transition in the preamble. I1 and I2 are adjacent expected samples around the zero-crossing point. They indicate the ideal sample moments. I'1 and I'2 are the samples actually taken. The idea behind the STA is that the theoretical time distance t_s can be obtained by system simulation of the transmitter data filter and channel models. The value of t_m can be measured and compared to t_s. Thus a timing error is generated by making the difference of t_m and t_s to control the programmable divider. Because in first order, the zero crossing transition area can be approximated by a linear function, the algorithm is relatively insensitive to amplitude and phase errors. So it is possible to perform the STA in parallel with the AGC and CPA.

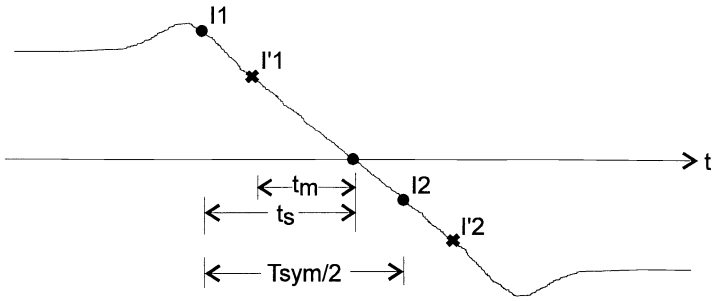

Fig. 5 Timing error estimation method

An efficient digital architecture for calculating t_m from the measured samples I'1 and I'2 was developed. It is based on a linear interpolation using a recursive bisection method. As a first estimation of the zero crossing, the middle of the interval defined by the sample moments of I'1 and I'2 is chosen. The value of the linear function defined by I'2 and I'1 is calculated in this point. Using an appropriate scaling of the time axis, this operation only requires an add and a shift function. Depending on the sign of this result a second estimation of the zero crossing is made, i.e. the zero crossing is either on the right or left side of the middle of the initial interval. The process can be repeated on the new interval which is twice as small as the

previous one. After each step, the accuracy is doubled. The finally achieved value for t_m is subtracted from t_s, which is externally set by a 6-bit control word for a fine adjustment to get the best eye diagram after FIR filtering. The overall timing accuracy is given in (4). It is determined by the number of bisection steps P and the ratio R of the symbol period to the master clock period. The error is expressed as a percentage of the symbol period. This formula also takes into account the rounding error due to the finite word length of the representation of the exact value t_s.

$$\text{timing accuracy} = 100\,[3*2^{-P-2} + 0.5/R] \quad \text{in \%} \tag{4}$$

Due to the exponential behaviour an overall accuracy of 2.7% of the symbol period can be achieved for P=6 and R=32. If the number of bisection steps is further increased, the accuracy will be limited by the resolution of the programmable divider as illustrated in Fig. 6.

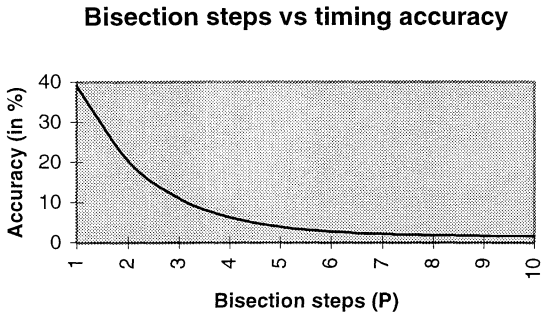

Fig. 6 : Timing accuracy as a function of bisection steps

5. CARRIER PHASE ACQUISITION

The burst-operated carrier phase control is accomplished in two modes : coarse phase acquisition during preamble and fine phase tracking (FPT) during data transmission. The phase error between the 16 QAM input signal and the local oscillator is measured by taking samples from the I and Q base band signals and generating a discrete error signal which is applied to a digital filter. A direct digital synthesiser (DDS) with image frequency output is employed as the local oscillator, whose phase is continuously adjusted by the update signal from the digital filter output as illustrated in Fig. 7.

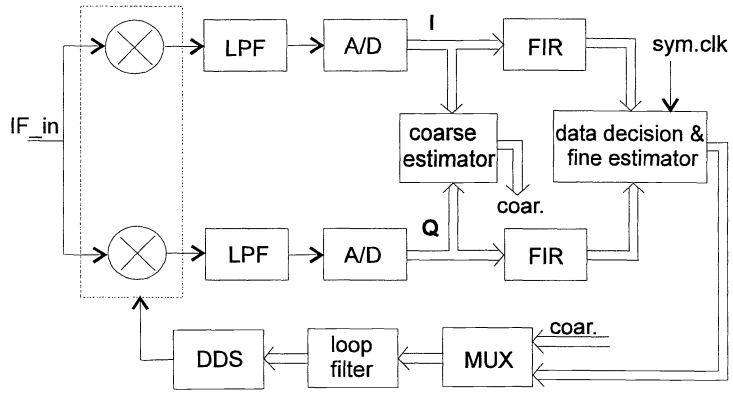

Fig. 7 Burst carrier phase acquisition block diagram

The coarse phase estimator is activated when the first AGC iteration is finished. It accepts 8-bit data I(nT) and Q(nT) directly at the A/D outputs for a minimum loop latency T. Since the transmitted preamble is treated to have a special BPSK

constellation with a long symbol period, a fast coarse phase error estimator is developed according to (5) without any knowledge of symbol timing:

$$\varepsilon(nT) = (|I(nT)| - |Q(nT)|) \cdot \mathrm{sgn}(I(nT) \cdot \mathrm{sgn}(Q(nT) \tag{5}$$

The resultant 10-bit phase error is fed to a digital filter and properly scaled to generate a control signal for updating the DDS phase offset register. Since the coarse phase locked loop is a first order digital loop, the number of iterations required to reach a sufficiently small phase error is related to the open loop gain G, the A/D effective number of bits and the AGC accuracy δ. For G=0.9, N_{eff}=5, and δ=±1dB, three iterations are required to guarantee a final phase error of less than $\pm 5^0$. The four-fold phase ambiguity problem suffered by each burst will be solved by a differential decoder after data decision.

The purpose of the fine phase tracking is to compensate the linear phase drifting due to frequency offset so that the acquisition range is burst-length independent. Moreover, the frequency stability requirements to the local oscillators at transmitter and receiver sides can be relaxed. The fine phase estimation is carried out using a decision-directed algorithm [7-8]. When the fine phase control is enabled, the preamble amplitude before data transition is used as an initial normalised value I_norm and Q_norm for calculating the decision levels. As the symbol constellation has been corrected to its near-optimum position by coarse phase control, data decision can be performed correctly. Thus the outer circle QPSK symbols (I_vector, Q_vector) can be detected as diagonal points and the new normalised values are calculated as following :

$$I\_norm(k+1) = \frac{7}{8} I\_norm(k) + \frac{1}{8} I\_vector(k+1) \qquad \text{k = 0,1,2 .....} \tag{6}$$

$$Q\_norm(k+1) = \frac{7}{8} Q\_norm(k) + \frac{1}{8} Q\_vector(k+1)$$

The discrete fine phase error is calculated by applying (6) to equation (5) and fed to the same digital filter as the coarse phase loop. The new decision levels at each iteration cycle are calculated as:

$$Dec\_I(k) = \frac{2}{3} I\_norm(k) \qquad \text{k = 0,1,2.....} \tag{7}$$

$$Dec\_Q(k) = \frac{2}{3} Q\_norm(k)$$

As the fine phase locked loop is a second order digital loop, the loop parameters should be properly designed to get a wider acquisition range and a stable operation.

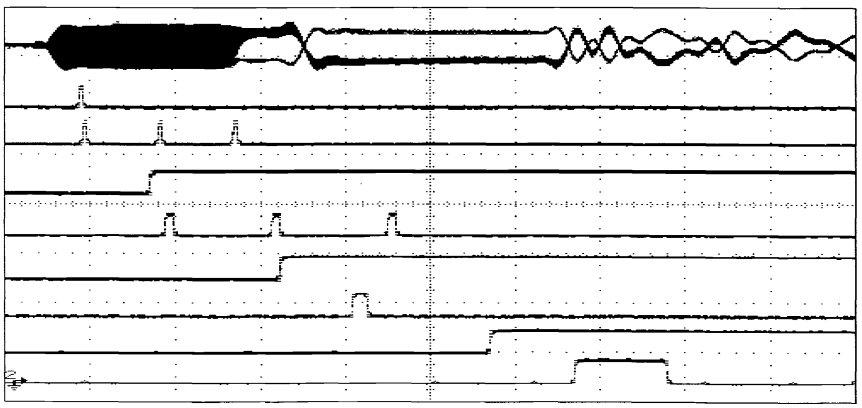

Fig. 8 Receiver timing sequence

To have an idea how the receiver synchronisation algorithms operate, Fig. 8 indicates the measured timing sequence. The signals are described from top to bottom. The top curve shows the base band I and Q waveforms. The second signal indicates the activity detection. The next signal shows three pulses for gain adjustment. Before the second adjustment a start CPA transition is generated. Signal 5 shows three pulses corresponding to the phase adjustments of the local oscillator. After the second adjustment a start STA transition is generated. Signal 7 indicates the detection of the toggle and the correct setting of

the symbol timing. The next waveform signals the enabling of the phase tracking algorithm and the last signal indicates when the fine phase algorithm is active.

6. DEMONSTRATION SET-UP AND MEASUREMENT RESULTS

The demonstration set-up for a burst-mode 16 QAM transceiver prototype is shown in Fig. 9, where a master slave transmitter configuration is connected via a tap to the receiver. A burst BER measurement circuit is built to evaluate the system performance. The measured eye diagram before data decision is shown in Fig. 10. The total acquisition time is about 23 symbols (A/D pipeline delay excluded). In addition, the BER with frequency offset (Δf) between TX and RX is measured for a burst length of 256 symbols and the result is shown in Fig. 11. The system is capable of handling a frequency offset of about 400Hz. It was verified that the acquisition range for the coarse phase loop is in reverse proportion to the transmitted burst length. The performance can be improved by activating the fine phase algorithm. When the fine phase loop is enabled, the acquisition range is dependent on the open loop gain and S/N. For a large S/N, a higher loop gain is helpful to enhance the acquisition range. However, if the S/N is not high enough, a high loop gain will degrade the BER performance.

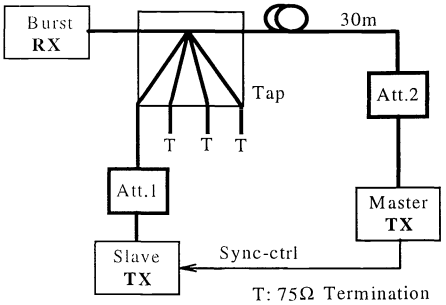

Fig. 9 Demonstration set-up

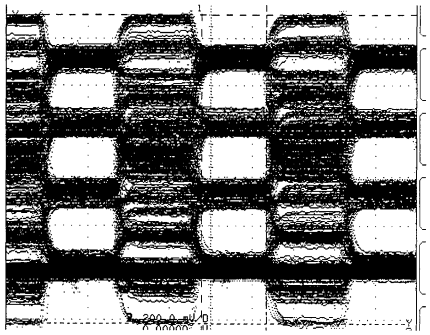

Fig. 10 Measured eye diagram

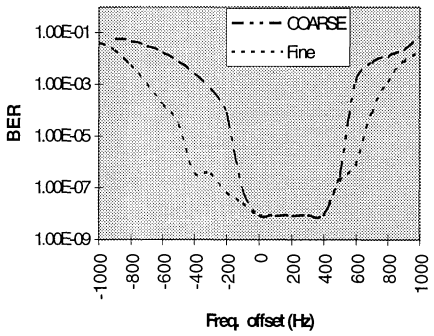

Fig. 11 BER with frequency offset

To examine the effect of the AGC accuracy on the initial acquisition performance, the BER versus Δf is measured when the input power varies 8 dB without AGC and only the coarse phase loop and the STA is in operation. The result is given in the 3D-graph of Fig. 12. It concludes that the allowable input power variation is ±2dB for little BER degradation. To obtain this, the decision level of each burst is dynamically controlled using the level measurement during the preamble. This further relaxes the required AGC accuracy. The system dynamic range is measured with no frequency offset by varying the attenuator between TX and RX. The result is shown in Fig. 13. The obtained dynamic range is 11dB and the sensitivity is -56dBm for a BER of $5*10^{-9}$.

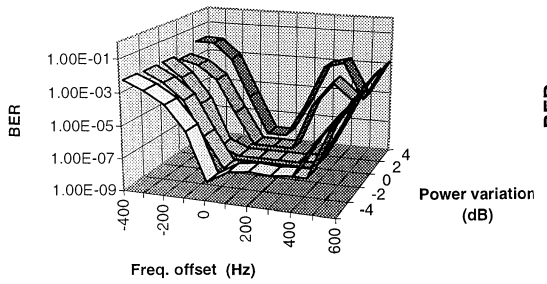

Fig 12 BER versus frequency offset and power variation

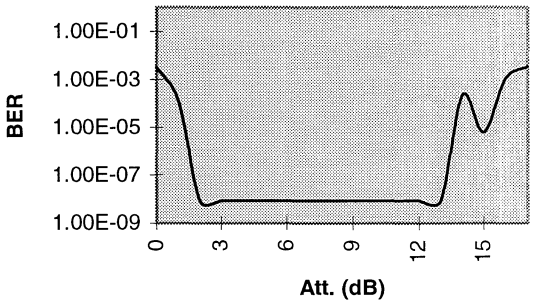

Fig. 13 BER vs input power variation

7. CONCLUSION

A burst-mode 16 QAM transceiver system using a combined TDMA/FDMA multiple access method for upstream transmission over CATV networks has been developed and demonstrated. A novel fast receiver synchronisation scheme has been proposed and digitally implemented using FPGA components. Measurements show an acquisition time of 23 symbols, a sensitivity of -56dBm and a dynamic range of 11dB for a BER of $5*10^{-9}$. It is expected that a further improvement of the performance can be achieved if chip design is considered.

ACKNOWLEDGEMENTS

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