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Submicrometer-Channel Organic Transistors with MHz Operation Range on Flexible Substrates by a Low-Resolution Fabrication Technique

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In this paper, the development of a simple and reproducible approach for the fabrication of n-type organic field-effect transistors with a 350 nm-long channel on flexible substrates is reported. The critical feature of the device, the channel length, is obtained using a self-alignment process that exploits the vertical step of a plasma-etched thin Parylene C layer, according to the so-called step-edge architecture. The fabricated devices can operate in continuous mode and show an average and maximum transition frequency of 2.5 MHz and 5.5 MHz, respectively. The possibility of easily obtaining high-performing, short channel organic transistors on flexible substrates, without the use of expensive and high-resolution techniques, represents an interesting step toward the miniaturization of flexible circuits in the field of large-area organic electronics.

1. Introduction

Among the organic electronic devices that nowadays drive the interest of the research community, organic field-effect transistors (OFETs) undoubtedly occupy a prominent role, thanks to their versatility and the several advantages that they can offer in terms of low fabrication costs, mechanical flexibility, and compatibility with large area deposition techniques.[1] However, despite their interesting features and apart from few examples, the full potential of OFETs has not been deployed yet in mass real-life applications. One of the fields that could greatly benefit from flexible and low-cost organic transistors, and therefore offer a first real application scenario, is the Internet of Things (IoTs), where cost-effective electronic tags would enable the link to smart objects at viable costs.[2] Yet, highly performing devices are required to intercommunicate and exchange continuous information in real time at high frequencies, i.e., in the high frequency to the ultrahigh frequency bands, from MHz to GHz. Such frequency range is still largely prohibitive for organic OFETs, especially when scalable, large-area processes must be adopted. In fact, up to now, the development of OFETs is mostly limited to those fields where a fast response is not strictly necessary, such as neuromorphic engineering, and sensing and biosensing applications.[3–6] Another issue with the adoption of OFETs regards applications where high currents are required, for example, for displays driving circuitry. In fact, due to their relatively low charge mobility, large-width (W) organic transistors are usually necessary, and this contributes to the increase of the area required to host simple electronic functions.

A common strategy to enlarge the transistor form factor consists in reducing the channel length (L), a process that has been efficiently employed by standard MOSFET technologies along the years, leading to a continuous miniaturization of the silicon-based MOSFET area and, as a consequence, to the increase of the density of devices per unit area, as well as the maximum operating frequencies. Unfortunately, scaling the channel length usually requires sophisticated fabrication techniques that can negatively impact on one of the main advantages of organic semiconductors-based technologies, i.e., the possibility of fabricating flexible circuits at low costs and high-throughputs. This aspect has de facto limited along the years the development of all those applications in which a high-density of organic devices is needed, such as high-density sensors arrays and complex circuits. Nevertheless, many strategies have been proposed so far for the fabrication of short-channel organic transistors, such as those based on the use of photolithographic approaches, including nanoimprint lithography, stencil lithography, and electron beam lithography. In particular, nanoimprint lithography allows to obtain channel lengths down to few tens of nm,[7,8]

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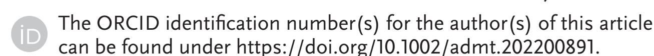
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and can also be used for the fabrication of flexible OFETs[9] or even adapted for roll-to-roll manufacturing.[10] Particularly interesting are the works of Zschieschang et al., who proposed an effective stencil lithography approach for the development of both n-type and p-type submicrometer-channel OFETs,[11,12] while e-beam lithography is known for enabling the realization of short-channel devices with channel lengths in the 100 nm range.[13,14] Beside high-resolution lithographic techniques, also nonlithographic, maskless, fabrication methods have been recently proposed for the development of short-channel OFETs. The potential of direct-writing approaches, such as fs-laser sintering of printed metallic inks, was demonstrated in the recent work of Passarella et al.,[15] who managed to reach a transition frequency of 22 MHz in a completely solution-processed flexible OFET structure with low operating voltages, and Perinot et al.,[16] who were able to reach the impressive transition frequency of 160 MHz on rigid substrates. Other maskless approaches for the fabrication of short-channel OFETs are the reverse-offset printing[17] and sophisticated inkjet solutions with subfemtoliter accuracy.[18] These high-resolution printing techniques represent promising solutions to reach channel lengths in the micrometer range.

In addition to the aforementioned solutions, an alternative and very effective approach to obtain short channels is the employment of vertical channel transistors (vOFETs), which are peculiar structures where the channel, differently from standard coplanar structures, develops perpendicularly with respect to the substrate. To date, the most widespread target application of vOFETs is optoelectronics, where different kinds of vertical organic light-emitting transistor (vOLETs) and combinations of vOFETs and OLEDs have been proposed.[19–25]

Several structures and materials have been explored to fulfil the goal of obtaining high-performing vOFETs, such as Schottky Barrier vertical organic field-effect transistors,[26,27] graphene-based vOFETs,[28,29] and, more recently, nanopillar vertical organic field effect transistors.[30] Furthermore, vertical organic static induction transistors,[31,32] and organic permeable base transistors[33–36] have also attracted considerable attention during the years, thanks to their very interesting performances, such as a maximum transition frequency of 40 MHz (albeit in pulsed mode)[37] and an outstanding maximum current density in the kA cm^{-2} regime.[38] However, many issues related to the fabrication process have been successfully solved, the realization of a high-performing permeable base transistor is still challenging.[39]

Among the different kinds of vertical channel FET structures, the so-called step-edge vertical OFET offers a very interesting solution. In this architecture, the vertical channel is obtained by employing a thin dielectric spacer (whose thickness defines the channel length) that separates the source and the drain contacts in a vertical stack. Depending on the chosen approach, it is possible to obtain both standard BG (Bottom Gate)-vOFETs and TG (Top Gate)-vOFETs,[40–48] and even vertical organic electrolyte-gated OFETs (vEGOFETs).[49,50] However, the reported approaches generally relies on high-resolution techniques, as those based on excimer laser, high-resolution masks alignments, and deposition of metal electrodes with nonconventional techniques (as oblique-incidence vacuum deposition technique), which make the proposed processes not easily up-scalable at low costs.

In this paper, we propose a Bottom-Contact Top-Gate (BCTG) step-edge short-channel OFET based on a Parylene C spacer and a fabrication method that allows obtaining submicron channels using a low-resolution fabrication process and a convenient large-area patterning technique that is compatible with flexible substrates. Parylene C is a very versatile material that is widely employed in the field of organic flexible electronics, for example, for the development of supernernstian pH sensors for cellular applications,[51] and high-performing vertical organic electrochemical transistors (vOECTs).[52] In particular, the proposed devices showed an average frequency response of 2.5 MHz, with a maximum value of 5.5 MHz, a transition frequency that is higher than those obtained by other step-edge vOFETs, such as for example the one reported by Uno et al.[43] (4 MHz, channel length 1 µm), Kudo et al.[44] (1.5 MHz, channel length 250 nm), and Takano et al.[47] (900 kHz, channel length 1 µm). The obtained results highlight a good reproducibility of the process and a good electrical stability of the devices, which can be operated in continuous mode and repeatedly characterized for extensive periods of time. In fact, another important aspect of our device is the possibility to operate it both in DC and AC modes without the need of a complicated bias setup,[37] and without any specific heat dissipation layer.[16] This aspect, although yet to be specifically characterized, represents an important feature of this structure, since to fully exploit the possibilities offered by high-frequency organic transistors, a continuous-mode operation is highly desirable. These features, together with the low-cost and low-resolution fabrication method, can open up interesting new scenarios in the field of organic electronics for sensing and flexible circuits in the IoT context.

2. Results and Discussion

2.1. Fabrication Process

All devices were fabricated onto a 250-µm thick polyethylene naphthalate (PEN) substrate. A first gold contact (bottom contact from now on) is deposited through thermal evaporation directly onto the PEN and then patterned through a low-resolution photolithographic process. Afterward, a Parylene C spacer (350-nm thick for all the devices fabricated in this work) is deposited on the whole substrate by chemical vapor deposition (CVD) at room temperature. On top of the spacer, a second gold contact (top contact from now on) is deposited and then patterned through a low-resolution photolithographic process, in partial overlap (5–20 µm range) with the bottom contact. These two contacts will act as source and drain of the transistors. In order to form the channel, the substrate is exposed to oxygen plasma (4 min at 200 W) in order to remove Parylene C from everywhere but under the top contact, thus exposing the bottom contact. The top contact acts here as a mask, making this step self-aligned. In order to prevent the top contact from being exposed too long to high-power oxygen plasma, the photoresist is left in place during the process and removed after the plasma step using acetone. After the fabrication of the source and drain electrodes, the substrates are cleaned with isopropanol and oxygen plasma (60 s at 100 W).

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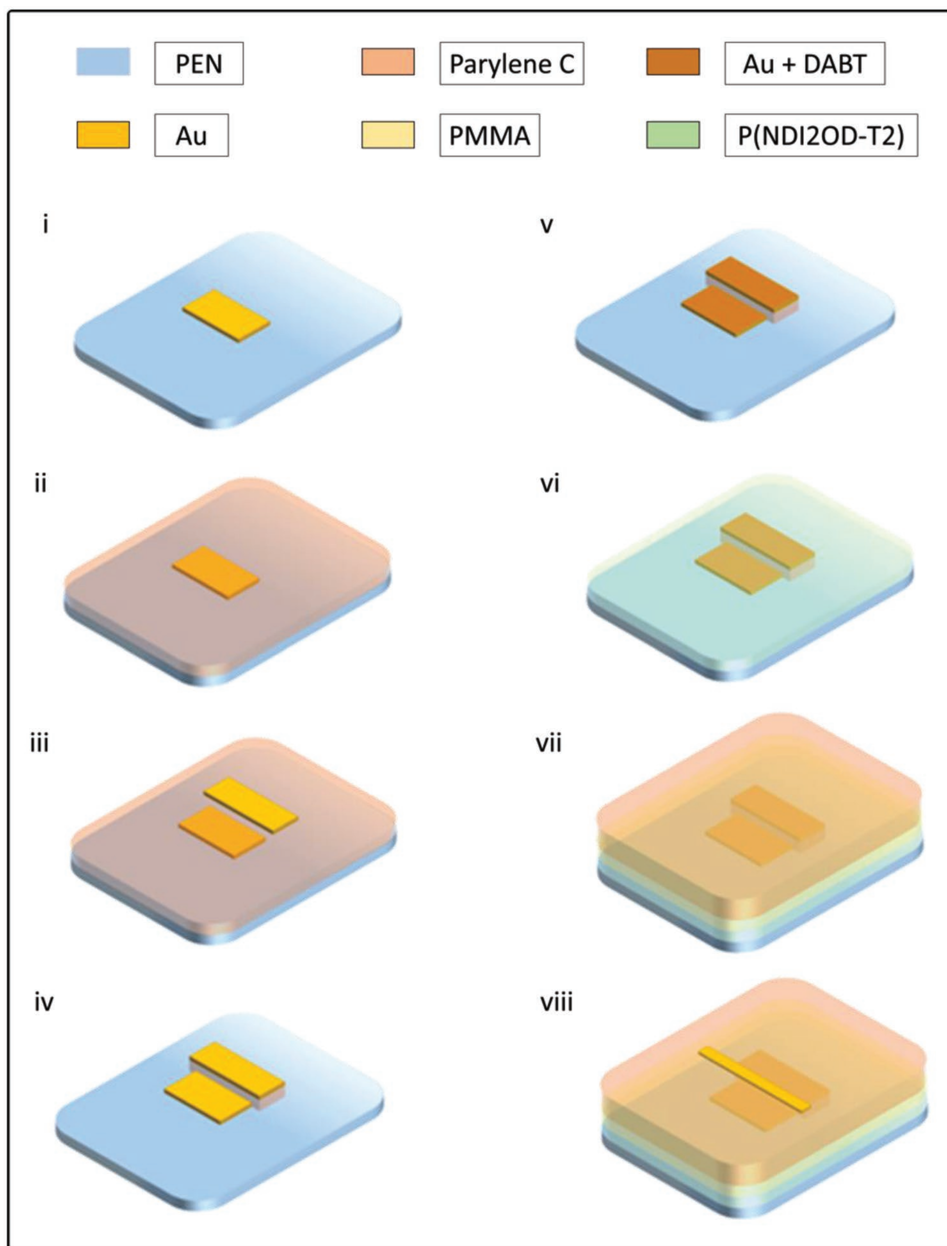

Figure 1. Fabrication process of the vOFETs. i) Deposition and patterning of the bottom electrode on PEN. ii) Deposition of a thin Parylene C layer by CVD. This layer acts as the spacer between the source and the drain of the transistors, thus ultimately determining the channel length. iii) Deposition and patterning of the top electrode. The photoresist is left in place after the photolithography in order to protect the gold contact during the following plasma treatment. iv) Patterning of the Parylene C layer by oxygen plasma treatment and removal of the photoresist. v) Application of DABT by solution dipping. vi) Off-centered spin coating of P(NDI2OD-T2). vii) Deposition of the dielectric stack (50 nm of PMMA and 260 nm of Parylene C). viii) Ink-jet printing of gold gate (width $L_w = 30$ µm).

Then, the surface of the electrodes is functionalized using a self-assembled monolayer of dimethylamino(benzenethiol) (DABT), following a recipe already developed in previous works.[53] This functionalization is known to promote an efficient charge injection of electrons into the semiconductor for n-type devices by lowering the work-function of gold.[54] Onto the treated contacts, a 7 g L^{-1} mesitylene solution of the copolymer poly{[*N*,*N*′-bis(2-octyldodecyl)-1,4,5,8-naphthalenedicarboximide-2,6-diyl]-alt-5,5′-(2,2′-bithio-phene)} (P(NDI2OD-T2, or Polyera ActivInk N2200) is deposited by off-centered spin-coating, and annealed at 120 °C for 30 min. The P(NDI2OD-T2) copolymer has been chosen as a model polymer to assess the proposed architecture, since it is an extensively studied material for n-type devices, and it has good electron transport properties both in coplanar devices, such as OFETs, and in out-of-plane configurations, e.g., in vertical diodes.[53–55] The next step is the deposition of the dielectric, which is composed by a thin spin-coated poly(methyl)methacrylate (PMMA) layer (50 nm) and a thicker chemical vapor deposited Parylene C layer (240–260 nm). In fact, Parylene-C,

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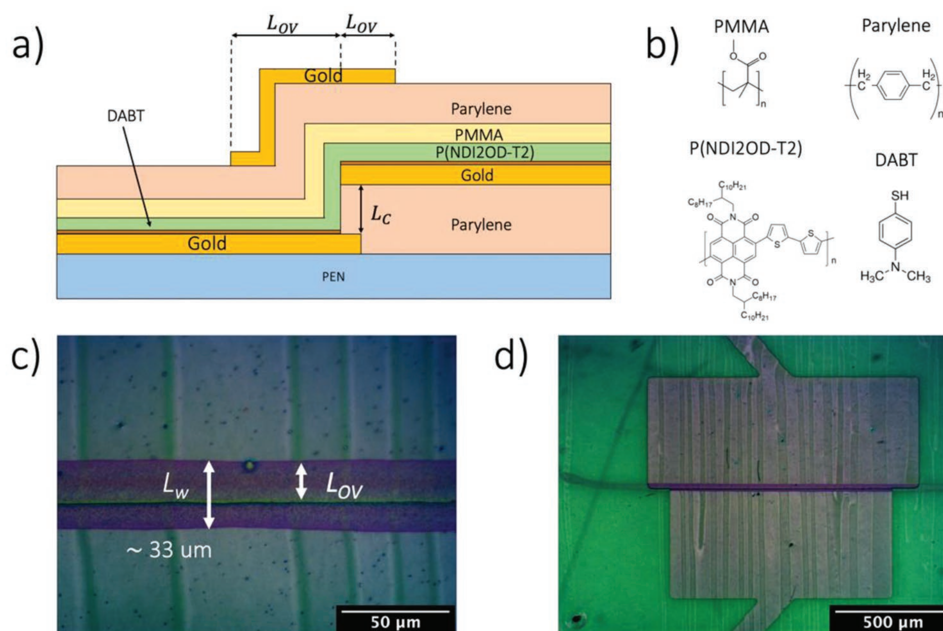

Figure 2. a) Structure of the complete vertical OFETs with materials and precise indications of the channel region and the overlaps between the gate and the source and drain contacts. b) Chemical formula of the materials used. c) Optical polarized image (top view) of the transistor channel region, with the overlaps between the gate and the source and drain contacts. d) Optical polarized image of the whole device.

owing to the presence of chlorides, is known to degrade the transistor performance when directly in contact with the chosen semiconductor.[56] Therefore, the thin PMMA layer was selected as optimum interlayer to separate the semiconductor from Parylene C. The transistor top gate (line width, L_W = 30 µm) is obtained by ink-jet printing of a gold ink (Dry-Cure Au-J 1010B) and annealed at 120 °C for 1 h. The final device is then annealed overnight at 120 °C inside a nitrogen-filled glovebox prior to the characterization. In **Figure 1**, the fabrication process workflow is presented, while in **Figure 2**a a more detailed section of the completed devices (with materials and specific region of interest) is shown. In Figure 2b, the chemical formulas of the employed materials are reported. In Figure 2c,d, polarized images of the channel regions (with the overlap between the gate and the source and drain contacts) and the overall devices are shown, respectively.

2.2. DC Characterization

The fabricated vOFETs were measured inside a glovebox under nitrogen atmosphere, after an overnight annealing at 120 °C. Transfer and output characteristic curves, in n-type operation mode using the top contact as source and the bottom one as drain, are shown in **Figure 3**. It is worth mentioning here that this structure, as well as other step-edge structures, presents an

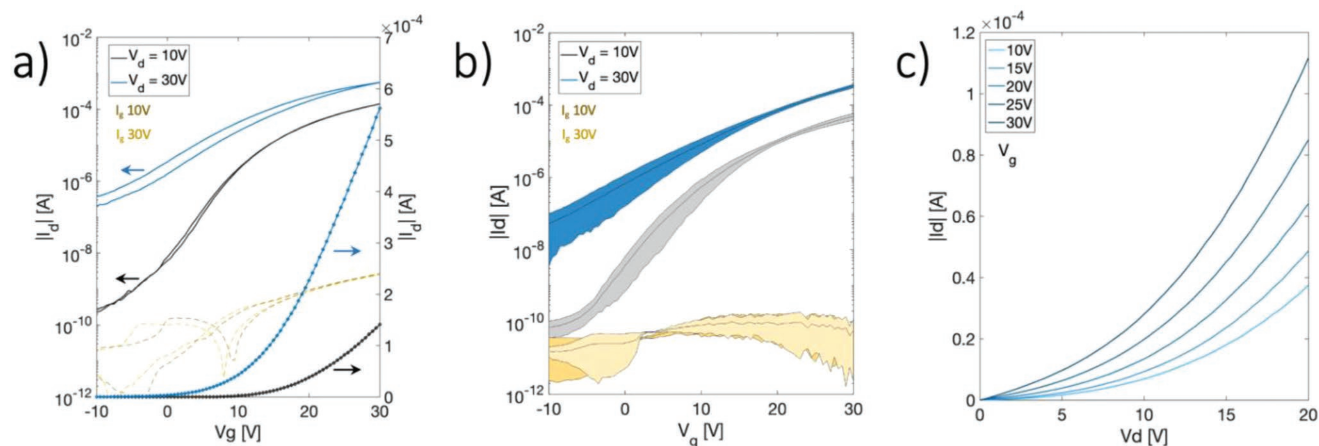

Figure 3. a) Transfer characteristics of the best device based on P(NDI2OD-T2). b) Mean transfer curves averaged over ten samples. c) Representative output characteristic curves.

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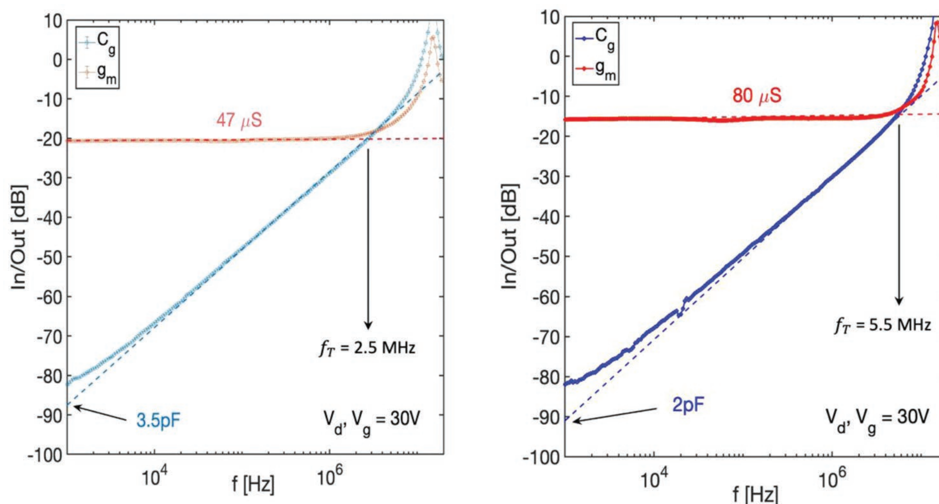

Figure 4. Experimental transition frequency extraction: average over ten samples (left) and best device (right).

asymmetry in its electrical characteristics (depending on which contact is set as the source), as shown in Figure S1 (Supporting Information). We therefore decided to focus on the configuration with the best performance in terms of transconductance, in order to optimize the frequency response of the device. In particular, in Figure 3a,b, the characteristic transfer curves of the best device and an average over ten identical devices at V_{ds} of 10 V (black curve) and 30 V (blue curve) are reported, indicating an overall good reproducibility of the process. The transistors are characterized by a good linear and quadratic relationship of $\boldsymbol{I_{ds}}$ in linear and saturation regime, respectively, with respect to V_{gs}. Moreover, good ON/OFF ratios, in the order of 10^6 (V_d = 10 V) and 10^3 (V_d = 30 V) are obtained, despite of the short channel. As a further analysis, the threshold voltage (V_{TH}) has been extracted both in the linear and the saturation regime, obtaining values of 15 and 13 V, respectively. The quasistatic average (over ten samples) normalized transconductance ($\boldsymbol{g_m/W} = [\partial \boldsymbol{I_{ds}}/\partial \boldsymbol{V_{gs}}]/\boldsymbol{W}$) has also been derived, obtaining a value of 0.5 mS cm^{-1} in saturation (at V_{ds} and V_{gs} of 30 V), with a maximum value of 0.8 mS cm^{-1}.

2.3. AC Characterization

To assess the AC performance of the vOFETs, the transition frequency f_T was measured, which is defined as the frequency at which small-signal gate (input) and drain (output) currents become equal. By definition, $f_T = g_m/2\pi(C_{gs} + C_{gd})$, where g_m is the channel transconductance and, C_{gs} and C_{gd} represent the gate-to-source and gate-to-drain capacitances, respectively, whose sum corresponds to the total gate capacitance C_g.

Given an overlap length (L_{ov}) around 15–20 µm, and knowing the channel length and width, as well as the dielectric capacitance per unit area, a theoretical total gate capacitance between 2.7 and 3.7 pF was estimated using a simple parallel plate capacitor model. For the purpose of this work, this model, although an approximation, holds well with the observed electrical characteristics, although further analysis is required to precisely characterize the complex capacitive behavior of this structure. Therefore, considering the normalized transconductance of 0.5 mS cm^{-1}, an f_T of about 2–3 MHz can be estimated.

To experimentally determine $\boldsymbol{f_T}$, we separately measured $\boldsymbol{g_m}$, $\boldsymbol{C_{gd}}$, and $\boldsymbol{C_{gs}}$ with the same electrical setup already introduced in the work of Perinot et al.[57] Average values of 1.8, 1.6, and 3.5 pF for $\boldsymbol{C_{gd}}$, $\boldsymbol{C_{gs}}$, and $\boldsymbol{C_g}$ were, respectively, extracted over ten devices, according to the parallel plates model. For $\boldsymbol{g_m/W}$, an average value of 0.47 mS cm^{-1} was obtained over ten samples, with a maximum of 0.8 mS cm^{-1}. These values of normalized transconductances are in very good agreement with the quasistatic ones. Finally, as shown in **Figure 4**, an $\boldsymbol{f_T}$ of 5.5 for the best device and an average value of 2.5 MHz were, respectively, extracted, again in good agreement with the previous estimations.

3. Conclusions

In this paper, we have introduced a simple approach for the fabrication of submicrometer channel flexible OFETs. The devices have been fabricated using low-resolution photolithography and a large-area, highly reproducible self-aligned technique based on oxygen plasma patterning of Parylene C thin layers. Interestingly, with the proposed solution, it was possible to obtain transistors with an operation frequency in the MHz range (up to 5.5 MHz) that can be characterized in continuous mode without any heat dissipation layer, thus representing a convenient approach for the development of compact, low-cost and high-performing OFET-based circuits onto flexible plastic substrates. Despite the nonidealities of the current version of the device, limitations that can be removed in future iterations by optimizing the semiconductor deposition and the gate/source–drain overlap, the present structure has promising potential applications for the development of high-speed organic logic circuits for flexible RFID tags and displays, flexible communication circuits for IoT applications, and high-density sensor arrays with integrated preamplification circuits for robotic skin.

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Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data supporting the conclusion of this article are available from the authors upon request, without undue reservation.

Keywords

low-resolution fabrication technique, MHz operation range, Parylene C, step-edge vertical transistors, submicrometer OFETs

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