Flip-chip bonding of Fine-pitch Ultra-thin Chips for SiF Applications

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Abstract

This paper describes the successful process investigations on ultrathin flip-chip bonding for fine-pitch applications on foil, using a novel bonding process involving Isotropic Conductive Adhesives (ICA). A Ag-based B-stage curing ICA was printed using state-of-the-art electroformed stencil on printed Ag circuitry, pre-cured and flip-chip bonded at low bonding force and short duration. The interconnection resistance measurements, performed before and after a stabilizing underfilling step, revealed low interconnect resistances down to 150 µm bond pad pitch. Finally, the reliability of the specimens prepared using this process was successfully evaluated by means of standard reliability test procedures such as thermal shock testing and accelerated humidity testing.

Introduction

The integration of ultra-thin chips (UTCs) in their bare-die form is key to the realization of fully flexible large-area electronic systems-in-foil (SiF). The Si chips need to be thinned down to sub-50 µm thickness to ensure their mechanical flexibility, as Si is inherently brittle and inflexible at higher thicknesses. At sub-20 µm thicknesses, the Si chips become extremely flexible, thus allowing integration in highly flexible foils [1]. This ultra-thinness of the chips, however, places significant constraints in the manner in which they are handled and integrated in a foil [2].

Flip-chip bonding is currently the most mature, widely available technology to integrate these chips [3]. Solders or anisotropic conductive adhesives (ACA) have so far been used commonly for flip-chip bonding [4]. Another approach to bonding of UTCs is flip-chip bonding using isotropic conductive adhesive (ICA). The flip-chip – ICA process offers certain key advantages over processes involving solders and ACAs for UTC bonding on foil. But this technology has hitherto not been given sufficient attention due to the limitations posed by adhesive printing technologies on the integration possibility of fine-pitch chips.

One of the key issues with ICA bonding at fine pitch is the wicking behaviour of the printed and still viscous ICA, causing short circuit after component placement. Furthermore long curing times for realizing the initial bonding are common with conventional ICA materials, which is not desirable in an industrial scenario. For these reasons a commercially available B-stage curing ICA with snap-curing properties for initial bonding was chosen and investigated in detail.

Methodology

The process flow for ICA bonding was defined as shown in Figure **1** with ICA dot printing on the printed foil circuitry followed by pre-curing, flip-chip bonding, underfilling and post-curing.

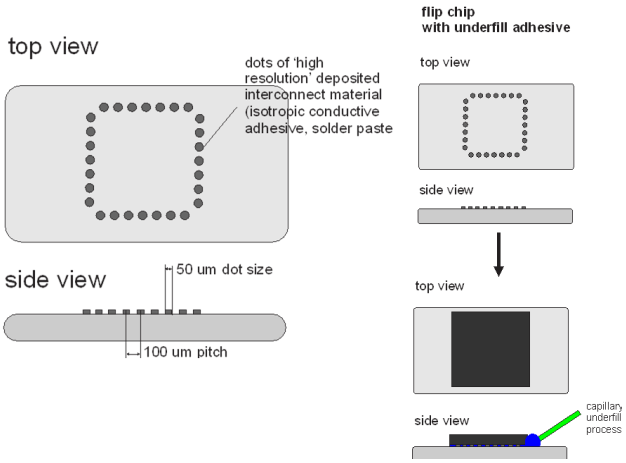

Figure 1. Flip-chip bonding process flow.

Process investigations focussed on three key aspects of flip-chip integration: ICA printing, underfill type selection and flip chip bonding process. These steps are explained in detail in the subsequent sections.

Test vehicles based on a 300 µm (IZM28) and a 150 µm (IZM40.2) pitch daisy-chain bare-die chips were used for all the experiments. These test chips were thinned down to 20 µm by the Dicing Before Grinding (DBG) process (at Disco Hi-Tec Europe GmbH, Germany). Monitoring the interconnection resistance at various stages of the bonding process viz. after B-stage bonding, after post-curing of adhesive and after underfilling, was considered a key qualifying parameter in process development. Hence, the foil circuitry was designed to enable 4-wire resistance measurements, as shown in Figure **2**. The test vehicle was screen printed with a fine mesh screen (from DEK, U.K.) using a Ag paste (DuPont 5025) on transparent polyethylene naphthalate (PEN) foils (Teonex Q65A from Dupont Teijin Films) with a thickness of 125 µm.

The interconnection resistances of the bare-die daisy chain chips were measured using a custom-built 4-wire test equipment. The IZM28 interconnections were

measured in pairs (8 per chip), while the interconnections of the IZM40.2 were measured individually (8 per chip).

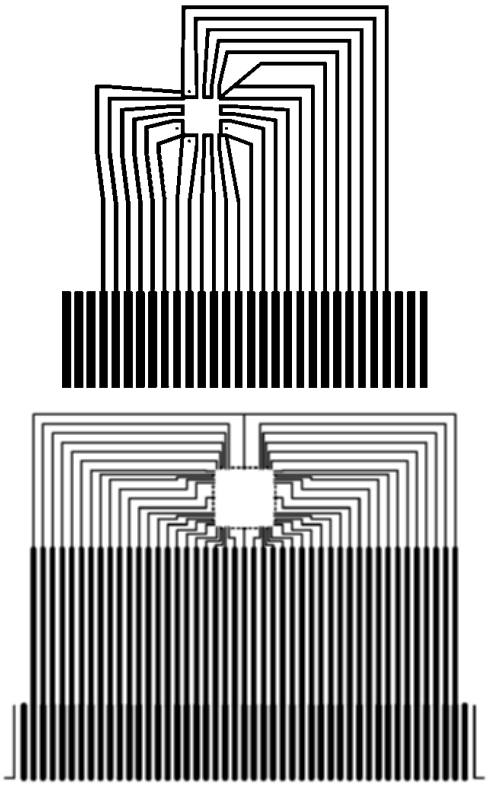

Figure 2. Foil circuitry for IZM28 *(top)* and IZM40.2 *(bottom)* enabling 4-wire measurements.

ICA dot printing and pre-curing

The first step in this ICA bonding process was the printing of ICA dots on foil circuitry using stencil printing. Initial orientation experiments were performed by manual stencil printing with in-house laser ablated metallic stencils. Subsequently, a 25 µm thick electroformed stencil (Vectorguard Platinum from DEK, U.K.) was procured and used in combination with a flat-bed screen printer (Horizon 03i from DEK, U.K.). Given the ultra-thinness of the stencil, its tensioning and dimensional stability while printing were of paramount importance for accurate alignment between the foil circuitry and the printed ICA dots. Hence, a special Vectorguard frame supplied by DEK was used for all the experiments.

The printed ICA dots were pre-cured according to supplier's specifications, at 100 °C for 30 minutes in a hot-air convection box oven. The resulting ICA dot height measured by a confocal microscope was approximately 12 µm.

B-stage bonding

The next step was placing and bonding the ultra-thin test chips. The first set of experiments was done using the 300 µm pitch IZM28 test chip. During the bonding process the adhesive required a temperature of 110 °C. The bonding line temperature was measured using a micro-thermocouple placed in between the chip and the substrate and recorded with a data logger.

With the bonding line temperature defined, the bonding time and force needed to be optimized. The boundary conditions for the B-stage bonding process of ultra-thin chips were set based on prior experiences with the ACA bonding process [5]. Several experiments were conducted with the bonding time ranging from 100 milliseconds to 5 seconds. But they did not reveal any significant difference in chip adhesion or bonding behaviour. So, for process stability reasons, a bonding time of 5 seconds was chosen.

Bonding pressure was defined in steps by starting at 4 MPa and increasing up to 60 MPa, and the indentation of the chip bumps into the printed ICA dots was evaluated (see Figure **3**).

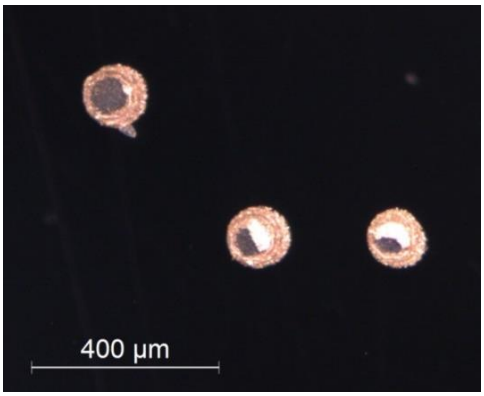

Figure 3. Imprinted ICA dots.

Due to the fact that there was no obvious difference in dot indentation, as well as to compensate for slight chip warpage, a bonding force of 45 MPa was chosen.

With the defined bonding settings (110°C, 45 MPa, 5 seconds) B-stage bonding on foil circuitry at 300 µm pitch resulted in an interconnection resistance distribution as shown in Figure **4** (left).

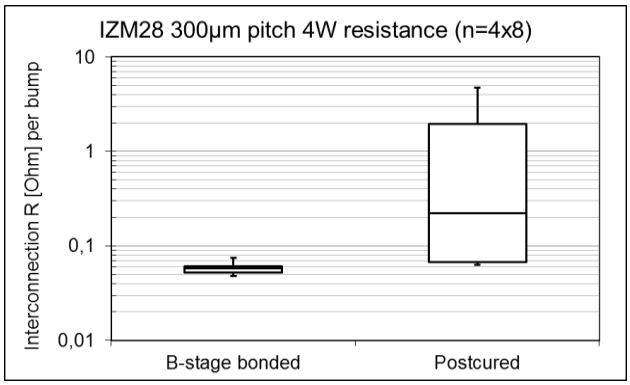

Figure 4. Interconnection resistance measured on Ag-printed circuitry after B-stage bonding *(left)* and after post-curing *(right)*.

B-stage bonding requires a post curing step of 160 °C for 20 minutes as per the datasheet. The resulting

interconnection resistance is plotted in Figure **4** (right). This process step had a negative impact on the interconnection. The CTE-mismatch of PEN (27.8 ppm/°C above T_g of 125°C) and the silicon chip (~3 ppm/°C) was too large, which caused (partial) chip delamination. So, the interim conclusion was to investigate the effect of CTE mismatch on interconnection resistance by post-curing B-stage bonded samples at different sequentially increased temperatures (see Figure **5**).

This investigation showed a significantly increased interconnection resistance values at post-curing temperatures above 70°C. It became clear that either post-curing should be done at low temperatures or the interconnection should be stabilized after B-stage bonding. Reformulating the ICA material for post curing was not an option. So, the process flow was changed to include the application of the underfill before the post-curing step, and curing it at room temperature or below 70°C.

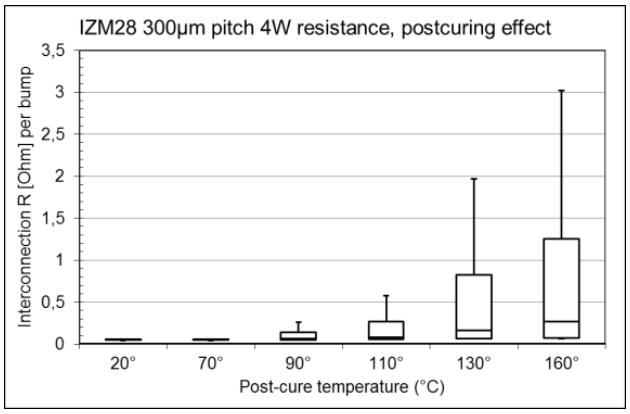

Figure 5. Interconnection resistance after post-curing at increased temperatures.

Underfill selection and post-curing

For the underfill selection 2 options were investigated, taking into account the properties of the materials used for the ICA bonding process and the nature of the interconnection.

1. Low temperature curing epoxy
2. Room temperature curing 2-component epoxy

The first underfill material used was an one-component low-viscosity (1200 mPa•s) epoxy curing at 70°C for 60 minutes. The capillary flow properties of this material was good with complete air-bubble-free gap filling within 30 seconds. However after curing the interconnection resistance was found to be significantly increased, mainly caused by the high shrinkage (4.4%) after curing.

The low viscosity (330 mPa•s), 2-component transparent epoxy showed good under-filling properties, with full capillary gap-filling occurring within seconds. This room temperature curing epoxy also resulted in a much better interconnection resistance performance. It was cured for 24 hours at RT followed by an ICA post-curing step of 160°C for 20 minutes.

The interconnection resistances were measured at certain intervals during the curing process (see Figure **6**), showing a very steady resistance over the curing cycle with an even improved interconnection resistance after post-curing.

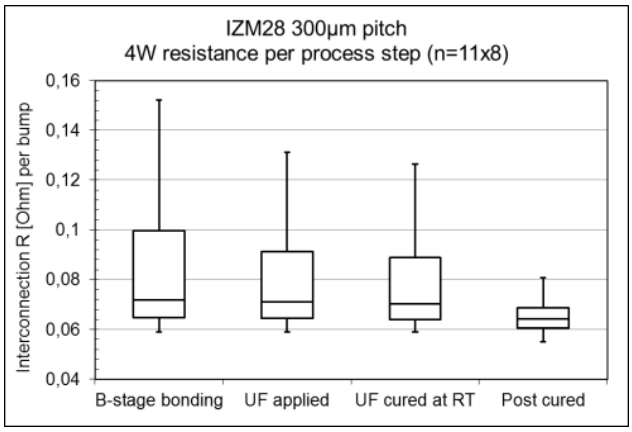

Figure 6. Effect of underfill curing on interconnection resistance.

Fine pitch bonding

Fine pitch bonding at 150 µm with the IZM40.2 daisy chain chip was done with the previously defined process settings:

1. Stencil printing ICA-dots
2. Cure in oven at 100°C for 30 minutes
3. B-stage bonding: 45-60 MPa, 5 seconds at 110°C
4. Application of underfill material (UF)
5. Cure at room temperature for 24 hours
4. Post-curing at 160°C for 20 minutes

The bonding pressure was set to 60 MPa, which is higher than in the case of IZM28, to compensate for significant warpage of the chips. After bonding, underfill application, curing and post curing the interconnection resistances of the bonded samples were measured and plotted in boxplots shown in Figure **7**.

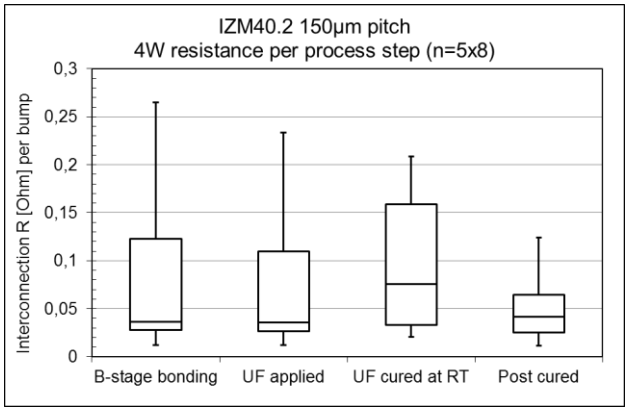

Figure 7. Interconnection resistance IZM40.2.

Alignment accuracy contributed more to the interconnection resistance deviation than in the case of

IZM28 chips, caused by the relatively smaller overlap of the ICA dot and the circuitry (see Figure **8**). This mismatch is mainly due to the foil shrinkage caused during the thermal curing (at 120°C for 10 minutes) of the circuitry printed using Ag paste. The mismatch is amplified for the finer circuitry corresponding to IZM40.2 than in the case of IZM28. This can be compensated by pre-shrinking the foil at a temperature higher than the maximum processing temperature it will be subjected to.

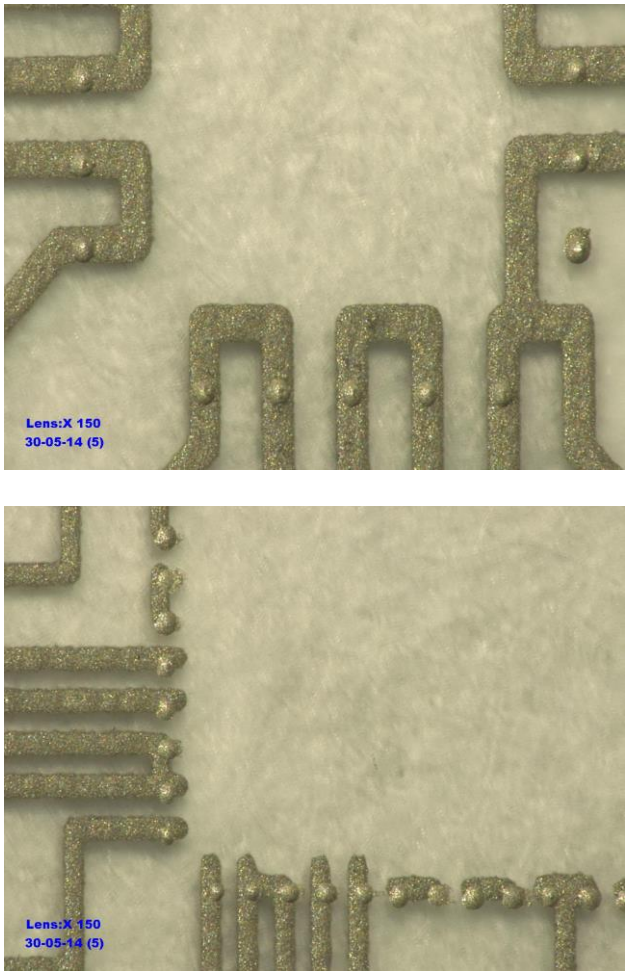

Figure 8. Alignment of ICA dots with respect to foil circuitry for IZM28 (top) and IZM40.2 (bottom).

Figure 9 shows a cross-section of a chip bonded using the ICA onto the foil circuitry, with the inset showing an enlarged view of two bond pads.

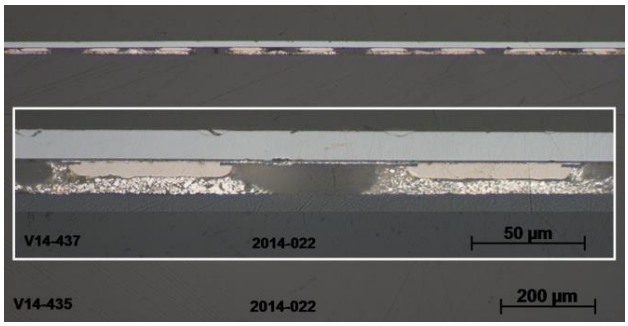

Figure 9. Cross-section of the flip-chip joint.

Reliability testing

A number of samples of both 300 µm and 150 µm pitch test chips have been subjected to reliability testing in the form of an accelerated humidity test (AHT) at 85°C / 85% RH and a thermal shock test (TST) at -40°C / +85°C (1 hour cycle) for 240 hours each. Interconnection resistances have been measured at certain intervals and shown in Figure **10** and Figure **11**. It is clear that there was only a minor increase in resistance during the humidity test, and no significant change during the thermal shock test. The differences in average interconnection resistance between the 150 µm and 300 µm pitch samples were mainly caused by a minor bulk resistance included in the measurement over 2 interconnections of the 300 µm pitch chip.

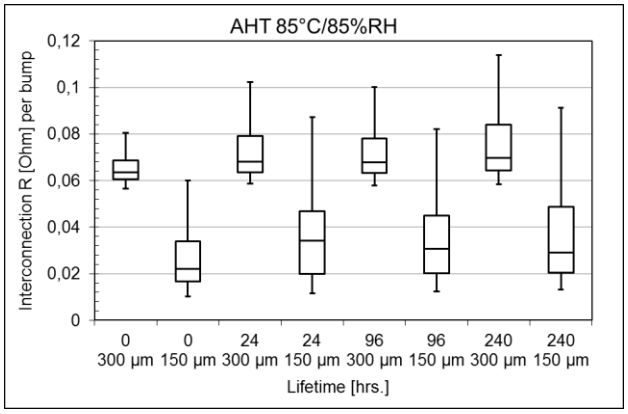

Figure 10. Results humidity test.

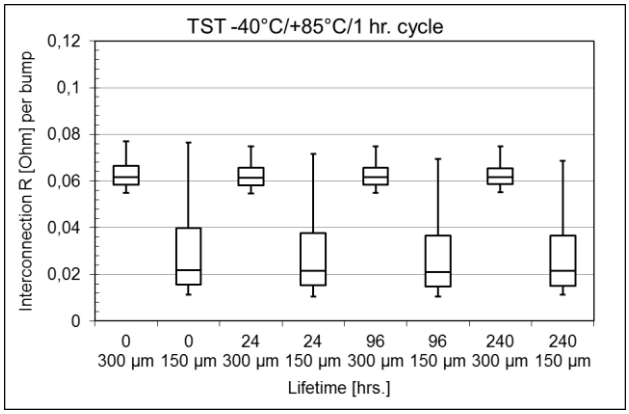

Figure 11. Results thermal shock test.

Demonstrator

Using the optimized process settings described above, a functional demonstrator was made. This demonstrator, called the "Smart Label", is shown in Figure **12**. It is a multi-sensor platform with a near field communication (NFC) chip (type M24LR64 from ST microelectronics), which is assembled on a screen printed Ag circuitry on PEN substrate using the developed flip-chip - ICA bonding process. The smallest bond pad pitch of the NFC chip is 200 µm. This demonstrator also has 01005 size SMT components, bonded using the same process. The

integration of these components was successful, as indicated by the response of the NFC chip to a NFC reader.

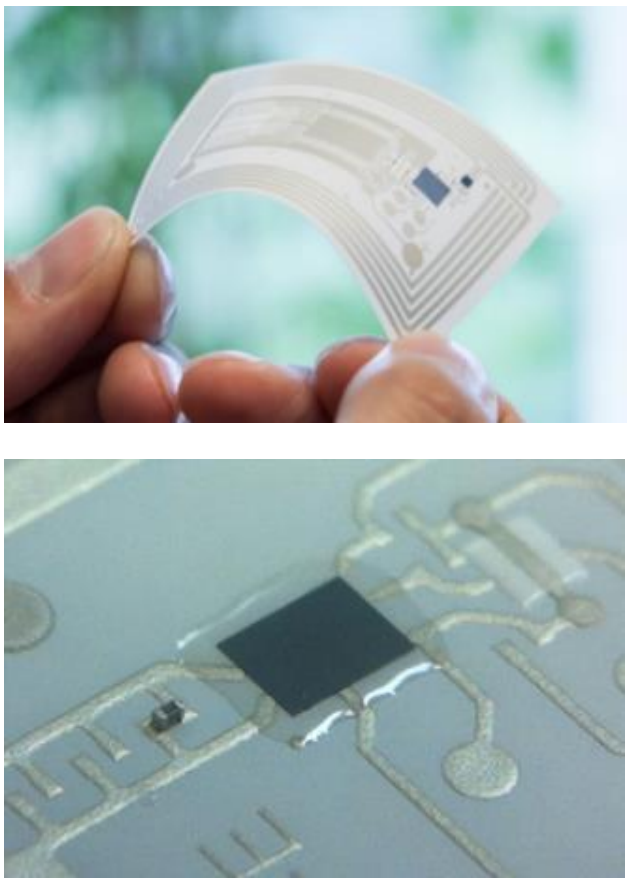

Figure 12. Smart Label: overview *(top)*, and detail showing a bare die NFC chip and a 01005 SMT capacitor bonded with B-stage curing ICA *(bottom)*.

Conclusions

From the experimental investigations it is concluded that flip-chip bonding using B-stage curing ICA is a feasible process for fine-pitch applications down to 150 µm. The position of the underfilling step in the developed process chain proved to be the key in ensuring the low contact resistances of the realized adhesive joints. Lifetime tests showed that the developed process is reliable. A functional demonstrator, containing a bare die NFC chip as well as 01005 size SMT components, was made using the optimized process settings, and tested successfully for near field communication.

The flip-chip – ICA bonding process for 300 µm pitch chip is currently being industrialized, by upscaling the developed technology in a production environment. The process for 150 µm pitch chip is currently being optimized with regard to the printing accuracy, by minimizing the effect of shrinkage of the low-cost PEN foil.

Acknowledgments

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