Programmable Logic Device Based Brushless DC Motor Control

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<< Brushless drive >>, << Reliability >>, << Electric vehicles >>, << Robust control>>, << Converter control>>

Abstract

In this article a three-phase BLDC motor controller for use in an Ultra-Light Electrical Vehicle is presented. The control is performed using a Programmable Logic Device (CPLD), which doesn't require any additional processor. In this way a robust and low-complexity control is obtained. For extending the speed range of the BLDC, a phase advance circuit is implemented as well. The power consumption of the controller is very low which is an interesting feature in battery applications.

Introduction

A drive for a light electrical vehicle is different from a servo system. For instance "braking" is not just a "negative torque", as this would result in going backwards at traffic lights if no position control is implemented [1]. So in fact, no position servo control is required, which makes the control easier. A BLDC control for a light electrical vehicle could be simple as it needs mainly combinatory tasks (AND, OR, Enable etc.) which can perfectly be performed by a Programmable Logic Device (PLD) with very few additional analog electronics. We do not have the typical constraints of servo drives for position control, where DSP solutions like the TMS320F2407 can be used [2]. Furthermore, the BLDC control should be very robust [3]. The controller also should be low cost, allowing to drive all wheels of an ultra-light electrical vehicle, without raising the total cost.

Overview of the controller

To drive an electric vehicle, only a torque control is needed. That type of control is implemented easily by combining some analog and digital electronics, a speed control might be necessary for functions like cruise control, traction control etc. but they are feature possibilities.

The block diagram of the controller is shown in Fig.1. For the implementation of the torque control two motor's currents are measured and the third is reconstructed. The maximum of the absolute values for the currents results in a one single signal for the control called collected current signal (CCS).

The CPLD block

The digital part is based on Complex Programmable Logical Device (CPLD)- XC2C64 [4], it contains 33 I/O which can be redistributed as desired. All inputs can be configured with internal Schmitt trigger, which is an important feature when using analog generated inputs. This can be done in the Integrated Software Environment (ISE) of Xilinx very easily. In a CPLD, all inputs and outputs are processed in parallel which means that -virtually- no speed limitations are present and that one can choose a motor with high number of poles and rpm. This is an advantage in concentrated pole BLDC motors, which tend to have a high number of poles and frequencies above 500Hz [5]. These types of

PLD have very low self consumption [6]. For this reason they are suitable for battery supplied applications.



Fig. 1 Block Graph for Controller

Current measurement block

The current measurement Block 2 in Fig. 1 measures the phase currents I_a and I_b of the BLDC motor. So two phase currents are measured and rectified. The current in the third phase is equal to negative sum the currents in the other two phases. A signal is made, which is the maximum of all absolute values of the currents. The schematic diagram of this block is shown in Fig. 2. So, the collected current signal (CCS) is passed to point A. The potential in this point (in condition when the currents are zero) is equal to a voltage drop on a diode and it is around -0.6 volts. The voltage of point A is shifted to a positive voltage B, to be compatible with positive set value for drive and brake torque.



Fig. 2 Schematic of the current measurement block

Driving and braking block

• Driving mode: overview

The shifted CCS is used to compare with a set value for the current (I_{limit}) in the driving and braking Block 3. Input signals come from two contactless handle position sensors, one for driving and one for braking [7] which set the current limit for the torque during driving or braking, see Fig 3.

So, the set value from the drive handle is compared with the output signal CCS from the current measurement block. If the set value is bigger than measured one, the output level on this block is "High" and the power transistor is turned off for a certain time off $T_{\rm off}$.



Fig. 3 Constant off-time current control

The "constant off time" is made with a comparator U_{101A} , an RC circuit (Fig. 4) and the Schmitt trigger in the CPLD. For that reason the control is called is called "constant off time" control. If the set value is less than measured CCS then the output value is "Low" and the power converter makes the current rise until the set value is achieved.

• Driving mode: experimental results

The set value from the gas handle (CH4-green) in Fig. 5 is compared with the CCS (CH1- yellow) and when the CCS increases the set value the capacitor C_{103} is discharged (CH3- magenta). The output voltage of the CPLD is shown by CH2 – blue and the constant off time modulation is 36µs in this case. Note that the real current is less noisy than the measurement.



Fig. 4 Schematic of the driving and braking block



Fig. 5 Diagram illustrating how the constant off time works

CH1(yellow) - shifted CCS in point BCH2(blue) - is the output signal of the CPLD

CH3 (magenta) – is the capacitor C_{103} voltage CH4(green) – is the set value from the gas handle

This type of control is very robust and easily implemented with the combination of analog circuits and a CPLD. For instance, if we would use a hysteresis control, the current signal could be disturbed and the commutation frequency would go in infinity. This cannot happen if we use constant off time control.

• Braking mode - overview

When the brake signal from the control board is activated, the controller switches off all lower transistors and pass modulated signal (common signal) to the upper transistors. The upper transistors short circuit the windings of the BLDC and the phase currents increase until one of them reaches the limit value. The algorithm brakes always irrespectively the motor rotation sense. Also one does not need signals from the Hall sensors which is an advantage that one still can brake, even if some of the sensor signals could be out of order. When the upper transistors are switched off, the current flow

continues and energy is passed to the battery trough the reverse diodes of the transistors. It acts like a step-up converter.

• Braking mode - experimental results

The setup to test the regenerative braking is tested is shown in Fig. 6. The AC induction motor is connected to the power grid through a three phase autotransformer. By this, we can regulate the torque of the AC motor. The AC motor is used to simulate the energy coming from the vehicle and represents the situation like coasting downhill or just braking.



Fig. 6 Setup for testing the regenerative braking mode.

The following diagrams in Fig. 7 and Fig. 8 show the most important signals in this mode. Note that the noise in the currents is an artifact of the oscilloscope with galvanic insulated channels.

Fig. 7 shows the regenerative braking and the commutation frequency of the upper transistors is around 25kHz, the rms value of the current I_a injecting to the supply rail is 39Amps and the voltage is around 152V.

Fig.8 shows braking mode in full short circuit (all upper transistors are switched on), the value of the generated current is around 35A, and the rotational frequency is decreased till 18Hz. This is corresponds to a speed 3,6 km/h (four pole motor, gear ratio around 7, diameter of the wheel 0.5m). At a speed of 3.6 km/h one can still use the mechanical brake to force the vehicle at standstill on a hill. By doing this no electric power is needed while braking at standstill. In Fig. 7 the current is almost sine wave as it is in fact no *BLDC* control.



The braking process dominates on driving, so if the driver pulls both handles (gas handle and brake handle), the vehicle will brake.

Phase advance - overview

The fourth block provides the necessary phase advance on phase current compared to the back emf. If the vehicle moves with high speed and without phase advance (PhA), the BLDC cannot deliver the same torque at high speed and the acceleration will be slow. This phase lagging can be neutralized by a phase advance [8], resulting in a higher efficiency and a higher torque at high speed. Another advantage is that the maximum speed range of the motor is extended even beyond the speed where the peak motor emf equals the battery voltage. If we give PhA on the exciting current this slope will be stronger and will provide the necessary torque. However, PhA between the back emf and the current is not required at low speed, and is not possible in the whole speed range using a simple position sensor. This block provides a second signal when the phase advance is to be switched on or off depending on the speed of the vehicle. Note that we use the control on a motor with surface magnets, where a deep flux weakening cannot be performed.

The principal is that we time from the previous edge to do the PhA. A current source charges a capacitor and its voltage starts to increase linearly, see Fig. 9 point C. A signal with a three times higher frequency is obtained by combining the three Halls sensors signals with EXOR functions. This signal drives a transistor which discharges the capacitor. The peak value of the voltage is hold in another capacitor – point D. One diode drop is used to be made a difference from the maximum value point E. By using a comparator which compares C and D signals we obtain the phase advance pulse. With a small quantity of analog electronics the PhA signal is implemented. From a certain speed on, a comparator with hysteresis on the voltage of point D, gives the signal Phase advance Enable (PhAE) and CPLD combines both of the pulses (PhA and the driving pulse).



Phase advance – experimental results

Fig. 10 shows the main signals into the PhA block and Fig.11 shows the driving pulse to the upper transistor with PhA in case PhAE is in High level.



Fig.10 Common signals of the Phase advance block:

CH1(yellow) the waveform of the voltage in point C

CH2(blue) - the waveform of the PhA signal, CH3(magenta) - the waveform of the signal "3xf" CH4(green) – the potential in point *E*



CH1(yellow) the waveform of the driven pulse to MOSFET,

CH2(blue) – the waveform of the PhA signal, CH3(magenta)- the waveform of the signal "3xf", CH4(green) – signal PhA Enable The Phase advance time is kept constant for the whole speed range of the BLDC.

The results for the no load test are shown in Fig. 12 and gives an impression how much we can expand the speed range of the BLDC. The experiment was made with a variable voltage source and fixed phase advance angle which is 17 electrical degrees at 3000 rpm. As we can see in the area of maximum power supply voltage, the maximum speed without phase advance is about 6000 rpm and with phase advance about 7700 rpm which corresponds to a 28% speed range extension.



Fig. 12 The no-load test

Note that the motor has surface magnets but that still a significant speed extension is reached. The increase of speed range is an advantage, but it realized at the expense of increasing the no load losses with 30%.

The setup for the load test is shown in Fig. 13. The both BLDCs machines are identical. The BLDC1 is used for driving and the second BLDC2 is used for electrical braking.



Fig. 13 Block diagram of the load test



The obtained results for this test are presented in Fig. 14.

Fig. 14 The load test results, power supply voltage of the power stage is 55V, where the different values of the PhA is tuned at 2000 rpm and PhAE is "0" (PhA is switched off)

As we can see from Fig. 14 even small values of the phase advance angle can increase the speed of the rotor and keeps this difference for the investigated range. To illustrate what the benefit of the implemented phase advance is on the performance of an ultra-light electrical vehicle, consider the following example. At 1881 rpm the speed of the vehicle will be 25km/h, with additional PhA 5° the motor speed is increased with almost 60 rpm, so the speed will increase to 26.1km/h.



Fig. 15 Current waveform without PhA:

CH1(yellow) the waveform of the driven pulse to MOSFET

CH2(blue) – the waveform of the CCS

CH3(magenta)- the waveform of the coming from Hall sensor "A"

CH4(green) – the waveform of the current I_a



Fig. 16 Current waveform with PhA: CH1(yellow) the waveform of the driven pulse to MOSFET CH2(blue) – the waveform of the CCS

CH2(blue) – the waveform of the coming from Hall sensor "A"

CH4(green) – the waveform of the current Ia

Fig. 15 shows the waveforms of the driving signal to the upper MOSFET by CH1 without PhA, the current through it by CH4, the CCS by CH2 and the Hall sensor's A signal. As we can see the ripples in CCS are small and this means the torque ripples are smaller [9].

Fig. 16 shows the waveforms of the driving signal to the upper MOSFET by CH1 with PhA, the current through it by CH4, the CCS by CH2 and the Hall sensor's A signal. As we can see the ripples in CCS are higher compare with the case without PhA but they are acceptable.

Temperature measurement

A temperature measurement Block 5 is used to protect the power stage and BLDC motor from overheating. Otherwise the permanent magnets could be demagnetized [9]. Two NTC sensors measure the temperatures of the power converter and the BLDC motor, also processed by CPLD.

Position estimation block

The position estimation Block 6 consists of Hall Sensors on the motor. This block is an interface between the Hall Sensors and the CPLD and contains pull up resistors as the Hall sensor outputs are open collector. The developed controller is shown in Fig. 17.



Fig. 17 Picture for PLD based BLDC controller.

Power supply

The power supply is based on self oscillating principle [10] with very low consumption in stand–by mode. It uses zero voltage switching which means high efficiency and high electromagnetic capability.

Power stage

The power stage is Block 8 of the controller and the block diagram is shown in Fig. 18. It consists of three legs (half-bridges), each with two transistors. The lower transistors in the half-bridge are IGBT's and are used for quadrant selection (S_2 , S_4 and S_6), the upper transistors (MOSFET's) are used for current control (S_1 , S_3 and S_5). This topology of power stage reduces the switching losses near to three times [11]. If the maximum of the absolute value of all currents exceeds a set value the active constant off time control transistor is turned off. The power stage still includes a Desaturation Protection (DP) [11] on the lower transistors in case of any malfunctioning. The DP follows the IGBT's collector emitter voltage which is related to the collector current through the power switch. The DP is a maximum current protection and if the current exceeds certain value the lower transistor is switched off for several milliseconds, the current starts decreasing. In this way we are able to prevent demagnetizing of the PM by limiting the maximum current through the BLDC [9].



Fig. 18 Block diagram of the power converter where: HA, HB and HC are driving signals to the upper transistors, LA, LB and LC are driving signals to the lower transistors, OC – optocouplers, DP is the desaturation protection, PS power supply

BLDC motors

According to the manufacturer, the efficiency of the BLDC with external rotor is 91%. The main parameters of the BLDC motor are shown in Table 1.

	Supply voltage [V]	Power [W]	Torque [Nm]	rpm [min ⁻¹]
Nominal parameters	100	1500	2.5	4300
Maximum parameters	140	4500	10	6000

Table 1: Main parameters of the BLDC

At nominal voltage, the losses into the motor are around 145W and with PhA they increase to 190W. As said before, the controller is able to operate motors with high number of pole and high rpm.

Conclusions

By combining the CPLD with analog circuits to generate the input signals, a very robust and lowcomplexity controller is obtained. The operation of the BLDC controller has been experimentally verified both without and with phase advance. The obtained results show that the low-complexity approach works and achieves satisfactory torque control. So, the choice of operating a BLDC drive by a PLD only, without processor allows several advantages:

1. A high reliability by the low complexity and low cost.

2. Easy to program in Hardware Description Language (HDL), Verilog or Schematic layout of the logical circuit in ISE [12], inputs and outputs can be reconfigured flexibly.

3. The CPLD has a very low consumption (2..3 mA) [6], with optocouplers and current sensors added the total consumption current doesn't exceed 90 mA on a 12V power supply.

4. The constant off time control is easy to be implemented with a small quantity of components and is more reliable than hysteresis control. For instance if the current signal is disturbed and we use hysteresis control the commutation frequency would go in infinity. This cannot happen if we use constant off time control.

5. At nominal voltage, the phase advance is able to extend the speed area of the BLDC significantly.

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