Industrial and Technical Aspects of Chip Embedding Technology

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Abstract

Embedding of semiconductor chips into organic substrates allows a very high degree of miniaturization by stacking multiple layers of embedded components, superior electrical performance by short and geometrically well controlled interconnects as well as a homogeneous mechanical environment of the chips, resulting in good reliability. At PCB manufacturing level, 50 µm thin chips have been embedded with pitches up to 200 µm in up to 18”x24” panels. Embedding of chips at 100µm pitch has been achieved at prototype level. Further developments of chip embedding can extend to even finer pitches without redistribution methods only with concurrent developments in ultra fine line patterning, plating methods and chemistries, assembly machines. New manufacturing processes should combine PCB processing and die assembly in one production line in order to benefit the most from this combination without the difficulties of transport between different manufacturing plants. Furthermore, new testing methodologies will be developed and a new supply chain will be created due to incorporation of embedding technologies to PCB production. This paper discusses in detail the technology and manufacturing challenges arisen from the integration of embedding technologies to PCB manufacturing processes.

1. Introduction

In most electronic systems, there is a continuing pursuit of further miniaturization and increased functionality. Current technologies provide organic substrates with high-density build-up layers and microvias, equipped on both sides with surface mount passive components and active chips in packages. The technological front has rapidly advanced from a 2D system-in-package (SiP) integration to a 3D-SiP integration to keep up with miniaturization trends. Towards this technology direction, chip and component embedding turns out to be a very promising technology route for even higher 3-dimensional integration of components. System requirements for signal frequencies in the order of several GHz can not be met by long bond wires and extensive interconnect paths on a board. In order to maintain signal integrity, much shorter and impedance-matched interconnects are required. Embedding allows to have conductors not only under but also over a component leading to a 3-dimensional packaging also on top of the embedded components. The component can be electrically connected to the top or bottom conductive layer or to both of them, e.g. in case of power ICs with contacts on both sides. A number of different embedding approaches have been presented in the past and a good overview is given in [1]. Among the most recent technologies, an Integrated Module Board (IMB) technology was developed by Helsinki University of Technology and industrialised by Imbera, with which chips are embedded in cavities into the core substrate [2].

In the frame of the EU-funded project “HIDING DIES” partners from industry and research organisations developed an embedding technology which is based on the "Chip-in-Polymer" concept of Fraunhofer IZM [3].

The basic concept remains the embedding of thin chips into build-up layers by the use of well established printed circuit board (PCB) technology. Electrical contacts to the chips are realisd by laser-drilled and metallised microvias as schematically shown in Figure 1.

Within the HIDING DIES project, the generic technology was further developed to offer versatile solutions for the realization of 3D-SiP modules. As a successor of HIDING DIES, a new EU-funded project “HERMES” has inaugurated with wide participation of European industries and research institutes with a broader scope of furthering the embedding technology borders at R&D level and more importantly of bringing embedding technology in real manufacturing PCB production. This paper intends to address all pertinent technical and industrial issues associated with industrialization of embedding technologies and make a brief introduction of the HERMES project to the international electronics manufacturing community.

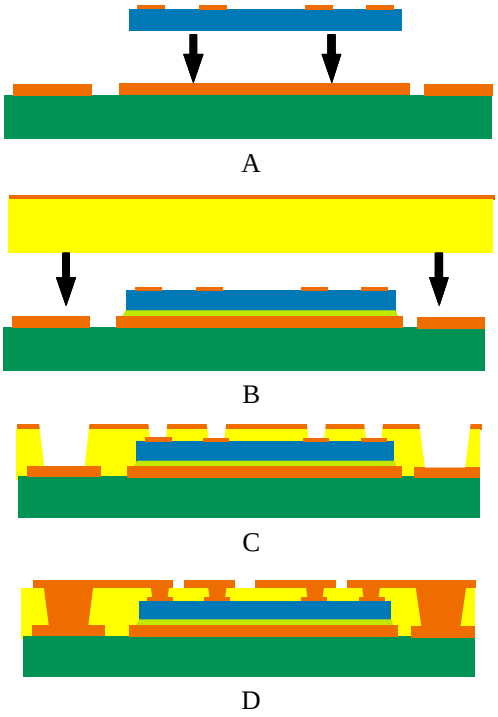

Figure 1. Process steps of chip embedding: (a) die bonding, (b) embedding in a polymer layer by vacuum lamination, (c) laser drilling of vias to chip and substrate, (d) metallisation of vias and Cu structuring.

2. Technological & Industrial considerations

Embedding technologies offer significant advantages in the miniaturisation of electronic systems and larger versatility in "More than Moore" roadmaps by facilitation of heterogeneous integration of electronic functions. Within the scope of this paper, the highlights of the embedding technologies will be briefly discussed and embedding technology challenges will be elaborated:

2.1 Technological drivers

Space: Embedded components leave more space for component placement on top and bottom of the board, making it easier to put passive components (resistors, capacitors) close to the active device, and also making routing easier (in less layers).

Eliminate wirebonding: Most packages of Si chips contain wirebonded chips which are moulded in polymer; by embedding the bare dies, the connections are made by PCB process steps, which eliminates wirebonding technology and overmolding. In this way, it is beneficial to integrate embedding technologies in PCB manufacturing environment.

Eliminate underfill: Embedded components do not need to be underfilled for reliability performance as it is for flip chip packages

BGA alternative: Embedding Si dies is a sound alternative for complex small pitch BGA packages (< 0.4 mm pitch is very difficult and not reliable)

Embedding technologies as alternatively shown in Figure 1 also greatly improve the system functionality of electronics among others by better RF performance and EMI shielding, low power demands and better heat dissipation solutions.

2.2 Manufacturing and market drivers

Low cost production: Through the large-scale production that is typical for PCB manufacturing, major cost improvements can be expected, provided that the yield can be optimised and controlled.

Equipment infrastructure: Many equipment developments for packaging and PCB manufacturing have become available. Wafer grinders, accurate placement machines, laser direct imaging equipment have been improved in quality, are fast enough, and are available at reasonable prices. This provides an industrial base for implementing fine-pitch packaging technology on large-scale PCB manufacturing lines.

Short time-to-market: Integration of embedding technologies in a PCB manufacturing line can ensure short time production of SiPs by actually merging front-end with back-end packaging segments in electronic packaging.

3. Technical aspects & challenges

Embedding technologies are about to be brought to a more advanced level of interconnection at finer chip pitches and interconnection lines regardless which innovative embedding technology strategy has been employed. The common trend in all technologies is even more precise placement and die bonding for better microvia alignment in combination with high speed die placement at high yield. In the HIDING DIES project, by using Fraunhofer IZM's Chip-in-Polymer technology, 50 µm thick chips with 100 µm I/O pad pitch were embedded without use of costly and fragile RDL layers. Figure 2 shows a chip embedded in RCC layers and a filled microvia, at a I/O pad pitch of 200 µm [4].

The major technical issues associated with embedding technologies at research and industrial level which will be also addressed in the HERMES project are discussed below.

3.1 Wafer preparation

Laser drilling of microvias and the PCB metallization process is not compatible with Al or Cu contact pads of semiconductor chips. Therefore, a further layer of 5 µm Cu is applied to the bond pads of the chips to be embedded. Other metallisations such as electroless Ni/Pd can be optimised for microvia plating. Passivation layers can be tested for their fragility as well as for their adhesion with the RCC laminate layers.

3.2 Chip placement and bonding

Placement accuracy is extremely crucial for chip embedding. The process tolerances for sequential die

bonding, via drilling and Cu structuring (Figure 1) have to be very low in order to achieve an acceptable yield. One of the requirements is that the machines for these three process steps should use the same alignment fiducials on the core substrate. Especially large substrates are multilayer cores with small thickness and provide very low contrast to fiducial marks.

Prior to chip placement, die ejection from a dicing blue tape takes place and should be optimised according to the adhesiveness of the tape, size and ultimate thickness of the chip. Adhesiveness of the tape is regulated by UV exposure and is to be reduced for component pick-up and placement without endangering the chip integrity.

Additional requirements to the placement accuracy are related to the PCB vision system. The PCB camera has to be able to cover the entire range of the proposed multilayer PCB cores as well as the problems related to the low contrast fiducial marks. Developments concentrate on the dynamics and the mechanical design of gantry systems to assure access to all PCB areas as well as to the dynamical behaviour of the gantry. Furthermore, a die bonder machine should have an advanced conveyor system. Support systems in the conveyor have to be developed to meet the tough thickness requirements. Warpage induced imperfections due to panel thickness should be bypassed by innovative conveying, supporting and clamping concepts. The conveying concept also has to assure minimal vibrations of the panel during the die bonding and other placement operation.

Chip bonding has been developed by using printable pastes and die attach films (DAF). Screen printing allows a precise control of volume and location of the adhesive paste, which is rather a problem for dispensing. Electrically conductive Ag-filled pastes or B-stage pastes can be used. Another method is the use of a die dicing attach film (DDAF). It is a UV dicing tape which has two layers, a conventional UV dicing foil and an adhesive layer on top. Wafers are mounted on the adhesive layer. The dicing blade has to cut the silicon and the top layer of the tape. In the picking process this layer remains at the chip and serves as adhesive. Die attach films have shown superior adhesive coplanarity compared to printed pastes, which is extremely important for precise epoxy thickness over the chip after RCC lamination, and for avoiding chip cracking. By using a Datacon 2200 apm placement and bonder machine a placement accuracy of ±10µm at 3σ was achieved on 18”x12” panels with a placement speed of 1000 components/hr [4].

3.3 Embedding by RCC lamination

The core substrate with the die bonded chips is covered from both sides with a RCC layer. Temperature and pressure profiles should be adjusted carefully to promote epoxy adhesion at all interfaces and avoid chip breakage. A thickness of 15-20 µm over the chip surface is desirable for the subsequent microvia opening and filling. The overlaying Cu layer serves as the base for package routing. Curing of the epoxies take places at about 185 °C for 60min. Detailed description of the lamination process is given in [5]. In the HIDING DIES project, multi-chip embedding up to 2 chip stacks has been successfully demonstrated. In the HERMES project, embedding of 4-chip stacks will be attempted to for higher 3D integration. A stack of embedded 4 chips is depicted in Figure 3. New developments in RCC laminates can improve significantly the adhesion on the chip surface and the reliability of the embedded packages by new epoxy formulations with adjusted thermo-mechanical properties.

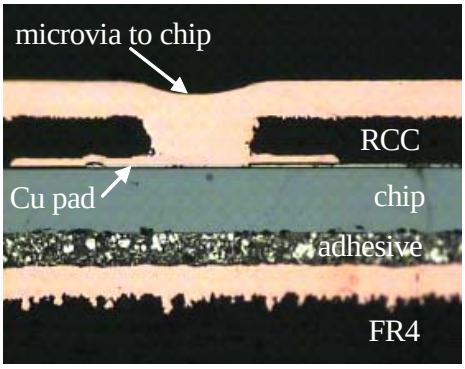

Figure 2: Cross-section of a microvia interconnect to an embedded chip.

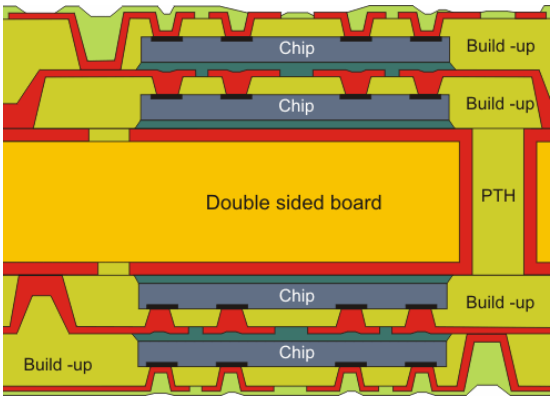

Figure 3: Delineation of 4-chip level embedding concept.

3.4 Ultra fine pitch interconnection methods

In the Chip-in-Polymer technology, interconnections are achieved via microvia laser drilling to chip pads and subsequent metallization, similarly to the established formation of microvias on PCBs. For microvia drilling a pulsed 355 nm UV laser has been used. It can ablate Cu as well as the RCC dielectric. Accurate alignment of the microvia drilling with respect to the underlying Cu pattern remains challenging for the yield of the interconnection. With the current I/O pad pitch (min. 150 µm) and the enlarged Cu pads on the chips, alignment based on fiducials on each 10x10 cm² (sub-)panel are sufficient. For smaller pitches it is expected that local fiducials, closer to each chip, will be necessary. After drilling, the microvias are chemically cleaned and then

treated by a Pd activation and electroless Cu deposition. The Cu layer is around 1 µm thick and acts as a seed layer for the consecutive Cu electroplating. A minimum thickness of 10 µm Cu is required in the microvias. By the use of special Cu plating chemistry a nearly complete filling of the microvias can be achieved, as shown in Figure 2. For pitches smaller than 100µm without use of fragile RDL layers, vialess interconnection methods can be alternatively used to avoid the crucial via drilling alignment on the chip pads.

3.5 Copper structuring and ultra fine line patterning

The top interconnection pattern is structured by a maskless process based on laser structuring. First a Sn layer of 1 µm thickness is applied by an immersion process. The conductor design is written into the Sn by laser ablation. The remaining Sn is then used as an etch mask. By a subtractive process, the Cu is etched and the Sn mask layer is stripped. A view on the final structure of an embedded chip with interconnects on top is shown in Figure 4. In HIDING DIES, 50 µm Cu interconnect lines have been structured. Under etching issues restrict the capability of structuring even finer line/spaces. Laser direct imaging (LDI) can simplify the structuring process by avoiding the need of etch masks. A LDI system with a wavelength of 355 nm can fast develop a dry resist to an etching mask. By well controlling the adhesion of the resist on the underlying Copper, the plating and etching chemistries, very fine L/S of 15-25 µm have been the targets for semi-additive processes.

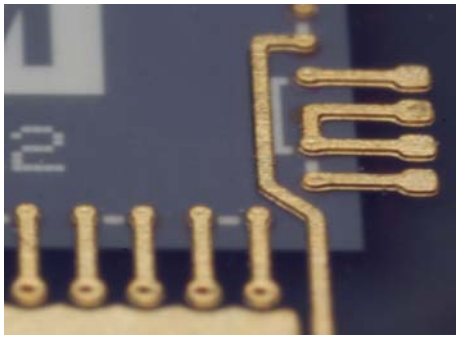

Figure 4: Copper structuring on top of an embedded test chip.

4. Industrial aspects & challenges

4.1 Integration in PCB process flow

One of the main challenges for the adoption of embedding technologies in a PCB manufacturing environment is the advancement of the established PCB process Know-how to meet the requirements raised from the implementation of embedding technologies. Process studies have shown that the existing subtractive technology faces serious problems for copper structuring at line widths of 50 µm and lower. The main problems are the control of the etched design and the uniformity of the line width. The line width uniformity is mainly influenced by variations of the electroplated copper thickness, the etching uniformity in the etching machine as well as the design of the printed circuit board. Variations in copper line width beyond process tolerances are due to fluctuations of the aspect ratio of the cavities etched for deposition of the copper lines. In turn, the aspect ratio variation can be reduced by lowering the copper thickness and/or the resist thickness. On one hand, the reduction of the resist thickness can improve the etching behavior and the cavity design resolution but from the other side the adhesion on the copper layer will be decreased and therefore under-etching phenomena will be triggered and will result in increasing the “opening” rate by the copper tracks. A promising solution is the semi-additive process that has the potential to form lines with high aspect ratios (copper thickness : line width) to provide interconnects with low resistance. The difference to the subtractive pattern technology used commonly in PCB industry is the usage of an ultra thin plating base that is removed by an etching process at the end of the pattern forming process without need to protect the electroplated copper formed pattern with a metal resist. The plating base can be electroless copper with high etching rate on a bare laminate. However, the cleanliness and oxide-free surfaces for the electroless deposition of the copper base still remains challenging in the PCB industry. Alternatively, a very thin copper foil coated on halogen free resin (RCC) can be also used. The copper foil should have a similar etching behavour as the corresponding electroless copper and a well tuned bonding strength for good adhesion on the epoxy but in parallel ease of complete removal by etching.

The integration of silicon components in the PCB manufacturing for the implementation of the embedding technologies is another challenging issue that requires much work until a new supply chain for the PCB industry is created due to adoption of embedding technologies. Extensive studies on component testing, component delivery for assembly needs, cleanliness of components etc. and their effect on overall yield and cost will raise the level of maturity and confidence for a progressive integration of embedding technologies in the PCB manufacturing floor. Besides the new supply chain for embedded components, new component assembly and plating equipment for semi-additive process should be integrated in an industrial process flow. Newly developed assembly machines should be able to pick and place components on PCB large panels e.g 18”x 24” in size with outstanding accuracy, high speed and yield. The semi-additive process for ultra fine line and ultra fine pitch processing will also require new plating machines which have to be also compatible with large panel sizes.

4.2 Manufacturability

The greatest potential of embedding technology can be only exploited with a set-up of an integrated manufacturing process that includes PCB processing and die assembly in one production line, in order to benefit the most from this combination (gaining density, shorter routing, space for SMD component assembly) without the difficulties of transport between lines and manufacturing plants.

4.2.1 PCB manufacturing equipment

Adaptations of PCB manufacturing equipment and processing parameters is needed to fulfil the requirements of embedding technology : board handling, procedures, automation, process control, inspection, etc. For the realisation of the chip embedding technology, modified and dedicated equipment for embedding and ultra-fine line technology is a must. From equipment viewpoint, verification and optimization of process parameters should be performed for defect reduction. Modification in transport systems and new handling concepts can reduce significantly mechanical damage of the board image. Modifications in software tools for AOI systems are needed and the usability regarding amount of pseudo defects and not recognized defects can be evaluated. Board handling in the AOI area and the prevention of mechanical defects will be another issue as well as cleanliness.

4.2.2 Die assembly equipment & registration accuracy

For the purpose of extending embedding technologies to chips with very fine pitches without RDL processing, very accurate placement machines should be developed and used. These machines can have the following distinctive characteristics:

- Die ejection and pick and place operation from the wafer for thin chips (50µm) up to 0.3 by 0.3 mm²
- Handling of wafers with UV-tape
- Wafer mapping data for component selection
- Appropriate multi-component capability
- Chip alignment with fiducials on the active chip side (top side)
- Chip placement accuracy 10 µm at 4 σ on a board size of 18”x 24”
- Appropriate placement speed

The development of such a placement machine follows the equipment advanced packaging and assembly industrial roadmaps. Complete analysis of accuracy issues for an embedding technology adapted to PCB manufacturing should entail accuracy of die dimensions, placement, global and local fiducials, via formation, line definition accuracy, etc. The effect of overall registration accuracy on yield and in turn on cost should be taken into consideration for further developmental plans for improving further the registration accuracy. Such continuing development efforts will influence the overall cost of transferring embedding technologies in the manufacturing environment.

4.2.3 Testing

Testing methodologies for embedded silicon chips should be developed for use in large scale production. Test strategies should contain AOI, AXI, electrical ICT and functional testing and should define which components will be tested and the confidence levels of the measurements.

4.3 Supply chain & Standardisation

The integration of embedding technologies requires changes in the supply chain for PCB industry and the need for organising a new chain in PCB industry specifically for embedding technologies. Additionally, standardization for tools, design formats, component geometries, testing is necessitated for promoting embedding technologies in all facets of manufacturing industries.

4.4 Yield analysis

Critical step for the industrialisation of embedding technologies is a thorough yield analysis of all the process steps at manufacturing level. A yield model that will be able to identify all critical parts in the processing is needed. As a result of machine, process, handling and registration optimisation the product yield can be derived. With a yield database, corrective actions can be taken for yield improvement. The yield data have to be used for cost modelling and via the cost modelling a target can be defined to estimate if the industrialisation of chip embedding technology is possible.

In specific, assembly manufacturers have to focus on yield analysis for the pick-and-place operation. Based on existing methods tools and vehicles can be developed to measure and improve chip assembly yield covering all aspects. The main focus areas are placement accuracy, chip defects resulting from pick and place process, software issues and component reject rate. Extensive evaluation tests have to be performed to validate the process yield and the yield-model. The experimental yield tests for the pick and place process will be used to determine most yield critical elements. The results and root cause analysis will constitute the basis for equipment and software improvements. All individual process yields of front-end and back-end processes should be combined to an overall manufacturing yield. Yield becomes increasingly important for those process steps that follow the chip placement. A high yield is necessary to reduce (expensive) scrap of production panels.

4.5 Cost modelling

Embedding components into a printed circuit board requires a manufacturing approach that is very much different from the classical PCB manufacturing followed by board assembly. Embedding can be also pursued by various scenarios which can have a different effect on the process cost. Based on different embedding scenarios, the process steps will be identified and the yield associated with each process step will be estimated. An overall cost model will be derived which can give clear indication which embedding scenario could yield a more economical manufacturing process. Assembly manufacturers can determine the cost of ownership related to pick and place operations and electronic assembly industry. Based on experiences in providing industrial customers reliable data to determine cost of ownership in the world of surface mount assembly new models have to be developed and adopted to the process developed for embedding components. Manufacturing facilities should incorporate these cost elements in all other manufacturing facets to come up with an overall cost model. The cost model can work as a feedback for tracking the most expensive process steps and try to find possibly alternative ways to reduce individual process cost and therefore the overall manufacturing cost.

5. Conclusions

Industrialisation of embedding technologies is the next step taken after the successful validation of embedding technologies at prototype level. New [7] undertaken efforts try to set up a new business model by merging the split business segments of PCB manufacturing and component assembly. The goal is a new integrated manufacturing line to offer low cost solutions for high density electronic systems. Many technological and manufacturing challenges arise from the industrialisation of component embedding technologies. The new manufacturing process should combine PCB processing and die assembly in one production line in order to benefit the most from this combination without the difficulties of transport between different manufacturing plants. Furthermore, new testing methodologies have to be developed and a new supply chain will be created due to incorporation of embedding technologies to PCB production. The conventional PCB manufacturing supply chain can be significantly changed with an inevitable impact on manufacturing cost. Therefore, new cost models stemming from the challenging merge will be generated. From a technological standpoint, ambitious technology objectives are set up for ultra fine line patterning at 15-25µm and ultra fine pitch embedding. These goals can become reality with a new very thin copper plating base, semi-additive processes, new plating platforms and chemistries and precise placement machines. A yield model should work as guide for corrective actions in the individual process steps for process optimisation.

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References

1. S. Norlyng, “Integrated component technologies: Opportunities, economics and trends”, IMAPS Nordic, October 2003.
2. T.Waris, R. Tuominen, J. Kivilahti, “Panel-sized inte grated module board manufacturing”, Proc. Polytronics Conference, Oct. 21- 24, 2001, Potszam.
3. A.Ostmann, A. Neumann, P. Sommer, H. Reichl, “Buried components in printed circuit boards”, Advancing Microelectronics, May/June 2005, pp. 13- 18.
4. A.Ostmann, D.Manessis, A. Neumann, H.Reichl, “Lamination technology for system-in-package manufacturing”, Proc. Microtech 2007-IMAPS UK, 6-7 March, 2007, UK.
5. D. Manessis, S-F.Yen, A. Ostmann, R. Aschenbrenner and H. Reichl, “Technical Understanding of Resin Coated Copper (RCC) lamination processes for realisation of reliable chip embedding technologies”, Proc. Electronics Components & Technology Conference (ECTC) 2007, Reno, NV, May 29- June 1, 2007, pp. 278-285.