Today's High Level Synthesis tools: a comparison

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Abstract:
High-level synthesis (HLS) tools greatly reduce the effort required in Register Transfer Level (RTL) design by automatically converting behavioral algorithms into synthesizable hardware descriptions. These tools are being actively developed, and even though they have been around for more than 10 years, they have only recently been adopted by industry.

As a result of the reduced designer effort, advantages of high level synthesis include an improved time to market and the possibility to do extensive design space exploration.

In this work, we present a comparison of some of today's tools based on our own experience of implementing an image processing algorithm. Different features are highlighted, such as design entry, capabilities, synthesis results, verification options and the learning curve for the designer. We have found that the high-level synthesis tools greatly differ in their features and also in the types of applications they can handle.

Because of design space exploration capabilities, the quality of HLS generated hardware is comparable to manual RTL design, in terms of area, latency and also power consumption. Among the tools that we have evaluated so far, the most impressive results were obtained using Catapult C from Mentor Graphics.

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