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A very compact 1MS/s Nyquist-rate A/D-converter with 12 effective bits

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***Abstract*— We present a very compact analog-to-digital convertor (ADC) for use as a standard cell. To achieve an inherent accuracy of at least 12-bits without trimming or calibration, extended counting A/D-conversion is used. Here, the circuit performs a conversion by passing through two modes of operation: first it works as a 1st-order incremental convertor and then it is reconfigured to operate as a conventional algorithmic converter. This way, we obtain a Nyquist-rate converter that requires only 1 operational amplifier and achieves 12-bit accuracy performance in 13 clock cycles with 9 bit capacitor matching. The circuit is designed in 0.18 μm CMOS with a thick oxide option. The resulting analog core occupies a chip area of only 0.011 mm^2 and the complete digital control and reconstruction logic (including additional test features and storage registers) is 0.02 mm^2. The analog blocks of the circuit consume 1.2mW and the digital 0.4mW. At a sample rate of 1 MS/s, the peak SNDR is 74.5dB and the dynamic range is 78dB, constant over the Nyquist band. The worst-case integral non-lineairity (INL) is within ± 0.55 LSB.**

I. Introduction

In signal processing applications, oversampling converters (such as sigma delta modulators) have a clear advantage over Nyquist-rate converters due to their heavily relaxed anti-aliasing filter requirements. However, in various systems Nyquist-rate A/D conversion is preferred: e.g. to convert multiple multiplexed channels or to do a conversion 'on demand' between asynchronous periods of inactivity. Also in a standard cell A/D-converter, Nyquist-rate operation is usually more intuitive than oversampled operation. In this case, also the chip-area is very important. Recently, successive approximation register (SAR) converters have been convincingly shown to be the most efficient Nyquist-Rate converters in the 8-10 bit range [1], [2]. However achieving more than 10-bit matching requires an unacceptable silicon area. Although calibration allows to achieve upto 12-bit linearity in a SAR converter [3], this is also at the expense of increased chip area. Moreover it complicates the testing time. Incremental converters form an alternative, but in order to achieve good performance a high-order converter is needed, which again leads to a relatively large chip area. In this work, we use a first-order extended counting [4], [5] and achieve better than 12 effective bits in an extremely small silicon area with a conveniently low clock frequency of only 13 MHz.

II. Extended counting

A. Principle

Extended counting A/D-conversion consists of two modes of operation: the first mode is the counting mode and the second the extended mode. In the counting mode the most significant bits are determined and the converter functions as an incremental converter (a $\Sigma\Delta$ modulator that is reset at the beginning of a conversion period). In this mode, the converter is insensitive to capacitor mismatch, which enables high accuracy operation. In the extended mode, the same hardware is reconfigured to do an algorithmic A/D-conversion to convert the lower bits. Here the accuracy is limited by capacitor mismatch but this is not a problem because only the least significant bits are converted.

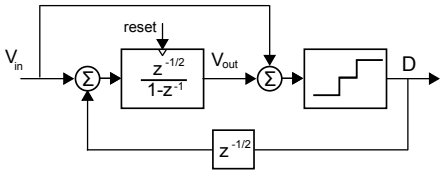

Fig. 1. Signal flow diagram during the counting conversion mode.

In this work, a first-order incremental conversion is used in the counting mode. A higher-order incremental conversion is also possible, but this leads to a large silicon area [6]. The corresponding system-level diagram during the counting mode is shown in Fig. 1. It consists of a 1st-order $\Sigma\Delta$ modulator with a 3-level quantizer and an input feedforward branch. The input feedforward branch is needed to reduce the signal swing at the output node of the integrator (V_{out}) [7]. The threshold levels of the 3-level quantizer are determined in order to further reduce the swing at the output node of the integrator (V_{out}). For this, the threshold levels have to be set to $\pm\frac{V_{ref}}{2}$. This way, the output swing is reduced to $\pm\frac{V_{ref}}{2}$. This is a significant improvement over prior extended counting converters [5] where the output swing was as high as $\pm 2V_{ref}$. It is important that the quantizer uses only 3 levels. This way we can use an inherently linear 3-level feedback DAC, which is readily available in a differential switched capacitor realization.

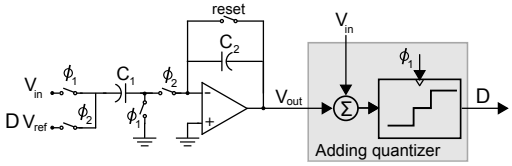

Fig. 2. Single-ended equivalent circuit during the counting conversion mode.

The circuit configuration during the counting conversion

mode is shown in Fig. 2. In reality the actual circuits are fully differential, but for the sake of simplicity the discussion is done here for a single-ended equivalent. It requires only 1 operational amplifier, 2 nominally matched capacitors C_1 and C_2, some switches and the "adding quantizer". This block consists of the combination of the input feedforward branch which is merged into the comparator block used to implement the quantizer. The operation of the circuit of Fig. 2 goes as follows. The reset signal is only active during ϕ_1 of the first conversion cycle. During ϕ_1, the input voltage V_{in} is sampled on the input capacitor C_1. Meanwhile the quantizer generates the code D_i, which can be 0 or ± 1. During ϕ_2, the top plate of the sampling capacitor C_1 is switched towards the opamp inverting node and the bottom plate is switched towards 0 or $\pm V_{ref}$ depending on the code D_i. Thus we obtain the output voltage $V_{out,i}$ for the ith step:

$$V_{out,i} = V_{out,i-1} + \frac{C_1}{C_2}(V_{in} - D_i V_{ref}) \tag{1}$$

If we have N counting steps, this recursion can be solved by taking into account that we have an initial reset. Then we can write the final counting voltage $V_{count} = V_{out,N}$ after the last counting step as follows:

$$V_{count} = \frac{C_1}{C_2}\left(NV_{in} - \sum_{i=1}^{N} D_i V_{ref}\right) \tag{2}$$

To reconstruct the input voltage V_{in} we can rewrite this as:

$$V_{in} = \frac{\sum_{i=1}^{N} D_i V_{ref} + \frac{C_2}{C_1} V_{count}}{N} \tag{3}$$

After the counting steps, the system goes into the extended conversion mode where the voltage V_{count} is measured by a more efficient but less accurate algorithmic A/D conversion technique, which results in a digital approximation $D_{ext}(V_{count})$ for the residue voltage V_{count}. Errors during the extended conversion are modelled by an additive error ε_{ext}. This error is an unknown function of the residue voltage V_{count}. Then we can write:

$$D_{ext}(V_{count}) = \frac{V_{count}}{V_{ref}} + \varepsilon_{ext} \tag{4}$$

Now we obtaion the overall digital output $D(V_{in})$ as:

$$D(V_{in}) = \frac{\sum_{i=1}^{N} D_i + D_{ext}(V_{count})}{N} \tag{5}$$

By combining this with (3) and (4), and taking into account that the capacitance ratio $\frac{C_2}{C_1}$ inevitably has a mismatch ε this can be rewritten as:

$$\begin{aligned} D(V_{in}) &= \frac{\sum_{i=1}^{N} D_i + (1+\varepsilon)(\frac{V_{count}}{V_{ref}} + \varepsilon_{ext})}{N} \\ &= \frac{V_{in}}{V_{ref}} + \underbrace{\frac{\varepsilon D_{ext}(V_N)}{N} + \frac{C_1}{C_2}\frac{\varepsilon_{ext}}{N}}_{\text{ADC error}} + O(\frac{\varepsilon^2}{N}) \end{aligned} \tag{6}$$

This equation indicates the essential property of the extended counting conversion technique: i.e. the effect of the mismatch errors is divided by N, the number of counting steps.

B. Extended conversion

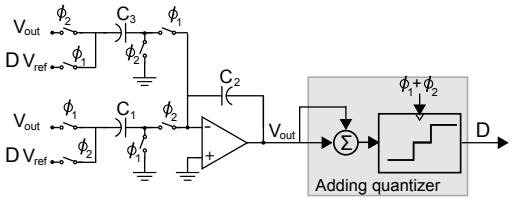

Fig. 3. Single-ended equivalent circuit during the extended conversion mode.

In principle any conversion technique can be used in the extended conversion, but to minimize the silicon area, in our realization, the same hardware is rearranged into a double sampling algorithmic A/D converter [8]. A single-ended equivalent of the configuration is shown in Fig. 3. The operational amplifier and the matched capacitors C_1 and C_2 are the same as for the counting conversion. Only one additional matched capacitor (C_3) is needed. Also the adding flash block is re-used as an ordinary flash block by connecting both input branches to the operational amplifier's output. Since the adding flash compares the sum of its 2 input branches to $V_{ref}/2$, this configuration corresponds comparing V_{out} to $V_{ref}/4$, which is the optimal threshold level for algorithmic A/D-conversion [8]. Due to the double-sampling this circuit updates V_{out} and D during each of the clock phases ϕ_1 and ϕ_2. To understand the basic operation we shall first discuss the even phase. If i is an even number, then at the beginning of the i'th phase the capacitors C_1 and C_2 are charged with the output voltage V_{i-1} of the previous (odd) phase. The capacitor C_2 is in the feedback loop of the operational amplifier. The top plate of the capacitor C_1 is switched towards the inverting input node of the opamp and its bottom plate is switched to $\pm V_{ref}$ depending on the value of the code D_i which was determined at the end of the previous phase. Neglecting the mismatch between the nominally matched capacitors, we obtain the output voltage V_i:

$$V_i = 2V_{i-1} - D_i V_{ref} \tag{7}$$

This voltage is available over the capacitor C_3 that is switched to the opamp output, and over the feedback capacitor C_2. At the end of this even phase the comparator is strobed to generate the next code D_{i+1}.

For the operation during the succeeding odd phase the role of the capacitors C_1 and C_3 is interchanged (fig. 3). For the rest the operation is equivalent to the operation during the even phase. Therefore eq. (7) holds for odd phases as well. To initialize the algorithm the voltage V_{count} is sampled on the capacitors C_2 and C_3 during the last phase of the counting conversion. Similarly the first extended code D_{N+1} is also already determined during the last phase of the counting conversion. If the total of steps in this extended conversion equals M then this recursion formula can be solved for V_{count}:

$$V_{count} \approx \sum_{j=1}^{M+1} 2^{-j} D_{J+N} \tag{8}$$

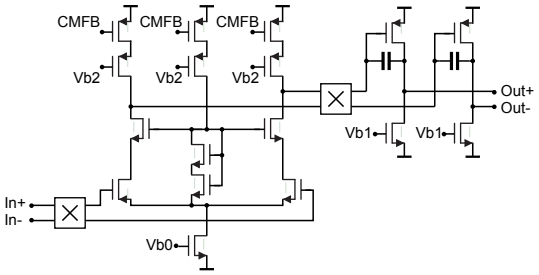

Fig. 4. Miller compensated opamp with chopping at the internal node.

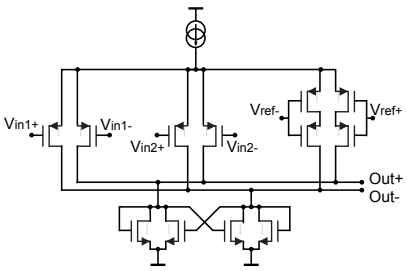

Fig. 5. Circuit for the adding flash.

Therefore $D_{ext} = \sum_{j=1}^{M+1} 2^{-j} D_{J+N}$ can indeed be considered as a suitable digital approximation of V_{count}.

It is well known that the accuracy of this algorithmic conversion is limited by mismatch of the nominally equal capacitors C_1-C_3 [8]. This was modelled by the additive error term ε_{ext} in eq. (4). In our process, small-area capacitors can be matched with 9-10 bit accuracy. Therefore, according to Eq. (6) the number of counting steps N should be at least 8 for 12-effective bits performance. In order to make sure that the performance is not limited by quantisation noise, the extended conversion generates a 12-bit output, which takes only 5 clock cycles. As a result the entire A/D-conversion takes 8+5=13 clock cycles, and generates a 15-bit output codeword, which guarantees that the conversion will not be limited by quantisation noise.

III. CMOS Implementation

The above described structure is designed in a standard 0.18μm process with a thick oxide option. To be able to handle 3 Volt signals, the analog core is implemented with thick oxide devices with a minimum channel length of 0.35μm.

The schematic of the operational amplifier is shown in Fig. 4. It is a 2-stage Miller opamp. To obtain a small silicon area, small devices are used in the input differential pairs, leading to an unacceptable $1/f$ noise. To tackle this, a chopping technique is used. As shown on the figure the chopping is performed at the internal node of the operational amplifier. This way, the chopping transients do not directly couple to the actual capacitors. The chopping frequency is equal to half the switched capacitor clock frequency.

The adding flash must compare the sum of V_{in1} and V_{in2} with $\frac{\pm V_{ref}}{2}$. Since this block is inside the incremental conversion loop, the specifications are quite relaxed. The implementation is detailed in Fig. 5. The addition of the 2 input signals

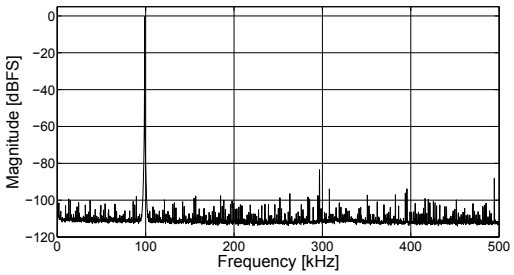

Fig. 6. Typical measured spectrum fora 99 kHz input sine wave (64 $\times$ averaged 2^{13}pt FFT). SNDR = 74.5 dB; THD = 82 dB; signal level = -0.4 dBfs.

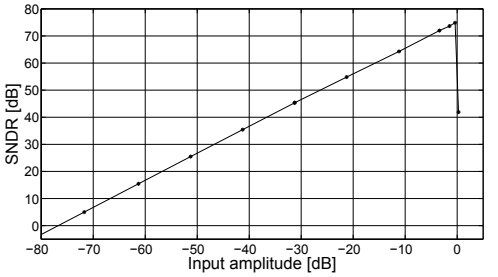

Fig. 7. Measured SNDR vs. input amplitude.

V_{in1} and V_{in2} is performed by parallel connecting two input differential pairs. To ensure a pseudo-linear operation over a large differential voltage range, long and narrow channels are used in the input differential pair transistors to obtain a relatively large gate overdrive at a low current level. The weight of $1/2$ for the V_{ref} input node is realized by using a series connexion of 2 transistors that are matched to the other differential pair transistors.

IV. Measured Results

We measured 15 packaged samples at the nominal sampling frequency of 1MS/s with $N = 8$ counting steps. All measured chips had very similar performance. A typical FFT-result is shown in Fig. 6. Here the converter, is driven by a nearly full scale sine wave with an input frequency such that the 5th harmonic still falls in the Nyquist band. The corresponding SNDR equals 74.5 dB and corresponds to the peak SNDR. The total harmonic distortion (dominated by the 3rd harmonic) equals 82 dB. From the plot no $1/f$ noise can be observed, which confirms the good operation of the chopper. Nearly identical performance is maintained when the input frequency is varied over the full Nyquist band.

Fig. 7 shows the SNDR vs. the input signal level. The plot exhibits a peak SNDR 74.5dB and a dynamic range (DR) of 78dB. All measured samples had peak SNDR and DR values within ± 0.5 dB of this. The dynamic range was also measured by applying a short circuit to the input terminals of the ADC to eliminate the noise of the buffer amplifiers (AD8138). In this case the corresponding dynamic range was 80 dB. From this short circuit measurement also the offset was measured. Although the chopper in the opamp greatly reduces

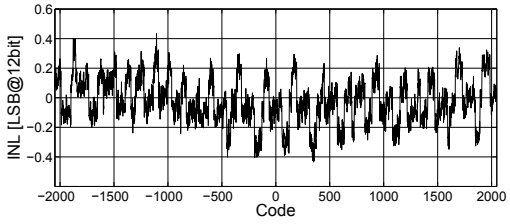

Fig. 8. Typical measured Integral non-linearity (INL) plot versus 12-bit code.

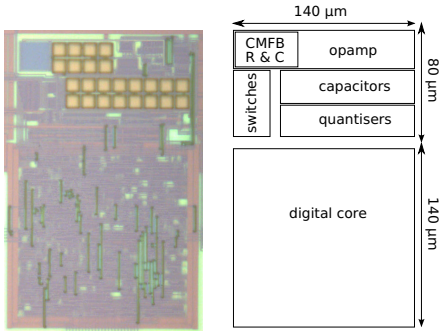

Fig. 9. Chip photo with floorplan.

the offset some residual offset was measured on all samples: this offset was within $[-0.7; +0.2]$ lsb, with an average value of -0.45 lsb.

The INL was measured through a code density test where a low-frequency (10 kHz) sine wave was applied to the input of the converter and 1 Msamples of data were collected with a logic analyzer. To generate the histogram, the raw 15-bit output data were truncated to 12-bit word-length. A typical result is shown in Fig. 8. In the plot the corresponding INL is within ± 0.44lsb@12bit. Of the 15 measured samples the worst case had still an INL within ± 0.55lsb@12bit

The power consumption of the analog blocks (with a 3.3 Volt supply) was 1.2 mW and the digital blocks (with a 1.8 Volt supply) was 0.4 mW. No dependence on the input signal frequency are amplitude was observed. The digital blocks have a lot of basically unnecessary test-functionality, which increases its silicon area and power consumption. A photograph of the chip with an annotated floor plan is shown in Fig. 9. The analog core only occupies 0.011 mm^2. Even with the (unnecessary large) digital circuit included, the complete converter fits in a rectangle of 0.031 mm^2. The performance is summarized in Table I. The FOM is calculated according to: FOM = Peak SNDR + $10 \cdot log10(\frac{P}{BW})$. This FOM is preferred over Walden's FOM because it respects basic noise vs impedance scaling laws [9, p. 357]. From the table it is clear that even in this relatively old technology the chip combines very good performance with an extremely small chip area, which is probably the smallest for a converter with 12 effective bits reported today.

V. Conclusion

We have presented a very compact Nyquist-rate analog-to-digital convertor (ADC) intended for use as a standard cell IP-block. The circuit achieves an inherent accuracy of at least 12-bits without trimming or calibration. For this, it uses extended counting A/D-conversion. This way, we obtain a Nyquist-rate converter that requires only 1 operational amplifier and achieves 12-bit accuracy performance in 13 clock cycles. Another key feature to reduce the silicon area is the use of small devices in the opamp and to eliminate the corresponding excess $\frac{1}{f}$ noise by using a chopping technique. The resulting analog circuit occupies an area of only 0.011 mm^2 and the digital control and reconstruction logic (including many not essential test features and storage registers) is 0.02 mm^2 in 0.18 μm CMOS. To our believe this is the smallest area reported for a complete 12-bit ADC. The analog blocks of the circuit consume 1.2mW and the digital 0.4mW. At a sample rate of 1 MS/s, the peak SNDR is 74.5dB and the dynamic range is 78dB, constant over the Nyquist band. The worst case INL is within ± 0.55 LSB

TABLE I

Performance summary of the 1MS/s ADC

Technology	0.18μm CMOS
Clock frequency	13 MHz
Power consumption	1.2 mW analog 0.4 mW digital (including test)
Dynamic range	78 dB (from sinewave test) 80 dB (from short circuit)
Peak SNDR	74.5 dB
Converter Area	0.011 mm^2 (analog core) 0.031 mm^2 (complete - including all digital)
FOM	159.4 dB (complete - including all digital)
worst INL	within ± 0.55lsb@12bit
worst offset	within $[-0.7 \ldots 0.2]$lsb@12bit

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