Improvement of the phase regulation between two amplifiers feeding the inputs of the 3dB combiner in the ASDEX-Upgrade ICRH system

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Abstract. The present ICRF system at ASDEX Upgrade uses 3dB combiners to forward the combined power of a generator pair to a single line [1]. Optimal output performance is achieved when the voltages at the two input lines of a combiner are equal in amplitude and in phase quadrature. If this requirement is not met, a large amount of power is lost in the dummy loads of the combiner. To minimize losses, it is paramount to reach this phase relationship in a fast and stable way. The current phase regulation system is based on analog phase locked loops circuits. The main limitation of this system is the response time: several tens of milliseconds are needed to achieve a stable state. In order to get rid of the response time limitation of the current system, a new system is proposed based on a multi-channel direct digital synthesis device which is steered by a microcontroller and a software-based controller. The proposed system has been developed and successfully tested on a test-bench. The results show a remarkable improvement in the reduction of the response times. Other significant advantages provided by the new system include greater flexibility for frequency and phase settings, lower cost and a noticeable size reduction of the system.

Keywords: 3dB combiner, phase, DDS, Asdex-Upgrade, ICRF

I. CURRENT ANALOG PLL-BASED SYSTEM

The current system involves two distinct synthesizers for each pair of generators as seen on figure 1. These synthesizers provide the initial signals which are amplified in later stages. The slave synthesizer (S) is driven externally by the internal oscillator (10 MHz) of the master synthesizer (M). The drive signal of the slave synthesizer first passes through a phase shifter that adjusts the phase difference between the two inputs of the 3dB combiner. The appropriate phase correction in the slave line is determined by a mixer whose output is a measure of the phase difference between the voltages at the combiner inputs. After low-pass filtering, the resulting signal is forwarded to the phase shifter which then locks the phase between S and M to 90°. The main limitation of this analog phase lock loop (PLL) system is the long response time as shown in figure 2 (a). Indeed, the measurement shows that several tens of milliseconds are required to achieve a stable state. During this response time, only a small amount of the available power is forwarded to the combiner's output. A large fraction of the power is thus lost due to dissipation in the 50Ω dummy loads. These losses can become even greater if the generators need to be switched off due to an arc in the line or due to a peak in the reflected power. In this case, the generators restart automatically after approximately

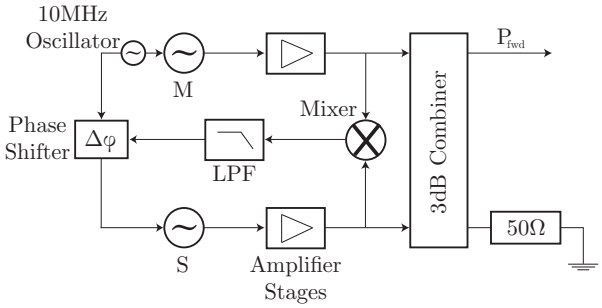

FIGURE 1. The current analog PLL system: the oscillator of the slave synthesizer (S) is driven by a phase shifted version of the internal oscillator of the master synthesizer (M)

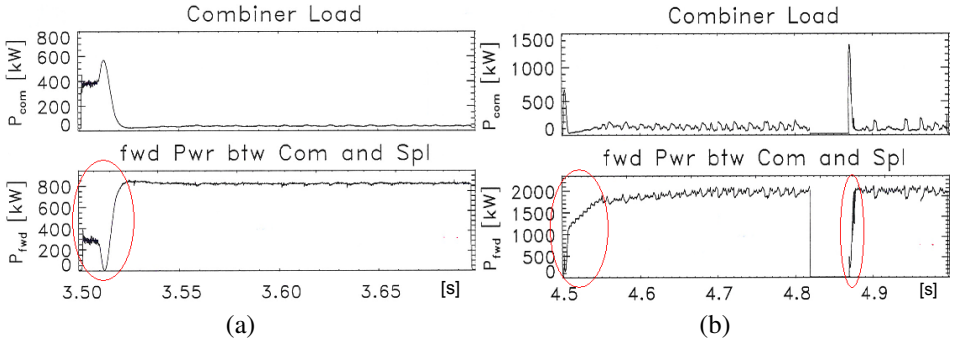

FIGURE 2. Slow response times in the current analog PLL system result in considerable losses in the combiner's dummy load and a drop in forwarded power

50ms. In this critical situation, the phase regulation system adds some ten milliseconds to the break delaying the re-establishment of maximum output power delivered by the combiner as seen on figure 2 (b).

II. PROPOSED DDS-BASED SYSTEM

In order to improve the response time of the current system, we make use of a multi-channel direct digital synthesis (DDS) device. In recent years, these devices have increasingly been used as an attractive alternative to analog-based PLL circuits as they are compact, digital frequency synthesizers that allow creation of arbitrary waveforms from a single, fixed-frequency reference clock with great precision. The architecture of the proposed system is shown in figure 3. Our test-bench uses the 409B from Novatech Instruments which includes a 32-bit AD9959 4-channel DDS from Analog Devices steered by a programmable microcontroller. The latter updates the DDS's registers to generate the required signals. The microcontroller receives its instructions via serial communication (RS232) from a software-based controller which runs on a PC as a real-time process. During the phase regulation feedback, these instructions consist of the phase settings of the DDS channels. The controller reads from a USB-based NI-6009 data acquisition card from National Instruments which samples the output signal of a phase

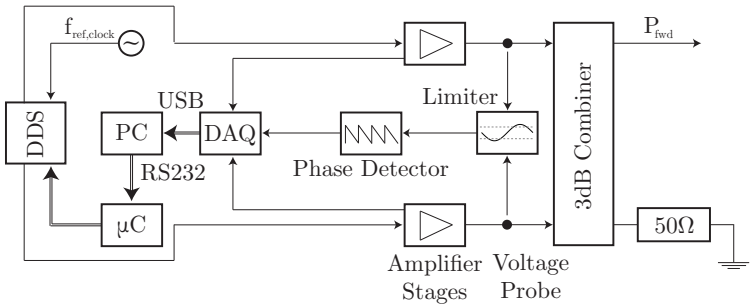

FIGURE 3. The proposed phase regulation system: a 4 channel DDS driven by a PC instructed microcontroller adjusts the phase difference between the generators for two generator pairs

detector as well as trigger signals (ON/OFF) from the amplifier stages at a sample frequency of 1.6kHz. The phase detector's output is a DC voltage which is a measure for the phase difference between the two RF signals obtained by voltage probes at the inputs of the combiner. A limiter is placed between the probes and the phase detector for proper amplitude conditioning: the phase error of the detector is approximately 2° when the amplitudes are equal, but increases rapidly with increasing amplitude difference. The software controller, written in C++, is a multi-threaded application: different tasks (data acquisition, microcontroller steering, ...) run concurrently. The application has two operation modes: static mode and automatic feedback mode. The static mode allows (via a graphical interface) to set the frequency and phase of the DDS channels and observe the real-time measurements. In the automatic feedback mode, the software continuously sends instructions via serial link to the microcontroller to adjust the generator phasing in order to meet the phase quadrature requirement at the input of the combiner. Since 4 channels are available, the adjustment is made for two combiner systems. As is the case with the current phase regulation system, each generator pair has a master and slave generator. Thus, during feedback, the DDS only alters the phase setting of the slave generator for each pair. Since the controller is a purely digital system, the changes to the phase are discrete. The time between each phase adjustment depends – in first order approximation – on the baud rate of the serial link and the microcontroller's processing speed. Figure 4 (a) shows the pulses sent on the RS232 serial link as well as the voltage output $\mathrm{V}(\Delta\phi)$ of the phase detector for a baud rate of 57.6kB. The time $\mathrm{T_{pulse}}$ required for the largest instruction to be written on the serial link to the microcontroller is approximately 1.7ms. Increasing the baud rate decreases $\mathrm{T_{pulse}}$ but introduces bit errors on the line which result in longer system response times as the instructions must be repeated. The microcontroller adds another 0.2ms to process the instruction and update the DDS registers, after which the phase of the corresponding slave generator is changed. The total execution time lapse $\mathrm{T_i}$ between the sending of an instruction from the software controller and the adjustment of the phase thus equals 1.9ms approximately. Since we adjust two channels, i.e. the slave channels of the two generator pairs, the delay between each generator pair adjustment is 1.9ms and the step time between each iteration for a single generator pair is 3.8ms. Figure 4 (b) shows the performance of the control system on the test-bench for two generator pairs with an initial 60° phase difference ($\Delta\varepsilon = 90^\circ - 60^\circ$) between master and slave generator of each pair. The feedback is acti-

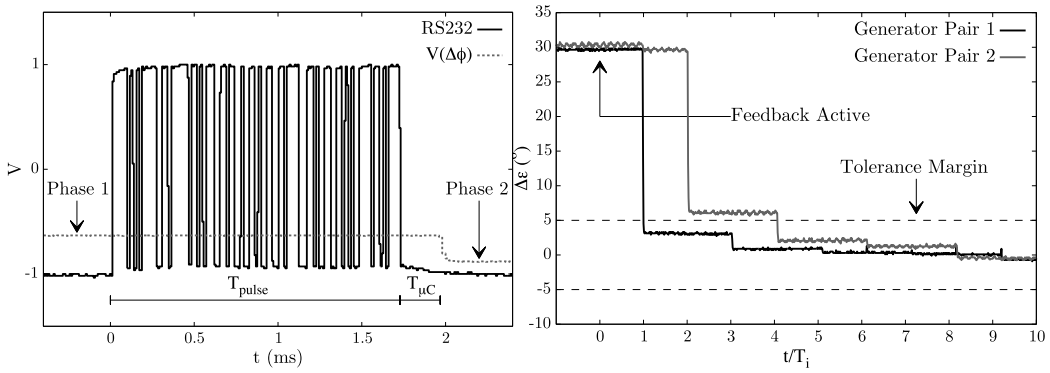

FIGURE 4. Performance of the proposed system: (a) instruction pulses on the RS232 serial link; (b) phase difference error $\Delta\varepsilon$ normalized to the instruction time T_i

vated at $t = 0$ and the first generator pair is in the tolerance margin after a time T_i while the second pair requires two iterations. The $\Delta\varepsilon$ step for each iteration is determined by a software-implemented PID controller. Note that the T_i lag of the second pair as well as the $2T_i$ iteration step time are also observed. The tolerance margin of 5% corresponds with losses in the combiner's load less than 0.2% of the maximum forwarded power.

III. RESULTS

The response times measured on the test-bench for the simultaneous control of two generator pairs range between 3.8ms for the expected initial phase error range ($\|\Delta\varepsilon\| < 20°$) and are smaller than 15.2ms for larger initial errors. This is a considerable improvement over the current analog PLL system which exhibits response times in the range of 20-50ms. No further optimization is required as response times smaller than 1ms introduce ringing: unwanted oscillations in the step response as the ramp-up time of the generators is around 0.5ms. Performance of the proposed system during a shot on the ICRF system of ASDEX-Upgrade are scheduled. Finally, room for improvement remains: the system should be capable of phase and frequency modulation with a precision of 0.1Hz, however this feature remains unexploited as the software controller has yet to include this functionality.

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