Simple Time Domain Analysis of a 4-Level H-bridge Flying Capacitor Converter Voltage Balancing

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***Abstract*—Flying Capacitor (FC) multilevel Pulse Width Modulated (PWM) converters are an attractive choice due to the natural balancing property of the capacitor voltages. The balancing can be studied in the time domain, which results in easy to interpret expressions regarding parameter influence. Time domain analysis is normally done by time averaging of the system model over a PWM-period. In this paper a new method is presented starting from the "voltage unbalance" excessive energy which has to be dissipated in the converter load by switching harmonics in the load current. This is applied on a four-level H-bridge converter, which has dynamics of a high order and is normally hard to describe in the dime domain. The proposed method results in time domain parameters exactly describing the behaviour and the balancing of the capacitor voltages of the four-level H-bridge converter.**

I. Introduction

Multilevel converters were developed as a result of a growing need for higher power converters, [1], [2]. In order to achieve this higher power rating, the voltage and current capabilities of the devices used in the converter need to be increased. Current insulated gate bipolar transistor (IGBT) technology extends up to 6.5 kV 900 A per switching device. Converters that make use of a series connection of switches, allow for the use of switches with reduced voltage ratings. These lower voltage switches have lower switching losses and can switch at a higher frequency. Higher switching frequencies and a smaller voltage step capability result in higher quality switching waveforms.

Flying capacitor (FC) multilevel converters are an attractive choice due to the natural voltage balance property. The natural balancing is achieved by applying a Phase Shifted carrier PWM (PSCPWM) method. The balancing of the capacitors is driven by load current high order harmonics, [3]-[6], namely, by the capacitor "voltage unbalance" excessive energy dissipation in the converter load by switching harmonics in the load current. Though it is accepted to consider a simplified series LR-load model, practically high frequency loss mechanisms like skin-effect and PWM eddy current core losses are expected to make voltage balance rate faster.

Traditionally the analysis of the natural balancing for FC multilevel converters is done in the frequency domain, [3]. This method is based on frequency domain transformations involving double Fourier series expansion, Bessel function coefficients etc. This approach is, in fact, not analytical, rather algorithmic, and difficult to apply in an everyday practice. It results in complex equations where it's hard to distinguish a good relationship between the capacitor voltage balancing behaviour and certain parameters of the system.

In recent work, [7], [8], [9], an alternative analysis of the FC converter is reported using a switched systems time domain approach based on stitching of analytical transient solutions for consecutive PWM period switching subintervals in conjunction with a small parameter technique [7]. This approach is more adequate for understanding voltage balance dynamics as it yields simple accurate truly analytical solutions. Small parameter approximation actually means inductance dominated load (inductance limited PWM ripple current) and reasonably low capacitor ripple voltage.

In this paper, a new technique is presented using a deeper insight in the capacitor voltage balancing process. The basic principle is that balancing is driven by the "voltage unbalance" excessive energy which has to be dissipated in the converter load by switching harmonics in the load current. Using this method, easy to interpret expressions for time constants and oscillation frequency are obtained. This way a complex high-order system can be described in the time domain, starting only from the losses generated by the harmonic currents.

II. Four-level H-bridge topology and natural balancing strategy

The topology of the 4-level H-bridge converter is depicted in Fig. 1. The complementary switches $(S_1, \overline{S_1})$, $(S_2, \overline{S_2})$, ..., $(S_6, \overline{S_6})$ are controlled by using a phase shifted carrier pulse width modulation (PSCPWM), depicted in Fig. 2. The normalized voltage command D controls the first leg (switches S_1, S_2 and S_3), the inverted normalized voltage command $-D$ controls the second leg (switches S_4, S_5 and S_6).

To describe the behaviour of capacitor voltage values, two modes are distinguished regarding both legs of the H-bridge FC converter. For the common mode, the corresponding capacitor voltages are equal $V_{C_1} = V_{C_3}$ and $V_{C_2} = V_{C_4}$. This can be regarded as the behaviour of the mean value of the corresponding capacitor's voltages corrected with the nominal

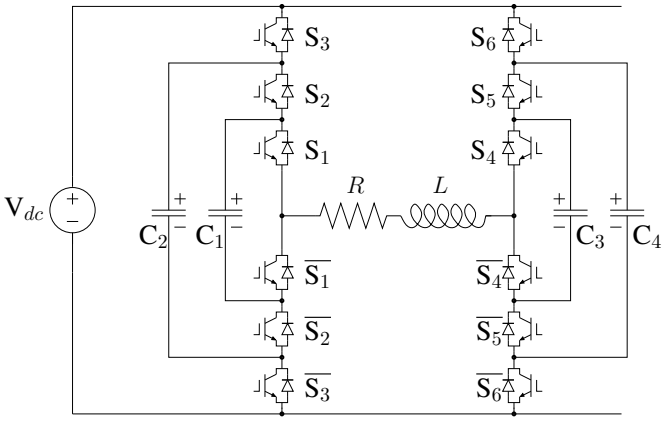

Fig. 1. Four-level H-bridge flying capacitor converter circuit topology.

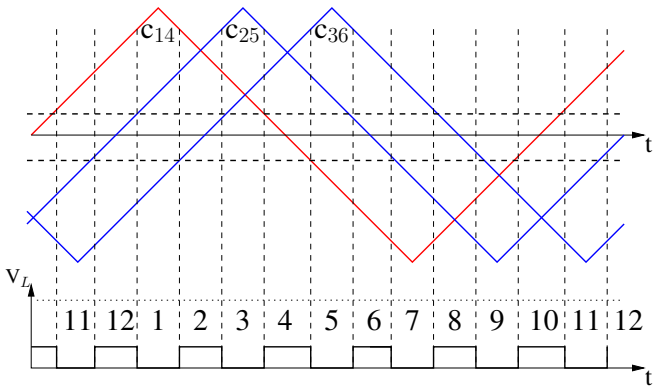

Fig. 2. Four-level H-bridge flying capacitor converter phase shifted carrier PWM strategy.

voltages:

$$V_{c1} = \frac{V_{C_1} + V_{C_3}}{2} - \frac{V_{dc}}{3}, \qquad V_{c2} = \frac{V_{C_2} + V_{C_4}}{2} - \frac{2V_{dc}}{3}. \tag{1}$$

For the differential mode, both capacitor voltages are opposite $V_{C_1} = -V_{C_3}$ and $V_{C_2} = -V_{C_4}$. The differential voltages are:

$$V_{d1} = \frac{V_{C_1} - V_{C_3}}{2}. \qquad V_{d2} = \frac{V_{C_2} - V_{C_4}}{2}. \tag{2}$$

III. Analytical Deduction of Periodic Time Constant

The periodic time constant of the balancing of the capacitor voltages of the four-level H-bridge converter is a measure for the dissipation of the unbalance energy. For the time domain analysis of the balancing some assumptions are made: a zero DC-bus voltage and charged flying capacitors C_1, C_2, C_3 and C_4. This changes nothing to the actual system. The periodic time constant is the time constant for the damping of the oscillation of the capacitor voltages. The calculation method will be worked out for a normalized voltage command D, holding to the following condition: $0 < D < 1/3$, as depicted

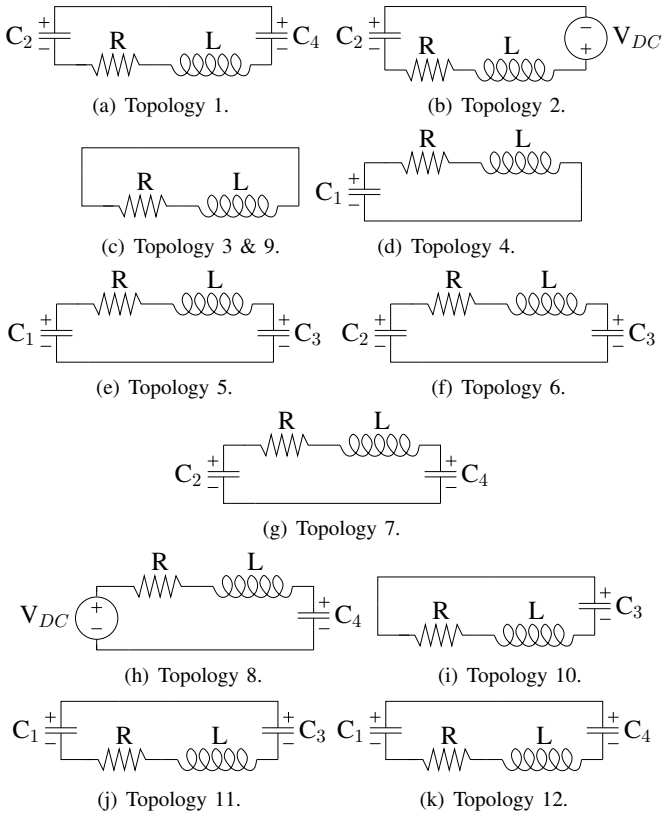

Fig. 3. Converter topology circuits generated by PSCPWM for $0 < D < 1/3$.

in Fig. 2. The topology circuits, corresponding with the switch states generated by the PSCPWM strategy, are depicted in Fig. 3. The duration of the intervals is:

$$\Delta t_1 = \Delta t_3 = \Delta t_5 = \Delta t_7 = \Delta t_9 = \Delta t_{11} = \frac{1/3 - D}{2} T_{\text{PWM}}, \qquad \Delta t_2 = \Delta t_4 = \Delta t_6 = \Delta t_8 = \Delta t_{10} = \Delta t_{12} = \frac{D}{2} T_{\text{PWM}}. \tag{3}$$

This method makes use of the small parameter approach. This includes two physical properties. First of all an inductance dominated load is assumed, giving an almost piece-wize linear ripple current. Second, the value of the flying capacitors is large enough, meaning the voltage ripple is relatively low, so the capacitor voltages can be considered constant within a switching period.

A. Common mode

Assuming zero DC-bus voltage V_{dc}, equal corresponding capacitor voltages $V_{C_1} = V_{C_3}$ and $V_{C_2} = V_{C_4}$ and zero load resistance, the load voltage and steady state current for $0 < D < 1/3$ are depicted in Fig. 4.

The load resistance is assumed to have a minor influence on the shape of the current, as depicted in Fig. 4 for $D = 1/6$, but an average load loss (average power dissipation) on

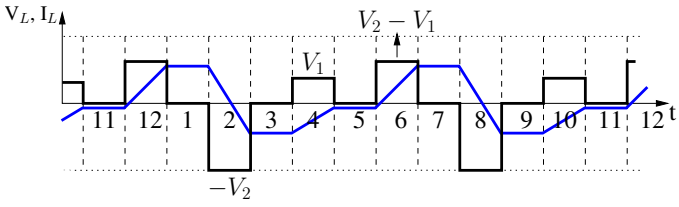

Fig. 4. Load voltage and steady state current assuming zero DC-bus voltage for $0 \leq D \leq 1/3$, for common mode (drawn for $D = 1/6$).

a switching period can be calculated:

$$P = \frac{1}{T_{\text{PWM}}} \int_0^{T_{\text{PWM}}} i^2(\tau)\, R d\tau. \tag{4}$$

This requires a correct parameterized knowledge of the current. As in regime conditions there is a zero mean current and a reference is needed to get to this zero mean current, it is necessary to use an arbitrary zero point and calculate the mean value, to be able to apply a correction for a zero mean current. For the next calculation, the zero current reference is taken at the first switching interval ($i^{(0)}$ is the current in the beginnen of the first interval, $i^{(1)}$ at the end of the first, and so on):

$$\begin{aligned} i^{(0)} &= 0, \\ i^{(1)} &= 0, \\ i^{(2)} &= \frac{-V_2 \Delta t_2}{L}, \\ i^{(3)} &= i^{(2)}, \\ i^{(4)} &= i^{(3)} + \frac{V_1 \Delta t_2}{L}, \\ i^{(5)} &= i^{(4)}, \\ i^{(6)} &= i^{(6)} + \frac{(V_2 - V_1)\, \Delta t_2}{L} = 0. \end{aligned} \tag{5}$$

These current values at the borders of the intervals can be used to calculate the average current in the intervals:

$$I_1 = \frac{i^{(0)} + i^{(1)}}{2};\ I_2 = \frac{i^{(1)} + i^{(2)}}{2};\ \ldots \tag{6}$$

The average current can now be calculated:

$$I_{avg} = \frac{I_1 \Delta t_1 + I_2 \Delta t_2 + I_3 \Delta t_1 + I_4 \Delta t_2 + I_5 \Delta t_1 + I_6 \Delta t_2}{T_{\text{PWM}}/2}. \tag{7}$$

The corrected currents are:

$$i^{(0)}_{corr} = i^{(0)} - I_{avg};\ i^{(1)}_{corr} = i^{(1)} - I_{avg};\ \ldots \tag{8}$$

In the next step, the ohmic loss generated by the current, (8), has to be calculated. For this the mean square current has to be calculated for every interval. This can be done using following expression for the mean square of a current segment:

$$\overline{I_1^2} = \frac{{i^{(0)}_{corr}}^2 + i^{(0)}_{corr} i^{(1)}_{corr} + {i^{(1)}_{corr}}^2}{3} \tag{9}$$

This can be done for every single interval. The harmonic power loss, on average over the PWM period, can then be calculated as:

$$P_{avg}(V_1, V_2) = \frac{R\left(\overline{I_1^2}\Delta t_1 + \overline{I_2^2}\Delta t_2 + \overline{I_3^2}\Delta t_1 + \overline{I_4^2}\Delta t_2 + \overline{I_5^2}\Delta t_1 + \overline{I_6^2}\Delta t_2\right)}{T_{\text{PWM}}/2}. \tag{10}$$

For a four-level H-bridge FC converter this gives:

$$P_{avg} = \frac{1}{36} \frac{RT_{\text{PWM}}^2 D^2 \left(V_1^2 - V_1 V_2 + V_2^2\right)(2 - 3D)}{L^2} \tag{11}$$

Now the average power loss over a PWM period caused by the harmonic current is known. To be able to calculate the periodic time constant, the average power loss over an oscillation period has to be known. So in the last step the "instantaneous" resistive power loss, (11), has to be averaged. Without any loss of generality, following initial condition assumption can be made:

$$\begin{aligned} V_1(0) &= V; \\ V_2(0) &= 0. \end{aligned} \tag{12}$$

Then from (32) this leads to:

$$\begin{aligned} V_1(t) &= V \cos \omega t; \\ V_2(t) &= \sqrt{\frac{C_1}{C_2}} V \sin \omega t. \end{aligned} \tag{13}$$

The average on the oscillation period of the square voltages are

$$\begin{aligned} \overline{V_1^2} &= \frac{V^2}{2}, \\ \overline{V_2^2} &= \frac{V^2 C_1}{2C_2}, \\ \overline{V_1 V_2} &= 0. \end{aligned} \tag{14}$$

Now the expression for the harmonic power loss becomes:

$$P_{avg} = \frac{1}{72} \frac{RT_{\text{PWM}}^2 D^2 V^2 (C_1 + C_2)(2 - 3D)}{C_2 L^2} \tag{15}$$

The law of conservation of energy says (averaged over an oscillation period and multiplied by 2 because there are two capacitors (C_1 and C_3)

$$\frac{\Delta\left(2C_1 \frac{V^2}{2}\right)}{T_{\text{PWM}}} \approx \frac{d\left(C \frac{V^2}{2}\right)}{dt} = -P, \tag{16}$$

with the power loss substituted:

$$\frac{d\left(\frac{2C_1 V^2}{2}\right)}{dt} = -\frac{1}{72} \frac{RT_{\text{PWM}}^2 D^2 V^2 (C_1 + C_2)(2 - 3D)}{C_2 L^2}, \tag{17}$$

what can be transformed in

$$\frac{d(V)}{dt} = -\frac{1}{144} \frac{RT_{\text{PWM}}^2 D^2 V (C_1 + C_2)(2 - 3D)}{C_1 C_2 L^2}. \tag{18}$$

The time constant can be found regarding following equation:

$$\frac{dV^2}{dt} = -\frac{V}{T_c}. \tag{19}$$

This results in the common mode periodic time constant:

$$T_c = \frac{144 L^2 C_1 C_2}{RT_{\text{PWM}}^2 D^2 (2 - 3D)(C_1 + C_2)},\ 0 < D < 1/3. \tag{20}$$

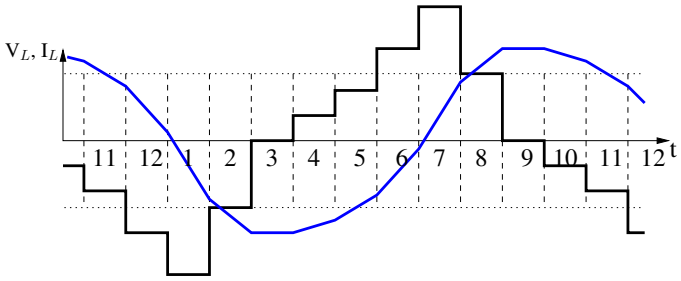

Fig. 5. Load voltage and steady state current assuming zero DC-bus voltage for $0 \leq D \leq 1/3$, for differential mode (drawn for $D = 1/6$).

For other ranges of D, the circuit momentary circuit topologies are different, resulting in a different current waveform. The resulting equations are:

$$T_c = \frac{1296L^2C_1C_2}{RT_{\text{PWM}}^2\left(9D-9D^2-1\right)\left(C_1+C_2\right)}, \quad 1/3 < D < 2/3,$$
$$T_c = \frac{1296L^2C_1C_2}{RT_{\text{PWM}}^2\left(D-1\right)^2\left(3D-1\right)\left(C_1+C_2\right)}, \quad 2/3 < D < 1. \tag{21}$$

B. Differential mode

Assuming zero DC-bus voltage V_{DC}, inverted corresponding capacitor voltages $V_{C_1} = -V_{C_3}$ and $V_{C_2} = -V_{C_4}$ and zero load resistance, the load voltage and steady state current for $0 < D < 1/3$ are depicted in Fig. 5.

This results in:

$$T_d = \frac{82944L^2C_1C_2}{A}, \tag{22}$$

with denominator

$$A = RT_{\text{PWM}}^2\left[C_1\left(1080D^3-1584D^2+448+729D^4\right) + C_2\left(-1728D^2+1728D^3+448\right)\right], \tag{23}$$

for $0 < D < 1/3$. The expressions for a higher normalized voltage command D are similar and as bulky as the previous.

The normalized decay rates (inverse of the time constants) are depicted in Fig. 6. It can be concluded that the differential time constant is much smaller. This can be seen already in the harmonic current in Fig.5, where the amplitude is much higher than in the common mode case, resulting in higher losses.

IV. Analytical deduction of frequency

The voltage balance frequency is calculated assuming zero DC bus and zero load resistance. The capacitor voltages are also assumed to be constant during a PWM period and have a certain voltage at the start. This time the difference between common mode and differential mode is not made in the beginning of the calculations. Starting from the load voltage, the piecewise linear current of the pure inductive load is calculated. There is no need to consider the (average) current reference in this case. Now the capacitor voltage changes for the individual switching intervals can be calculated easily. By adding the changes for the intervals over a switching period, the total change of the capacitor voltages can be calculated.

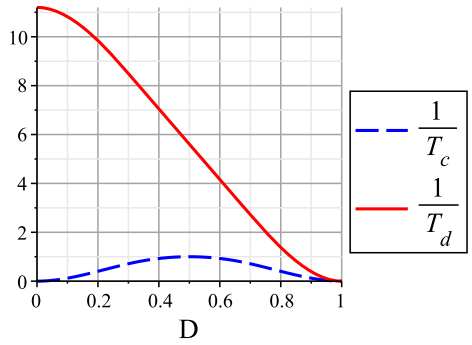

Fig. 6. Common and differential mode normalized decay rates.

Following the switch sequence of the PWM of Fig. 2 and using the interval durations of (3), the load current at the end of the first interval is:

$$i^{(1)} = -\frac{V_2\Delta t_1}{L} + \frac{V_4\Delta t_1}{L}, \tag{24}$$

with the current at the end of the following intervals:

$$\begin{aligned} i^{(2)} &= -\frac{V_2\Delta t_1}{L} + \frac{V_4\Delta t_1}{L} - \frac{V_2\Delta t_2}{L}, \\ &\vdots \\ i^{(11)} &= \frac{V_1\Delta t_2}{L} - \frac{V_4\Delta t_2}{L}, \\ i^{(12)} &= 0. \end{aligned} \tag{25}$$

Just as expected, the current ends where it started, at zero. To be able to calculate the voltage variation over an interval, the average current during that interval is necessary:

$$\begin{aligned} I^{(1)} &= \frac{i^{(12)}+i^{(1)}}{2} = -\frac{V_2\Delta t_1}{2L} + \frac{V_4\Delta t_1}{2L}, \\ &\vdots \\ I^{(12)} &= \frac{i^{(11)}+i^{(12)}}{2} = \frac{V_1\Delta t_2}{2L} - \frac{V_4\Delta t_2}{2L}. \end{aligned} \tag{26}$$

The current in each interval changes the voltages of the capacitors that are connected in the circuit during that interval. During interval 1, capacitors C_2 and C_4 are connected in the circuit. Their voltages change during interval 1:

$$\begin{aligned} \Delta v_2^{(1)} &= \frac{I^{(1)}\Delta t_1}{C_2} = -\frac{V_2\Delta t_1^2}{2LC_2} + \frac{V_4\Delta t_1^2}{2LC_2}, \\ \Delta v_4^{(1)} &= -\frac{I^{(1)}\Delta t_1}{C_4} = \frac{V_2\Delta t_1^2}{2LC_4} - \frac{V_4\Delta t_1^2}{2LC_4}. \end{aligned} \tag{27}$$

The total capacitor voltage variation of a PWM period is the summation of the voltage changes of the intervals for each capacitor:

$$\begin{aligned} \Delta V_1 &= \Delta v_1^{(4)} + \Delta v_1^{(5)} + \Delta v_1^{(11)} + \Delta v_1^{(12)}, \\ \Delta V_2 &= \Delta v_2^{(1)} + \Delta v_2^{(2)} + \Delta v_2^{(6)} + \Delta v_2^{(7)}, \\ \Delta V_3 &= \Delta v_3^{(5)} + \Delta v_3^{(6)} + \Delta v_3^{(10)} + \Delta v_3^{(11)}, \\ \Delta V_4 &= \Delta v_4^{(1)} + \Delta v_4^{(7)} + \Delta v_4^{(8)} + \Delta v_4^{(12)}. \end{aligned} \tag{28}$$

When using "on-average" derivative approximation (small parameter approximation)

$$\begin{aligned}\Delta V_1' &= \frac{\Delta V_1}{T_{\text{PWM}}},\\ \Delta V_2' &= \frac{\Delta V_2}{T_{\text{PWM}}},\\ \Delta V_3' &= \frac{\Delta V_3}{T_{\text{PWM}}},\\ \Delta V_4' &= \frac{\Delta V_4}{T_{\text{PWM}}},\end{aligned} \tag{29}$$

and after substituting the voltage variations and the interval durations (3) in these equations, following linear system can be found:

$$\begin{bmatrix}\Delta V_1'\\ \Delta V_2'\\ \Delta V_3'\\ \Delta V_4'\end{bmatrix} = \begin{bmatrix} 0 & \frac{2}{C_1} & 0 & \frac{\left(9D^2-2\right)}{C_1}\\ -\frac{2}{C_2} & 0 & -\frac{\left(9D^2-2\right)}{C_2} & 0\\ 0 & \frac{\left(9D^2-2\right)}{C_3} & 0 & \frac{2}{C_3}\\ -\frac{\left(9D^2-2\right)}{C_4} & 0 & -\frac{2}{C_4} & 0\end{bmatrix} \cdot \begin{bmatrix}\Delta V_1\\ \Delta V_2\\ \Delta V_3\\ \Delta V_4\end{bmatrix} \tag{30}$$

These equations can be simplified when accounting for the common mode and differential mode.

A. Common mode

Substutition of $V_{C_3} = V_{C_1}$ and $V_{C_4} = V_{C_2}$ in (30) gives:

$$\begin{bmatrix}\Delta V_1'\\ \Delta V_2'\end{bmatrix} = \begin{bmatrix} 0 & D^2\frac{T_{\text{PWM}}}{8LC_1}\\ -D^2\frac{T_{\text{PWM}}}{8LC_2} & 0\end{bmatrix} \cdot \begin{bmatrix}\Delta V_1\\ \Delta V_2\end{bmatrix}. \tag{31}$$

This system has the common mode solution:

$$\begin{aligned}V_1(t) &= V_1(0)\cos\omega_c t + \sqrt{\frac{C_2}{C_1}}V_2(0)\sin\omega_c t,\\ V_2(t) &= V_1(0)\cos\omega_c t - \sqrt{\frac{C_1}{C_2}}V_2(0)\sin\omega_c t,\end{aligned} \tag{32}$$

with

$$\omega_c(D) = \frac{T_{\text{PWM}}D^2}{8L\sqrt{C_1C_2}},\ 0 < D < 1/3. \tag{33}$$

B. Differential mode

Substutition of $V_{C_3} = -V_{C_1}$ and $V_{C_4} = -V_{C_2}$ in (30) gives:

$$\begin{bmatrix}\Delta V_1'\\ \Delta V_2'\end{bmatrix} = \begin{bmatrix} 0 & \left(4-9D^2\right)\frac{T_{\text{PWM}}}{72LC_1}\\ -\left(4-9D^2\right)\frac{T_{\text{PWM}}}{72LC_2} & 0\end{bmatrix} \cdot \begin{bmatrix}\Delta V_1\\ \Delta V_2\end{bmatrix} \tag{34}$$

This system has the differential mode solution:

$$\begin{aligned}V_1(t) &= V_1(0)\cos\omega_d t + \sqrt{\frac{C_2}{C_1}}V_2(0)\sin\omega_d t,\\ V_2(t) &= V_1(0)\cos\omega_d t - \sqrt{\frac{C_1}{C_2}}V_2(0)\sin\omega_d t,\end{aligned} \tag{35}$$

with

$$\omega_d(D) = \frac{T_{\text{PWM}}\left(4-9D^2\right)}{8L\sqrt{C_1C_2}},\ 0 < D < 1/3. \tag{36}$$

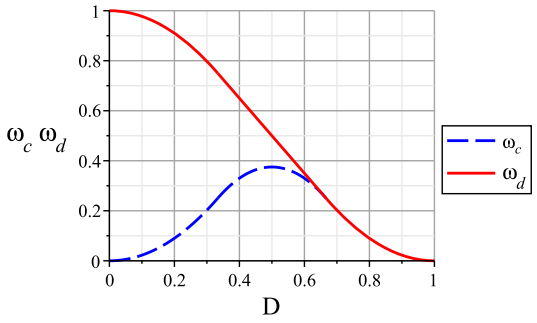

Fig. 7. Four-level H-bridge flying capacitor converter phase shifted carrier PWM strategy.

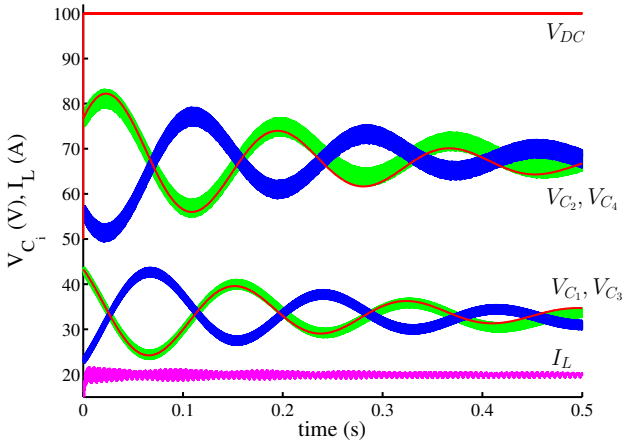

Fig. 8. Differential mode balance simulation results ($D = 0.3$).

The frequencies for the other D regions: For $1/3 < D < 2/3$:

$$\begin{aligned}\omega_c(D) &= \frac{T_{\text{PWM}}\left(6D-6D^2-1\right)}{24L\sqrt{C_1C_2}},\\ \omega_d(D) &= \frac{T_{\text{PWM}}\left(5-6D\right)}{72L\sqrt{C_1C_2}},\end{aligned} \tag{37}$$

and for $2/3 < D < 1$:

$$\omega_c(D) = \omega_d(D) = \frac{T_{\text{PWM}}\left(D-1\right)^2}{8L\sqrt{C_1C_2}}, \tag{38}$$

The normalized common and differential mode frequencies are depicted in Fig. 7.

V. Simulations of the Derived Model

The time domain parameters can be used to model a step response of the capacitor voltages. The derived model is compared with accurate switched simulations. The used parameters are: $V_{dc} = 100V$; $R = 1.5\Omega$; $L = 1mH$; $C_1 = 700\mu F$; $C_2 = 350\mu F$; $T_{\text{PWM}} = 408\mu s$ (2.45kHz). The differential mode parameters are checked in Fig. 8 for $D = 0.3$. The common mode is applied in Fig. 9 for $D = 0.25$.

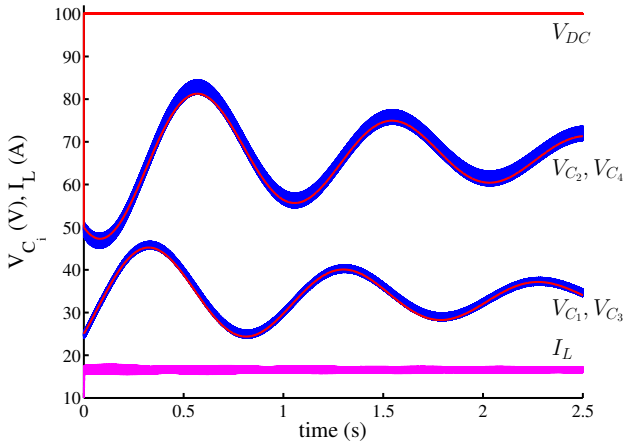

Fig. 9. Common mode balance simulation results ($D = 0.25$).

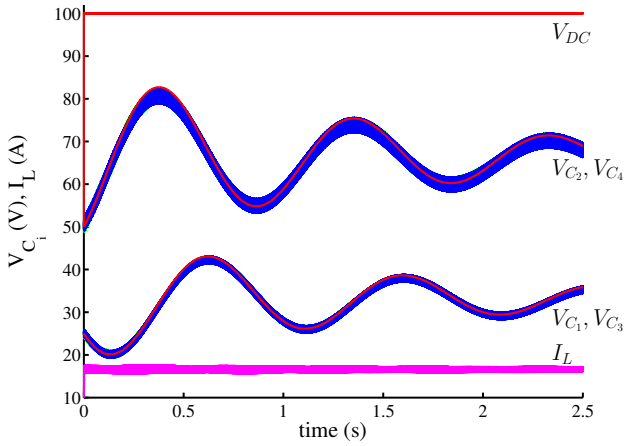

Fig. 10. Common mode balance simulation results for a lag modulation strategy ($D = 0.25$).

VI. Lead and lag modulation strategies and AC-modulation

So far, we assumed the carrier based voltage modulation strategy (Fig. 2) that can be referred to as the lead one because the carrier wave C_{14} leads C_{25} and C_{25} leads C_{36}. For the alternative lag modulation strategy, the carrier wave C_{36} leads C_{25} and C_{25} leads C_{14}. The inverse sequence of the carrier signals generates the inverse switching states order, but has no influence on the parameters itself. The lag modulation may be formally accounted for by changing the signs of all the sinusoidal terms in (32), (35). The accurate switched simulation and average voltage balance dynamics approximation results for the two modulation strategies are presented in Fig.10.

Once the expressions of the voltage balance dynamics parameters are obtained for DC PWM, the expressions for AC PWM can be found by the time averaging of the DC PWM voltage balance frequency and decay rate (inverse time constant) along the sinusoidal voltage command trajectories, [8], [9], [10]. This way, the common mode angular frequency and time constants must be replaced by their respective values "averaged" on a fundamental period accounting for their symmetric, even behavior for $0 < D < 1$ and $-1 < D < 0$.

VII. Conclusion

Starting from the fact that the capacitor voltage balancing depends on the harmonic power loss in the load, it is shown that it is possible to find the parameters that describe the voltage balancing dynamics. The obtained expressions are equal to the once obtained by using averaging of the system models of every switch interval, which takes much more calculation. The used technique gives a possiblity to find the voltage balance dynamics parameters of a high order system in a simple way.

The paper presented the method used for a four-level H-bridge FC converter, resulting in the voltage balance dynamics equations. These expressions clearly reveal the dependencies on inductive load parameters, capacitances, carrier frequency, and normalized DC (and AC) voltage command. They are confirmed by extensive accurate switched simulations.

Acknowledgment

S. Thielemans wishes to thank the Research Foundation-Flanders (FWO-Vlaanderen, project G.0011.08) for the financial support.

A. Ruderman and B. Reznikov gratefully acknowledge Elmo Motion Control and General Satellite Corporation management respectively for on-going support to advanced applied power electronics research support.

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