Metal bonding with ultra-thin layer for optical applications

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Adhesive bonding is a well-known technics to assembly dies or wafer on a host substrate through polymer or solder bumps. To combine electronic and photonic systems on a single chip, we propose hereby to use AuSn alloy as bonding medium combined to waferscale technology and post-bonding III-V processing alleviating so the need of alignment accuracy between wafers. For instance, high density LED's array could be realized on driving CMOS wafer taking benefits from the nice electrical, thermal and mechanical properties of this alloy. We present our first technological results using patterned thin bonding layer made of a multilayer Au-Sn composite.

Introduction

In the framework of the flip-chip technology, several methods were developed to join two wafers or a die to a wafer. For most of the optical applications, a III-V die requires to be bonded on a Si, SOI (Silicon On Insulator) or CMOS wafer. Several kinds of material were investigated like Spin On Glass (SOG) [1], polymer (polyimide [2] or BCB [3]...) or metal through solder bumps [4] to heterogeneously integrate photonic components such as photodiodes, laser diodes or photodetectors. But SOG and polymer materials are bad thermal conductors which can strongly affect the device characteristics and leading sometimes to component failure. Moreover some applications necessitate the bonding medium is an electrical conductor. The solution is to use a metal or alloy as intermediate layer. A number of manufacturers (UEC, VPEC, AET...) chose this way to bond their LEDs to a heat conductive substrate. In this case, the LEDs were fabricated before the bonding. We propose hereby as an alternative to have an inline approach aiming at, for instance, realizing a high density top emitting LEDs array on a driving CMOS substrate for 1200 dpi (corresponding to a LED pitch of 21 μm) printheads. This method consists in processing the LEDs after having bonded the III-V die on the CMOS wafer equipped of metal bonding pads. By this way, an accurate alignment between both wafers is not necessary since the position of the photonic devices on the electronic chip is ensured by the subsequent photolithography steps of the wafer-scale processing.

Among the hard solders (which show an elastic deformation under stresses in normal usages), the AuSn alloy is the most interesting candidate. Indeed, it owns a larger thermal conductivity than others, a moderate bonding temperature (just above 280°C), excellent thermal, mechanical and electrical properties, and the ability to solder without flux [5]. So we present hereby our first results about the three most important technological steps of the process flow we have developed on dummy III-V dies and Si wafers in order to perform the bonding by means of ultra-thin AuSn bonding pads: fabrication of pads followed by their physical isolation and the bonding step itself.

Fabrication of the multilayer composite

The principle of the bonding by means of pads with a low thickness is shown in Fig.1.

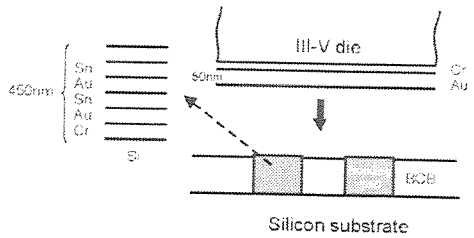
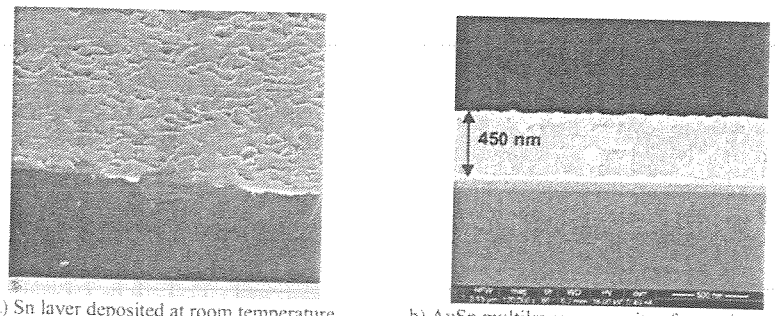


Fig.1. Schematic illustration of the bonding with AuSn multilayer composite pads

AuSn solder preforms were widely used for the bonding of flat samples but the impossibility to pattern it makes it unsuitable. The most interesting methods are evaporation and sputtering. Evaporation was chosen instead of sputtering since the sputtered eutectic alloy is submitted to oxidation and the patterning by means of lift off is better with evaporation. The metallization scheme consists of Au and Sn layers alternatively deposited forming a multilayer composite structure. In order to obtain a nice layers quality and consequently an accurate control of the thickness, we had to optimize the evaporation parameters.

Au and Sn layers were deposited on the Si wafer as depicted in Fig.1 while a wetting Au layer is evaporated on the die in a vacuum chamber to avoid Sn oxidation. On both wafers, we use an underlying Cr layer which is used for its properties of adhesion and as good diffusion barrier. The cap layer of the composite is made of Au to prevent Sn from a rapid oxidation. The total thickness of the Au-Sn composite before bonding is 500 nm while the one of each Au and Sn layer is chosen to obtain a good subsequent mixing between both metals and reach the eutectic composition of the alloy (80 wt.% Au) whose the melting temperature is around 280°C. Our first tries showed very bad results (Fig.2a) due to a problem of Sn adhesion. So it was necessary to carry out an optimization of the different evaporation parameters. In particular, inserting a special cooling system in the chamber allowed us to strongly reduce the sample temperature down to -100°C, leading so to a better adhesion of Sn.



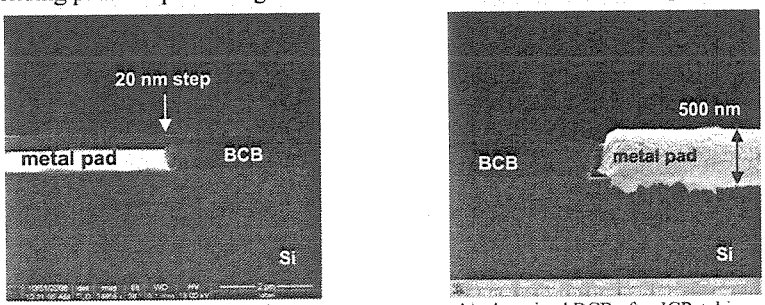
a) Sn layer deposited at room temperature b) AuSn multilayer composite after optimization

Fig. 2. metal layers after evaporation

After this improvement, it was possible to achieve a multilayer composite made of Au and Sn layers without any network of holes and with an extremely flat surface (roughness of several nanometers). On Fig.2b it is difficult to distinguish each layer because of the interdiffusion phenomenon which is already active during the deposition process but it doesn't prevent from having the expected evaporated thickness.

Isolation of the bonding pads

In order to avoid a short-circuit on the driving CMOS wafer (due to electrical connections between its Cu pads), the composite doesn't have to be deposited everywhere on the wafer. So bonding pads must be fabricated on the Cu ones by means of a classical lift-off process. But since the subsequent bonding step is based on a liquid state of the alloy and requires to apply a pressure, the bonding pads will squeeze and can form an uniform AuSn layer. The solution is to isolate each pad from the others thanks to a polymer layer which is fabricated through a planarisation process. BCB (Benzocyclobutene) was chosen as the isolating material because it owns good gap-filling, planarisation after deposition, and mechanical properties. Moreover, in case of a CMOS wafer, it will protect the ILD (InterLayer Dielectric) material whatever it is during the subsequent steps. First BCB was spin-coated on the Si wafer covering the AuSn bonding pads at the same time. After optimization, its thickness was high enough to obtain a BCB surface step of only about 20 nm due to the 500 nm-thick pad edges (Fig.3a). Then the BCB layer was etched by ICP. That's crucial the final BCB thickness is high enough to avoid the leak of the alloy but it doesn't have to exceed the surface of the bonding pads not preventing so the contact between die and wafer (Fig.3b).



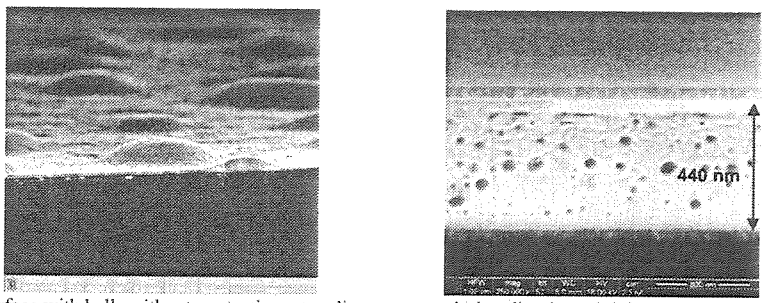
a) BCB layer after spin coating b) planarized BCB after ICPetching

Fig.3: BCB-metal pad planarization

Bonding step

The next step consists in joining both die and wafer. Our first study is currently carried out on unpatterned pieces with eutectic AuSn as bonding medium. A pressure is applied to achieve an intimate contact between both die and pad surfaces and also to prevent the well-known balling effect (Fig.4a). Balls can be as thick as 2 µm. At 330°C, the temperature is high enough to allow the melting of Sn and a solid-liquid interdiffusion happens but it won't degrade the BCB layer (T_g=350°C). Sn under its liquid form wets the two adjacent Au layers creating Au-Sn alloys and liquid and solid components will interdiffuse rapidly. During this step, the Au layer from the top die is also diluted and participates to the formation of the alloy, leading so to the sintering between both substrates. The bonding sequence can be done in less than 30 min. An example of the

resulting AuSn layer is given in Fig.4b. Both wafer and die were nice attached and Cr acts well as a diffusion barrier since it has not changed. The reduction of the AuSn layer thickness was evaluated to only about 60 nm. But some problems require to be solved. Indeed we can notice some bubbles appeared (with a maximum diameter of about 50 nm). The wetting Au layer of the die is not completely mixed with the AuSn multilayer composite. And it seems two phases were created. A deeper study by means of EDX or XRD would reveal the nature of these phases. Moreover an optimization of the bonding step is currently carried out to avoid the bubbles formation and to improve the mixing of the Au wetting layer. Shear tests will be performed to characterize the bonding quality.



a) surface with balls without contacting a top die b) bonding layer joining two wafers

Fig.4. views of the AuSn multilayer composite after a sequence at 330C

Conclusion

AuSn alloy appears as the best material in order to perform die (or wafer) to wafer bonding aiming at combining electronic and photonic systems on a single chip requiring electrical links. Our aim is to use low thickness pads. As an example, it could be a very suitable method to realize high density LEDs array on a CMOS driving wafer. We presented hereby the first results about the most important technological steps used in this bonding process taking into account the requirements of the bonded components and their subsequent fabrication steps. The bonding step itself needs to be optimized whereas the bonding by means of the pads is under study.

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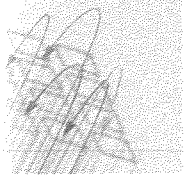

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