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A Reconfigurable Digital Platform for the Real-Time Emulation of Copper Access Networks

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Abstract *– In this paper, a reconfigurable platform for the real-time digital emulation of copper access networks is presented. The instrument, using hard real-time DSP techniques on Xilinx Virtex II FPGAs, is capable of accurately reproducing the physical layer of a xDSL connection. The magnitude and absolute phase of the insertion and return loss of the twisted pair access loop consisting of cables with various characteristics and length is digitally emulated over the full VDSL bandwidth. The innovative character of the digital approach over conventional loop emulation techniques is demonstrated and its performance is assessed using several test cases.*

Keywords *– xDSL, VDSL, Real-time, Emulation, Physical Layer, DSP, FPGA*

I. INTRODUCTION

The wide scale deployment of fibre optic backbone networks is already a fact, yet, for the last mile(s) up to the subscriber, the reuse of current copper access networks is standard practice. In most cost studies, this so-called ‘last mile’, connecting individual houses, takes the biggest share, and the reuse of the twisted pair telephony cables, which are already in place, is favored. This explains the success of Digital Subscriber Line technology (xDSL), which can support megabit data rates over the phone lines connecting nearly every home. Copper pair networks were designed for voice traffic with a limited bandwidth of 3.4 kHz, but HSDL, ADSL, T1, E1 and VDSL may exceed voice bandwidth more then a thousand fold. The efficient exploitation of copper pair access networks at high bandwidth therefore presents a formidable challenge, and the capability of accurately analyzing and emulating specific access line cables and topologies has become quite important.

A reconfigurable digital module for the emulation of the physical layer of communication systems is presented. The feasibility of such a system is demonstrated through the development of a proof-of-concept digital access loop emulator for VDSL applications within the framework of the European MEDEA+ project MIDAS [1]. This prototype instrument can emulate (i.e. imitate in real time) quite complex phone line networks in a lab environment. So, for the first time, cable measurements can be made in the field and later transferred to the emulator, to replicate field installed phone lines precisely.

II. PROBLEM ANALYSIS

A. Access Loop Topologies

The connection between the xDSL subscriber and the local exchange usually consists of a cascade of twisted pair lines, which can vary in type and length. In some cases open ends of unused twisted pair, so-called bridged taps, are connected in parallel somewhere along the loop (Figure 1).

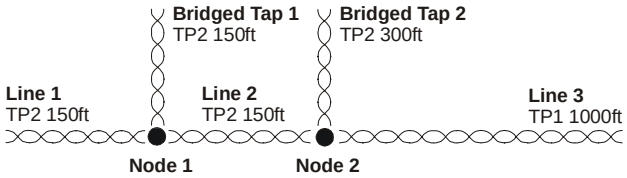

Figure 1 : ANSI 'VDSL 4' Access loop topology

A topology of lines and bridged taps gives rise to echoes or reflections, which interfere with the original signal. The transfer function of a typical line topology is shown in Figure 2. A highly irregular low pass pattern appears, which illustrates the complex task xDSL equipment has to perform to provide reliable, high-speed data transmission over this medium.

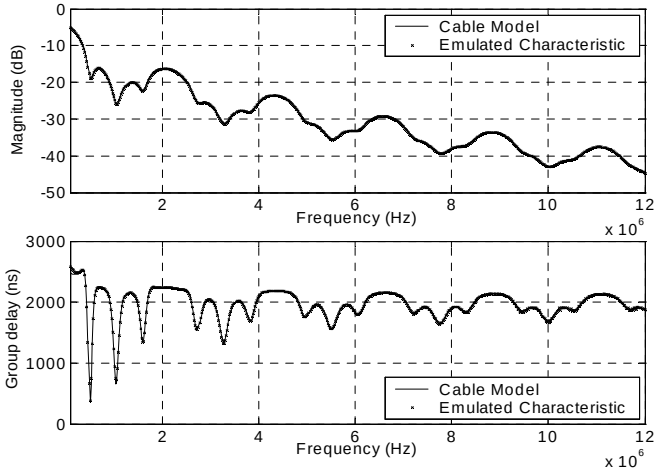

Figure 2 : ANSI ‘VDSL 4’ Insertion Loss: Emulation vs model

B. Analog Access Loop Emulator Shortcomings

Passive analog line emulators are a valuable asset to xDSL designers as they allow the emulation of transmission line topologies in a lab environment. However, these instruments have limited flexibility, typically only supporting a standardized set of loops ([2],[3],[4]). Analog line emulators are bulky in design and usually require more than one instance of the instrument to emulate a full loop topology. Furthermore, emulators based on lumped elements can exhibit precursor energy, resulting in an incorrect impulse response of the loop.

Passive analog emulators aim to accurately reproduce the primary transmission line parameters (R,L,C and G) of a twisted pair, instead of the secondary parameters (attenuation, group delay, impedance, return loss). Although being products of the primary parameters, the secondary parameters are of importance to the performance of xDSL communication equipment, and a direct emulation of the secondary parameters would be beneficial for the achievable accuracy. Lastly, analog component tolerances, combined with variations caused by environmental conditions and aging, may pose a performance barrier for accurate and consistent channel emulation.

Active analog line emulators address some of the above limitations, notably lack of flexibility and the presence of precursor energy, but others remain unsolved. Active analog emulators are generally limited to the emulation of a single segment, such that to emulate a complex loop topology, several devices may be needed. Due to the use of active components, this type of emulator has a higher noise floor than its passive counterparts.

III. A RECONFIGURABLE HARDWARE PLATFORM FOR DIGITAL EMULATION

A. Introduction

An FPGA based digital signal processing module is presented that is capable of emulating the physical layer of communication systems. Depending on the technology for which the emulator is being deployed, different behavioral characteristics and specifications will apply. This myriad of different requirements makes the design of the module more challenging, and illustrates the flexibility of the digital emulator concept. The feasibility of such a system is demonstrated through the development of an access loop emulator for VDSL applications.

B. Real-time Digital Emulation

A lossy transmission line can be described by three parameters : its characteristic impedance Z_0, the exponential wave propagation function $\gamma(\omega)$ and its length L. In [7] and [8] it is shown that a transmission line can be emulated exactly with a system that decomposes the line behaviour into the exponential wave propagation function and its characteristic impendance as illustrated in Figure 3.

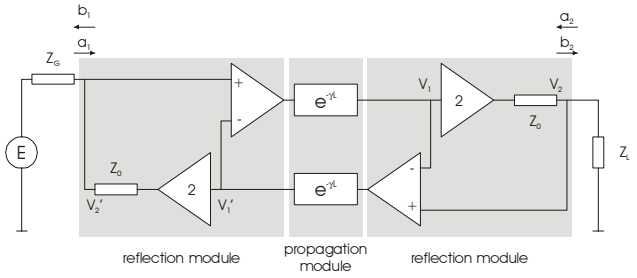

Figure 3 : Equivalent transmission line structure

The two reflection modules are responsible for the immediate effects due to impedance mismatch at the loop ends. The propagation module, emulating the exponential wave propagation function in real-time, is the scope of this paper. The digital approach has a number of advantages over the classical analog designs techniques when considering physical layer emulation:

Reconfigurability— The capability of reconfiguring the platform is an important asset. It allows to change physical layer models to include additional aspects that were not covered in the original models or even add new models without making labor intensive hardware modifications. The applications of the processing core are not only confined to loop emulation. Its reconfigurable nature, combined with a high performance analog front-end results in a versatile platform suitable for a wide range of instrumentation applications.

Reproducibility— A digital core produces consistent results over a prolonged time period and is not prone to aging and environmental influences as are analog designs. However, the necessary conversion to and from the analog domain reduces the deterministic character. In-system calibration procedures can compensate for the introduced inaccuracies, without any modification to the actual hardware platform, as the compensation is performed digitally.

Delay Emulation— The correct emulation of group delay of the transmission medium is important. Advanced communication systems typically use one or more mechanisms to compensate for the frequency-dependent characteristics of the transmission medium, commonly called equalizers. From a digital perspective, group delay can be emulated efficiently using delay lines, supporting very long delays, whilst maintaining a fine granularity. Analog delay lines, although feasible, cannot achieve the same combination of flexibility and range.

Time variant, fading channels— An important parameter for evaluating a technology is its stability against channel variations. This impairment is typically observed in wireless communications but also exists in the telephone access network. Temperature variations affect the primary loop

characteristics, especially the resistance per unit length [5]. The need for evaluating the capability of the transmission technology to cope with these channel variations has been identified recently in [6]. Although a testing method based on heating or cooling real cable sections is proposed, digital emulation provides a far more accurate and reproducible means to realize the equivalent channel variations.

C. Design Constraints

Digital emulation has several advantages over the current passive and active analog approaches, yet faces a set of technology-related hurdles, which are discussed below. The combined specifications on linearity, bandwidth, dynamic range, noise floor and accuracy are very high and require state-of-the-art components and novel design approaches, as the emulator needs to outperform the already high performance xDSL equipment in order to successfully validate it.

Hard delay Constraints— The correct emulation of the phase response, and of its first derivative, the group delay, is a constraint not often found in the design of a digital (sub)system. Strict end-to-end delay budgets need to be met, resulting from the physical propagation along the emulated line segments. The available computational window, i.e. the time available to perform the necessary calculations, is equal to the delay of the emulated physical medium, minus the time needed for the A-to-D and D-to-A conversions and the delay of the analog low pass filters. This means that for one of the shortest sections in the ETSI and ANSI VDSL test loops, a 150 ft cable, only 300 nsec processing time is available (Figure 8). It is clear that very high performance digital filter structures are needed, especially for the shorter cable lengths. The delay budget needs to be carefully distributed over the building blocks of the system.

Bandwidth— The bandwidth of the system is limited by the throughput rate of the FPGA based signal processing core, through the Nyquist condition. A sample rate of 32 MSPS is necessary to process the full VDSL bandwidth of 12 MHz without too stringent anti-aliasing filter specifications. The samples are then processed at 160 MHz, minimizing the computational latency. These high core speeds can only be reached using custom placement macros in the Xilinx place and route tools. Typical clock rate improvements, such as pipelining the critical paths, cannot be applied here as this increases throughput delay.

Noise floor and dynamic range— The use of active components puts a compromise on the noise floor performance and dynamic range of any device, compared to a completely analog approach. The noise level due to round-off inside the digital core is minimized by using a processing word width of 32 bit. The analog frontend, which takes care of the A/D and D/A conversion will present itself as a limiting factor. In that respect, special care was taken to optimize the design from a system perspective.

D. Digital FPGA Filter Core

In literature, a number of attempts to perform physical layer emulation digitally are documented. In most cases, simplifications are made to the original model to reduce complexity or to increase the feasibility of a real-time implementation. This leads to partially inaccurate representations of the physical medium of interest.

In [9], a frequency domain approach for telephone access network emulation is described using digital techniques. However, the approach does not result in an accurate reproduction of a real loop topology, for two reasons: first, the author uses block-based processing of the input signal stream, which inevitably results in a misrepresentation of the group delay response of the topology, because the sampling window generally exceeds the group delay of most loop topologies. Secondly, the author describes a unidirectional solution, discarding the effects of loop reflections on the transmitter end. In the domain of powerline communications, Götz and Dostert propose a reduction of the theoretical model derived in [10], by only extracting the dominant paths in what is perceived as a multi-path environment and employing FIR filter structures to approximate the channel response. A real-time implementation such as the one proposed in [11] certainly profits from this complexity reduction, but fails to include all details of the original channel. The proposed hardware concept again only provides unidirectional emulation of the channel, suffering from the same limitations as in [9].

The filter architecture proposed in this paper splits a loop topology as shown in Figure 1 into building elements, namely lines and bridged taps and remains close to the actual cable layout. Apart from lines and bridged taps, which have a physical equivalent, a virtual element, the node, is introduced as well : the node represents the splices where cable sections are joined together and are responsible for the frequency dependent reflections that occur due to characteristic impedance mismatches between cable sections.

All cable sections are represented by a cascade of a filter section and a delay line that emulates the (constant part of the) group delay of the section. A line, a node and a bridged tap are combined in what is referred to as a 'basic building block' or BBB (Figure 4). Multiple BBB are concatenated to form the corresponding cable topology (Figure 5).

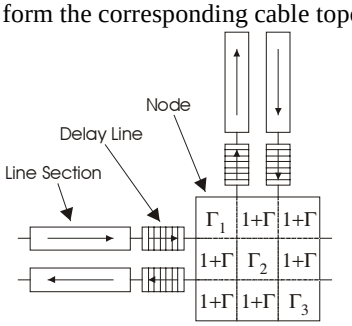

Figure 4 : BBB detail

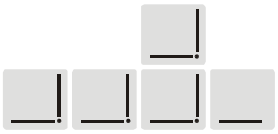
Figure 5 : Topology Decomposition in BBBs

Line en node sections are devised from several configurable, bi-directional 2nd order IIR filters processing a 32-bit wide input in five clock cycles using only three 32x18 bit multipliers and four adders. In order to process 32 MSPS with minimal latency, an internal clock rate of 160 MHz is needed. If such a design is combined with careful delay distribution over the building blocks, lines as short as 150ft can be accurately emulated.

The FPGA design comprised of the aforementioned configurable building blocks defines the loop topology. The actual frequency dependent characteristics of the lines and nodes are defined by uploading a set of parameters to the modules. The generation of these coefficients is outside the scope of this paper [12].

Each building block is in-system reconfigurable, thus allowing the emulation of time varying parameters such as temperature influences. In order to maximize the flexibility of an FPGA design some building blocks can be bypassed and the line propagation time can be adjusted using a configurable delay line. This highly modular and flexible approach allows the accurate emulation of ETSI and ANSI VDSL test loops 0 to 4 as well as custom loop topologies. This is in sheer contrast with commercially available access loop emulators, only supporting ETSI and ANSI loops 0,1 and 2 with limited flexibility.

E. Hardware Overview

The digital propagation module consists of two identical interconnected boards each hosting a high performance 14-bit ADC, one 14-bit DAC and a USB 2.0 interface (Figure 6, Figure 7). One module interfaces to a hybrid connected to the subscriber DSL modem and the other module connects through a second hybrid with the central office equipment. As only four extended eurocard sized boards are needed, a complete emulator only takes a volume of only l8 dm^3.

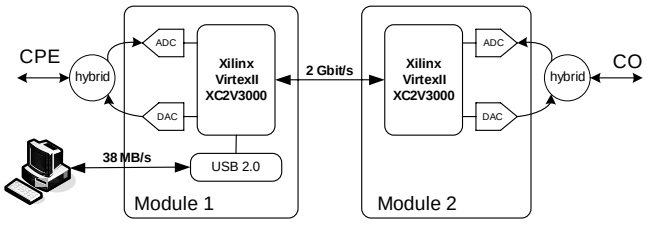

Figure 6 : Dual module emulation set-up

The hard real time signal processing is performed on two Xilinx Virtex-II XC2V3000-6 FPGAs, each mounted on a separate board, with a full duplex communication link of 1 Gbit/s each way interconnecting them. In order to address even more complex line topologies, each board can be equipped with a second, identical Xilinx Virtex-II FPGA, doubling the number of available logic gates up to 12 million.

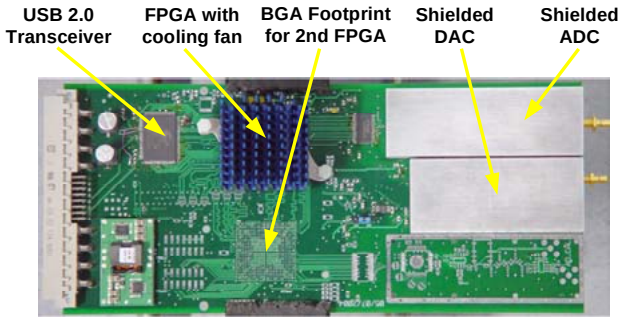

Figure 7 : The digital processing core

Special care was taken in the design of the analog frond-end. First of all, custom shielding made of a solid metal slab was fabricated in order to achieve an isolation better than 104 dB between the A/D and D/A channel.

Secondly, the noise floor of each channel was optimised. This results in a system with a noise floor below –140 dBm/Hz and a dynamic range of over 90 dB (Figure 11). The control platform of the system is an embedded PC running Linux with a custom USB kernel module. The USB 2.0 connection is used to configure the FPGAs and perform settings afterwards.

The FPGA based signal processing core combined with the high performance analog front-end and a fast PC-link makes this module a versatile hardware platform suitable for a broad range of instrumentation applications.

IV. RESULTS

In this section, the performance of the emulator core is evaluated against a simulation model of the test loops. The reference simulation model is generated using a Matlab-based simulation tool, the FTW xDSL simulation tool [13], which contains model data for all standardized DSL test loop sets. All test loops evaluated here are extracted from the standardized reference test loops mentioned in [3], [4] and are based on the models provided in [2], to provide a basis for objective reference. The measurements shown in the following paragraphs are obtained without the reflection modules in place, to evaluate the performance of the digital core.

The specifications adhered to are those listed in [3]: a maximum magnitude deviation of 3 % on a dB scale and a group delay error of less then 3 % on a linear scale. A schematic view of the topologies covered in the different test cases is shown in Figure 8.

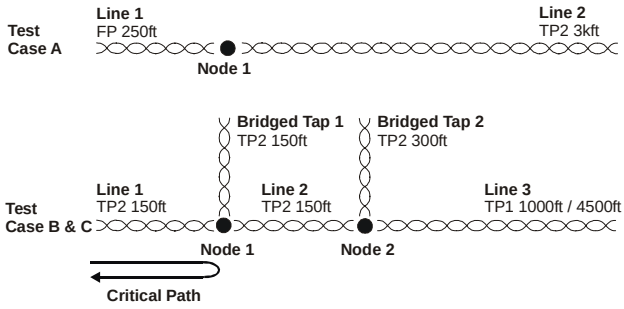

Figure 8 : Loop topologies test case A, B & C

A. Test Case "VDSL 2"

The ANSI VDSL 2 test loop consists of a cascade of two transmission line sections, with a relatively long second section representing street cabling, and a first, shorter section, which may represent cabling at the subscriber's premises. Figure 9 indicates the accuracy with which the loop is emulated. The rather long TP2 section already introduces considerable attenuation at higher frequencies, yet the measured frequency response remains closely matched to the expected model, to within 0.5 dB. The emulated loop topology exceeds ETSI requirements: the group delay always remains within the 3% allowed margin of error, with an average deviation of less than 20 ns.

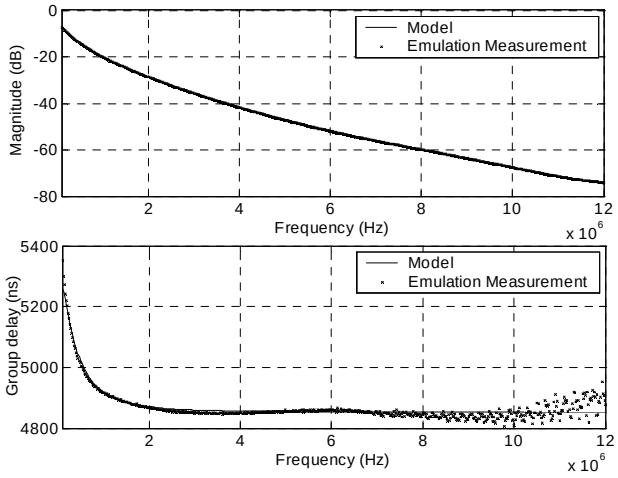

Figure 9 : Results S_{21} topology "VDSL2"

B. Test Case "VDLS 4 – 1kft"

An example of a complex loop topology is the ANSI VDSL 4 test loop. Its topology and resulting characteristic was already shown in Figure 2. This topology is an excellent example of delay limited design and the careful distribution of the delay over the building blocks. The first node, where signal reflections occur, is encountered after only 150 ft, this corresponds to a round-trip delay of 457 ns. This figure includes the propagation delay across the propagation modules and the signal conversion circuits, which amounts to approximately 200 ns, leaving only 257 ns to digitally process the incoming signals. The capability to digitally emulate short line sections is clearly demonstrated. The location of the notches, and their depth, is clearly defined indicating correct emulation of both group delay and amplitude response of the two bridged taps. Figure 10 shows the close correspondence between the model of the emulated topology and the measurements. The group delay remains within the allowed margin of error (dashed line), except for the lowest frequency notches, where the margin is exceptionally tight. However, the severity of this deviation is debatable, considering the fact that xDSL equipment will generally avoid transmission in these notches. With exception of these notches, group delay emulation is accurate to within a 50 ns margin.

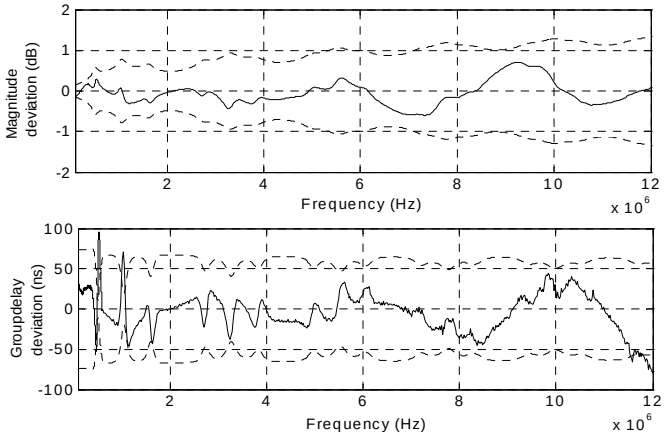

Figure 10 : Emulation Error VDSL4 1kft

C. Test Case "VDSL 4 - 4.5 kft"

As an illustration of the dynamic range that can be reached with the digital building block concept, a VDSL4 test loop with a 4500 ft TP1 section is shown in Figure 11. Above 6 MHz, the attenuation remains below 98 dB. The group delay maintains compliance up to 4.5 MHz, above which noise prohibits an accurate phase measurement. However, the average group delay is maintained up to 6 MHz.

Finally, the scattering parameter $S_{11}(\omega)$ of this loop topology is shown in Figure 12, demonstrating the delay accurate emulation of extremely short line sections. Accurate representations of the reflections at both the network side and the customer side are important in the evaluation of xDSL equipment, as high level reflections of the upstream signal may mask the considerably lower power downstream signal. Secondly, correct emulation of the group delay at both sides of the loop is necessary to realize the correct input impedance of the loop, which is dependent on the characteristic impedance of the line section, but also on the frequency response of the propagation module. The performance of the

emulator is exemplary as even in the notches, the emulator accurately reproduces the complex loop behaviour.

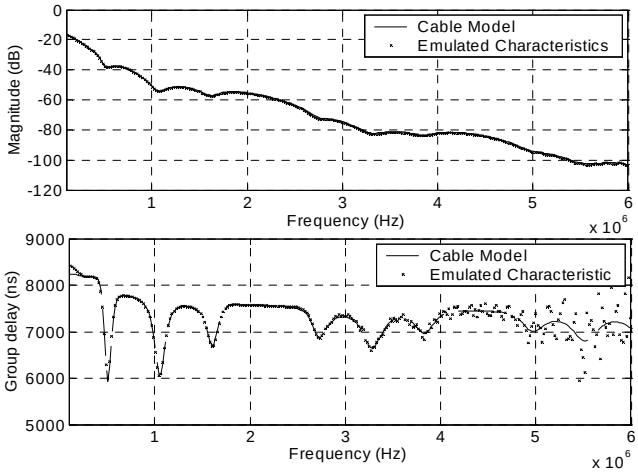

Figure 11 : Results S_{21} topology "VDSL4 4.5kft"

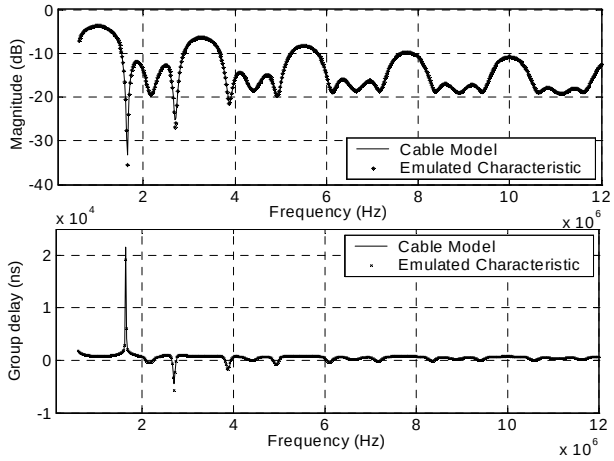

Figure 12 : Results S_{11} topology VDSL 4 4.5kft

V. CONCLUSION

In this paper, a reconfigurable platform for the emulation of telephone access networks is presented. The multi-million gate FPGA design is capable of emulating both amplitude and absolute phase of a complex line topology, even for very short line sections, and reproducibly achieves a substantially better accuracy than current, commercially available emulators. The modular building block concept, easy reconfiguration and high performance analog signal handling make this a very flexible instrument for further exploration and development of xDSL technology.

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