A Digital Calibration Technique for the Correction of Glitches in High-Speed DAC's

B. Catteau, P. Rombouts and L. Weyten
Ghent University (UGent), Dept. ELIS, Sint-Pietersnieuwstraat 41, 9000 Ghent, Belgium
Email: benoit.catteau@elis.UGent.be

***Abstract*— The accuracy of high-speed DAC's is limited by dynamic effects such as glitches. Here, a digital calibration technique to compensate this effect is presented. Because of the digital approach, this solution can not be an exact correction of the phenomenon, but a band limited attenuation. The approach consists of adding a (digital) compensation signal to correct the glitch. Both a 2-tap and a 4-tap correction are investigated and it is shown that they can greatly reduce spurs over a bandwidth of 30% and 60% of the Nyquist band respectively, provided the glitch energy is known. Next, it is shown how an adaptive calibration with an additional low-speed calibration ADC can be used to estimate the glitch energy. Simulations confirm that the spectral performance can be greatly improved this way.**

I. Introduction

Nowadays many applications require highly accurate digital to analog converters (DAC's). Especially in communication systems, where digital modulation techniques are applied, excellent spectral performance is required at sampling rates that approach GHz frequencies [1], [2]. At such high frequencies the dynamic performance of the DAC is a limiting factor. E.g. glitches can significantly decrease the performance due to timing imperfections in the DAC circuitry. A common approach to reduce this problem is the use of unit elements and segmentation. In this work we investigate a fully digital calibration technique to correct this effect. This allows the use of binary weighted elements, which are assumed in the discussion, but the approach can be applied equally well to DAC's with unit elements or segmentation.

The overview of the paper looks as follows. In Section II we develop a theoretical model and in Section III we explain the solution that has been adopted. Section IV shows what RSD coding is and the calibration method follows in Section V. Section VI motivates the theory by simulation results and Section VII concludes this paper.

II. The origin of glitches

The precision of a DAC deteriorates because of two kinds of errors: static and dynamic errors. For high speed DAC's, the latter are equally important. First, we will develop a model for the dynamic error.

We can divide the possible dynamic errors into two kinds: the dynamic settling error and the dynamic glitch error. The dynamic settling error occurs when the DAC output varies compared to the desired one. A glitch originates from imperfect timing during the change between two consecutive states of the converter. In [3] it has been shown that the dynamic settling error is of minor importance as opposed to the dynamic glitch error.

Consider a binary weighted, current-steering DAC, as in Fig. 1. In such a DAC, at a clock transition, some sources switch off, and some others switch on. Due to unavoidable timing inaccuracy, none of the sources switch exactly at the same time. This lack of synchronicity is the origin of dynamic glitch errors (Fig. 2).

To model this phenomenon, we will assume that the current summing node is linear. This way we can state that the output signal

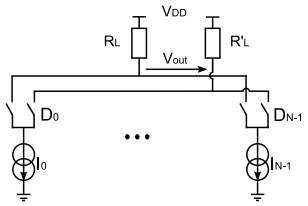

Fig. 1. A current-steering DAC

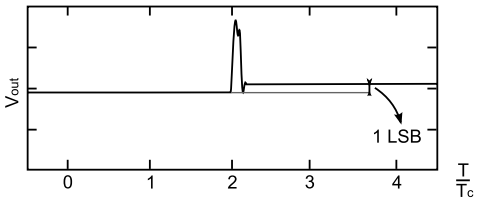

Fig. 2. Typical glitch at a major carry transition in a binary weight coded DAC resulting in 1 LSB difference.

$V_{out}(t)$ consists of a sum of the current waveform i of each source:

$$V_{out} = \sum_j i_j = \sum_j D_j \, I_j \cong \sum_j D_j \, 2^{-j} \, I_0 \qquad (1)$$

where i_j stands for the contribution of the j'th current source, D_j is the digital code applied to the j'th source of the DAC, which can be 1 or -1, I_j is the nominal value of source j and I_0 is the nominal value of the most significant bit (MSB). From this model, it is clear that by reducing the errors occurring at a single current source, we will improve the characteristics of the DAC. We consider the actual output of one current source as the sum of the nominal output and two error contributions, the static and dynamic one (Fig. 3).

Focussing on the dynamic error signal, the first delay ϵ, and the second delay $\epsilon + \phi$ are the origin of glitches.

We have chosen to reduce the impact of the glitches in the digital domain, thus not correcting the analog waveform. This means that the sampling clock is a limiting factor and that we will not be able to perfectly correct the glitch itself. Additionally, this digital approach imposes the use of redundancy into the DAC, as will become clear.

III. Digital solution

Because we intervene only in the digital domain, the solution will be band limited. We represent the glitch by a Dirac delta. Since glitches are short compared to one clock period, this is a defensible assumption. In the digital domain, we can only change the input signal at the sampling clock edges. In our model, glitches occur when a current source switches, and since the input signal is known, this means that the location of the glitch is known as well. To correct the glitch, we will modify the digital codes before and after the glitch.

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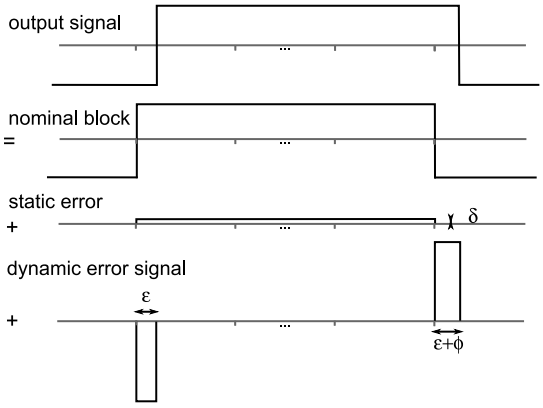

Fig. 3. We consider the generated pulse as a sum of the nominal one and the static and dynamic error. Due to synchronicity problems, there are glitches arising, one at the start of the pulse and one at the end.

To correct the effect of the glitch Dirac delta from $-\frac{f_s}{2}$ to $\frac{f_s}{2}$, a rectangular correction in the frequency domain is needed. This corresponds to a sinc function in the time domain. Here, we have considered only the two simplest solutions for implementation reasons. The first is using a 2-tap correcting signal (= the shortest estimation of a sinc pulse), and the second a 4-tap one, (Fig. 4). This means that we have to introduce delay in order to correct codes before the glitch occurs. We have:

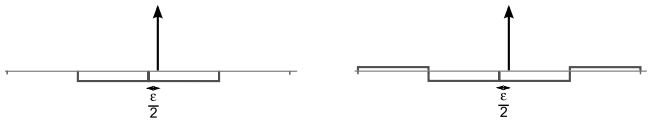

Fig. 4. The two correction signals mentioned, left 2-tap, right 4-tap. the arrow signifies the glitch represented as Dirac delta.

$$\mathcal{F}\left(A\,\delta(t-\epsilon/2)\right) = \epsilon\, I = A \tag{2}$$

for a glitch with length ϵ occurring at time $t = 0$ and weight A. $\mathcal{F}$ here stands for the fourier transform operator and δ is the Dirac delta. When we apply the 2-tap solution, we obtain in the frequency domain:

$$\frac{\alpha\, A}{2\, T}\,\mathcal{F}\left(u\left(t+T\right)-u\left(t-T\right)\right) = \alpha\, A\, sinc\left(2\, f\, T\right) \tag{3}$$

where α is a tuning parameter, $u(t)$ is the heaviside function and $sinc(x)\left(\equiv \frac{\sin(\pi\, x)}{\pi\, x}\right)$, the normalized sinc function. By setting α equal to 1, we can match the energy of the glitch, causing a zero DC error and retaining 20dB suppression up to 0.13 f_s. If we overcompensate (we introduce DC error by tuning α to 1.1), it is possible to maintain the afore-mentioned suppression and to expand the frequency band to 0.17 f_s. In Fig. 5(left), the grey curves indicate the effect of the solution, the glitch being a Dirac delta. With α set to 1.1, we can see that the zero error has been moved along the frequency axis. The 4-tap solution gives us more freedom, so here the DC error can be left zero. The correction now looks like

$$\begin{aligned} A\,\mathcal{F}\Big(-\frac{a}{2\,T}\,u\left(t+2\,T\right)+\frac{1+b}{2\,T}\,u\left(t+T\right)- \\ \frac{1+b}{2\,T}\,u\left(t-T\right)+\frac{a}{2\,T}\,u\left(t-2\,T\right)\Big) = \\ A\left[(1+b)\;sinc\left(2\,f\,T\right)-2\,a\,sinc\left(4\,f\,T\right)\right] \end{aligned} \tag{4}$$

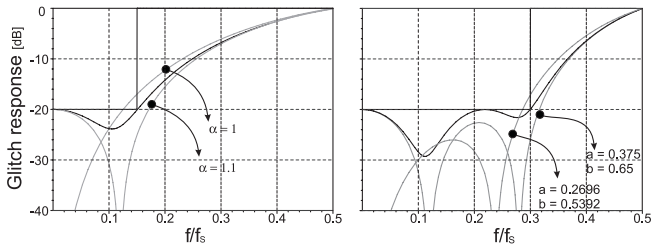

Fig. 5. The magnitude of the amplitude spectrum A, of a 18 % long compensated glitch (2-tap, left) and a 9,5 % long glitch (4-tap, right). Beside the specification and the effect of compensating a Dirac delta (grey colour), the black curves indicate the course of the three compensated shaped pulses.

and has been visualized in Fig. 5(right). Compared with the 2-tap solution, we can expand the frequency range to 0.29 f_s, where we still have an attenuation of 20 dB and no error at DC ($2\,a = b$). But, just like the 2-tap solution, we can overcompensate, keeping 20 dB attenuation and expanding our frequency band up to 0.32 f_s.

However, the actual glitch is not a Dirac delta, but has an unknown shape. Referring to our model (Fig. 3) it is a square pulse. But, due to more complicated switching behaviour, the shape can be different. To examine the influence of this, we have simulated the effect of a pulse of finite time with different shapes (Fig. 6). We have found that the shape of the glitch is not determining. Though, the longer the glitch lasts, the more the solution is under pressure. We have seen that the glitch can maximally be 18 % long for the 2-tap to retain 20 dB of spur suppression up to 0.15 f_s, and 10 % long for the 4-tap compensation up to 0.3 f_s (Fig. 5). This indicates that this digital approach is robust as long as the energy of the glitches can be measured appropriately.

Fig. 6. The three different shapes we examined the robustness with: a rectangle and two triangles as the actual form of the glitch

IV. RSD

If we want to use the DAC itself for calibration, redundancy is required. This is important, because a glitch appears at a state transition, e.g. from $D_i = -1$ to $D_i = 1$. If we want to correct this with one DAC, we need to preserve the transition from -1 to 1, and compensate using the remaining current sources. Adding a third switch to every current source (Fig. 8(a)) it is possible to introduce a third level, i.e. $D_i = 0$. Consequently, the binary words have to be translated into three level words or 'trits'. By doing this, choices have to be made, because now we can apply different 'trits' with exactly the same current result (Fig. 7). For example, the combination of trits $D_i = < 0\ 1\ 0\ 0\ \ldots >$ gives exactly the same analog signal as $D_i = < 1\ -1\ 0\ 0\ \ldots >$. We exploit these possibilities and preserve the glitch, while still changing the digital values around the glitch. Note that this type of redundancy was called RSD (Redundant Signed Digit) and has widely been used in pipelined A/D converters [4].

Adding a third switch to the architecture, complicates the switch-driver circuitry. Hence, not one current source is used, but this 'logical' source can be built out of 2 smaller real sources (Fig. 8(b)). This brings along that for every 'trit', now two sources can cause glitches. Here, the second option is chosen.

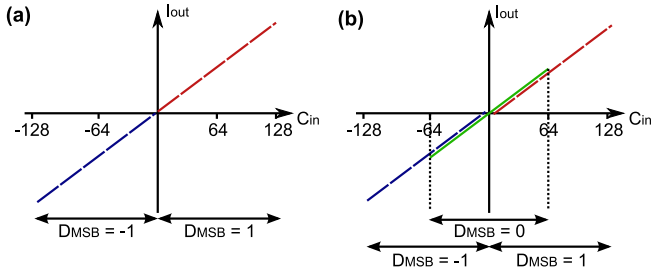

Fig. 7. (a)The normal coverage C_{in} of an eight bit DAC.(b)An eight bit binary weighted DAC with RSD, the overlap indicated for the most significant current source.

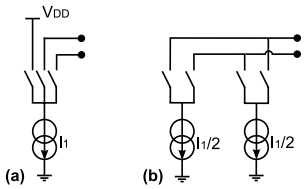

Fig. 8. Actual RSD coding: a 'logical' current source is built out of two real current sources. Both real sources can show a dynamic error.

V. Calibration

The calibration requires a calibration ADC and occurs at start-up. During this calibration cycle the DAC is clocked at its full speed. Although the principle is general we will assume the calibration ADC runs a factor 100 slower than the main DAC. This could e.g. correspond to a DAC clock of 250MHz and a reference high-accuracy ADC sampling at a rate of 2.5MHz which can certainly be achieved with today's $\Sigma\Delta$ modulation technology [5]. However, the calibration principle also works if the calibration ADC is more than a factor 100 slower than the DAC. This calibration ADC is connected to the output of the DAC via a lowpass filter (Fig. 9) and errors are measured at rather low frequency. The lowpass filter could e.g. be a simple first-order RC filter. Because of imprecise values of the components in this analog lowpass filter and because the ADC most likely has a gain error with regard to the DAC, direct comparison of the ADC output with the digital input is rather dangerous. By using adaptive calibration, we can avoid these possible calibration errors. The same calibration scheme will always be followed:

$$e_{new} = e_{old} + \Delta\left(ADC_{\text{reference}} - ADC_{\text{measurement}}\right) \qquad (5)$$

where e_{new} is the correction applied to the DAC, Δ the adaptation size, and $ADC_{\text{reference}}$ and $ADC_{\text{measurement}}$ the result obtained from the ADC for the reference signal and the trit that needs to be calibrated respectively.

An actual converter requires calibration of both the static and the dynamic errors, which are both done with the same setup (Fig. 9). However in the following discussion we will focus on the dynamic error and assume that the static errors have already been corrected.

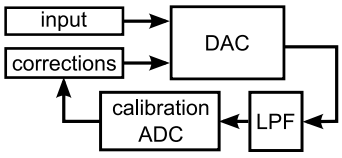

Fig. 9. General overview of the calibration setup.

The dynamic calibration is done for each current source separately, starting from the least significant to the most significant. The calibration of one current source requires two phases. In a first phase, the difference between the delay to switch on and off is determined, which corresponds to ϕ in Fig. 3. To obtain this, we apply an appropriate sequence. This is illustrated on Fig. 10 for the calibration of the second most significant current source. This sequence alternates at the (very high) clock speed of the DAC. Hence, the output of the lowpass filter will be the mean output value of the DAC, which is captured by the calibration ADC. The measured value contains the average value of the two alternately applied input values plus a contribution of the glitch and of the correction pulse. Now the error signal is obtained by subtracting the measured value from the nominal average value. As long as the contribution of the glitch and the contribution of the correction pulse don't cancel, the error is non-zero and the correction is updated according to (5).

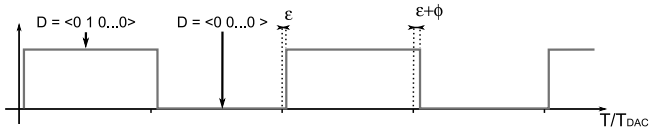

Fig. 10. The sequence applied when compensating the difference between the on and off delays, for the calibration of the second current source.

The second phase in the dynamic calibration of a current source takes care of the delay, or ϵ in Fig. 3. In measuring this contribution, the following problem occurs. Switching on and switching off results in a glitch of which the low-frequency content has the same magnitude but the opposite sign. This way both can easily cancel each others low-frequency contribution, making it impossible to measure this error with the calibration ADC. A solution for this problem is to apply a sequence that is switching at the (slow) clock frequency of the calibration ADC. This is shown in Fig. 11 for the calibration of the second current source. Here the DAC is configured to switch between two values that should give the same analog output current. Again the actual output of the DAC contains contribution of static errors, the glitch error and the contribution of the correction pulse. In our procedure the static errors should be calibrated first. So we assume that this contribution is zero at this point. Referring to Fig. 11, we see that both the second and the third current source switch. However, we calibrate from back to front, thus contribution of the third source should be cancelled. After lowpass filtering the glitches are convolved with the impulse response of the filter. The ADC measures at a low clock frequency and will show only one value per glitch, resulting in a square waveform at the output of it. The mean of this digital signal is being subtracted by applying a digital filter. The amplitude of this square wave is the error signal resulting from the difference between the correction pulse and the glitch, and is used to update the correction parameters, according to (5).

VI. Simulation results

To validate our calibration approach, we have made a simulation model of a high-speed DAC, where both dynamic and static errors are included. We consider a 16-bit DAC, where 8 additional bits are added to eliminate the effect of digital truncation errors. The calibration ADC is assumed to have infinite precision. All the current sources were assigned a random static mismatch (of 1%). To study our dynamic calibration technique, also dynamic errors (of about 1% of the clock period) were added according to the model of Fig. 3 to the two most significant current sources.

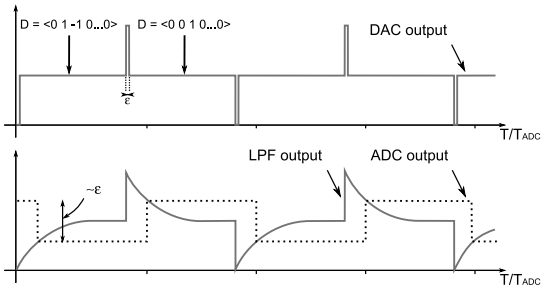

Fig. 11. The calibration sequence when measuring the delay of the source being calibrated and the other sources. Here, the on and off delay is assumed to be the same. The dotted line shows the signal after the ADC.

The entire calibration consists of a static calibration and a dynamic calibration. Fig. 12 shows the simulated output spectrum of the DAC driven by a 2-tone input signal (with frequencies 0.096 f_s and 0.085 f_s), before and after the static calibration. Obviously the spurs are only slightly reduced, by the static calibration. This motivates the need of the dynamic calibration

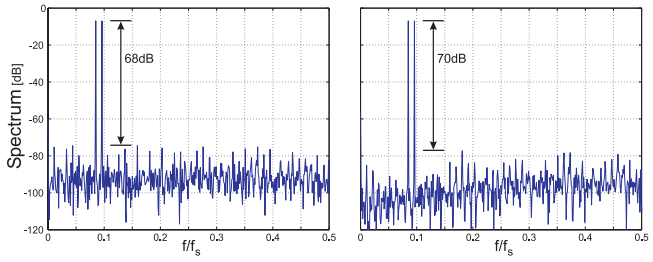

Fig. 12. Two-tone output spectrum of the DAC, before (left) and after static calibration (right).

The dynamic calibration occurs in an adaptive loop. To illustrate the dynamics of this adaptation process, the value of the correction term during the calibration is depicted in Fig. 13, for the case where the difference in rise/fall times (ϕ) is measured. A typical damped convergence is observed. The overall results after a full calibration of

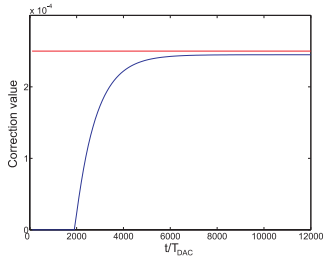

Fig. 13. Dynamics of the adaptive loop. The theoretical correction is shown on the figure, as well as the adaptation of the real value.

the simulation model are shown in Fig. 14 both for the 2-tap and 4-tap correction. In both cases the worst case spurs are not significantly improved. However, as predicted by the theory in section III the spurs are greatly attenuated over a bandwidth of 0.15 f_s and 0.3 f_s for the 2-tap and 4-tap correction respectively. Over this bandwidth a SFDR of more than 90 dB is obtained, confirming the theory.

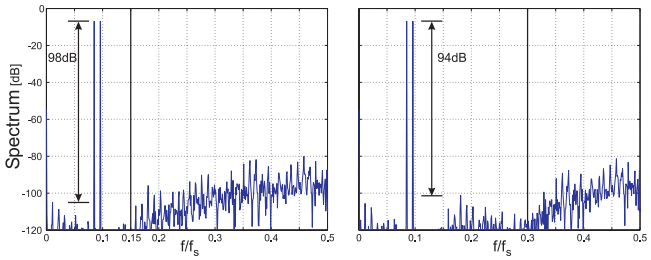

Fig. 14. Two-tone output spectra of the fully calibrated DAC, for the 2-tap (left) and the 4-tap (right) correction.

VII. Conclusion

We have presented a digital domain approach to compensate dynamic glitch errors in high-speed DAC's. Therefore, this solution is not an exact compensation of the phenomenon, but a band limited attenuation. We found that the glitch energy is the determining factor and that the actual shape of the glitch is relatively unimportant. We have examined a 2-tap and a 4-tap solution. The simplest 2-tap solution can reduce the effect of the glitches with 20 dB over a bandwidth of 30% of the Nyquist-band. The slightly more complex 4-tap solution achieves the same attenuation over 60% of the Nyquist-band. Based on this we have shown that an adaptive calibration with an additional accurate but low-speed calibration, can accurately estimate and hence also correct the glitches. Simulations confirm that greatly enhanced performance can be obtained, this way.

Acknowledgment

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