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PV/Battery Grid Integration Using a Modular Multilevel Isolated SEPIC-Based Converter

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Abstract: Photovoltaic (PV) plants can be built rapidly when compared with other conventional electrical plants; hence, they are a competent candidate for supplying the electricity grid. The output power of the PV modules can be used in plug-in electric vehicles (PEVs) DC charging stations to reduce the burden on the electricity grid, particularly during peak load hours. To integrate PV modules and electric vehicles (EVs) with the electricity grid, the modular multilevel converters (MMCs) topologies producing staircase voltage waveforms are preferred as they are able to deliver less total harmonic distortion (THD) and higher efficiency in addition to lower voltage stress on semiconductor switches. In conventional centralized MMC topologies, a direct connection to a high-DC-link input voltage is required which is not appropriate for PV plants. A new MMC topology for PV/EV/grid integration is proposed in this paper, where the individual PV arrays are directly connected to each phase of the AC grid to harvest the maximum available power point. A current-source converter (CSC) based on a single-stage isolated SEPIC converter is adopted as the submodule (SM) for the proposed MMC topology given its outstanding features, such as low input ripple current, high efficiency, high power factor, and flexible output voltage higher or lower than the input voltage. The single-stage SMs can operate in both DC/DC and DC/AC operating modes. Proper controllers for each mode of operation are designed and applied to supply constant current from either the PV modules or the battery cells by eliminating the second-order harmonic component. The performance of the proposed converter is verified by simulations and a downscaled prototype controlled by TMSF28335 DSP.

Keywords: photovoltaic systems (PV); modular multilevel converters (MCs); maximum power point tracking (MPPT); electric vehicles (EVs); SEPIC converter; grid-connected topology; state-space analysis

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1. Introduction

The transport sector is a principal contributor to greenhouse gas emissions (GHGs) and environmental contamination [1]. Aside from GHGs, on- and non-road vehicles emit hazardous pollutants such as oxides of nitrogen (NOx), carbon monoxide (CO), particulate matter, and sulphur, which leads to numerous death-dealing diseases for human beings [1]. Electric vehicles (EVs), including plug-in electric vehicles (PEVs), battery electric vehicles (BEVs), and hybrid electric vehicles (HEVs), show a steadily more appealing pathway to alleviate environmental concerns caused by these harmful air pollutant emissions [2].

Usually, the local AC grid typically provides the power demanded by the battery system inside the EV. Nevertheless, the environmental benefits of EVs can be realized only when they are charged by green energy sources such as solar photovoltaic (PV), fuel cell, wind, ultra-capacitor, etc. [3]. Solar PV, among all, is the most favoured since it is a truly renewable energy source with low maintenance costs and can be adopted in diverse applications. As the output power of the PV cells is DC, it can be directly employed to

charge a PHEV through offboard DC fast chargers, thereby decreasing operational cost, reducing the dependency on the AC grid, and increasing energy efficiency and reliability, in addition to further minimizing GHGs [3]. Moreover, solar PV energy can be converted and injected into the AC grid [3,4].

Numerous studies on solar PV-based EV chargers and their associated control algorithms are reported in the literature [5,6]. The power conversion in PV-based EV chargers generally includes two stages, where the host (PV) and battery sides are separately controlled by the front- and back-end stages [4,7]. On the other hand, the grid-tied topology usually utilizes a DC/DC boost (step-up) converter followed by a voltage-source inverter (VSI). The power converters employed can be either non-isolated or galvanically isolated from the AC grid. The isolated converters can step up the voltage in addition to meeting the required safety standards. In [7], a VSI is used to interface a DC distribution system and the AC grid, and bidirectional DC/DC power converters are employed as battery chargers for PHEV. Unidirectional DC/DC converters are also used to regulate the power flow from PV modules to the DC distribution system. A two-stage grid-connected topology controlled by an adaptive neuro-fuzzy inference system (ANFIS) is presented in [4], which manages to obtain the maximum available power from the solar PV system for the AC grid during daylight and provides constant DC voltages at the battery side during peak hours. In [8], a DC–DC boost converter is used at the DC bus to augment the available voltage from the PV modules and charge the battery of the PHEV. A three-level neutral point clamped (NPC) inverter topology is applied to convert the augmented DC voltage and integrate the solar PV system into the medium voltage AC grid. However, the conventional DC–DC boost converter used in these topologies suffers from high voltage stresses on the semiconductor devices, the reverse-recovery problem of the output diode, and high conduction and switching losses since it is needed to operate at a high duty cycle [9].

Several interleaved DC/DC converters have been developed in the literature to achieve a high step-up voltage gain without an extreme duty cycle ratio [9–17]. Coupled inductor (CI), switched-capacitor, switched-inductor, and built-in transformer (BIT) are the typical components employed in interleaved converters to solve the reverse-recovery problem of diodes and achieve a high-voltage conversion ratio. Furthermore, the turns-ratio of the CI and the BIT can add more degrees of freedom to regulate the voltage gain. An interleaved high step-up DC/DC converter combining CI, BIT, and switched-capacitor was presented in [9], and was used to integrate the PV arrays into an EV DC fast charging station. A non-isolated high step-up DC/DC converter with soft-switching was proposed in [10], in which a Dickson switched-capacitor was used to extend the voltage conversion ratio. To avoid high current spikes, resonant inductors are inserted in the Dickson switched-capacitor circuit. An interleaved boost converter followed by a bifold Dickson voltage multiplier was used in [11] to increase the voltage gain. Another interleaved high step-up converter was presented in [12], which can recycle the leakage energy of CIs and reduce large voltage spikes across the semiconductor devices, thanks to its passive clamp performance. The interleaved converter in [13] recycles the leakage energy of CI without an additional clamp circuit. Active clamp circuits and an integrated regenerative snubber, in addition to dual CIs in series connection, were employed in the non-isolated high step-up DC/DC converter in [14]. Interleaved topologies benefit from low current stresses and voltage spikes on the semiconductor devices, soft-switching, the reduced size of the magnetic components, and high efficiency, in addition to low input current ripple. Hence, they are promising candidates for high current and power density solar PV systems [17]. Nonetheless, the increased number of components, hence, the high cost and size, and the reduced power conversion efficiency have made them less favoured for EV chargers [18]. As an alternative, single-stage charging configurations have been employed in the literature [18,19]. Transformer-less bidirectional Z-source inverters have attracted great interest in PV grid-interconnected systems, which can also be modified and applied to EV battery charging infrastructures. These barriers in Z-source-based single-stage structures include increased size of components and voltage stress on the semiconductor devices.

Modularized multi-level converters (MMCs) generating staircase voltage waveforms at the AC side are promising solutions for PV–EV–grid integration [20,21]. They are capable of delivering low total harmonic distortion (THD) at the AC side (without applying conventional harmonic reduction techniques [22,23]). Therefore, they will demand smaller electrolytic capacitors (filters) on both the AC and DC sides [24]. High efficiency, low current stress, and low voltage spikes across semiconductor devices are remarkable features of these converters.

A new modular grid-connected topology with an energy storage system is proposed in this paper for the EV/PV/integration, in which isolated single-stage SEPIC-based converters are used as submodules (SMs). Low input ripple current, high power factor, and non-inverted flexible output voltage (higher/lower than the input voltage) are the essential features of the SMs. High efficiency at high input voltages is one of the other excellent benefits delivered by an SEPIC-based SM. Moreover, the SEPIC-based SMs can operate in both DC/DC and DC/AC operation modes without adding an extra DC/DC or DC/AC converter. The battery packs of the PEVs are connected to the PV modules in the DC/DC mode, while in DC/AC mode, the AC grid is interfaced with either the PV modules or the battery packs.

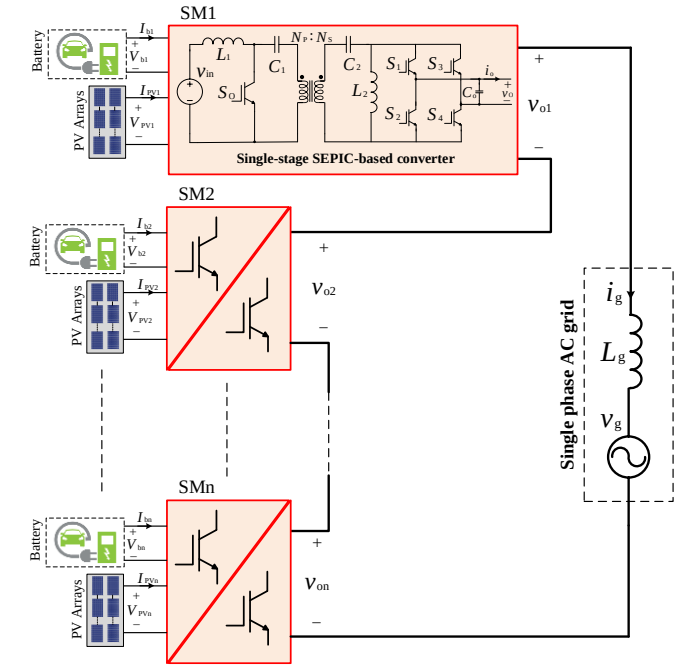
The new modular inverter connects the individual PV modules to the medium voltage AC (MVAC) grid to harvest the maximum possible energy. Maximum power point tracking (MPPT) under different conditions is not discussed in detail in this paper; however, more details can be found in [25,26]. Unlike centralized configurations, in which the entire DC voltage available from the PV modules at the DC bus is used as the input for single- or two-stage topologies, in this paper, individual PV arrays are connected to each phase. Therefore, harvesting the MPP is much more straightforward [27]. Moreover, the whole output power will not be lost if a problem happens in a single PV module, thanks to the modularized structure of the proposed topology.

The SEPIC-based SMs need very small input capacitances at the input side so that the PV modules can operate at the maximum power point efficiently. As the input capacitor is a crucial element affecting the PV system reliability particularly, reducing their values will positively affect the total reliability of the system. The modulation strategy of the employed SEPIC SMs has been modified in this work to allow for storing the second-order energy components inside the SMs to keep the PV modules operating with a constant continuous input current. Embedding battery packs with the PV modules allows for storing their energy when the grid does not need the support for PV modules. The battery charging process is conducted using the same SMs without adding extra components.

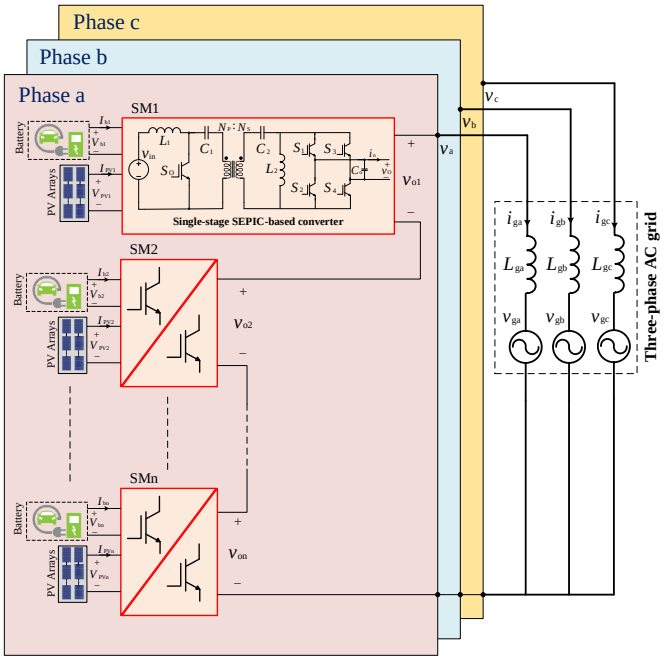
The rest of the paper is organized as follows: the proposed MMC topology is introduced in Section 2, and its operation at the system level is illustrated in Section 3. Operation modes and state-space modelling on the SMs' level are provided in Sections 4 and 5, respectively. Simple hysteresis and proportional-resonant (PR) controllers control the input and output voltages in different operation modes in Section 6. Simulations and experiments in Section 7 verify the proposed topology. Finally, this paper is concluded in Section 8.

2. The Proposed MMC Topology

Figure 1 shows single- and three-phase layouts of the proposed MMC topology for large-scale photovoltaic plants (LSPVs) based on the isolated single-stage SEPIC converter together with battery electric vehicle (BEV) as the energy storage system (EES).



(**a**)



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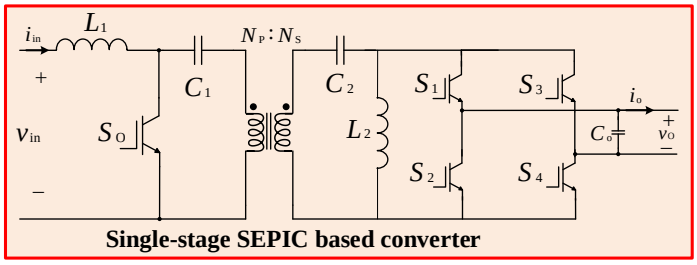


(**c**)

Figure 1. Modular grid-connected MMC topology with EES. (**a**) Single-phase layout. (**b**) Three-phase layout. (**c**) Single-stage SEPIC-based SM.

To support DC/DC (PV modules to EES) and DC/AC (PV or EES to the AC grid) operation modes, the selected SM must be able to provide (i) flexible voltage higher or lower than the input voltages from the PV modules or battery (ii) galvanic isolation between the input and output sides to meet the safety standards of the grid. The SEPIC-based converter is adopted in this work as the SM has outstanding features, including low input ripple current, high efficiency, high power factor (PF), and flexible output voltage higher or lower than the input voltage. As seen in Figure 1c, the SEPIC SM consists of five semiconductor switches (S_o, $S_1 \rightarrow S_4$), two inductors, L_1 and L_2, and three capacitors, C_1, C_2, and C_o. Moreover, a high-frequency transformer (HFT) with turns' ratio N_s:N_P can be employed, so the input and output sides are galvanically isolated to comply with the grid's codes. In addition, the HFT can provide additional voltage boosting if required. The SM's operation modes and steady state-space representation will be presented in the following subsections.

3. System-Level Operation

Assuming that the three-phase layout of the proposed MMC topology is connected to the three-phase MV grid through the grid inductors (L_{ga}, L_{gb}, and L_{gc}) with internal resistances (r_{ga}, r_{gb}, and r_{gc}), the total voltage delivered per phase at the grid side equals the summation of the individual voltages of the series-connected SMs and can be expressed as

$$\sum_{i=1}^{n} v_{oi} = V_o \sin(\omega t + \theta) \tag{1}$$

with V_o and θ being the magnitude of the output voltage of the SMs and the phase-shift with respect to the grid voltage, respectively.

If the three-phase MMC delivers the active power P to the AC grid at a power factor cosφ, then the magnitude of the output voltage V_o, the phase-shift θ, and the per-phase magnitude of the output current I_g for the grid voltage vg(t) = Vg sin(ωt) can be written as

$$I_g = \frac{2P}{3V_g \cos(\varphi)} \tag{2}$$

$$\theta = \tan^{-1}\left[\frac{r_g I_g \sin(\varphi) + \omega L_g I_g \cos(\varphi)}{V_g + r_g I_g \cos(\varphi) - \omega L_g I_g \sin(\varphi)}\right] \tag{3}$$

$$V_o = \left[\frac{V_g + r_g I_g \cos(\varphi) - \omega L_g I_g \sin(\varphi)}{\cos(\theta)}\right] \tag{4}$$

4. Modes of Operation

For each SM, single-pole-double-through (SPDT) relays S_{PV} and S_{bj} (j = 1, 2, 3) can be used, as shown in Figure 2, to connect the SM to the PV array the battery pack, or the AC grid. Thus, the proposed MMC can operate in two different modes (DC/DC and DC/AC), depending on the connection of the relays. In addition, a pair of SPDT relays, $S_{g,}$ is used to connect the AC grid to the output terminals of the SM. The resulting modes of operations will be discussed in more detail in the following section.

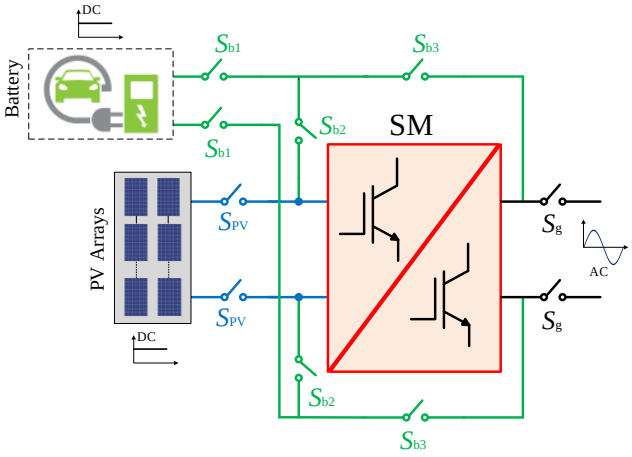


Figure 2. SM equipped with SPDT relays for different operation modes.

4.1. DC/AC Operation (from PV Modules/Batteries to the AC Grid)

The SPDT relays connections when the real power is delivered from the PV modules, and the battery packs to the AC grid are shown in Figure 3a,b, respectively. To deliver power from the PV modules to the AC grid (Figure 3a), all the SPDT relays are opened except *Spv* and *Sg*. Thus, the PV modules will be able to support the AC grid, especially during daylight when the PV arrays are generating their highest attainable power. If the power provided by the PV modules is not sufficient to support the AC grid, the SPDT relays S_{bj} (j = 1, 2) can be switched on instead of the relays S_{pv} (Figure 3b). In both cases, the SEPIC-based SM operates as a DC/AC converter.

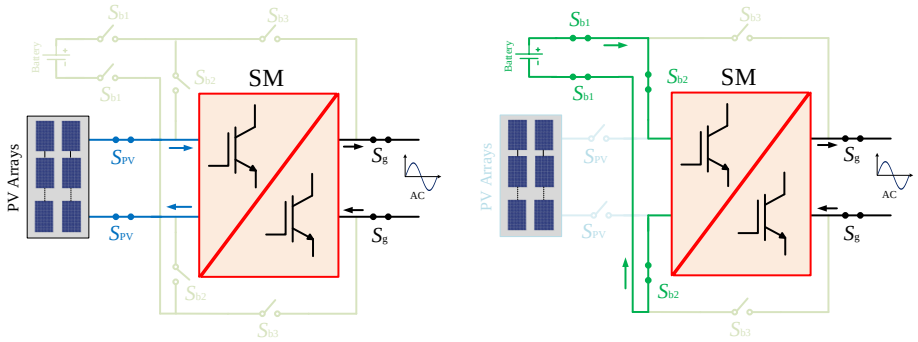


Figure 3. SPDT relays connections. (**a**) DC/AC (from PV to the AC grid). (**b**) DC/AC (from battery to the AC grid).

It should be mentioned that in the DC/AC mode, the PV modules/the battery packs are required to operate at constant voltages and currents, and therefore the input current to the SM should be constant and continuous. However, as the single-phase SEPIC SMs are connected to the single-phase AC grid, the output current and voltage are sinusoidal at the grid frequency (50/60 Hz). Consequently, the second-order harmonic will be re-elected to the input side, causing the input current to have an undesired second-order harmonic which will interrupt the maximum power point tracker (MPPT). Therefore, as shown in Figure 4, the SEPIC-based SM converter should be able to store the second-order voltage or current harmonics in a storage element. To do so, the SM is designed and controlled to operate in three subintervals. In other words, an extra subinterval is considered to store the second-order component in the inductor L_2.

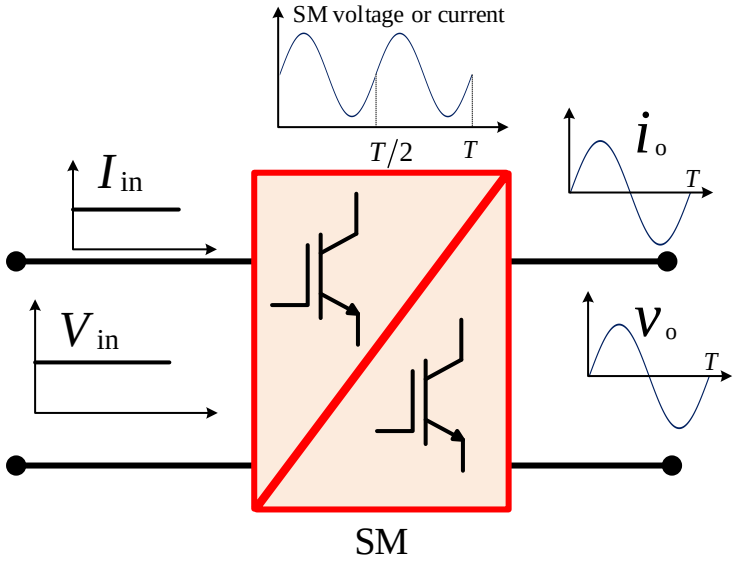


Figure 4. SM waveforms during DC/AC conversion.

The DC/AC mode includes three subintervals whose equivalent circuits for the positive half-cycle (when $v_g > 0$) are illustrated in Figure 5a–c:

- ***Subinterval 1* ($0 \leq t < t_{on1}$):** During the first subinterval (see Figure 5a), the switch S_o is turned ON, so the inductor L_1 is being charged by the input DC voltage (from either PV modules or the battery packs), and its current i_{L1} is linearly increasing. The capacitors C_1 and C_2 discharge into the inductor L_2, increasing its current i_{L2} in a straight line. The output capacitor C_o, on the other hand, discharges into the AC grid. This mode will last for $t_{on1} = d_1.t_s$, with d_1 and t_s being the duty-cycle ratio and the switching time of the SM.
- ***Subinterval 2* ($t_{on1} \leq t < t_{on1} + t_{on2}$):** During this subinterval ($t_{on2} = d_2 \cdot t_s$), the switch S_O is turned OFF. As a result, the inductor L_1 discharge into the capacitors C_1 and C_2, while the inductor L_2 is still being charged by turning S_2 and S_3 ON from the output capacitor C_o. Therefore, this subinterval provides the required decoupling between the input and output sides, as shown in Figure 5b.
- ***Subinterval 3* ($t_{on1} + t_{on2} \leq t < t_s$):** During this subinterval ($(1 - d_1 - d_2)t_s$), the switch S_O is kept in the OFF state, so the inductor L_1 is still discharging into the capacitors C_1, C_2, and C_o, increasing their voltages. For the positive half-cycle ($v_g > 0$), the switches S_1 and S_4 are turned ON. Therefore, the inductor L_2 discharges into the output capacitor C_o (see Figure 5c).

The key output waveforms for the positive half-cycle ($v_g > 0$) are presented in Figure 5d, in which for $N = N_S/N_P$, the voltage $v_{Ceq}(t)$ and the equivalent capacitor C_{eq} are as below:

$$\begin{cases} v_{Ceq}(t) = Nv_{C1}(t) + v_{C2}(t) \\ C_{eq} = \frac{C_1 C_2}{C_1 + N^2 C_2} \end{cases} \quad (5)$$

In addition, D represents the duty-cycle ratio corresponding to the main switch S_o, which in this mode is equal to

$$D(t) = d_1(t) + d_2(t) = \frac{V_O}{V_O + NV_{in}} \quad (6)$$

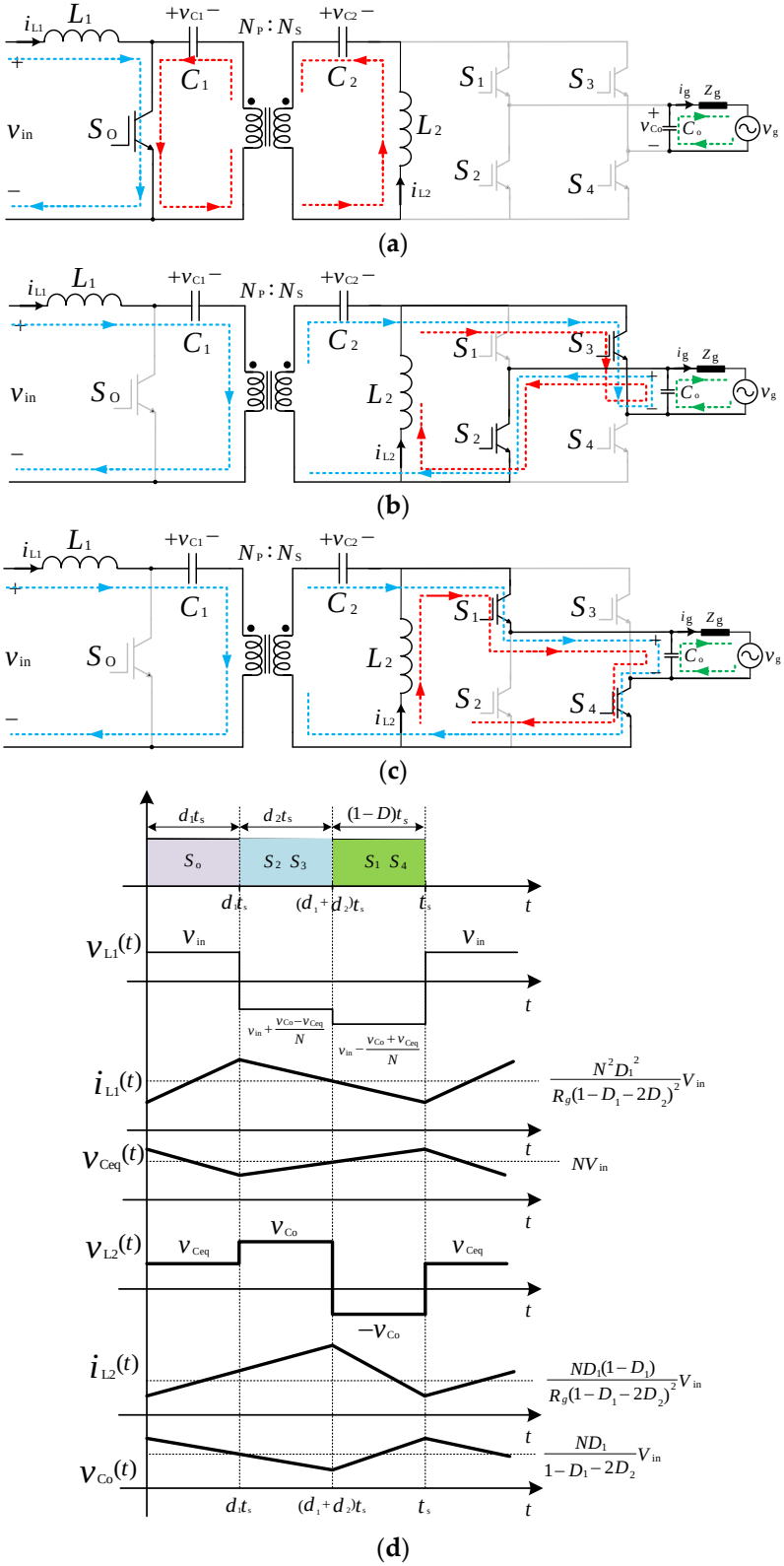


Figure 5. SEPIC-based SM as a DC/AC inverter for the positive half-cycle (v_g >0): (**a**) Subinterval 1 ($0 \leq t < t_{on1}$). (**b**) Subinterval 2 ($t_{on1} \leq t < t_{on1} + t_{on2}$). (**c**) Subinterval 3 ($t_{on1} + t_{on2} \leq t < t_s$). (**d**) Key output waveforms (with $D = d_1 + d_2$).

4.2. DC/DC Operation (Batteries Being Charged by the PV Modules)

The active power can be transferred from the PV modules to the battery packs as long as the AC grid does not demand active power support from the PV modules during

the daytime. Accordingly, the SPDT relays S_{bj} (j = 1, 3) and S_{PV} are connected while disconnecting relays S_g, as shown in Figure 6.

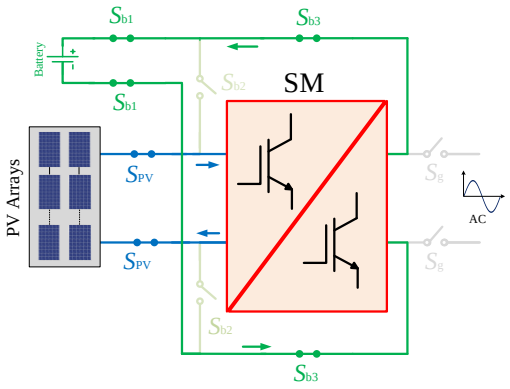


Figure 6. SPDT relays connections in the DC/DC mode (from the PV modules to the battery packs).

This mode includes two subintervals whose equivalent circuits are demonstrated in Figure 7a,b:

- ***Subinterval* 1 ($0 \leq t < t_{on}$)**: During the first subinterval (see Figure 7a), the switch S_o is turned ON, resulting in the inductor L_1 being charged by the input DC voltage (from the PV module). Concurrently, the capacitors C_1 and C_2 are discharging into the inductor L_2. Therefore, i_{L1} and i_{L2} are linearly increasing. The output capacitor C_o, on the other hand, discharges into the battery pack. The duration of this period is $t_{on} = d \cdot t_s$, with and t_s being the duty-cycle ratio and the switching time of the SM.
- ***Subinterval* 2 ($t_{on} \leq t < t_s$)**: During this subinterval ($(1 - d)t_s$), switch S_o is turned OFF. Therefore, the inductor L_1 discharge into the capacitors C_1 and C_2, leading them to be charged. Switches S_1 and S_4 are turned ON to mimic the operation of the typical SEPIC converter and provide a path for the current passing the inductor L_2 to flow through the output capacitor C_o, increasing its voltage (see Figure 7b).

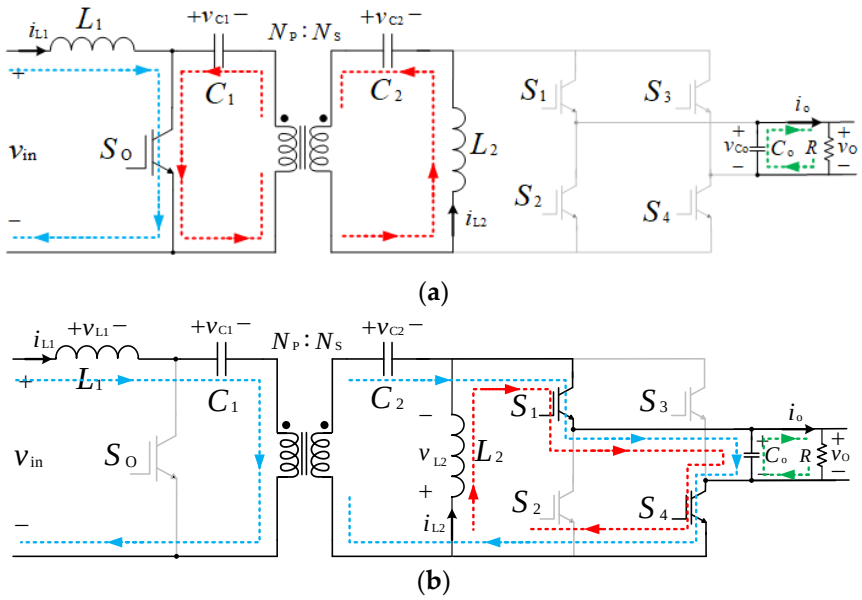
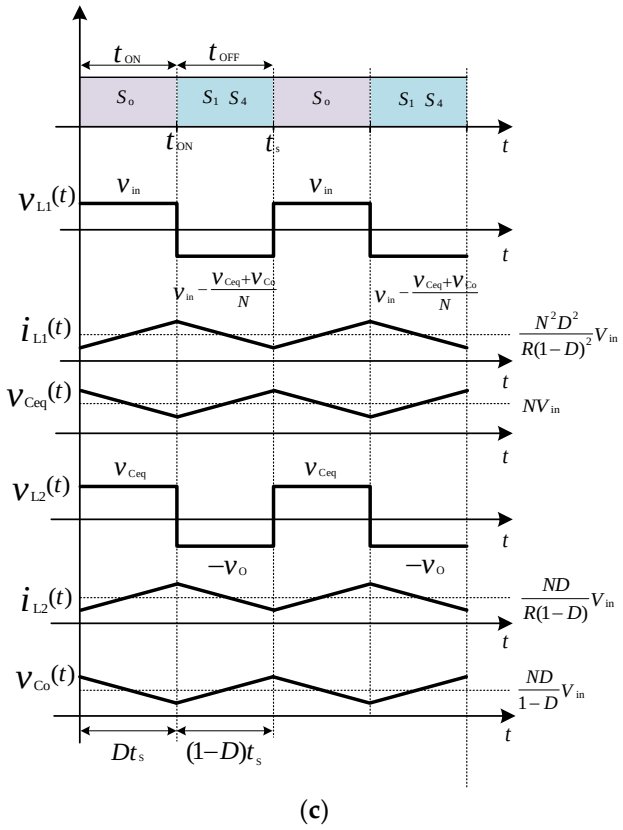


Figure 7. *Cont.*



(**c**)

Figure 7. SEPIC-based SM as a DC/DC converter: (**a**) Subinterval 1 ($0 \leq t < t_{on}$). (**b**) Subinterval 2 ($t_{on} \leq t <$ ts). (**c**) Key output waveforms.

The key output waveforms are presented in Figure 7c, where for $N = N_S/N_P$, the voltage $v_{ceq}(t)$ and the equivalent capacitor C_{eq} are in (5).

5. State-Space Modelling of the Proposed SEPIC-Based SM

As described in the previous section, the proposed SEPIC-based SM operates in two and three states for DC/DC and DC/AC modes, respectively. The states can be averaged over a switching period to extract the state-space model [28,29].

5.1. DC/AC Operation (from PV Modules/Batteries to the AC Grid)

The state-space model of the proposed SEPIC-based SM can be developed over the switching period t_s by writing a set of first-order differential equations governing the circuit:

$$\begin{cases} \dot{x}(t) = A_i x(t) + B_i u(t) \\ y(t) = C_i x(t) \end{cases} \quad (7)$$

where the matrices A_i, B_i, and C_i (where i = 1, 2, 3) represent the system, the input, and the output matrices of the three subintervals in Figure 5, respectively. The state vector $x(t)$ can be expressed as $x(t) = [i_{L1}(t)\ v_{Ceq}(t)\ i_{L2}\ (t)\ v_{Co}(t)]^T$. The input signal $u(t) = v_{in}(t)$ is the output voltage of PV modules or battery packs, and the output $y(t) = v_{Co}(t)$ is the output capacitor voltage.

The three subintervals of the DC/AC operation mode are time-weighted and averaged to extract the nonlinear averaged state-space model as

$$\begin{cases} \dot{\overline{x}}(t) = A\overline{x}(t) + B\overline{u}(t) \\ \overline{y}(t) = C\overline{x}(t) \end{cases} \quad (8)$$

where the matrices A, B, and C are as follows [28]:

$$\begin{cases} A = A_1 d_1 + A_2 d_2 + A_3(1 - d_1 - d_2) \\ B = B_1 d_1 + B_2 d_2 + B_3(1 - d_1 - d_2) \\ C = C_1 d_1 + C_2 d_2 + C_3(1 - d_1 - d_2) \end{cases} \tag{9}$$

The nonlinear averaged model in (8) can be linearized under the small-signal assumption by finding deviations around steady-state operating points (the roots of $\dot{\overline{x}}(t) = A\overline{x}(t) + B\overline{u}(t) = 0$) to derive required transfer functions. After applying Laplace, the small-signal model can be represented as:

$$\begin{bmatrix} \dot{\widetilde{i}}_{L1}(s) \\ \dot{\widetilde{v}}_{\mathrm{Ceq}}(s) \\ \dot{\widetilde{i}}_{L2}(s) \\ \dot{\widetilde{v}}_{Co}(s) \end{bmatrix} = A_{\mathrm{inv}} \begin{bmatrix} \widetilde{i}_{L1}(s) \\ \widetilde{v}_{\mathrm{Ceq}}(s) \\ \widetilde{i}_{L2}(s) \\ \widetilde{v}_{Co}(s) \end{bmatrix} + B_{\mathrm{inv}} \begin{bmatrix} \widetilde{v}_{\mathrm{in}}(s) \\ \widetilde{d}_1(s) \\ \widetilde{d}_2(s) \end{bmatrix} \tag{10}$$

$$\widetilde{v}_o(s) = C_{\mathrm{inv}} \begin{bmatrix} \widetilde{i}_{L1}(s) \\ \widetilde{v}_{\mathrm{Ceq}}(s) \\ \widetilde{i}_{L2}(s) \\ \widetilde{v}_{Co}(s) \end{bmatrix} \tag{11}$$

where the matrices A_{inv}, B_{inv}, and C_{inv} at steady-state operating points are as follows:

$$A_{\mathrm{inv}} = \begin{bmatrix} \frac{\partial \dot{\overline{i}}_{L1}(t)}{\partial \overline{i}_{L1}(t)} & \frac{\partial \dot{\overline{i}}_{L1}(t)}{\partial v_{\mathrm{Ceq}}(t)} & \frac{\partial \dot{\overline{i}}_{L1}(t)}{\partial \overline{i}_{L2}(t)} & \frac{\partial \dot{\overline{i}}_{L1}(t)}{\partial v_{Co}(t)} \\ \frac{\partial \dot{\overline{v}}_{Ceq}(t)}{\partial \overline{i}_{L1}(t)} & \frac{\partial \dot{\overline{v}}_{Ceq}(t)}{\partial v_{\mathrm{Ceq}}(t)} & \frac{\partial \dot{\overline{v}}_{Ceq}(t)}{\partial \overline{i}_{L2}(t)} & \frac{\partial \dot{\overline{v}}_{Ceq}(t)}{\partial v_{Co}(t)} \\ \frac{\partial \dot{\overline{i}}_{L2}(t)}{\partial \overline{i}_{L1}(t)} & \frac{\partial \dot{\overline{i}}_{L2}(t)}{\partial v_{\mathrm{Ceq}}(t)} & \frac{\partial \dot{\overline{i}}_{L2}(t)}{\partial \overline{i}_{L2}(t)} & \frac{\partial \dot{\overline{i}}_{L2}(t)}{\partial v_{Co}(t)} \\ \frac{\partial \dot{\overline{v}}_{Co}(t)}{\partial \overline{i}_{L1}(t)} & \frac{\partial \dot{\overline{v}}_{Co}(t)}{\partial v_{\mathrm{Ceq}}(t)} & \frac{\partial \dot{\overline{v}}_{Co}(t)}{\partial \overline{i}_{L2}(t)} & \frac{\partial \dot{\overline{v}}_{Co}(t)}{\partial v_{Co}(t)} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-D_1)}{NL_1} & 0 & \frac{-(1-D_1-2D_2)}{NL_1} \\ \frac{(1-D_1)}{NC_{\mathrm{eq}}} & 0 & \frac{-D_1}{C_{\mathrm{eq}}} & 0 \\ 0 & \frac{D_1}{L_2} & 0 & \frac{-(1-D_1-2D_2)}{L_2} \\ \frac{(1-D_1-2D_2)}{NC_{\mathrm{o}}} & 0 & \frac{(1-D_1-2D_2)}{C_{\mathrm{o}}} & \frac{-1}{R_g C_o} \end{bmatrix} \tag{12}$$

$$B_{\mathrm{inv}} = \begin{bmatrix} \frac{\partial \dot{\overline{i}}_{L1}(t)}{\partial v_{\mathrm{in}}(t)} & \frac{\partial \dot{\overline{i}}_{L1}(t)}{\partial d_1(t)} & \frac{\partial \dot{\overline{i}}_{L1}(t)}{\partial d_2(t)} \\ \frac{\partial \dot{\overline{v}}_{Ceq}(t)}{\partial v_{\mathrm{in}}(t)} & \frac{\partial \dot{\overline{v}}_{Ceq}(t)}{\partial d_1(t)} & \frac{\partial \dot{\overline{v}}_{Ceq}(t)}{\partial d_2(t)} \\ \frac{\partial \dot{\overline{i}}_{L2}(t)}{\partial v_{\mathrm{in}}(t)} & \frac{\partial \dot{\overline{i}}_{L2}(t)}{\partial d_1(t)} & \frac{\partial \dot{\overline{i}}_{L2}(t)}{\partial d_2(t)} \\ \frac{\partial \dot{\overline{v}}_{Co}(t)}{\partial v_{\mathrm{in}}(t)} & \frac{\partial \dot{\overline{v}}_{Co}(t)}{\partial d_1(t)} & \frac{\partial \dot{\overline{v}}_{Co}(t)}{\partial d_2(t)} \end{bmatrix} = \begin{bmatrix} \frac{1}{L_1} & \frac{(V_{\mathrm{Ceq}}+V_{\mathrm{Co}})}{NL_1} & \frac{2V_{\mathrm{Co}}}{NL_1} \\ 0 & \frac{-(I_{L1}+NI_{L2})}{NC_{\mathrm{eq}}} & 0 \\ 0 & \frac{(V_{\mathrm{Ceq}}+V_{\mathrm{Co}})}{L_2} & \frac{2V_{\mathrm{Co}}}{L_2} \\ 0 & \frac{-(I_{L1}+NI_{L2})}{NC_{\mathrm{o}}} & \frac{-2}{NC_{\mathrm{o}}}(I_{L1}+NI_{L2}) \end{bmatrix} \tag{13}$$

$$C_{\mathrm{inv}} = \begin{bmatrix} \frac{\partial \overline{v}_{Co}(t)}{\partial \overline{i}_{L1}(t)} & \frac{\partial \overline{v}_{Co}(t)}{\partial v_{Ceq}(t)} & \frac{\partial \overline{v}_{Co}(t)}{\partial \overline{i}_{L2}(t)} & \frac{\partial \overline{v}_{Co}(t)}{\partial v_{Co}(t)} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \tag{14}$$

Finally, the line-to-output (known as the perturbation transfer function) and line-to-control transfer functions are derived:

$$G_{v_{\mathrm{in}}}(s) = \left.\frac{\widetilde{v}_{\mathrm{o}}(s)}{\widetilde{v}_{\mathrm{in}}(s)}\right|_{\widetilde{d}_1(s)=\widetilde{d}_2(s)=0} = C_{\mathrm{inv}}(sI - A_{\mathrm{inv}})^{-1}B_{\mathrm{inv}} \tag{15}$$

$$G_{d_1}(s) = \left.\frac{\widetilde{v}_{\mathrm{in}}(s)}{\widetilde{d}_1(s)}\right|_{\widetilde{d}_2(s)=0} = C_{\mathrm{inv}}(sI - A_{\mathrm{inv}})^{-1}B_{\mathrm{inv}} \tag{16}$$

$$G_{d_2}(s) = \left.\frac{\widetilde{v}_{\mathrm{o}}(s)}{\widetilde{d}_2(s)}\right|_{\widetilde{v}_{\mathrm{in}}(s)=\widetilde{d}_1(s)=0} = C_{\mathrm{inv}}(sI - A_{\mathrm{inv}})^{-1}B_{\mathrm{inv}} \tag{17}$$

where I is the unity matrix. The control transfer functions G_{d1} and G_{d2} (derived by neglecting input voltage disturbance) will later be used in the control loops of the input voltage v_{in} (PV or battery voltage) and output voltage v_o (grid voltage), respectively.

5.2. The Calculated Duty-Cycle Ratios for Second-Order Harmonic Elimination

The duty-cycle ratios d_1 and d_2 can be calculated to eliminate the second-order harmonic component. The instantaneous power equation of the converter can be obtained from

$$V_{in} I_{in} = L_2 \frac{di_{L2}}{dt} . i_{L2} + v_o(t) i_o(t) \tag{18}$$

Assuming that the current through L_2 has a DC component plus an AC component of 2ω as

$$i_{L2} = I_{L2} + I_{2nd} \sin(2\omega t + \varphi) \tag{19}$$

with I_{2nd} being the amplitude of the second-order component. Assuming a resistive output load, the desired output voltage and current can be expressed as

$$\begin{cases} i_o(t) = I_o \sin(2\omega t) \\ v_o(t) = V_o \sin(2\omega t) \end{cases} \tag{20}$$

After substituting (19) and (20), Equation (18) can be rewritten as

$$V_{in} I_{in} = 2\omega I_{L2} I_{2nd} L_2 \cos(2\omega t + \varphi) + \underbrace{\omega L_2 I_{2nd}^2 \sin(4\omega t + \varphi)}_{\cong 0} + \frac{V_o I_o}{2} - \frac{V_o I_o}{2} \cos(2\omega t) \tag{21}$$

Assuming that η_{SM} = 100% (i.e., $P_{in} = V_{in} I_{in} = P_o = V_o I_o / 2$), Equation (21) can be rewritten as

$$2\omega I_{L2} I_{2nd} L_2 \cos(2\omega t + \varphi) = \frac{V_o I_o}{2} \cos(2\omega t) \tag{22}$$

Therefore, the amplitude and phase of the second-order component can be extracted as

$$\begin{cases} \varphi = \frac{\pi}{2} \\ I_{L2} = I_{2nd} = \frac{V_o I_o}{4\omega L_2} \end{cases} \tag{23}$$

As the input DC current (battery/PV current) needs to be kept constant, the first row of the average model equations in (8) must be zero:

$$\dot{\bar{x}}_1(t) = \dot{\bar{i}}_{L1}(t) = \frac{-(1 - d_{1ff}(t))}{NL_1} \bar{v}_{Ceq}(t) + \frac{-(1 - d_{1ff}(t) - 2d_{2ff}(t))}{NL_1} \bar{v}_o(t) + \frac{1}{L_1} \bar{v}_{in}(t) = 0 \tag{24}$$

with d_{1ff} and d_{2ff} being feed-forward duty-cycle ratios. Finally, Equations (24) and (6) can be solved simultaneously to extract d_{1ff} and d_{2ff} as follows:

$$\begin{cases} d_{1ff}(t) = \frac{\bar{v}_o(t)(\bar{v}_{Ceq}(t) - \bar{v}_o(t)) + N\bar{v}_{in}(t)(\bar{v}_{Ceq}(t) - N\bar{v}_{in}(t))}{(\bar{v}_{Ceq}(t) - \bar{v}_o(t))(N\bar{v}_{in}(t) + \bar{v}_o(t))} \\ d_{2ff}(t) = D(t) - d_{1ff}(t) \end{cases} \tag{25}$$

5.3. DC/DC Operation (PV Modules to Batteries)

Using the same procedure as DC/AC operation mode, the two subintervals of the DC/DC operation mode are time-weighted and averaged to extract the nonlinear averaged state-space model as follows [28,29]:

$$\begin{cases} \dot{\bar{x}}(t) = A\bar{x}(t) + B\bar{u}(t) \\ \bar{y}(t) = C\bar{x}(t) \end{cases} \tag{26}$$

where the matrices A, B, and C are as follows:

$$\begin{cases} A = A_1 d + A_2(1-d) \\ B = B_1 d + B_2(1-d) \\ C = C_1 d + C_2(1-d) \end{cases} \tag{27}$$

The nonlinear averaged model in (26) can be linearized under the small-signal assumption by finding deviations around steady-state operating points (the roots of $\dot{\overline{x}}(t) = A\overline{x}(t) + B\overline{u}(t) = 0$) to derive required transfer functions. After applying Laplace, the small-signal model can be represented as

$$\begin{bmatrix} \dot{\widetilde{i}}_{L1}(s) \\ \dot{\widetilde{v}}_{\mathrm{Ceq}}(s) \\ \dot{\widetilde{i}}_{L2}(s) \\ \dot{\widetilde{v}}_{Co}(s) \end{bmatrix} = A_{\mathrm{dc}} \begin{bmatrix} \widetilde{i}_{L1}(s) \\ \widetilde{v}_{\mathrm{Ceq}}(s) \\ \widetilde{i}_{L2}(s) \\ \widetilde{v}_{Co}(s) \end{bmatrix} + B_{\mathrm{dc}} \begin{bmatrix} \widetilde{v}_{\mathrm{in}}(s) \\ \widetilde{d}(s) \end{bmatrix} \tag{28}$$

$$\widetilde{v}_o(s) = C_{\mathrm{dc}} \begin{bmatrix} \widetilde{i}_{L1}(s) \\ \widetilde{v}_{\mathrm{Ceq}}(s) \\ \widetilde{i}_{L2}(s) \\ \widetilde{v}_{Co}(s) \end{bmatrix} \tag{29}$$

where the matrices A_{dc}, B_{dc}, and C_{dc} at steady-state operating points are as follows:

$$A_{\mathrm{dc}} = \begin{bmatrix} 0 & \frac{-(1-D)}{NL_1} & 0 & \frac{-(1-D)}{NL_1} \\ \frac{(1-D)}{NC_{\mathrm{eq}}} & 0 & \frac{-D}{C_{\mathrm{eq}}} & 0 \\ 0 & \frac{D}{L_2} & 0 & \frac{-(1-D)}{L_2} \\ \frac{(1-D)}{NC_{\mathrm{o}}} & 0 & \frac{(1-D)}{C_{\mathrm{o}}} & \frac{-1}{RC_o} \end{bmatrix} \tag{30}$$

$$B_{\mathrm{dc}} = \begin{bmatrix} \frac{1}{L_1} & \frac{(V_{\mathrm{Ceq}}+V_{\mathrm{Co}})}{NL_1} \\ 0 & \frac{-(I_{L1}+NI_{L2})}{NC_{\mathrm{eq}}} \\ 0 & \frac{(V_{\mathrm{Ceq}}+V_{\mathrm{Co}})}{L_2} \\ 0 & \frac{-(I_{L1}+NI_{L2})}{NC_{\mathrm{o}}} \end{bmatrix} \tag{31}$$

$$C_{\mathrm{dc}} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \tag{32}$$

Finally, the line-to-output and line-to-control transfer functions are derived:

$$G_{v_{\mathrm{in}}}(s) = \left.\frac{\widetilde{v}_{\mathrm{o}}(s)}{\widetilde{v}_{\mathrm{in}}(s)}\right|_{\widetilde{d}(s)=0} = C_{\mathrm{dc}}(sI - A_{\mathrm{dc}})^{-1}B_{\mathrm{dc}} \tag{33}$$

$$G_d(s) = \frac{\widetilde{v}_{\mathrm{in}}(s)}{\widetilde{d}(s)} = C_{\mathrm{dc}}(sI - A_{\mathrm{dc}})^{-1}B_{\mathrm{dc}} \tag{34}$$

The transfer function G_d is derived by neglecting input voltage disturbance and will later be used in the control loop of the input voltage v_{in} (the battery voltage).

6. Controller Design

6.1. DC/AC Operation (from PV Modules/Batteries to the AC Grid)

Figure 8 demonstrates the SM control design when the proposed MMC topology operates as a DC/AC converter, and the power flows from the PV modules to the AC grid. The active power P, in this case, is determined by the maximum available power from the PV modules. For simplicity, it is assumed that all the PV modules operate under the same weather conditions (irradiance, temperature, partial shading, etc.). The reference input (PV)

voltage v_{in}* is computed from the MPPT controller. Then, a simple hysteresis-based sliding mode controller controls the actual input voltage v_{in} [30]. A proportional-resonant (PR) controller tuned at the grid frequency $\omega_o = 2\pi f$ is utilized to control the output voltage v_o.

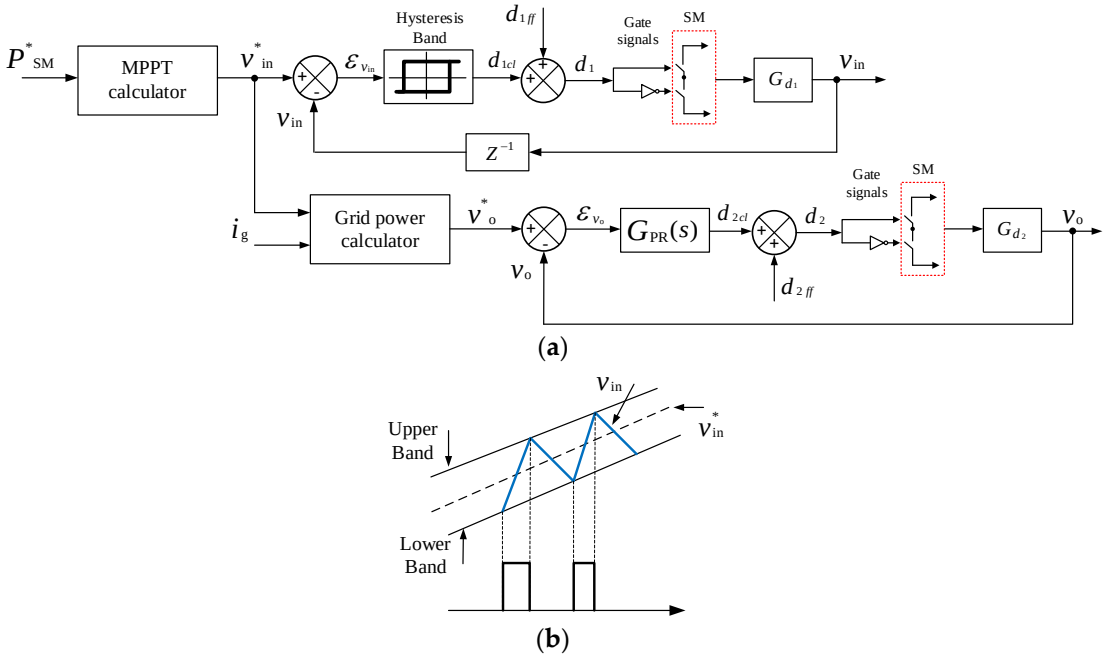


Figure 8. SM controller during DC/AC conversion from PV modules to the AC grid: (**a**) block diagram. (**b**) Hysteresis band (d_{cl}: closed-loop control duty-cycle ratio; d_{ff}: feedforward duty-cycle ratio).

Figure 9 depicts the SM control design when the proposed MMC topology operates as an inverter, and the power flows from the battery packs to the AC grid. Again, hysteresis and PR controllers control the input and output voltages, respectively. Compared to the previous case with PV modules as the input power supply, the active power is determined by the optimal discharge current from the batteries to maximize their effective lifetime and capacity. In addition, the batteries' discharging currents are flexible as there is no maximum power point to operate at. Instead, the reference current is chosen based upon the nominal values recommended by the manufacturer to maximize their lifetime. However, the control scheme after the MPPT or the battery voltage calculator will remain unchanged.

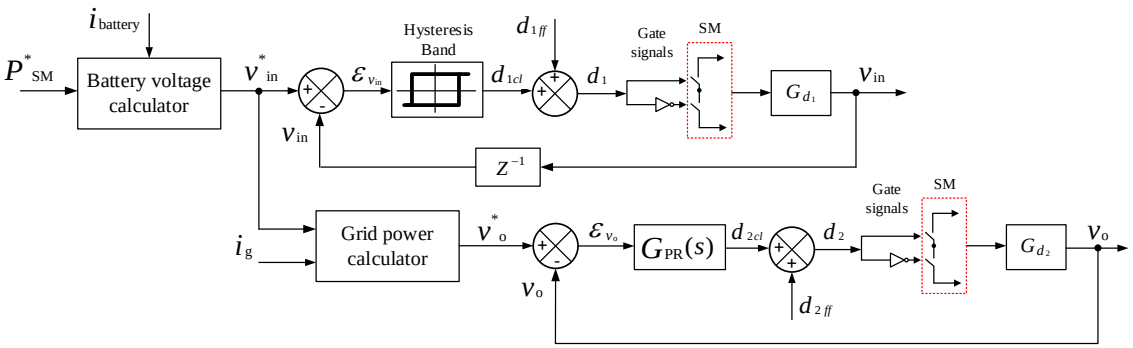


Figure 9. SM controller during DC/AC conversion from batteries to the AC grid (d_{c1}: closed-loop control duty-cycle ratio; d_{ff}: feedforward duty-cycle ratio).

As discussed in Section 4.1, the additional subinterval in DC/AC operation modes (from PV modules/batteries to the AC grid) provides an extra degree of freedom to control input and output sides together. In other words, the second-order harmonic component is

trapped; hence, the input current will be kept constant while generating sinusoidal output voltages and currents.

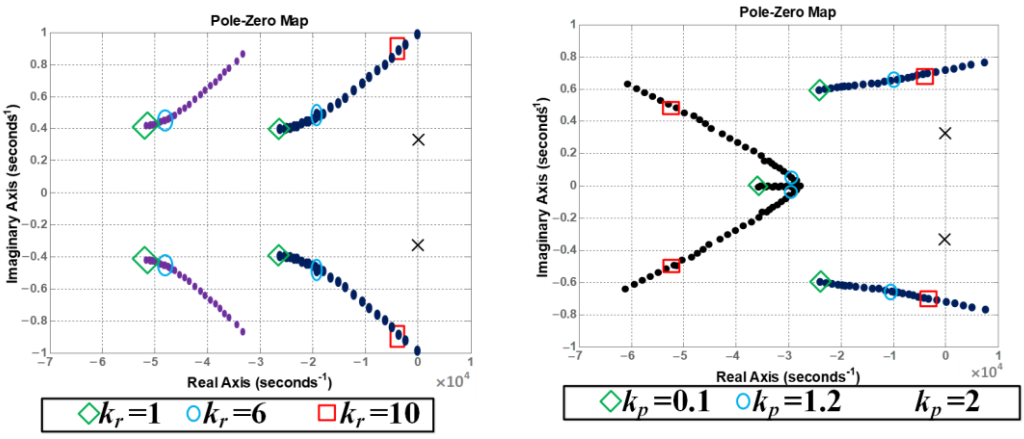
For the output side control, the feed-forward duty-cycle ratio d_{2ff} will generate the output voltage v_o depending on the measured grid voltage and the required output power. The closed-loop PR controller will fix the error in calculation due to the parasitic resistances of the passive elements, semiconductor switches, or any other mismatches by adding the closed-loop duty-cycle ratio d_2. The PR controller is tuned at the grid frequency $\omega_o = 2\pi f_o$ as:

$$G_{PR}(s) = k_p + \frac{k_r s}{s^2 + {\omega_o}^2} \tag{35}$$

To ease the selection of the proportional gain k_p and the resonant gain k_r, an average value of d_2 is selected at $\frac{1}{2}$ in G_{d2} with the transfer function values listed in Table 1. The SISOTOOL interactive toolbox in MATLAB/SIMULINK® is used to select reasonable values for the controller gains by plotting the root loci of the closed-loop system in two different ways. Firstly, the proportional gain k_p is kept constant at 1, and the resonant gain k_r is increased in the range of [1:10]. Secondly, k_r is kept constant at 1 while k_p is changed from [0.1:2]. The resultant root loci are shown in Figure 10. The values of the gains are selected in these ranges to keep the system stable, increase the controller's bandwidth, and reduce the overshoot. Reasonable system performance in terms of compromising bandwidth and stability is chosen when $k_p = 1.2$ and $k_r = 6$.

Table 1. Parameters of the SIMULINK/MATLAB model.

Parameters	Value
Number of modules	$n = 80$
SM rated power	$P_{SM} = 4.2$ kW
SM inductors	$L_1 = 0.5$ mH $L_2 = 10$ mH
SM capacitors	$C_1 = C_2 = 10$ µF and $C_o = 1$ µF
SM Switching frequency	$f_s = 50$ kHz
Transformer turns' ratio	$N = 1$
PV module	Grape Solar GS-S-420-KR3 ($P_m = 420$ W, $V_{mp} = 48.73$ V, $I_{mp} = 8.62$)
PV array	10 parallel × 1 series
Battery pack voltage	$V_{bat} = 200$ V
Grid line-to-line voltage	$V_{O(rms)} = 24.5$ kV
Grid impedance	$L_g = 1$ mH, $r_g = 0.5$ Ω
Grid frequency	$f = 50$ Hz



(**a**) (**b**)

Figure 10. Pole-zero maps of the output-loop controller: (**a**) k_p = 1 and k_r = [1:10], and (**b**) k_r = 1 and k_p = [0.1:2].

6.2. DC/DC Operation (from PV Modules to Battery Packs)

Figure 11 shows the SM-level control design when the proposed MMC topology is used to charge the PV batteries. The active power P is determined by the maximum available power from the PV modules, and the reference input voltage v_{in}* is calculated from the MPPT controller. Then, the actual input voltage v_{in} is controlled by a simple hysteresis controller. For simplicity, it is assumed that the PV power will not exceed the rated power of the SMs and the batteries, so the output voltage (battery's voltage) can be left uncontrolled.

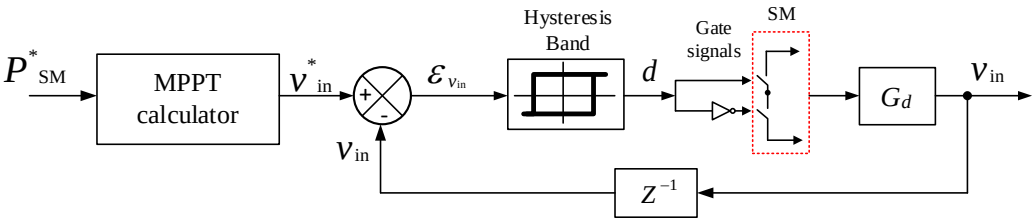


Figure 11. SM controller during DC/DC conversion from PV modules to batteries.

7. Verification

7.1. Simulation Study

The parameters listed in Table 1 are used in MATLAB/Simulink to verify the operation modes of the proposed MMC topology (i.e., DC/AC (from PV modules/batteries to AC grid) and DC/DC (from PV modules to batteries)) in two case studies.

Figure 12 shows the simulation results for the DC/AC operation mode and when the power is transferred from the PV modules to the AC grid. The total output power in Figure 12a increases from zero to the maximum of around 1 MW in 100 ms and then decreases to around 0.6 MW at t = 300 ms because the irradiance dropped to 60% for all PV modules simultaneously at t = 300 ms to simulate the dynamic response. The grid voltage and current are shown in Figure 12b. The output voltage and the input (PV array's) current of the first SMs in the three phases are also plotted together in Figure 12c. Figure 12d shows the input PV current of the first SMs in the three phases where the controller has successfully removed the second-order harmonic components from each PV module.

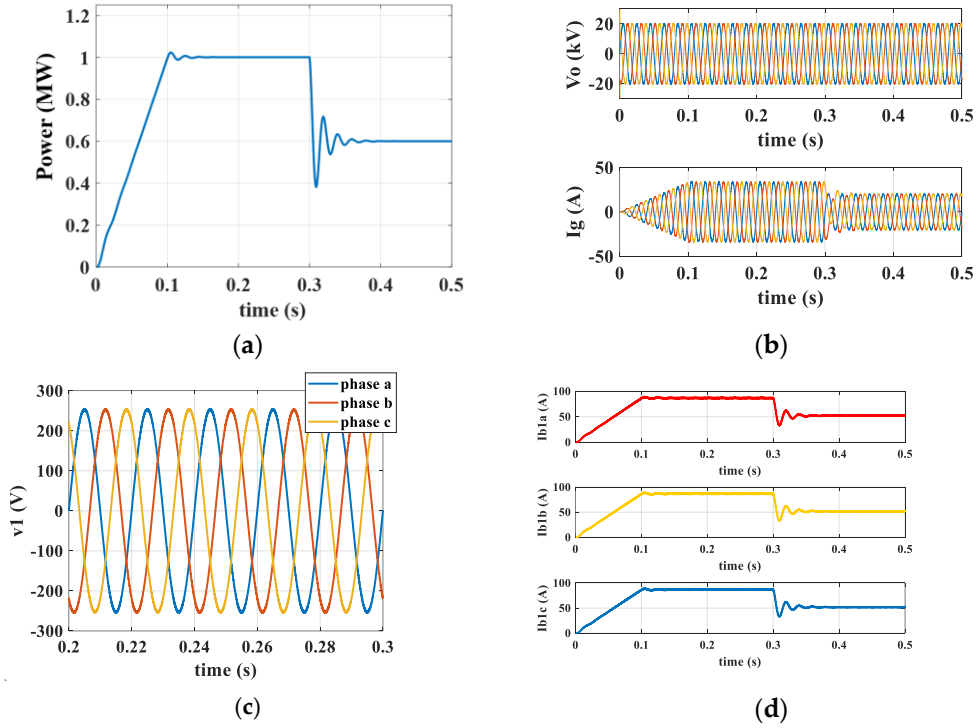


Figure 12. SIMULINK/MATLAB simulations of the proposed MMC for DC/AC conversion: (**a**) total output (grid) power; (**b**) grid voltage and current; (**c**) output voltage of SM1; (**d**) PV arrays current (input current) of SM1.

Figure 13 shows the simulation results to test the operation when the batteries are used to support the grid. As shown in Figure 13a, the power transferred to the grid increases from zero to the maximum of 1 MW in 100 ms. The grid voltage and current are shown in Figure 13b. The output voltage and input (battery's) current of the first SMs in the three phases are plotted in Figure 13c,d, respectively.

Figure 14 shows the simulation results when the SM is controlled to supply the batteries at 200 V by the PV modules at the maximum power of 4.2 kW. To verify the dynamic response of the proposed MMC topology, the output power of the PV modules is dropped to 50% of its maximum at t = 0.3 s. Figure 14a shows the PV module's voltage when it has been increased from 50 V to 60 V as the operational point has been moved from the maximum power point to the right of the current-vs.-voltage curve. Figure 14b shows the PV module's current. Figure 14c shows the battery's charging current, while Figure 14d shows the power flowing from the PV module to the 200 V battery pack.

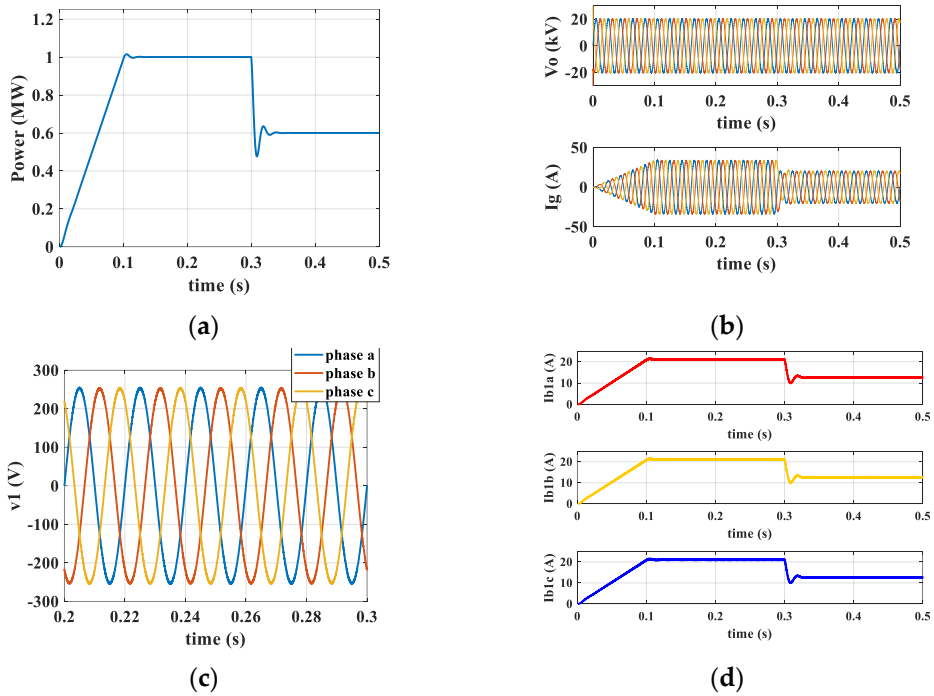


Figure 13. SIMULINK/MATLAB simulations during DC/AC inversion from batteries to the grid: (**a**) total output (grid) power; (**b**) single-phase grid voltage and current (**c**) output voltage of SM_1. (**d**) Battery packs' current of SM_1.

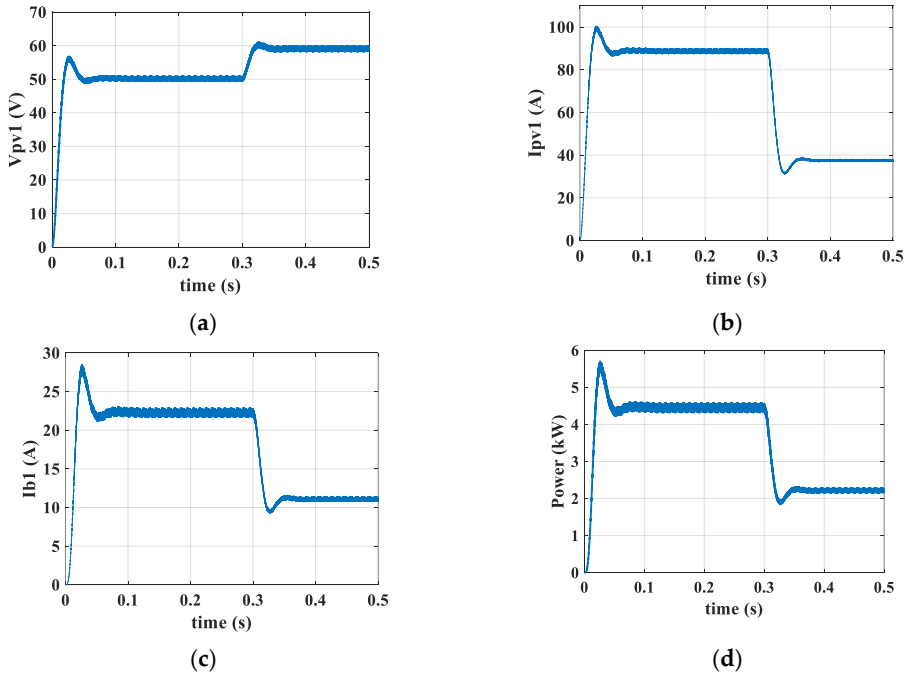


Figure 14. SIMULINK/MATLAB simulations during DC/DC battery charging. (**a**) PV arrays voltage of SM1. (**b**) PV arrays current of SM1. (**c**) Battery current. (**d**) Charging power.

7.2. Experimental Study

The experimental setup for the three-phase implementation of the proposed MMC with 12 SMs and the block diagram of the connection of the SMs are shown in Figures 15 and 16, respectively. Each SM is rated at 750 W, and hence the maximum available power from the whole system is rated at 9 kW. The parameters listed in Table 2 are used for the experiments, and a digital signal processor (DSP-TMS320f28335) is used to control the MMC. DC power

supplies have been employed to mimic the PV modules. In addition, the system's output is connected to the local grid, and its rated power (approximately 9 kW) is converted to the LV AC grid to verify the operation of the three-phase topology.

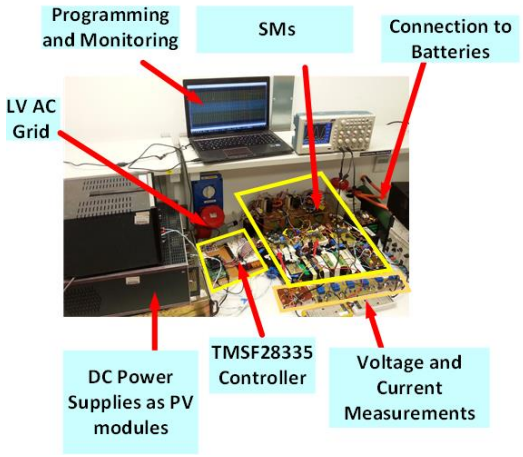


Figure 15. Experimental setup of the proposed MMC with 12 SMs.

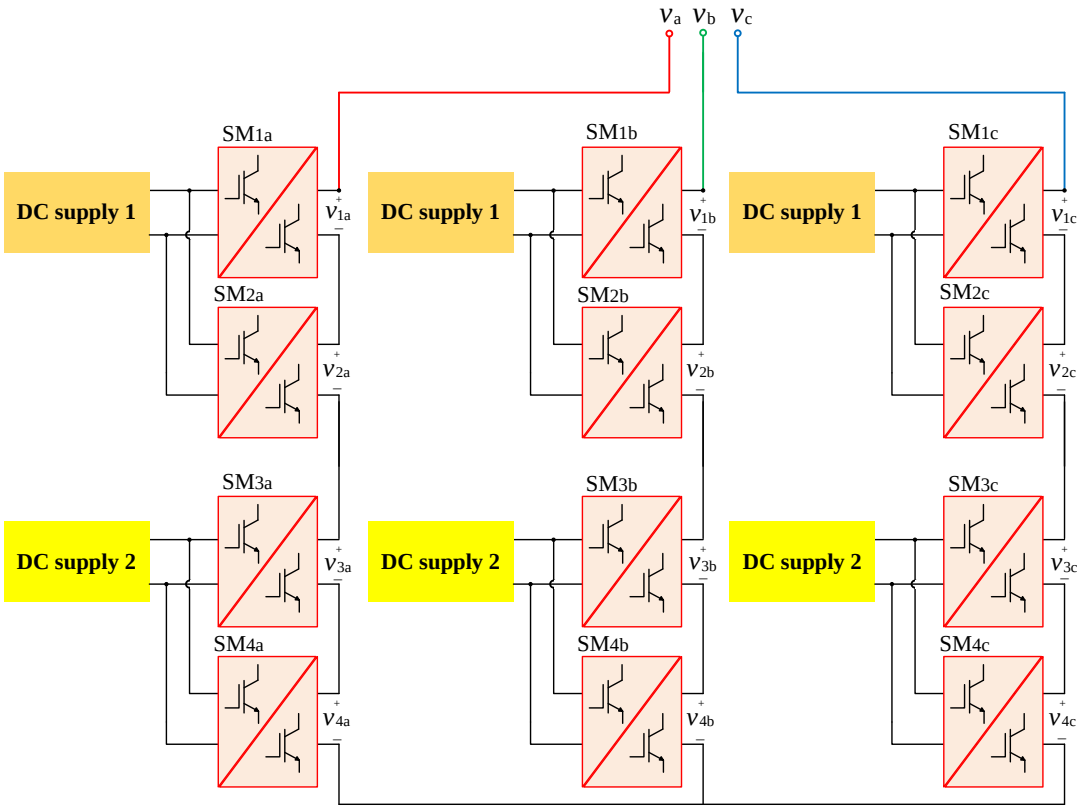


Figure 16. The block diagram of the connection of the SMs in experiments.

The battery pack is shown in Figure 17. Each SM is connected to a battery segment consisting of eight series lithium-ion battery cells rated at nearly 30 V. An EMUS battery management system (BMS) continuously monitors each cell's voltage, temperature, and current through a dedicated cell module circuit that controls the battery packs to ensure safety requirements. The required data, including voltage, current, and temperature measurements of the battery segments, is sent to the central controller using a controller area network (CAN) communication bus.

Table 2. Parameters of the experimental setup.

Parameters	Value
Number of modules	$n = 4$
SM rated power	$P_{SM} = 750\ W$
SM inductors	$L_1 = 1$ mH $L_2 = 10$ mH
SM capacitors	$C_1 = C_2 = 10$ µF and $C_o = 1$ µF
SM switching frequency	$f_s = 20$ kHz
Transformer turns' ratio	$N = 1$
DC supplies	Keysight N8761A Sorensen SGI 100/150
Battery pack voltage	$V_{bat} = 200$ V
Grid phase voltage	230 VAC
Grid impedance	$L_g = 1$ mH, $r_g = 0.5\ \Omega$
Grid frequency	$f = 50$ Hz
Battery pack voltage	$V_{bat} = 200$ V
Grid phase voltage	230 VAC

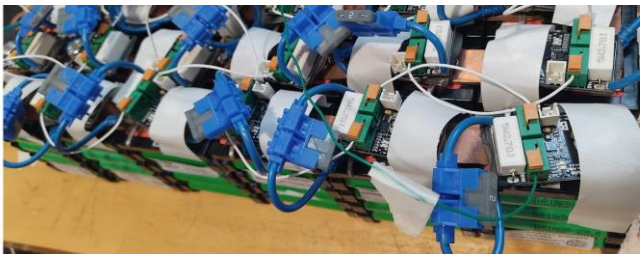


Figure 17. Battery segments consisting of 8 series lithium-ion battery cells together with a CAN communication bus.

Figure 18 shows how the 12 outputs of the SMs are synchronized and connected to the electricity grid. The proposed MMC is connected to the grid through an autotransformer to increase the output voltage gradually. The voltage at the point of common coupling (PCC) with the autotransformer is measured by the voltage sensing boards, and the values are sent to the DSP via the analog-to-digital (ADC). At the start, the DSP controls the switches of the MMC to generate the same voltage as the PCC, so the current is always zero, and no power flows into the electricity grid. The auto-transformer dial increases the voltage manually until the full voltage is reached. Then, the circuit breaker (CB) is closed, and the system is connected to the grid completely.

The module-level control shown in Figure 19 is applied in experiments since there might be small mismatches between the SMs, or they might even be supplied from different power supplies. The central controller generates the same duty-cycle ratios for all SMs.

The SM controller shown in Figure 20, on the other hand, will generate the small-signal duty-cycle ratios for the SMs depending on their power share. Because all SMs in each phase share the same output current, the output voltages of the kth SM (i.e., v_{ok}) will depend on the ratio of the power generated by this SM (i.e., p_k) with respect to the total generated by the full system (i.e., P):

$$v_{ok} = \frac{p_k}{P} v_o \tag{36}$$

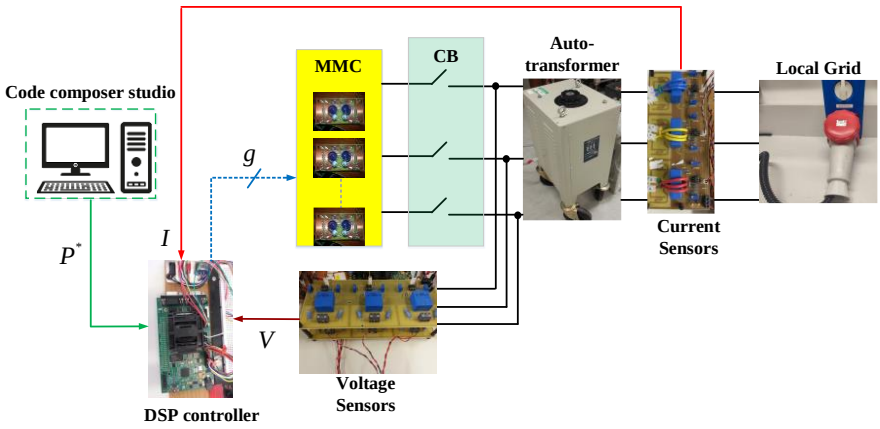


Figure 18. Grid-connection steps.

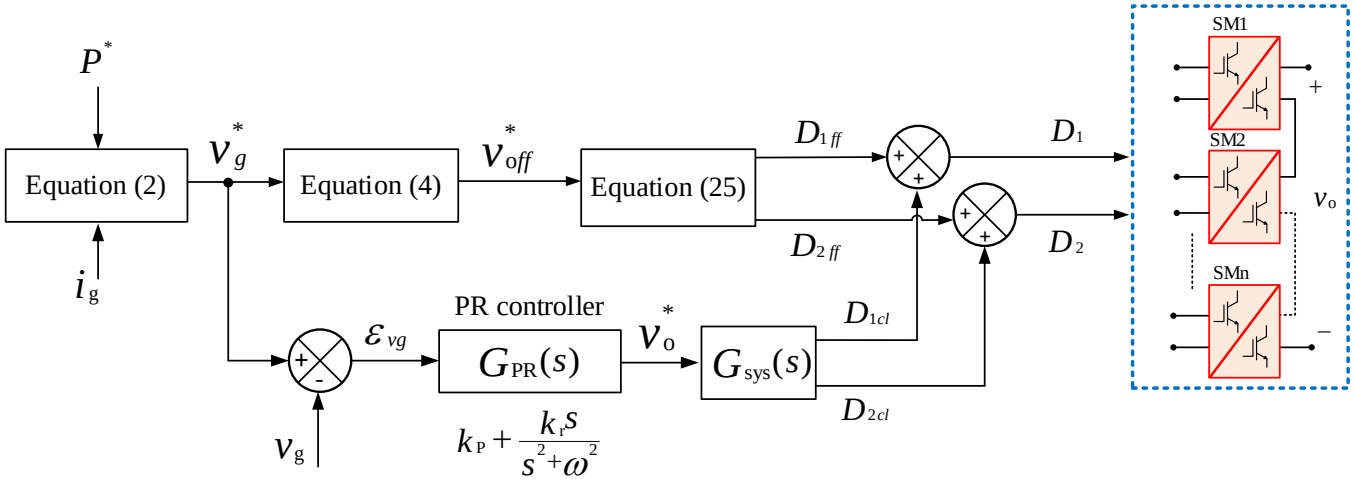


Figure 19. Central controller in the experiments (per phase).

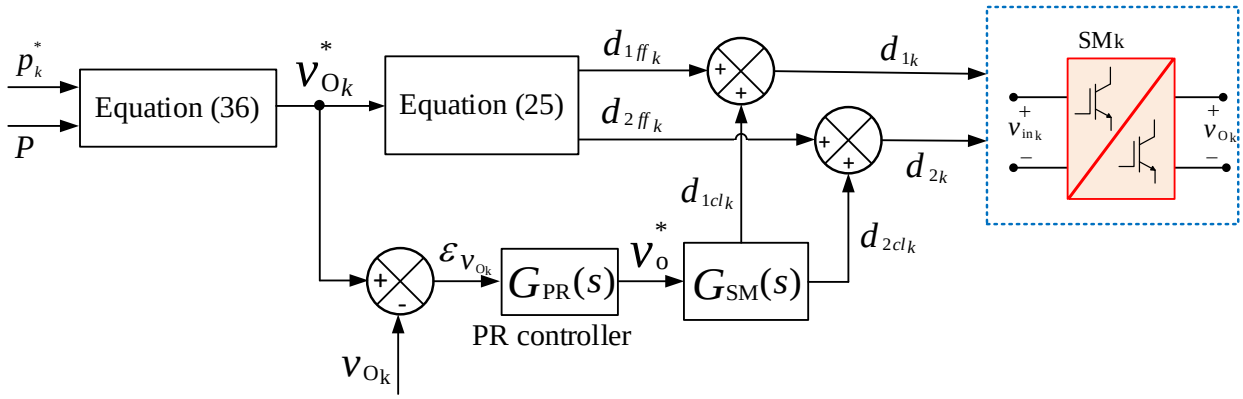
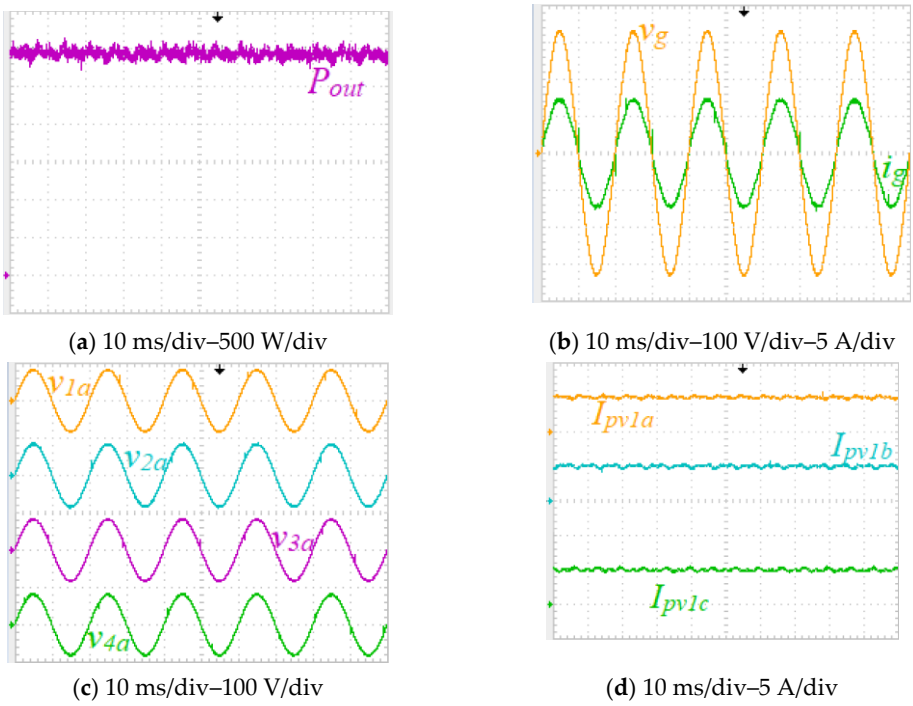


Figure 20. SM's control system in the experiments.

Experimental results during DC/AC operation are displayed in Figure 21, where the measured total output (grid) power of the MMC and the single-phase grid voltage and current are shown in Figure 21a,b, respectively. Further, the output voltages of the first four SMs in phase "a" are shown in Figure 21c. The input currents of the first SMs in the three phases are demonstrated in Figure 21d. The experimental results, in this case, are conducted to validate part of the computer simulations carried out in Figure 13.

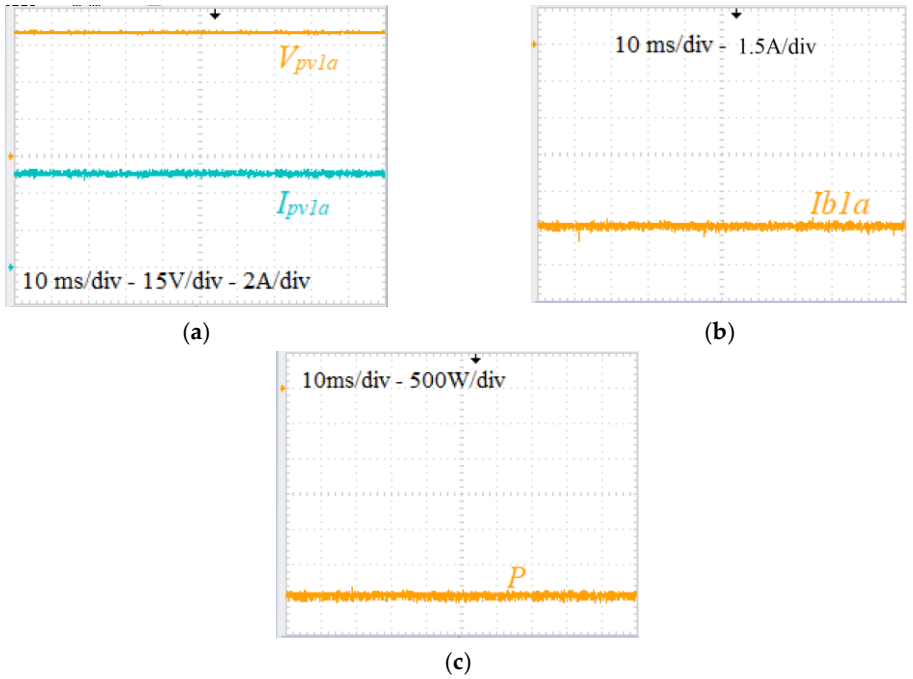


(**a**) 10 ms/div–500 W/div (**b**) 10 ms/div–100 V/div–5 A/div

(**c**) 10 ms/div–100 V/div (**d**) 10 ms/div–5 A/div

Figure 21. Experimental results during DC/AC inversion from DC sources to the grid. (**a**) Total output (grid) power; (**b**) single-phase grid voltage and current; (**c**) output voltage of the first four SMs; (**d**) first SM's input current (PV current).

To show the DC/DC operation mode of the SMs when the system is used to charge the battery segments through the DC voltage sources (as PV modules), the charging test has been carried out, and the results are shown in Figure 22. The input voltage and current of the first SM are depicted in Figure 22a. Further, the output current (of the first SM) charging the battery segment and the charging power are shown in Figure 22b,c, respectively.

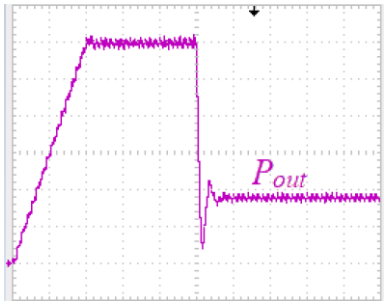


(**a**) (**b**)

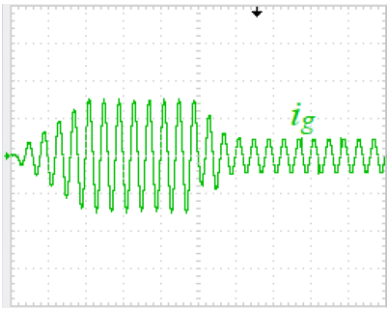
(**c**)

Figure 22. Experimental results during DC/DC operation mode from DC sources to the grid. (**a**) PV voltage and current of the first SM; (**b**) SM1′s (battery's) output current; (**c**) charging power.

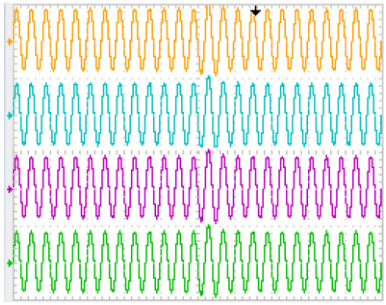
To evaluate the stability of the proposed system, the output power P_{out} is first increased to 3 kW in 100 ms, then after 150 ms, it is suddenly dropped by almost 75% (to roughly 750 W). As shown in Figure 23b, the grid current i_g is tracking the variations in the output power P_{out}, decreasing to 25% of its maximum value after 250 ms. The same is observed for the three-phase input currents of the first SM (PV currents), whilst the output voltages of the first four SMs (v_{1a}, v_{2a}, v_{3a}, and v_{4a}) remain constant.



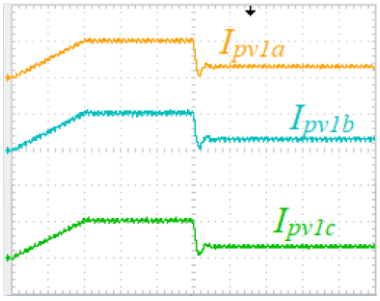
(**a**) 50 ms/div–500 W/div



(**b**) 50 ms/div–5 A/div



(**c**) 50 ms/div–100 V/div



(**d**) 50 ms/div–5 A/div

Figure 23. Experimental results during sudden 75% drop in power. (**a**) Total output (grid) power; (**b**) single-phase grid voltage and current; (**c**) output voltage of the first four SMs; (**d**) first SM's input current (PV current).

8. Conclusions

This paper proposes a new MMC topology for PV/EV/grid integration in which isolated single-stage SEPIC-based converters are used as the SMs. The SMs can operate in DC/DC mode (the PV modules charge the batteries) and DC/AC mode (the power is fed into the AC grid by PV modules or batteries). Therefore, there is no need to add an extra DC/DC or DC/AC converter. The main benefits delivered by the isolated SEPIC-based SMs are low input ripple current, high power factor, and non-inverted flexible output voltage (higher/lower than the input voltage). High efficiency at high input voltages is the other excellent benefit of an SEPIC-based SM. They need very small input capacitances at the input side so the PV modules can operate efficiently at the maximum power point. State-space modelling of the proposed MMC topology is presented to obtain the SMs transfer functions and design the control schemes. The proper controller for each mode of operation is designed and applied to supply constant current from either the PV modules or the battery cells and ensure that the second-order harmonic current components that appear in the input voltage and current are eliminated so the PV modules and/or the battery cells can operate efficiently. Simulations using MATLAB/Simulink and experimental results using a scaled-down prototype validate the performance of the proposed MMC topology and show the feasibility of the selected control designs.

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