A Boost PFC Converter with Programmable Harmonic Resistance

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***Abstract*— Power factor correction converters with low harmonic input resistance are desirable loads to support the reduction of the harmonic distortion on the feeding grid. Therefore, a novel control strategy is proposed. Whereas previously proposed controllers tried to obtain a resistive behavior of the converter with a constant input impedance for all frequencies, including the fundamental, the proposed control strategy allows to set a harmonic input resistance independent of the fundamental input impedance. Consequently, the harmonic input resistance remains low, even when the input power of the converter is decreased. This paper describes the operation of a digitally controlled boost PFC converter with the new control algorithm. Experimental tests on a 1 kW prototype show that a practical realization of the algorithm is possible and that a programmable harmonic input resistance of the converter is obtained.**

I. Introduction

In order to comply with the international standards for electromagnetic compatibility, capacitive diode bridge rectifiers are often replaced by power factor correction (PFC) converters. These PFC converters provide a constant output voltage while their input current waveform is shaped to comply with the standards. Several approaches are in use nowadays, depending on the application type, the cost of implementation and the required input power. For low power applications, several converter types, such as fly-back, Ćuk, SEPIC, boost, ..., operating in the discontinuous conduction mode are employed [1]–[3]. After all, these converters behave more or less resistive at their input when operated in the discontinuous conduction mode (DCM). Consequently, only one control loop is required for these PFC converters. Though the power factor of such converters is not unity their input current waveshape meets the standards in most cases.

For applications requiring a higher input power, device stresses and problems with conducted emission limit the use of these DCM converters. Therefore, PFC converters operated in the continuous conduction mode (CCM) are employed [4]–[8]. In these applications, an input current controller is applied in order to obtain either a sinusoidal line current, independent of the line voltage distortion, or a resistive line current behavior. Though both approaches guarantee a high power factor at the input of the converter, a converter with resistive input will contribute to the damping of harmonic oscillations of the feeding grid.

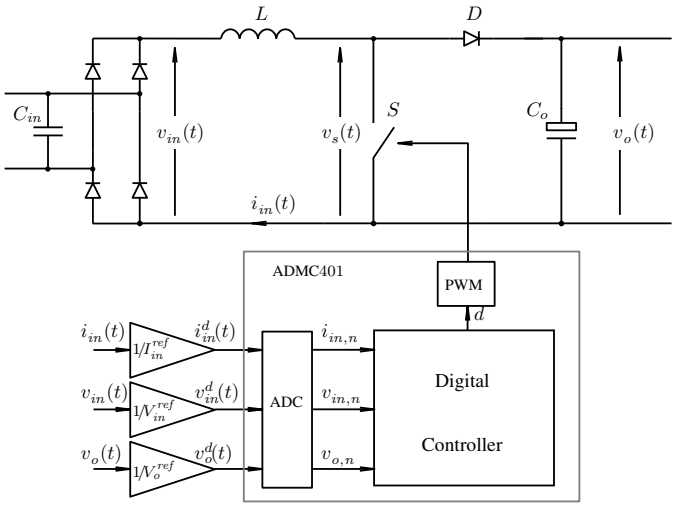

Fig. 1. A typical boost PFC converter with digital controller

Recently, some papers have appeared in the field of power quality in which it was proven that such resistive behavior for harmonics is preferable [9]–[11]. In these papers, a shunt harmonic impedance (SHI) is proposed as a central damper for grid oscillations. Moreover, it is possible to attenuate grid resonances by implementing the resistive input behavior as a secondary function [12] on all converters which are connected to the grid. Nevertheless, for recently proposed converters with resistive input, this input impedance is equal for both the fundamental component and the harmonics. As a result, the harmonic input impedance of these converters changes with the input power of the converter, which is determined by the fundamental input impedance. Hence, the damping of grid resonances will vary over time as the input power of most converters is time dependent. Therefore, a new control strategy for a boost PFC converter has been developed in order to have a programmable resistive input impedance for harmonics, independent of the input impedance of the fundamental. As a result, the converter will keep its potential to damp grid oscillations, even for a low input power of the converter. The algorithm is based upon duty-ratio feedforward, a control strategy previously employed to obtain a resistive input behavior for a boost PFC converter [8].

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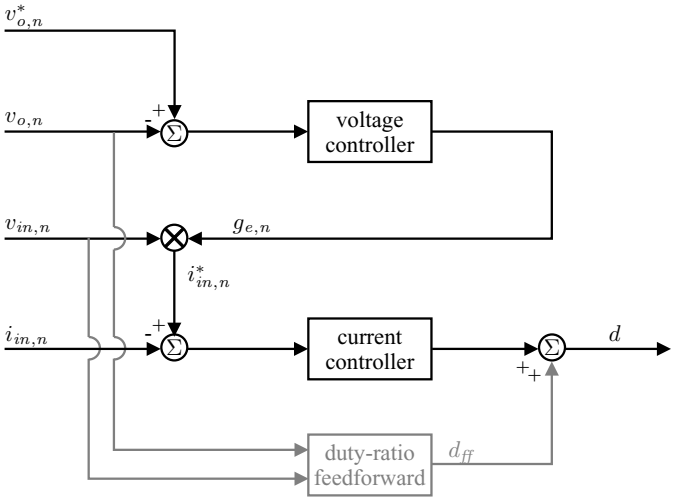

Fig. 2. Black: a typical two-loop control scheme for a boost PFC converter, gray: duty-ratio feedforward

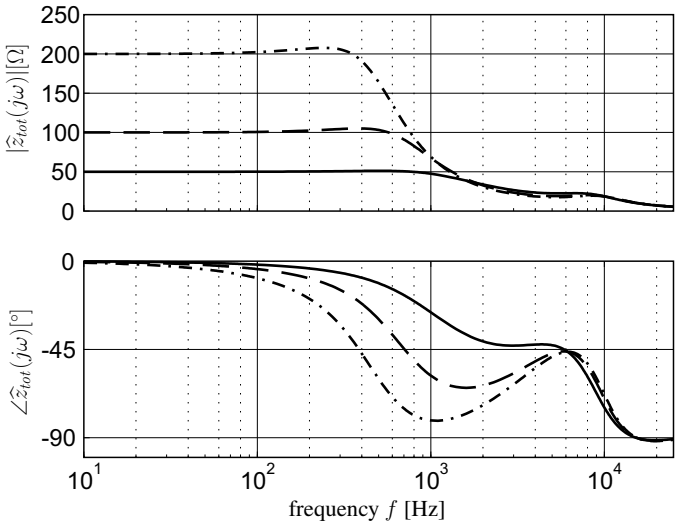

Fig. 3. Small-signal input impedance of a boost PFC converter with duty-ratio feedforward

II. Digital Control of Boost PFC Converters

The topology of a boost power factor correction (PFC) converter is depicted in Fig. 1. The converter consists of an input filter, a diode bridge and a boost dc-dc converter containing a switch S, a diode D, an input inductor L, and an output capacitor C. In order to digitally control both the input impedance and the output voltage, the inductor current $i_{in}(t)$, the input voltage $v_{in}(t)$, and the output voltage $v_o(t)$ must be sensed, scaled, and sampled. This way, these control variables are converted into their dimensionless digital samples $i_{in,n}$, $v_{in,n}$, and $v_{o,n}$, respectively. This conversion can be described as a division by a reference value (I_{in}^{ref}, V_{in}^{ref}, V_o^{ref}), followed by a sampling process [8].

A typical controller for a boost PFC converter consists of two control loops, Fig. 2 (black lines): an input current control loop, which is usually a fast loop, and an output voltage control loop, which is much slower than the current loop. The output voltage controller balances the input and the output powers of the converter to obtain a constant output capacitor voltage by changing the desired (dimensionless) input conductance $g_{e,n}$ of the converter. The product of this input conductance and the input voltage of the converter yields the desired input current $i^*_{in,n}$ of the converter. The input current controller commands the PWM-unit which controls the switch S. In many cases both controllers are implemented as PI-controllers.

In [8] a new control strategy for the current control loop was proposed to improve the resistive behavior of the converter. The control scheme is shown in Fig. 2 (gray lines). The ideal steady-state duty-ratio is calculated using the sampled values of the input and the output voltage

$$d_{ff} = 1 - \frac{v_{in}}{v_o} = 1 - \frac{v_{in,n} V_{in}^{ref}}{v_{o,n} V_o^{ref}}. \qquad (1)$$

This steady-state duty-ratio d_{ff} is added to the output of the input current controller. As a result, the input current tracking is improved and the frequency range for which the converter behaves resistively is extended to higher frequencies.

In order to quantify the improvements, the small-signal input impedance of a boost PFC converter with duty-ratio feedforward was calculated in [8]. The resulting input impedance of the converter for different values of the desired input impedance are displayed in Fig. 3. This figure shows that the converter with feedforward has a resistive harmonic impedance of

$$Z_{in,h} = \frac{1}{g_e} = \frac{Z_{in}^{ref}}{g_{e,n}}, \quad \text{with} \quad Z_{in}^{ref} = \frac{V_{in}^{ref}}{I_{in}^{ref}}, \qquad (2)$$

for a frequency range dependent on the programmed value of the input conductance g_e. Hence, a resistive impedance can be achieved with this algorithm for frequencies up to 1 kHz. For higher frequencies, the converter will behave as a parallel connection of a resistor and a capacitor, due to the capacitance of the EMI-filter.

However, the input conductance g_h for harmonics always remains equal to the input conductance g_1 of the fundamental ($g_h = g_1 = g_e$) when this control strategy is applied. Consequently, the input conductance of the harmonics decreases for lower power levels, together with the damping potential of the converter. Moreover, for lower values of the desired input conductance, the influence of the input capacitance of the converter will gain significance (dashed and dash-dotted curves in Fig. 3) and the frequency range for which the resistive behavior is obtained becomes limited to the low-order harmonics ($<$ 300 Hz for $g_e < \frac{1}{200\Omega}$).

III. Control Strategy for a Programmable Harmonic Resistance

A. General Operation of the Control Strategy

Since the most desirable behavior is achieved with high values of the input conductance (Fig. 3), a converter with a pronounced damping of harmonic resonances should have a

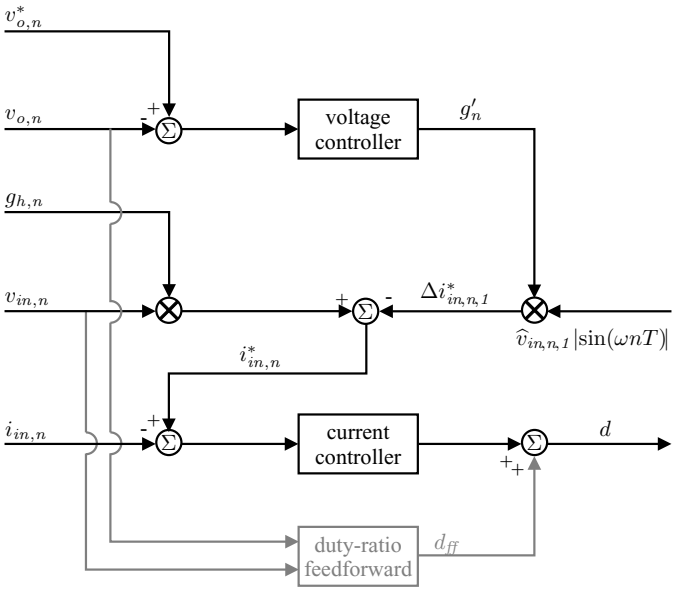

Fig. 4. Control strategy for a programmable harmonic input conductance

high, constant harmonic input conductance g_h for the entire power range. Therefore, the output voltage controller should only change the input conductance g_1 of the fundamental to balance the input and output power, and leave the harmonic input conductance g_h unaffected. Such a control strategy is depicted in Fig. 4. The input conductance for harmonics is now an external input and can be programmed to be a constant. In order to change only the input conductance of the fundamental, the output of the output voltage controller g' is multiplied with the fundamental component of the line voltage. The result is used to adjust the desired value of the input current $i^*_{in,n}$. The input conductance of the fundamental can now be calculated as $g_1 = g_h - g'$. Hence, the input conductance of the fundamental can be changed independently of the input conductance for the harmonics.

As the boost PFC converter is only capable of transferring energy from the mains to the load, the range of input conductances must be positive. Moreover, when $g_{1,n}$ and $g_{h,n}$, defined as

$$g_{1,n} = g_1 Z^{ref}_{in}, \quad g_{h,n} = g_h Z^{ref}_{in}, \tag{3}$$

are dimensionless digital quantities, they are restricted to values less than 1. Consequently, the input conductances g_1 and g_h are limited to

$$0 < g_1 < \frac{1}{Z^{ref}_{in}}, \quad 0 < g_h < \frac{1}{Z^{ref}_{in}}. \tag{4}$$

Therefore, the highest harmonic input conductance g_h which can be achieved and which also corresponds to the best damping of grid resonances, is $(Z^{ref}_{in})^{-1}$. When g_h is set to zero, a sinusoidal line current is obtained, independently of the input power of the converter, which is determined by g_1.

B. The Phase-Locked Loop

In order to obtain the required fundamental component of the line voltage, a phase-locked loop (PLL) is employed. The block diagram of this loop is displayed in Fig. 5. The method to obtain the fundamental component of the input signal uses very common components such as a lowpass filter and a PI-controller. Nevertheless, as input of the PLL, the line voltage is reconstructed by inverting the input voltage (at the dc-side of the diode bridge) during half of each line period. This way, an alternating signal is obtained as input of the PLL without the need to measure the line voltage at the ac-side of the diode bridge. In the ideal case, the input voltage should be inverted each time the line voltage reaches zero to obtain the line voltage. However, since in real converters the input voltage does not reach zero, the detection of these zeros is very hard to accomplish. Therefore, the waveform is inverted when a predefined threshold voltage v_{th} is crossed. Though this introduces some distortion in the input waveform of the PLL, the sinusoidal waveform obtained at the output of the PLL will be nearly in phase with the fundamental component of the line voltage. The phase error can be easily calculated for a sinusoidal line voltage $\widehat{v}_{in}\sin(\omega t)$. The input of the PLL $v_{PLL,in}$ can be expressed as

$$\begin{cases} v_{PLL,in} = \widehat{v}_{in}\sin(\omega t) & \omega t \in [0, \pi - \theta_x] \cup [\pi, 2\pi - \theta_x] \\ v_{PLL,in} = -\widehat{v}_{in}\sin(\omega t) & \omega t \in [\pi - \theta_x, \pi] \cup [2\pi - \theta_x, 2\pi] \end{cases} \tag{5}$$

where θ_x is the phase shift between the effective switching point and the ideal switching point, the zero of the line voltage (Fig. 5). The fundamental component of this waveform can be obtained with a fourier analysis, yielding

$$\begin{cases} v_{PLL,in,1} = A_1 \sin(\omega t) + B_1 \cos \omega t \\ A_1 = \widehat{v}_{in}\left\{1 - \dfrac{2\theta_x}{\pi} + \dfrac{\sin(2\theta_x)}{\pi}\right\} \\ B_1 = \widehat{v}_{in}\left\{\dfrac{1}{\pi} - \dfrac{\cos(2\theta_x)}{\pi}\right\} \end{cases} \tag{6}$$

For small values of θ_x, where $\sin(2\theta_x) \approx 2\theta_x$ and $\cos(2\theta_x) \approx 1$, the above equations simplify to $A_1 = \widehat{v}_{in}$ and $B_1 = 0$, so the fundamental component of $v_{PLL,in}$ will be equal to the line voltage $\widehat{v}_{in}\sin(\omega t)$. If the angle θ_x becomes significant, the phase shift ψ between the fundamental component of the line voltage and the output of the phase-locked loop becomes visible. It can be estimated with

$$\tan\psi = \frac{B_1}{A_1}. \tag{7}$$

When the amplitude of the fundamental component of the line voltage is e.g. $\sqrt{2} \cdot 230\ V$, the implementation of a detection level of 50 V results in an error θ_x =8.8° in the detection of the zero of the line voltage. Evaluation of (7) learns that in this case the phase shift between the fundamental component of the line voltage and the fundamental component of the input of the PLL is less than 1°. This means that a safe threshold voltage can be chosen which guarantees a low

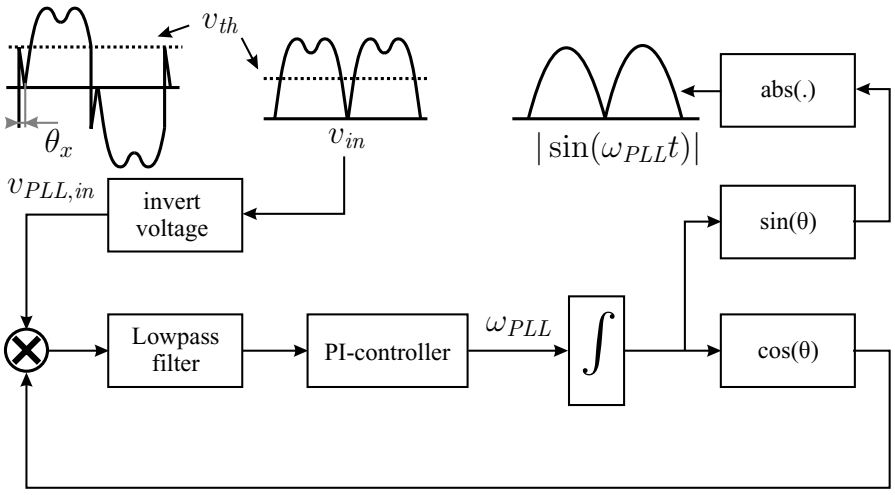

Fig. 5. The block diagram of the phase-locked loop

phase shift ψ and ensures good detection of the zero of the line voltage. As a result, if the parameters of the lowpass filter and the PI-controller of the PLL are tuned well, the estimated waveform of the PLL will be very close to the fundamental of the line voltage. The presence of significant harmonics on the line voltage may lead to some extra phase shift. Moreover, measures must be taken to prevent multiple inversions of the input voltage, since harmonics can cause multiple crossings of the threshold. A simple solution is to disable the detection as long as the input voltage remains lower than another (higher) threshold. When such measures are taken and no multiple inversions occur, this algorithm is hardly disturbed by harmonics. When the harmonic content of the voltage is low, other PLL-strategies are possible, such as the method proposed in [13].

C. Operation in the Discontinuous Conduction Mode

The objective of the proposed control strategy is to obtain a resistive behavior of the converter for harmonics, independent of the input power of the converter. Nevertheless, when the input power of the converter is decreased, this converter may start to operate in the mixed conduction mode (MCM, combination of DCM near the zero-crossings and CCM in the remainder of the line period), while the duty-feedforward algorithm of section II was only intended for operation in CCM. As a result, the extension of this digital control algorithm for operation in MCM must be used [7]. This extension includes the correction of the input current samples by a factor κ, given by

$$\kappa(t) = \frac{dv_o(t)}{v_o(t) - v_{in}(t)}. \tag{8}$$

With this extension, the line current distortion can be significantly reduced. Nevertheless, some distortion will exist, due to the changing dynamics of the converter in the discontinuous conduction mode.

When the input power of the converter is low, another problem yielding line current distortion may arise. The amplitude of the fundamental component of the reference current is low, while the harmonic components (which are independent of the input power) are large, leading to negative values of the input current reference. However, due to the diode bridge at the input of the converter, the inductor current cannot become negative and it will be clamped to zero during the periods where the desired input current is negative. As a result, the input impedance of the converter for harmonics may display some undesirable variations when the input power of the converter is low and the voltage distortion high.

IV. Experimental results

For the experimental verification of the control algorithm a 1 kW boost power factor correction converter is employed. The converter has an input capacitor of 470 nF, an inductor of 1 mH, and an output capacitor of 470 μF. The switches are MOSFET SPP20N60S5 and diode RURP3060. The converter is supplied from a linear amplifier (PAS1000 of Spitzenberger & Spieß). Under normal operating conditions, the line voltage is 230 V, 50 Hz, while the output voltage is programmed to be 400 V. The reference values of the control variables are

$$\begin{cases} V_{in}^{ref} = 399\ V, \quad V_o^{ref} = 452\ V, \\ I_{in}^{ref} = 10.4\ A, \quad Z_{in}^{ref} = \dfrac{V_{in}^{ref}}{I_{in}^{ref}} = 38.4\ \Omega. \end{cases} \tag{9}$$

The converter is controlled by the ADMC401 digital signal processor of Analog Devices. The sampling of the input current and input voltage is synchronized with the switching of the converter, at 50 kHz, while the sampling of the output voltage is performed at 1 kHz. The key waveforms of the converter at full load and with a sinusoidal line voltage, are shown in Fig. 6.

The locking of the phase-locked loop is shown in Fig. 7. Though the output of the phase-locked loop is generated each switching cycle, the calculations required for the locking of the phase-locked loop are performed only each 0.2 ms, which explains the quantisation that can be observed in the lower

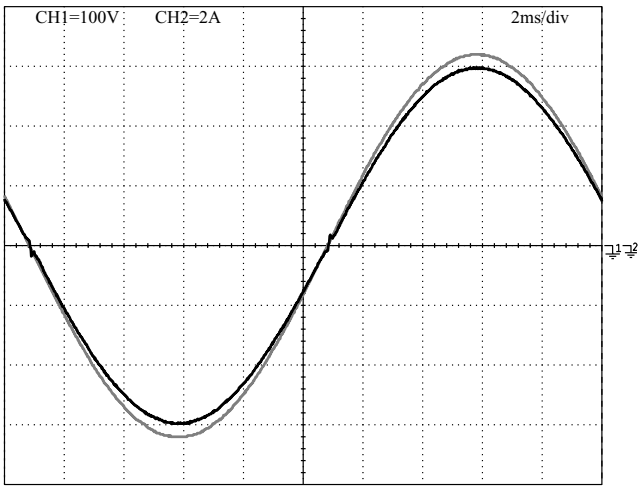

Fig. 6. Line current (black curve) and line voltage (gray curve) of the boost PFC converter at full power, with $g_1 = g_h$ and with sinusoidal line voltage

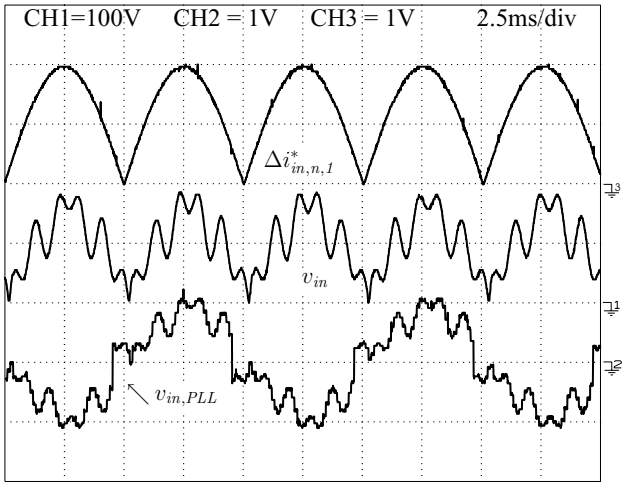

Fig. 7. Upper trace: output of the PLL, center trace, input voltage of the converter, lower trace: flipped input voltage used as input for the PLL

trace of Fig. 7). The input voltage of the converter (at the dc-side of the diode bridge) is displayed in the center trace. For this experiment, a line voltage waveform with huge distortion has been chosen: 10% of 5^{th} and 7^{th} harmonic, and 20% of 11^{th} harmonic, corresponding to a total harmonic distortion of the line voltage of 24.5%. Although the input voltage is not flipped exactly at the point where the line voltage reaches zero (lower trace in Fig. 7), the phase-locked loop is able to follow the line voltage with the correct fundamental frequency and only a very small phase-shift between the PLL-output (upper trace of Fig. 7) and the input voltage (center trace). For input voltage waveforms with a 'normal' distortion, the phase-shift is virtually zero.

In the experimental waveforms of Figs. 8–10, the harmonic input resistance of the converter is set to its minimum (maximum of g_h), which is equal to $Z_{in}^{ref} = 38.4\ \Omega$. In a first experiment, the influence of the new control algorithm on the operation of the converter with sinusoidal line voltage

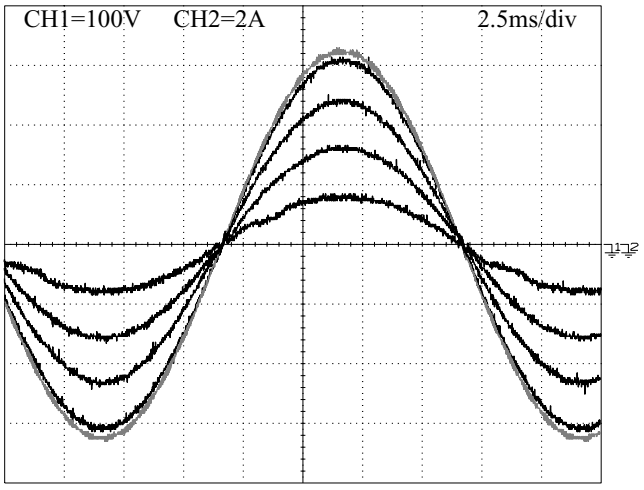

Fig. 8. Line current (black curve) and line voltage (gray curve) of the boost PFC converter at 980 W, 752 W, 508 W and 253 W input power, with $g_1 = g_h$ and with sinusoidal line voltage

TABLE I
EXPERIMENTAL MEASUREMENTS OF THE THD AND THE POWER FACTOR FOR SINUSOIDAL LINE VOLTAGE

P_{in}[W]	THD [%]	power factor
980	1.04	1.000
752	0.96	0.999
508	1.10	0.999
253	4.70	0.998

was evaluated. The results are shown in Fig. 8 and Table I. Both the figure and the table confirm that the line current of the converter shows a very low distortion as long as the converter operates in continuous conduction mode (input power greater than 500 W [7]): the power factor is unity, while the total harmonic distortion of the line current is only 1% in a power range between 500 W and 1000 W. Since for lower input power the converter starts operating partially in the discontinuous conduction mode, the line current shows some distortion. Nevertheless, when sample correction is employed, the THD of the line current is limited to only 4.70% for operation at 253 W.

The new control strategy was also evaluated with a distorted line voltage waveform, supplied by the linear amplifier, and consisting of a fundamental 50 Hz-voltage and different low-order harmonics: 10% of 5^{th} harmonic voltage component, and 5% of 7^{th} and 11^{th} harmonic, corresponding with a total harmonic distortion of the line voltage of 12.25%. This voltage waveform is represented by the gray trace in Figs. 9 and 10. In Fig. 9, the input conductance of both the fundamental and the harmonics are set to their maximum value, corresponding with a theoretical input impedance of 38.4 Ω. Since the input power according to this value exceeds the power rating of both the converter and the power source, this test was performed with reduced line voltage amplitude. The results are displayed in

TABLE II

HARMONIC ANALYSIS OF THE WAVEFORMS OF FIGS. 9 AND 10

P_{in}	1014 W[1]		980 W		746 W		509 W		263 W	
h	$\lvert Z_{in,h}\rvert[\Omega]$	$\angle Z_{in,h}[^\circ]$	$\lvert Z_{in,h}\rvert[\Omega]$	$\angle Z_{in,h}[^\circ]$	$\lvert Z_{in,h}\rvert[\Omega]$	$\angle Z_{in,h}[^\circ]$	$\lvert Z_{in,h}\rvert[\Omega]$	$\angle Z_{in,h}[^\circ]$	$\lvert Z_{in,h}\rvert[\Omega]$	$\angle Z_{in,h}[^\circ]$
1	40.4	0.1	54.9	0	72.8	0	108.3	-0.2	215.4	-1.5
5	40.2	1.1	40.1	1	40.2	1.1	40.5	1	43.0	8.7
7	40.3	0.1	40.1	0.7	39.9	0.7	40.1	0.9	45.3	12.3
11	42.0	1	41.6	1	41.5	0.5	41.7	0.4	60.5	20.7

[1]This experiment was performed at reduced voltage

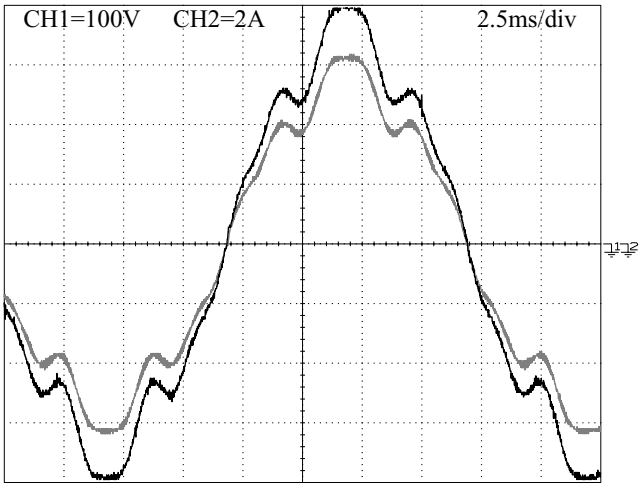

Fig. 9. Line current (black curves) and line voltage (gray curve) for line voltage with 5^{th}, 7^{th} and 11^{th} harmonic distortion, for 1014 W input power (with $g_1 = g_h$at its maximum, and with reduced line voltage amplitude)

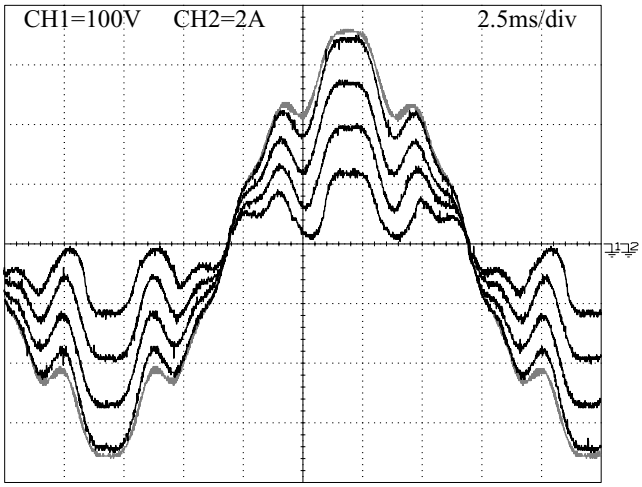

Fig. 10. Line current (black curves) and line voltage (gray curve) for line voltage with 5^{th}, 7^{th} and 11^{th} harmonic distortion, for 980 W, 746 W, 509 W, and 263 W input power

Fig. 9 and the first column of Table II, both showing resistive behavior (very low phase angle $\angle Z_{in,h}$) of the converter with an impedance very close to Z_{in}^{ref}. The other columns of Table II show the input impedance at other power levels (980 W, 746 W, 509 W and 263 W), corresponding with Fig. 10. While the impedance of the fundamental increases with decreasing input power, the magnitude of the harmonic impedance for the 5^{th}, the 7^{th} and the 11^{th} harmonic is constant for a wide power range from 500 W to 1 kW and remains very close to the programmed value. Also the phase angle of the harmonic impedances remain low, confirming the resistive nature of this impedance. The three upper black traces in Fig. 10 show a clearly visible reduction of the fundamental component of the line current, while the amplitude of the harmonic components is maintained.

Even when the converter starts operating in the discontinuous conduction mode, corresponding to the lowest black trace, the waveshape is hardly affected, which shows that the magnitude of the impedance remains more or less at its desired value. Nevertheless, Table II demonstrates that the phase angle increases for the harmonics. The reason for this distortion is clearly visible in the lowest black curve of Fig. 10: the combination of the large harmonic components of the inductor current and the low fundamental component leads to a negative reference value for this inductor current, which is not achievable, due to the diode bridge at the input of the converter.

V. CONCLUSION

Power factor correction converters with low harmonic input resistance are desirable loads to help reducing the harmonic distortion on the feeding grid. Therefore, a novel control strategy was proposed. Whereas previously proposed controllers tried to obtain a resistive behavior of the converter with a constant input impedance for all frequencies, including the fundamental, the proposed control strategy allows to set a harmonic input resistance independent of the fundamental input impedance. Consequently, the harmonic input resistance remains low, even when the input power of the converter is decreased. This paper describes the operation of a digitally controlled boost PFC converter with the new control algorithm. Experimental tests on a 1 kW prototype show that a practical realization of the algorithm is possible and that the harmonic input resistance of the converter can be programmed very accurately in a wide power range of the converter.

VI. Acknowledgements

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