Analyse en ontwerp van een vermogenversterker met hoog uitgangsvermogen voor millimetergolftoepassingen in een SiGe-BiCMOS-technologie

Analysis and Design of a High Power Millimeter-Wave Power Amplifier in a SiGe BiCMOS Technology

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"Begin at the beginning
and go on until you come to the end, then stop."
— Lewis Carroll

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of what, then, is an empty desk a sign?"
— Albert Einstein

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— Heinrich Harrer

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List of Acronyms

A

AC	Alternating Current
ACPR	Adjacent Channel Power Ratio
AM	Amplitude Modulation
APSK	Amplitude Phase Shift Keying

C

CATV	Cable TV
CB	Common Base
CE	Common Emitter
CM	Common Mode
CMOS	Complementary Metal Oxide Semiconductor

D

DAT	Distributed Active-Transformer
DC	Direct Current

DM	Differential Mode

E

EIRP	Equivalent Isotropically Radiated Power
EM	Electromagnetic
ESD	Electrostatic Discharge

F

FoM	Figure of Merit

G

GaAs	Gallium Arsenide
GaN	Gallium Nitride
GCPW	Grounded Coplanar Waveguide
GND	Ground

I

IC	Integrated Circuit
InP	Indium Phospide
ITRS	International Technology Roadmap for Semiconductors

M

MM-wave	Millimeter-wave
MMIC	Monolithic Microwave Integrated Circuit

P

PA	Power Amplifier
PAE	Power Added Efficiency
PGS	Patterned Ground Shield
PM	Phase Modulation
PSK	Phase Shift Keying

Q

QAM	Quadrature Amplitude Modulation

R

RF	Radio Frequency

S

SATCOM	Satellite Communications

SiGe	Silicium Germanium
SnPb	Tin-Lead
SRF	Self-Resonance Frequency

V

VoIP	Voice over IP
VSAT	Very Small Aperture Terminal

W

WiGig	Wireless Gigabit Alliance

Nederlandstalige samenvatting –Dutch Summary–

Onze huidige samenleving wordt gekenmerkt door een immer toenemende nood aan bandbreedte wat leidt tot de exploratie van nieuwe delen van het elektromagnetische spectrum voor datatransmissie. Dit resulteert in een stijgende interesse en ontwikkeling van millimetergolf (mm-wave) circuits die de mogelijkheid bieden tot korte afstand multi-gigabit draadloze transmissies bij 60GHz. Deze relatief nieuwe applicaties zullen aanwezig zijn naast reeds gevestigde mm-wave commerciële producten waaronder satellietsystemen in de Ka-band (26.5GHz - 40GHz) die volgende zaken toelaten: video uitzending, spraak over IP (VoIP), internet toegang in afgelegen gebieden, ... Beide hebben behoefte aan significante linaire vermogensversterking door de hoge attenuatie typisch voor dit gedeelte van het elektromagnetisch spectrum, echter, satellietsystemen vereisen een gesatureerd uitgangsvermogen dat makkelijk een grootte-orde hoger ligt (uitgangsvermogen boven de 30dBm / 1W).

Monolitisch microgolf geïntegreerde circuits (MMICs) die gebruik maken van III-V chip technologieën, bvb.: gallium arsenide (GaAs), gallium nitride (GaN), zijn tot op de dag van vandaag de geprefereerde keuze om efficiënte mm-wave vermogenversterkers (PA) met hoog gesatureerd uitgangsvermogen (>30dBm) te implementeren. Om de commerciële haalbaarheid van consumentenproducten binnen dit marktsegment verder te verhogen is een lage productiekost voor de vermogenversterker, samen met de mogelijke integratie van bijkomende functionaliteit, uitermate wenselijk. Deze kenmerken komen overeen met de positieve punten van silicium gebaseerde chiptechnologieën zoals CMOS en SiGe BiCMOS. Deze technologieën hebben echter een doorslagspanning lager dan 2V bij nodes toepasbaar voor mm-wave producten, terwijl III-V transistoren met een equivalent frequentiebereik doorslagspanningen boven de 8V demonstreren. Hierdoor liggen de uitgangsvermogens van CMOS en SiGe BiCMOS Ka-band vermogenversterkers zelden boven de 20dBm wat de grootste hin-

dernis vormt om deze technologieën te gebuiken voor satellietcommunicatie (SATCOM).

Om het gelimiteerde uitgangsvermogen van een enkele versterkingscel in een silicium technologie, veroorzaakt door de lage doorslagspanning, te overwinnen, zal het vermogen van verschillende vermogenversterkers moeten worden gecombineerd op chip. Dit vereist de integratie van passieve componenten met een hoge Q-factor op chip binnen een relatief kleine oppervlakte. Die componenten moeten in staat zijn tot een impedantietransformatie, vereist om de optimale lastimpedantie voor de verschillende versterkingscellen te creëren, en moeten een efficiënte vermogencombinatie op chip kunnen realiseren. In vergelijking met III-V technologieën vormt dit een bijkomende uitdaging door het gebruik van een silicium substraat dat hogere verliezen introduceert. Eens een voldoende hoog uitgangsvermogen is gerealiseerd op chip dient het probleem om dit signaal naar de buitenwereld te verplaatsen zich aan. Verder zal er ook een hogere hittegeneratie plaatsvinden bij hogere uitgangsvermogens door de beperkte efficiëntie van mm-wave PAs. Dit betekent dat een chip naar bord interface met een lage thermische weerstand en een elektrische connectie met lage verliezen moet worden bedacht.

Bewijs van de haalbaarheid van silicium als een serieuze kandidaat voor de integratie van Ka-band medium- en hoogvermogen versterkers zal enkel worden geleverd door langdurig onderzoek en de creatie van een dergelijke versterker. Het is binnen deze context dat het initiële doel voor het hier gepresenteerde werk werd opgesteld. Dit bestaat uit de creatie van een vermogenversterker met een gesatureerd uitgangsvermogen hoger dan 24dBm (meer dan 27dBm is wenselijk), een versterking groter dan 20dB en een efficiëntie boven de 10% (meer dan 15% is wenselijk). Deze specificaties werden bedacht met de preconditie dat een 250nm SiGe BiCMOS technologie (IHP's SG25H3) zou worden gebruikt met een f_T van 110GHz en een collector naar emitter doorslagspanning in open basis condities (BV_{CEO}) van 2.3V. Het gebruik van deze technologie is een significante uitdaging door de gelimiteerde snelheid aangezien de vuistregel bestaat uit het nemen van een vijfde van de f_T als de maximale werkfrequentie, wat zich weerspiegelt in de haalbare efficiëntie van het toegevoegd vermogen (power added efficiency, PAE). Hiertegenover staat dat de mogelijkheid tot implementatie in deze "oudere" technologie bewijst dat de toekomstige integratie in een snelle technologie (bvb.: IHP's SG13G2, f_t=300GHz) heel wat potentieel biedt. Naast problemen veroorzaakt door de limitaties van de chip technologie, laten de opgestelde specificaties toe om generieke moeilijkhe-

den te identificeren m.b.t. het ontwerp van een hoogvermogen versterker in silicium, bvb.: ontwerp van efficiënte vermogenscombinatie op chip, thermische organisatie, conversie van enkelzijdige naar differentiële signalen, ...

Door de academische aard van dit werk was de intentie om de begane paden te verlaten en alternatieve topologieën te verkennen. Dit heeft geleid tot het gebruik van een aandrijftrap die gebruik maakt van translineaire lussen voor de instelling van de stroom en een transformator versie van de Wilkinson vermogenscombinatie die voorheen enkel werd gebruikt bij kabeltelevisie (CATV) toepassingen. Alhoewel de vermogencombinatie 2dB meer vermogenverlies dan voorzien opleverde door de hoger dan verwachte substraatverliezen, toonden beide topologieën heel wat potentieel voor verdere integratie. Daarenboven werd een diepgaande analyse uitgevoerd op de uitgangstrap die gebruik maakt van positieve feedback om de versterking te verhogen. Het volledige ontwerp bestaat uit een vermogenscombinatie van vier klasse AB vermogenversterkers samen met teststructuren van welke de performantie werd geverifieerd door middel van probes.

Door de reeds eerder vermelde, hoger dan verwachte, verliezen in de vermogencombinatie op chip zijn ook het totale uitgangsvermogen en PAE een factor 2dB lager dan verwacht op basis van de simulaties. Het resultaat is een gesatureerd uitgangsvermogen bij 32GHz van 24.1dBm met een PAE van 7.2% en een kleinsignaal versterking van 25dB. Dit demonstreert de mogelijkheid om SiGe BiCMOS aan te wenden bij het ontwerp van medium-vermogen mm-wave applicaties. Bovendien bereikt de hier voorgestelde PA het tweede hoogste gesatureerd uitgangsvermogen bij vergelijking van SiGe BiCMOS vermogensversterkers met een centrale frequentie binnen of in de buurt van de Ka-band. Het 1dB compressiepunt van deze versterker ligt bij 22.7dBm wat dicht aanleunt bij het gesatureerd uitgangsvermogen en resulteert in lage spectrale teruggroei in vergelijking met commerciële GaAs PA's (vergeleken met een 2MBaud 16QAM ingangssignaal bij 10dB back-off).

Verschillende mogelijkheden tot verbetering resteren. De meest belangrijke is het herontwerp van de vermogencombinatie op chip om de verliezen te reduceren en het totale uitgangsvermogen en PAE te laten toenemen. Ook het overplaatsen van het ontwerp naar een snellere chiptechnologie kan mogelijks resulteren in een beduidende toename van de efficiëntie van de uitgangstrap met het nadeel dat meer versterkers moeten worden gecombineerd. De overgang naar een snellere chiptechnologie zou bijkomend toe-

laten om dit ontwerp te gebruiken voor alternatieve mm-wave applicaties zoals automotive radar bij 79GHz en WiGig bij 60GHz.

English summary

Our current society is characterized by an ever increasing need for bandwidth leading towards the exploration of new parts of the electromagnetic spectrum for data transmission. This results in a rising interest and development of millimeter-wave (mm-wave) circuits which hold the promise of short range multi-gigabit wireless transmissions at 60GHz. These relatively new applications are to co-exist with more established mm-wave consumer products including satellite systems in the Ka-band (26.5GHz - 40GHz) allowing e.g.: video broadcasting, voice over IP (VoIP), internet acces to remote areas, ... Both need significant linear power amplification due to the high attenuation typical for this part of the spectrum, however, satellite systems demand a saturated output power which is easily an order of magnitude larger (output powers in excess of 30dBm / 1W).

Monolithic microwave integrated circuits (MMICs) employing III-V chip technologies, e.g.: gallium arsenide (GaAs), gallium nitride (GaN), have historically been the preferred choice to implement efficient mm-wave power amplifiers (PA) with a high saturated output power (>30dBm). To further increase the commercial viability of consumer products in this market segment a low manufacturing cost for the power amplifier, together with the possible integration of additional functions, is highly desirable. These features are the strongpoint of silicon based chip technologies like CMOS and SiGe BiCMOS. However, these technologies have a breakdown voltage typically below 2V for nodes capable of millimeter-wave applications while III-V transistors with equivalent frequency performance demonstrate breakdown voltages in excess of 8V. Because of this, output powers of CMOS and SiGe BiCMOS Ka-band power amplifiers rarely exceed 20dBm which poses the main hurdle for using these technologies in satellite communication (SATCOM).

To overcome the limited output power of a single amplifying cell in a silicon technology, caused by the low breakdown voltage, multiple power amplifiers cells need to have their output power effectively combined on-chip.

This requires the on-chip integration of high-Q passives within a relative small area to realize both the impedance transformation, to create the optimal load impedance for the different amplifier cells, and implement an efficient on-chip power combination network. Compared to III-V technologies this is again a challenge due to the use of a silicon substrate which introduces higher losses. Once a large enough on-chip output power is created, the issue of launching this signal to the outside world remains. Moreover, due to the limited efficiency of mm-wave PAs, the generated on-chip heat will increase when larger output power are required. This means a chip-to-board interface with a low thermal resistance and a low loss electrical connection needs to be devised.

Proof of the viability of silicon as a serious candidate for the integration of medium and high power Ka-band amplifiers will only be delivered by long term research and the actual creation of such an amplifier. In this context, the initial goal for the presented work is proposed. This consists of the creation of a power amplifier with a saturated output power above 24dBm (preferably 27dBm), a gain larger than 20dB and an efficiency in excess of 10% (preferably 15%). These specifications where conceived with the precondition of using a 250nm SiGe BiCMOS technology (IHP's SG25H3) with an f_T of 110GHz and a collector to emitter breakdown voltage in open base conditions (BV_{CEO}) of 2.3V. The use of this technology is a significant challenge due to the limited speed, rule of thumb is to have at least one fifth of the f_T as the operating frequency, which reflects in the attainable power added efficiency (PAE). On the other hand, proving the possible implementation in this "older" technology shows great potential towards the future integration in a fast technology (e.g.: IHP's SG13G2, f_t =300GHz). Next to issues caused by limitations of the chip technology, the proposed specifications allows to identify generic difficulties with high power silicon PA design, e.g.: design of efficient on-chip power combiners, thermal management, single-ended to differential conversion, ...

As this work is of an academic nature the intention of this design was to leave the beaten track and explore alternative topologies. This has led to the adoption of a driver stage using translinear loops for biasing and a transformer-type Wilkinson power combiner previously only used in cable television (CATV) applications. Although the power combiner showed 2dB more loss than expected due to higher than expected substrate losses, both topologies show promise for further integration. Furthermore, an in-depth analysis was performed on the output stage which uses positive feedback to increase its gain. The entire design consists of a four-way power com-

bining class AB power amplifier together with test structures of which the performance was verified by means of probing.

Due to the previously mentioned higher than expected loss in the on-chip power combiner, the total output power and power added efficiency (PAE) was 2dB lower than expected from simulations. The result is a saturated output power at 32GHz of 24.1dBm with a PAE of 7.2% and a small signal gain of 25dB. This demonstrates the capability of SiGe BiCMOS to implement PA's for medium-power mm-wave applications. Moreover, to the best of the author's knowledge, this PA achieves the second highest saturated output power when comparing SiGe BiCMOS PA's with center frequency in or close to the Ka-band. The 1dB compression point of this amplifier lies at 22.7dBm which is close to saturated output power and results in a low spectral regrowth when compared to commercial GaAs PA's (compared with 2MBaud 16QAM input signal at 10dB back-off).

Many possible improvements to this design remain. The most important would be the re-design of the on-chip power combiner, possibly with a floating ground shield, to reduce the losses and increase the total output power and PAE. Also the porting of the design to a faster chip technology might result in a considerable increase of the output stage efficiency at the cost of needing to combine more amplifier cells. The transition to a faster chip technology would additionally allow to use this design for alternative mm-wave applications like automotive radar at 79GHz and WiGig at 60GHz.

List of publications

Publications in international journals

- **R. Pierco**, G. Torfs, J. Verbrugghe, B. Bakeroot and J. Bauwelinck, *A 16 Channel High-Voltage Driver with 14 Bit Resolution for Driving Piezoelectric Actuators*, IEEE Transactions on Circuits and Systems – I: Regular Papers, **[Accepted]**

- **R. Pierco**, G. Torfs, T. De Keulenaer, B. Vandecasteele, J. Missine and J. Bauwelinck, *A Ka-band SiGe BiCMOS power amplifier with 24 dBm output power*, Microwave and Optical Technology Letters, Vol. 57, Nr. 3, March 2015, pp. 718-722

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- R. Vaernewyck, J. Bauwelinck, X. Yin, **R. Pierco**, J. Verbrugghe, G. Torfs, Z. Li, X.Z. Qiu, J. Vandewege, R. Cronin, A. Borghesani, and D. Moodie, *113 Gb/s (10 x 11.3 Gb/s) ultra-low power EAM driver array*, Optics Express, Vol. 21, Nr. 1, January 2013, pp. 256-262

- **R. Pierco**, Z. Li, G. Torfs, X. Yin, J. Bauwelinck, and X.Z. Qiu, *Diode string with reduced clamping-voltage for ESD-protection of RF-circuits*, IET Electronics Letters, Vol. 48, Nr. 6, March 2012, pp. 317-318

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MOS technology for receiving multilevel signals up to 80Gbps, 10th Conference on PhD Research in Microelectronics and Electronics (PRIME), June 29 - July 3, 2014, Grenoble, France

- **R. Pierco**, T. De Keulenaer, G. Torfs, and J. Bauwelinck, *Analysis and design of a high power, high gain SiGe BiCMOS output stage for use in a millimeter-wave power amplifier*, 10th Conference on PhD Research in Microelectronics and Electronics (PRIME), June 29 - July 3, 2014, Grenoble, France

- R. Vaernewyck, J. Bauwelinck, X. Yin, **R. Pierco**, J. Verbrugghe, G. Torfs, Z. Li, X.Z. Qiu, J. Vandewege, R. Cronin, A. Borghesani, and D. Moodie, *A 113 Gb/s (10 x 11.3 Gb/s) ultra-low power EAM driver array*, Proceedings of the 38th European Conference and Exhibition on Optical Communication (ECOC), September 16-20, 2012, Amsterdam, Netherlands

Publications in national conferences

- **R. Pierco**, *The army of silicon ants versus the GaAs/GaN elephant in the battle for power efficient satellite communication* 14th FEA PhD symposium, Interactive poster session, pp. 70, December 6, 2013, Gent, Belgium

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Patents

- **R. Pierco**, J. Bauwelinck, and X. Yin, *ESD protection device with reduced clamping voltage*, European patent grant , EP2568501 B1, July 2, 2014

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1

Introduction

In recent years we have seen an increasing interest in millimeter-wave circuits, spurred by the possibility of short range multi-gigabit transmissions [1]. Emerging applications in this part of the spectrum are, to mention only some: WiGig, automotive radar and wireless backhaul systems [2]. Next to these relatively new applications, satellite systems operating in the Ka-band portion of the millimeter-wave spectrum have gained traction and SATCOM customer acceptance in the past decade [3]. What these upcoming mm-wave applications have in common is the need for linear power amplifiers, what differentiates them is the level of output power required.

Historically MMICs exploiting III-V semiconductor technologies have been preferred for mm-wave power amplifiers. These technologies provide the benefit of high electron mobility, high breakdown voltage and the availability of high-Q passives [4]. However, the viability of mm-wave mass-market applications hinges on the combination of a low production cost and a dense integration of functions for which silicon technologies are superior. While the increase of transistor cut-off frequency, f_T, of advanced SiGe BiCMOS and CMOS technologies above 200GHz makes it possible to apply these for mm-wave applications, simultaneous decrease in breakdown voltage makes it difficult to create high power amplifiers.

1.1 Motivation for SiGe BiCMOS millimeter-wave power amplifiers

1.1.1 Millimeter-wave chip technologies

Realizing a mm-wave Power Amplifier (PA) is possible in a variety of chip technologies. To choose the appropriate technology a figure of merit (FoM) employed by the International Technology Roadmap for Semiconductors (ITRS) [5] is used. This FoM incorporates the PA output power P_{OUT}, the PA power gain G, the power-added-efficiency PAE and the carrier frequency f and equals:

$$FOM_{PA} = P_{OUT} \cdot G \cdot PAE \cdot f^2 \tag{1.1}$$

In order to compare chip technologies using equation 1.1, two seperate equations have been proposed in [5] which use transistor parameters such as f_{max}, BV_{CEO} (BV_{GD} in case of CMOS) and peak f_T current density J_{pfT} ($I_{ON}/2$ in case of CMOS). This results in a FoM expressed in $GHz^2 \cdot W/mm$ which is shown in Fig.1.1 for both existing and roadmap based chip technologies.

From Fig.1.1 it can be concluded that SiGe BiCMOS technology is able to deliver PAs with better performance than CMOS and InP technologies and similar performance as GaN technology. However, calculation of the FOM in the ITRS was done with rather unrealistic assumptions like ideal passive components and a PAE of 50%. Due to the lossy silicon substrate in SiGe BiCMOS technologies, the quality of passives will be degraded in comparison to GaN and InP which means that the GaN FOM will be higher than the SiGe BiCMOS FOM in realistic designs. Moreover, due to the finite quality of passives in silicon technologies it isn't possible to achieve high impedance transformation ratios with a reasonable PAE which means that the FOM of SiGe BiCMOS and CMOS will be lower for higher required output powers. Silicon technologies, however, provide the benefit of low production cost and the possibility to integrate different functions together with the PA. When comparing SiGe BiCMOS and CMOS the conclusion is that SiGe BiCMOS will provide a clear technological benefit which is mainly due to the higher breakdown voltage and higher transconductance.

From an economical perspective SiGe BiCMOS will be many times cheaper than compound technologies like GaAs, GaN and InP. In comparison to CMOS the development of BiCMOS is one or two technology nodes behind. However for the same node the bipolar transistor is roughly twice as fast as an NMOS transistor [6]. Due to the larger feature size, a BiCMOS

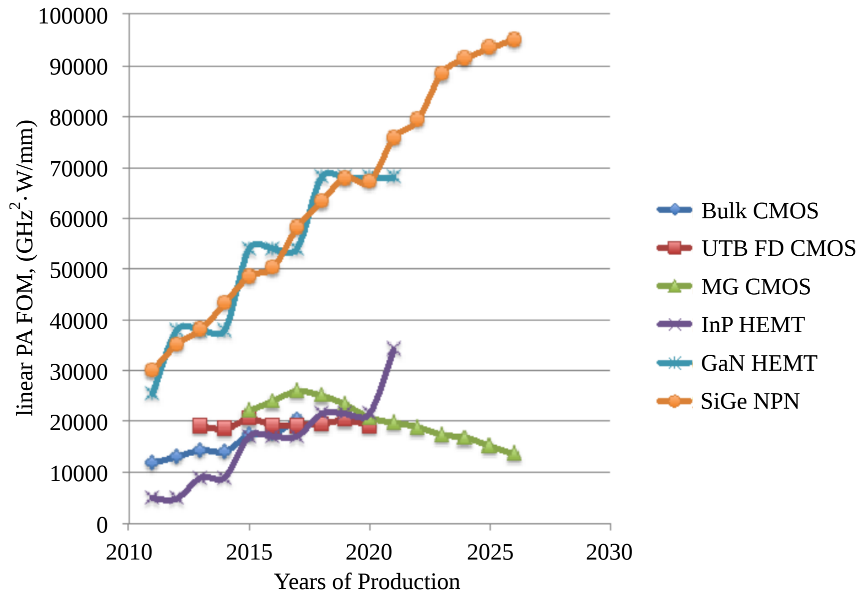

Figure 1.1: PA performance of existing chip technologies and different transistor technology roadmaps capable of mm-wave PAs. Reproduced from: International Technology Roadmap for Semiconductors (ITRS) 2013.

process will be approximately half as expensive as an equally fast CMOS process as is shown in Fig.1.2 [7]. Only when large digital blocks need to be integrated, the use of CMOS possibly becomes interesting due to the resulting smaller chip size.

1.1.2 Evolution of SiGe BiCMOS technologies

An important measure for the performance of a chip technology in terms of PA capability is the product of the f_T and the limiting breakdown voltage. For SiGe BiCMOS the collector-emitter breakdown voltage (BV_{CEO}, open base condition) is typically used which leads to the well-known Johnson limit [8]. The Johnson limit dictates that:

$$f_T \cdot BV_{CEO} < \frac{v_{sat} \cdot E_{bd}}{2\pi} \tag{1.2}$$

For Si bipolar transistors, Johnson originally used $v_{sat} = 6 \cdot 10^6 cm/s$ and $E_{bd} = 2 \cdot 10^5 V/cm$, with v_{sat} the electron saturation velocity and E_{bd} the maximum electrical field from bulk to drain. This results in a limit of

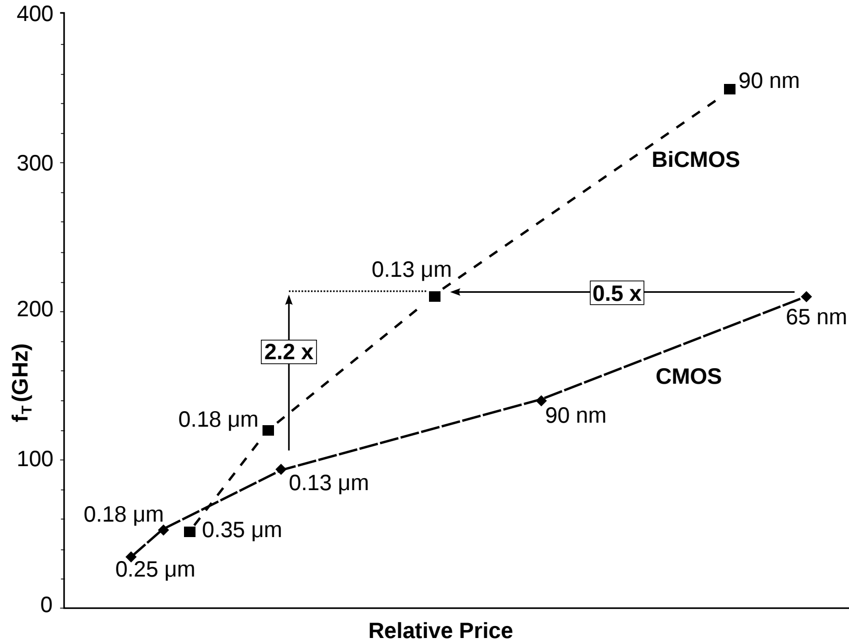

Figure 1.2: Comparison of price vs. performance of BiCMOS and CMOS for different technology nodes.

approximately $190 GHz \cdot V$ which has been crossed around the year 2000 and it has been shown that the product of BV_{CEO} and f_T isn't constant but increases with f_T with a minimal value of approximately $500 GHz \cdot V$ [9].

The f_T and BV_{CEO} values for several modern mm-wave SiGe BiCMOS technologies are depicted in Fig.1.3 together with the original Johnson limit. From this graph it can be noticed that higher f_T technologies also have a higher $f_T \cdot BV_{CEO}$ which means that the suitability of SiGe BiCMOS as a PA-enabling technology is increasing. This last statement is only true if the passives used for on-chip power combination and impedance transformation further improve which enables to counter the diminishing breakdown voltages. To realize this, dedicated SiGe BiCMOS technologies add thick top metal layers and increase the height of the dielectric separating the top metal layers and the substrate [10]. Advancements on both the front of on-chip passives and the f_T BV_{CEO} product will thus result in the possible application of SiGe BiCMOS technologies for an increasing range of mm-wave products.

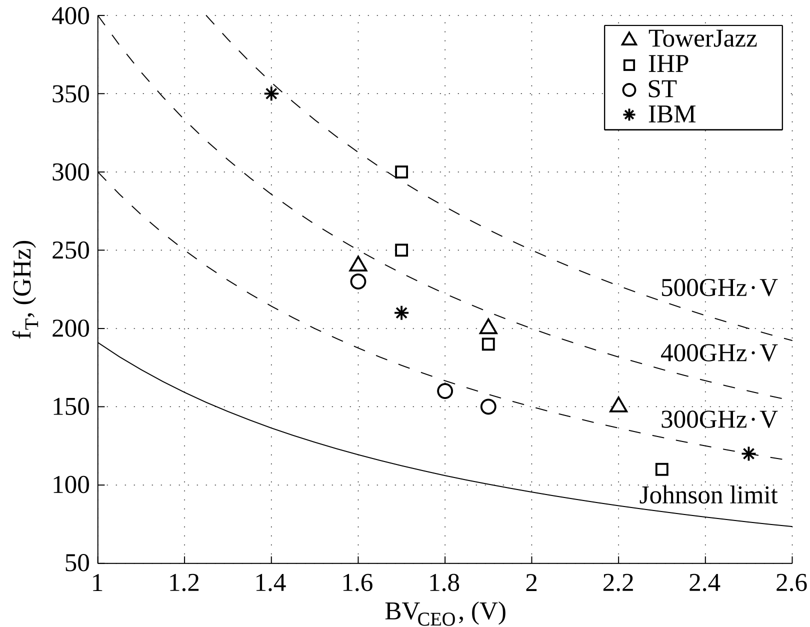

Figure 1.3: f_T and BV_{CEO} of modern SiGe BiCMOS technologies together with the original Johnson limit ($\approx 190GHz \cdot V$).

1.2 Overview of the work

During the past 4 years the author has conducted research at the INTEC_design laboratory which is part of the department of information technology (INTEC) at Ghent University and specialized in the development of high-speed and high-frequency electronic circuits. Within this group, engineers are offered the opportunity to attain hands-on experience in complex industrial-driven design projects. It was from one of these projects that the research, discussed in this dissertation, originated.

1.2.1 Design of a Ka-band SiGe BiCMOS power amplifier

In this dissertation the design of a Ka-band power amplifier for use in a satellite uplink is discussed. Since this is a critical component in very small aperture terminal (VSAT: dish antenna diameter < 3m) applications, the possibility to implement this PA in a SiGe BiCMOS technology is investigated due to the commercial benefits in comparison to III-V technologies as previously mentioned. A quick literature study reveals that SiGe BiCMOS PAs in the Ka-band rarely deliver more than 23dBm saturated output

power and their 1dB compression point is typically below 20dBm [11–13]. At the same time, GaAs and GaN commercial PAs used for Ka-band SATCOM provide around 30dBm (one watt) of saturated output power with a 1db compression point approximately one dB lower [14, 15].

The goal of this research is to investigate whether silicon based technologies are able to become a worthy alternative for III-V technologies for the implementation of medium and high Ka-band PAs and to identify the main challenges involved. To achieve this a Ka-band power amplifier will be designed which aimes to achieve an output power above 24dBm and preferably up to 27dBm with a 1dB compression point not more than 1.5dB below the saturated ouput power. To keep the drive requirements for the PA limited, a gain of more than 20dB is preferred with an efficiency above 10% and preferably larger than 15%. This is a very challenging task since a 250nm SiGe BiCMOS technology is chosen with an f_T of 110GHz and a BV_{CEO} of 2.3V.

1.3 Outline

The organization of this dissertation is the following. In Chapter 2 the challenges attributed to millimeter-wave power amplifier design are given together with general PA design problems like chip-to-board interconnection and thermal issues. This leads to a number of design considerations discussed in Chapter 3 which will further on lead to a number of design decisions regarding the topology (single-ended versus differential) and the amplifier class (depending on chip technology, gain, linearity and required efficiency). A critical part of any PA is the output stage which is the subject of Chapter 4. An analysis of the implemented feedback mechanism is given together with a discussion on the differential and common-mode stability. Furthermore, the loadline matching, the design of the balun and the layout of this output stage, are explained. In Chapter 5 the driving stage is given which is additionally responsible for the biasing of the output stage. Since both the output and driving stage are differential, a pre-driver stage is implemented which accomplishes the single-ended to differential conversion. This, together with the power combination and distribution strategy and the designed on-chip power combiner/splitter, is described in Chapter 6. In order to come to a complete functional chip, biasing and ESD circuitry needs to be added which is the subject of Chapter 7 together with the layout of the testboard solution. By means of the measurement setup discussed in Chapter 8 the main characteristics of the PA are verified. This is compared to the state-of-the-art in the final chapter of this dissertation (Chapter 9) in

which conclusions towards the performance of this design are drawn. In addition to this, possible improvements and future design possibilities are described here.

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2

Millimeter-wave power amplifier challenges

When moving to mm-wave frequencies the problems that existed with classic power amplifier design at microwave frequencies become increasingly difficult to solve. Furthermore some new problems arise due to the nature of mm-wave signals. One of the main challenges is to reach the needed output power with the technology at hand. While the gain-bandwidth product of silicon technologies is increasing with device scaling, the breakdown voltages go down [1], [2]. Due to the decrease in transistor breakdown voltages, the impedance transformation needed at the amplifier will become bigger. As a result the Q-factor of the matching structure needs to increase to keep the efficiency at a reasonable level [3] as will be shown in Section 2.1.2. At the same time the Q-factor that can be reached for on-chip passives is severely limited at mm-wave frequencies due to the silicon substrate. When all these challenges have been met, there is still the issue of effectively launching the power on and off the chip which will be discussed in Section 2.3. Since the efficiency of mm-wave PAs is limited, the generated heat on-chip will increase when large output powers are required. This means that appropriate measures need to be taken to assure that the chip performs as anticipated.

2.1 Transistor breakdown voltages

2.1.1 Fundamental limits

While the maximum voltages that can be applied to a MOS transistor are determined by BV_{OX} and BV_{DSS} [2], respectively the gate-drain/source oxide breakdown voltage and the drain-source breakdown voltage, the maximum voltage that a bipolar transistor can withstand at the collector is determined by BV_{CEO} and BV_{CBO}. These two values represent two extreme cases where BV_{CEO} gives the breakdown voltage from collector to emitter in case the transistor is biased by means of a current source at the base and BV_{CBO} roughly compares to the maximum voltage between collector and base when biased with a current source at the emitter [4]. Since BV_{CBO} typically is two to three times higher than BV_{CEO}, the average (or DC) collector emitter voltage V_{CE} of a transistor can exceed BV_{CEO} if the emitter current is tightly controlled and the impedance at the base is kept low [5]. Due to the occurence of thermal runaway the average V_{CE} can only slightly exceed BV_{CEO}, however, the peak collector-emitter voltage (of a time-varying signal) can go up to the avalanche breakdown limit which comes down to the limit imposed by BV_{CBO} if the holes which flow back to the transistor base are effectively shunted to ground [6]. The voltage that a bipolar transistor can withstand at its base is furthermore determined by the BV_{EBO}, however, this value isn't of practical use for most (if not all) PA circuits. The bipolar transistors used in this design are part of IHP's SG25H3 process and have following breakdown voltages: BV_{CEO} =2.1V$_{min}$/2.3V$_{typ}$, BV_{CBO} = 4.5V$_{min}$/ 6V$_{typ}$ and BV_{EBO} = 0.3V$_{typ}$.

By applying an appropriate biasing circuit the useful collector voltage can be more than doubled as can be seen in Fig.2.1. Two types of biasing are applied in Fig.2.1 with the first using a constant base current (dashed lines). The second biasing corresponds to the common base transistor in a cascode configuration which has a more or less constant emitter current (see Chapter 4). Next to biasing by means of a constant base current or a more or less constant emitter current (as with a cascode), a transistor can also be biased by a constant base emitter voltage as is the case in a common emitter amplifier. This will lead to maximum collector voltages that lay somewhere between BV_{CEO} and BV_{CBO}.

The lower limit of the useful collector voltage will be determined by the knee voltage (V_k) of the transistor which is the collector emitter voltage at which the transistor leaves the saturation region. In Fig.2.1 it can be seen that V_k will also be positively influenced by biasing a bipolar transistor with a constant emitter current. This case leads to a saturation voltage of

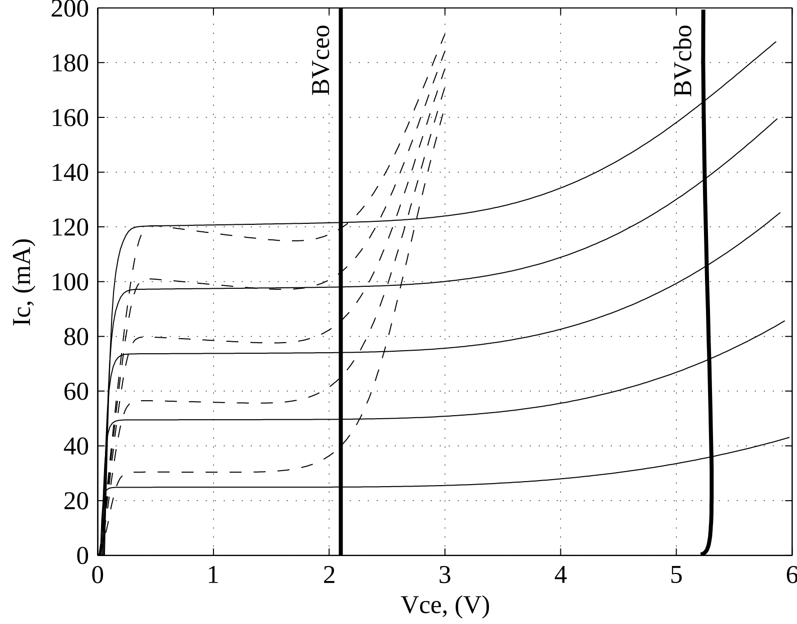

Figure 2.1: Bipolar collector current I_C in function of collector emitter voltage V_{CE} for biasing in a cascode configuration (solid curves) and by means of a constant base current (dashed curves).

roughly 0.15V while this will be around 0.3V for the transistor biased with a constant base current.

2.1.2 Impedance transformation

To explain the necessity of impedance transformation we can calculate the needed load resistance R_l at an amplifier output in function of the desired amount of output power P_{out} and the supply V_{cc} and knee voltage V_k [7]:

$$R_l = \frac{(V_{cc} - V_k)^2}{2P_{out}} \tag{2.1}$$

When trying to attain half-a-watt of output power with a supply voltage of 3.3V and a knee voltage of 1.3V (corresponds to simulated values for a cascode output stage, see Section 4.4.2), the needed load resistance at a single-ended output stage comes down to 4Ω. To achieve matching to a standard impedance of 50Ω, an impedance transformation of 12.5 will be needed. One of the most straightforward methods of creating an impedance transformation network is by means of a resonant LC network or a so called

"L-match" [8]. This consists of a series inductor L followed by the parallel combination of a capacitor C and the actual load resistance of which the impedance needs to be transformed. To get an idea of the power efficiency that this kind of matching can attain, the power enhancement ratio E is first defined. This ratio comes down to the impedance transformation ratio r of which the losses in the matching network are taken into account [9]. This means that for a lossless impedance transformation the E will be equal to r. The realizable efficiency for an L-match network in function of the power enhancement ratio for different Q-factors is shown in Fig.2.2.

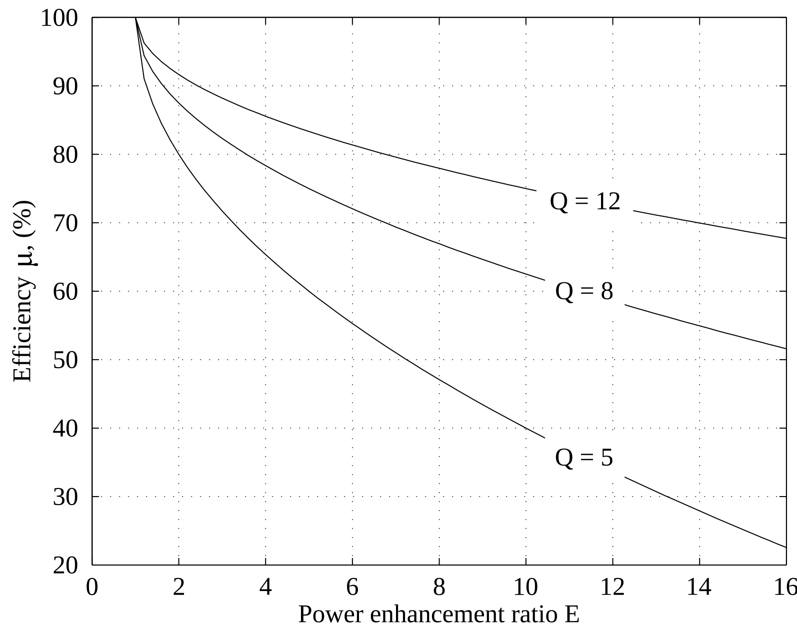

Figure 2.2: Maximum attainable efficiency for a certain power enhancement ratio E in case of a resonant LC impedance transformation network.

If the previously discussed impedance transformation ratio of 12.5 is considered together with an L-match and an inductor Q-factor of 12, then the maximum attainable efficiency is 72.5%. Although this is still reasonable, the topology of an LC-match requires the use of an additional RF-choke to provide a supply voltage to the amplifier. Creating this inductor would be very hard at mm-wave since it needs to have a large inductance value, have a high Q and have a self-resonance frequency higher than the PA carrier frequency. A better solution would then be to design an inductor that resonates with the output capacitor of the amplifier at the PA frequency.

Another way of creating an impedance transformation network is by using a transformer which has the benefit that the efficiency of the impedance transformation is independent of the impedance ratio and the maximum efficiency η is then given by [9]:

$$\eta = \frac{1}{1 + 2\sqrt{\left(1 + \frac{1}{Q_1 Q_2 k^2}\right)\frac{1}{Q_1 Q_2 k^2}} + \frac{2}{Q_1 Q_2 k^2}} \tag{2.2}$$

In equation 2.2 the factors Q_1, Q_2 and k are the Q-factor of the primary, the secondary and the coupling factor between windings respectively. This formula assumes that an optimum value for the winding inductances is used which is sometimes not realizable on-chip. Furthermore it should be noted that, although the maximum efficiency is independent of the winding ratio, the Q-factor of the winding inductances will typically be lower for higher winding ratios due to practical inductor design considerations. The efficiencies that can be achieved for a transformer for a coupling factor k of 0.6, 0.7 and 0.8 and secondary Q-factor of 5 and 12 in function of the primary inductance Q-factor is shown in Fig.2.3.

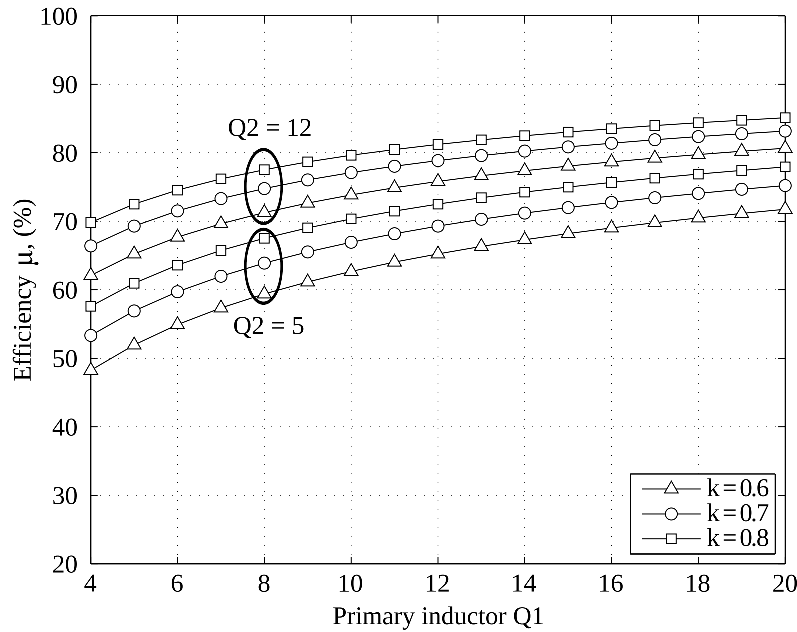

Figure 2.3: Efficiency of an impedance transformation by means of a transformer for various values of the primary and secondary Q-factor (Q1 and Q2 respectively) and coupling factor k.

Compared to an LC-match circuit, the transformer additionally has the benefit that it takes less chip area since primary and secondary take the same area as a single inductance whereas the L-match needs two seperate inductors. Furthermore a transformer allows to use a differential amplifier which further lowers the needed impedance transformation. Another solution to lowering the needed impedance transformation is to use power combining of several amplifiers which lowers the needed output power of a single amplifier which in its turn will lower the needed impedance transformation.

2.2 Inductor loss mechanisms

When implementing an impedance transformation using on-chip inductors, the main source of loss will typically be the limited Q-factor of the inductor. Following is a discussion on the different loss mechanisms that can be found in an on-chip inductor. Insight in these mechanisms allows to design inductors with a higher Q-factor but also explains why Q-factors typically drop when going to the mm-wave frequency domain. The loss in inductors can be split up into the two main contributors which are the metal and the substrate used in a certain chip technology [10].

2.2.1 Metal losses

Losses caused by the metal used to realize the inductor come from three different sources:

- The DC resistance of the metal.
- Reduction of the conducting part of the metal cross-section due to:
  - The skin effect caused by the self-induced magnetic field.
  - The proximity effect caused by the magnetic field induced by adjacent conductors.

Both the skin and proximity effect will increase with increasing frequency which means that these will become increasingly important for mm-wave inductors. In order to reduce the losses attributed to the metal, the main solution is to increase the conductor cross-section (by using for instance stacked metals) and increase spacing between adjacent conductors.

2.2.2 Substrate losses

Substrate losses are caused by currents induced in the substrate by either the electric field (potential currents) leading to dielectric losses or the magnetic field (Eddy currents) which causes Eddy losses. The magnitude of these currents is determined by the resistivity of the substrate which is approximately 10Ω-cm for most modern silicon processes and 10^7 - 10^9 Ω-cm for GaAs [11]. This shows that the quality of passives on GaAs (and GaN) will be many times higher than on silicon. When considering a silicon substrate and small inductors (diameter order of magnitude 100μm or smaller) the dielectric losses are the major contributor to the total quality factor for frequencies from 10GHz up to 40-50GHz [12].

Dielectric losses can be reduced by adding a ground shield consisting of either metal or polysilicon/buried N^+,P^+/N-well layers. By applying a pattern to this shield as depicted in Fig.2.4, the generation of Eddy currents in this shield is avoided. The patterned ground shield (PGS) will reduce the penetration of the electric field into the substrate. In order to shield the magnetic field, the thickness of the shield needs to significantly exceed the skin depth of the used conductor which means that there will only be magnetic shielding at high frequencies (typically above 10GHz) [13]. However due to the added capacitance by the ground shield the self-resonance frequency (SRF) of the inductor will drop. As a result adding a PGS typically isn't done above 20GHz. All this means that for small inductors a PGS can improve the Q-factor for frequencies between 10GHz and 20GHz. For larger inductors (diameters larger than 100μm) the dielectric losses can be the dominant loss factor for frequencies down to 2.4GHz [2]. In this case addition of a PGS can be beneficial.

An alternative to the PGS is the use of a floating shield which consists of parallel metal strips in a mesh configuration as shown in Fig.2.5. Since the shield is floating, the added capacitance is minimized, which means that the change in SRF will be negligible while the Q-factor can potentially increase [15]. To prevent a non-zero voltage on the floating strips it is required that a balanced inductor design is used. Additionally the presence of a floating shield can help to overcome metal density rules.

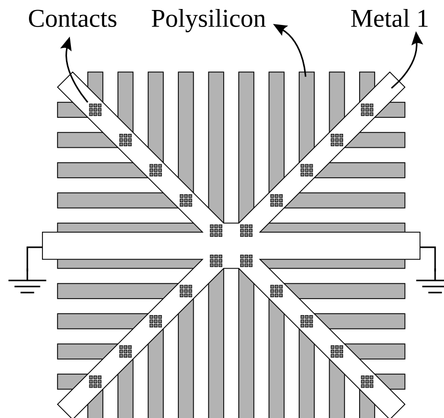

Figure 2.4: Patterned ground shield (PGS) consisting of polysilicon and metal 1 as used in [14].

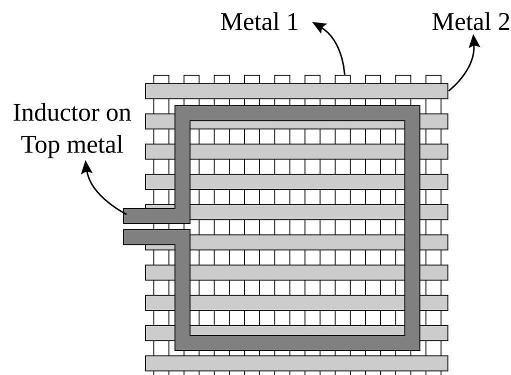

Figure 2.5: Floating shield consisting of metal 1 and metal 2 in a mesh configuration as described in [15].

2.3 Millimeter-wave chip-to-board interconnection and testing

2.3.1 Wirebonding to board

Over 90% of all available chips today are interconnected (either to a package, interposer or board) using wirebonding [16]. This is due to the reliable nature of wirebonding interconnections and the availability of low-cost infrastructure. However, wirebonding leads to a low-pass network due to the bonding loop inductance together with the bonding pad capacitance which will exclude many mm-wave applications of using this technology.

By adding ground bondwires next to the signal bondwire and reducing the length of the wires by placing the chip inside a board cavity, performance can be improved. But even with these measures and a bondwire length of 400μm the loss is roughly 0.4dB at 29GHz [17]. Next to the losses from the wirebonding, the test board's grounded coplanar waveguides (GCPW's) and connectors will add a significant amount of loss. It is shown in [18] that for instance a 30.4mm long GCPW trace implemented onto a Rogers RO4003C substrate with 2.4mm connectors leads to a total loss of 3.5dB and 4.5dB for the LoPro and non-LoPro substrate version respectively. This means that to correctly characterize and test a millimeter-wave chip, probing is required.

2.3.2 Flip-chip interconnection

An alternative to wirebonding is the use of flip-chip to connect the mm-wave chip to the board which excludes the low-pass characteristics of wire-bonds. In a flip-chip bonding technique, dots/bumps (solder balls or soft gold) are applied to the bondpads, subsequently the chip is flipped and bonded to the board (by means of thermosonic, thermocompression or a reflow process). A large amount of combinations of different pad sizes and bump heights are possible as is thoroughly discussed in [19]. Putting all these variations in a 3D EM simulator (Microwave CST) shows that all of them achieve bandwidths above 50GHz [20]. A cross-section of two possible setups suitable for millimeter-wave high power (inclusion of heat sink) applications using a wire-bonded and flip-chipped asic setup are shown in Fig.2.6 (a) and (b) respectively.

Both mounting methods shown in Fig.2.6 have their merit. The flip-chip solution will become inevitable when large bandwidth signals need to be launched onto the testboard. However, this solution has inferior thermal performance in comparison to the bondwired asic which has the backside soldered directly to the heatsink. It should be noted that this requires the backside of the chip to be metallized. Next to the lower thermal performance, another disadvantage of using a flip-chipped asic is that the board needs the same (high) resolution as the chip which increases the price. Regarding the bondwire solution, when the bondwire connections prove to be insufficient to characterize the chip with the testboard there is always the option to probe the asic and only connect DC-connections (or low speed signals) by means of bondwires.

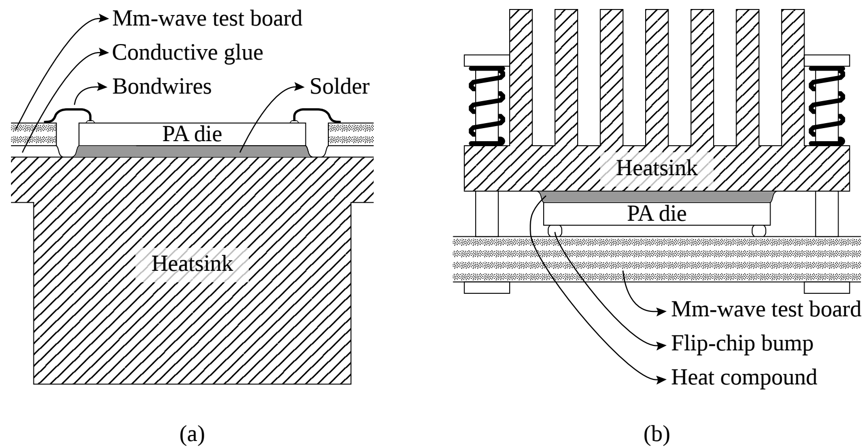

Figure 2.6: Cross-section for two possible millimeter-wave PA test setups using (a) a bondwired asic and (b) a flip-chipped asic.

2.4 Thermal issues

A typical technology design kit includes models for the self-heating of the transistors due to the non-zero thermal resistance of the silicon substrate. This model is good in providing the temperature for a single transistor, however, it doesn't take into account the proximity of other "hot" transistors. Also the connection between the chip backside and the die paddle of the package (and the connection further to the board heat sink) is not included. For most chip designs this kind of predictions of transistor temperature will match closely to the real-life temperature. However, while designing a power amplifier, this kind of self-heating model might prove insufficient. In order to get a better estimate of on-chip transistor temperatures a 3D CST model of the PA was implemented which is depicted in Fig.2.7.

The 3D model of Fig.2.7 includes the layers which will have a significant effect on the heat generation. This mainly comes down to the bulk silicon substrate and the silicon dioxide layers in which the metal is routed. Heat sources in this model are the transistors of the output stage and the hottest transistors of the driver stage. The interface between the backside of the chip and the board/heatsink is discussed later on (see Section 2.4.2).

This model needs to be calibrated which is done by placing a single cuboid in the silicon substrate (which has a thermal ground at the backside) with the same width and length as a transistor of which the temperature is calculated by means of the design kit. The power dissipation inside this cuboid is chosen to be the same as this of the transistor in the design kit. Next, the

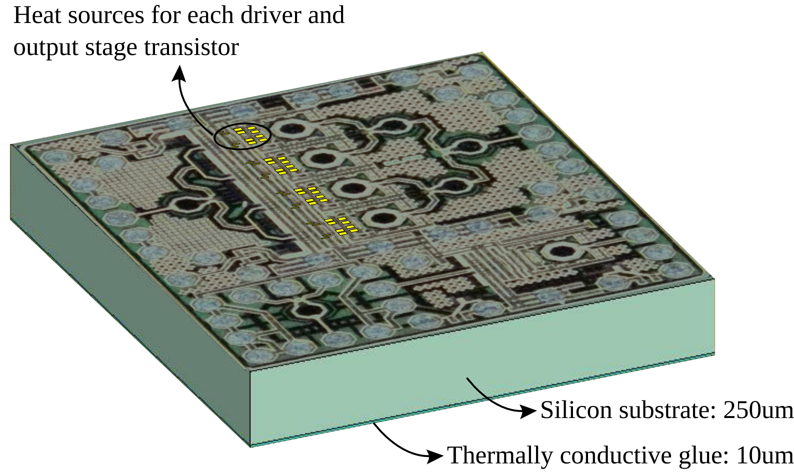

Figure 2.7: 3D CST model used for on-chip heat simulations together with chip layout overlay.

height of the cuboid is varied until the same temperature is simulated with the 3D model as was achieved with the self-heating model of the design kit.

2.4.1 Inter transistor heat exchange

A power amplifier will typically dissipate a large DC power (3.55W for the PA discussed in this dissertation) inside a relatively small area (in this case: 0.425mm^3) which means that the thermal resistance of the chip substrate and the interface connecting the substrate to the heatsink needs to be low to achieve reasonable on-chip temperatures. Regarding inter transistor heat exchange, the main factor of interest is the thermal conductivity of the substrate which should be as high as possible. The advantage of using a silicon substrate is that in comparison to most of the compound semiconductor technologies (e.g.: GaAs, InP) it has a larger thermal conductivity and lower susceptibility to degradation due to transient pulse stress [21].

The thermal conductivity for different semiconductor substrates shown in Fig.2.8 not only shows that silicon has the highest thermal conductivity when compared to compound chip technologies, it also demonstrates that the thermal conductivity drops with increasing temperatures. This means that power dissipating transistors can be placed closer on a silicon substrate compared to any other compound substrate. In order to determine an appropriate spacing between transistors the substrate to heatsink interface needs to be included as will be shown in Section 2.4.2.

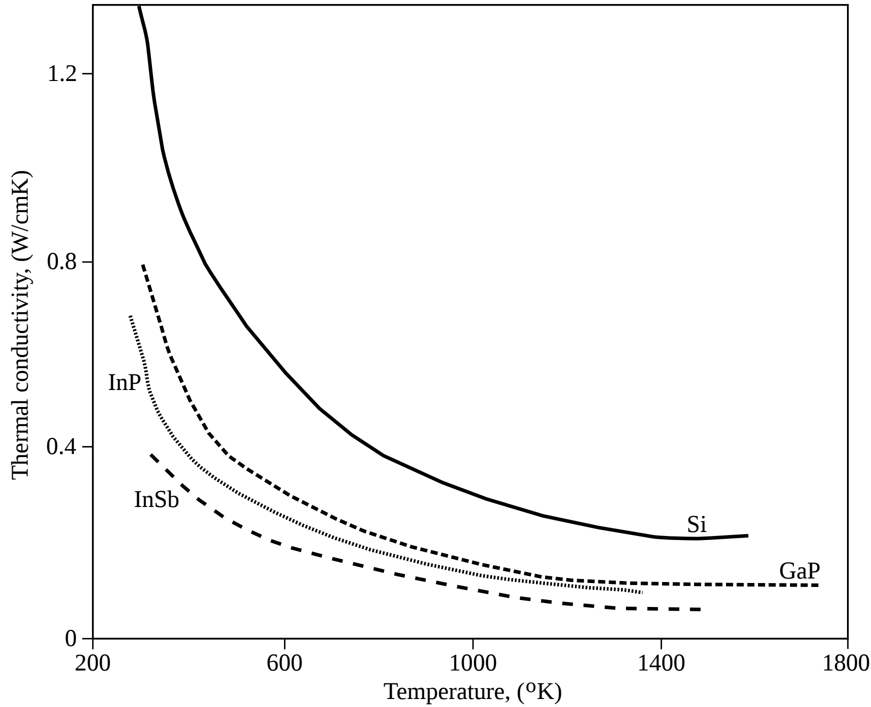

Figure 2.8: Thermal conductivity of different semiconductor substrates in function of temperature. Reproduced after [21].

2.4.2 Chip to heatsink interface

A critical part in the transport of heat from the chip to the heatsink is the interface between the die backside and the heatsink. The PA was mounted with its backside directly onto the heatsink by means of thermally conductive glue (epoxy-silver: 0.9W/m·K) and soldering (SnPb: 50W/m·K). The resulting simulated on-chip temperature for an interface with a thickness of 10μm is depicted in Fig.2.9.

From Fig.2.9 it immediately becomes clear that a good thermal contact with the heatsink will be decisive in achieving reasonable on-chip temperatures and chip performance. When comparing the glued version to the soldered PA a maximum temperature of 365.8^{o}K (92.65^{o}Celsius) and 349.8^{o}K (76.65^{o}Celsius) is simulated respectively with a 10μ thick interface layer (estimated from visual inspection of a mounted die). However it should be taken into account that the real-life version will have a non-uniform thick interface layer which additionally might have some holes (voiding). Fur-

thermore, the bonding phase (epoxy) and the conducting phase (silver) of expoxy resins have the tendency to segregate at the interface which means that the actual thermal conductivity can be much lower [22]. Measurements of the PA performance hinted towards an on-chip temperature around 90°C which, based on self-heating, leads to transistor temperatures of 150°C. As a result the only decent PA performance was achieved with the soldered version.

Also noticeable in Fig.2.9(a) is the slightly higher transistor temperature for the inner transistors of the PA output stage (output stage is represented by the hottest transistors) which is caused by the limited distance between the transistors causing inter transistor heat exchange.

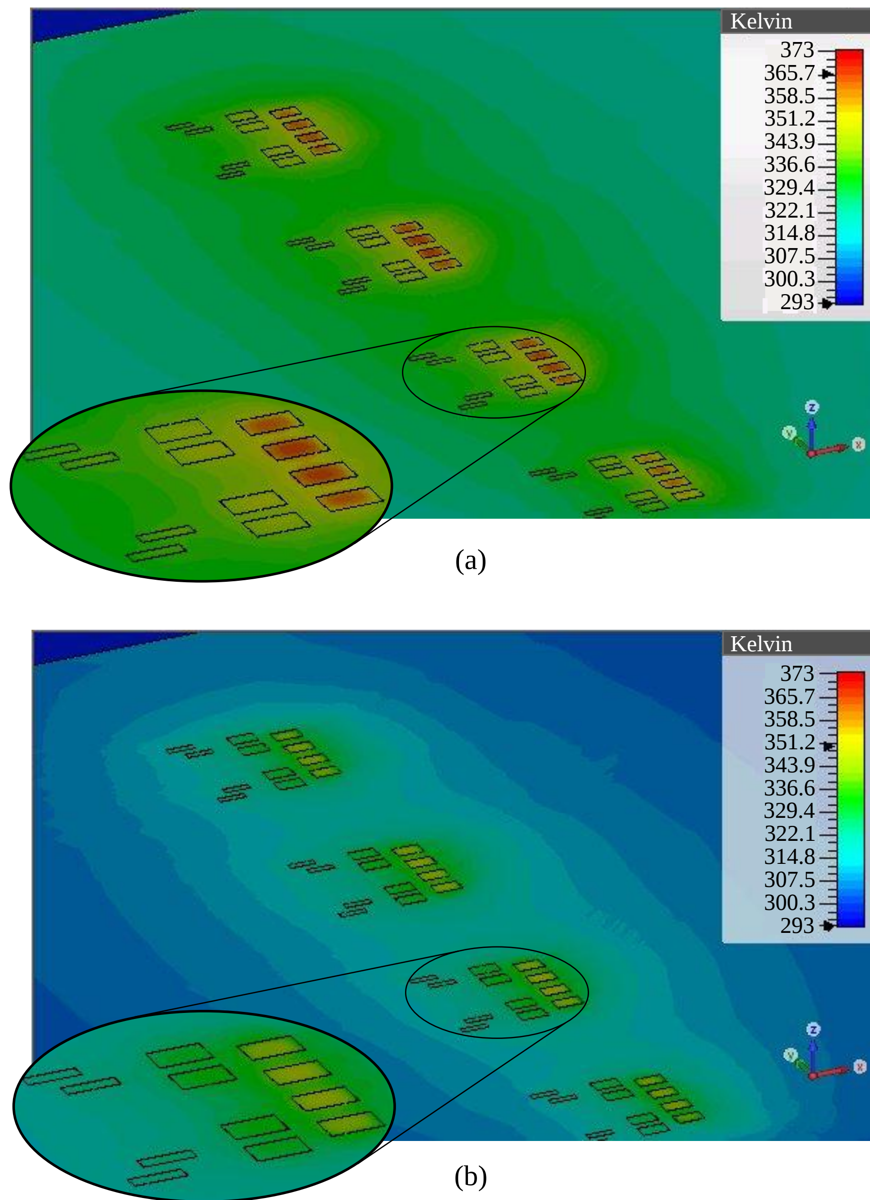

Figure 2.9: On-chip temperature obtained by means of CST heat simulation in case of (a) the PA die glued to heatsink with thermally conductive glue (epoxy-silver: 0.9W/m·K) and (b) the PA die soldered (SnPb: 50W/m·K) directly onto the heatsink. Thickness of the interface layer is 10μm.

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3

Power amplifier design considerations and specifications

The main specifications of a power amplifier are the gain, efficiency, linearity and output power. Based on the output power, the needed efficiency and production cost an appropriate chip technology needs to be chosen. This will, together with the needed gain, determine how many driving stages are needed which will be further discussed in Section 3.2. The amplifier class used, will be decided based on the efficiency and linearity required. An overview of the possible classes and their suitability for RF integration is given in Section 3.3. The chip technology, and more in particular the f_T and breakdown voltages, may also exclude some types of amplifiers.

3.1 Single-ended versus differential

The problem with using a single-ended topology is the ground bounce caused by the impedance of the on-chip ground. This will cause degeneration which in turn will reduce the gain and PAE of the amplifier stages. Also the voltage present on the on-chip ground may cause undesirable feedback between the different stages of the amplifier and it can even lead to instability [1]. The two contributing factors to the ground impedance are the impedance of the on-chip ground itself and the inductance of the bondwires connecting the on-chip ground to the external ground. While the inductance

between the on-chip ground and the external ground can be lowered by increasing the number of ground bondwires, the minimum impedance of the on-chip ground is limited by the resistance of the metal connections and the space that is left between the circuits to route the ground plane. By providing multiple parallel ground/power lines the inductance of these supply domains can be minimized.

Using a differential amplifier avoids ground bounce by the creation of a local virtual ground [1], [2]. An additional benefit of a differential output stage is that the needed impedance transformation is two times lower for the same delivered output power in case a transfomer is used. This is due to both differential output transistors which only need to generate one half of the output voltage swing.

3.2 Number of driving stages

Next to achieving a certain amount of gain and meeting the output power requirement, the efficiency (η) and power added efficiency (PAE) are important PA measures since these imply less DC current consumption and a relaxed requirement on the heat dissipation for a certain output power. These two measures are defined as:

$$\begin{aligned} \eta &= \frac{P_{RFout}}{P_{DC}} \\ \text{PAE} &= \frac{P_{RFout} - P_{RFin}}{P_{DC}} \end{aligned}$$

with:

P_{DC}: amplifier DC power

P_{RFout}: amplifier output power

P_{RFin}: amplifier input power

From the η and PAE formula follows that:

$$\text{PAE} = \left(1 - \frac{1}{Gain}\right) \cdot \eta \tag{3.1}$$

When the gain of an amplifier stage is large enough the PAE will equal η as can be deducted from equation 3.1. However a very large gain might induce stability issues due to feedback through the on-chip ground plane/rails and power rails.

A power amplifier with high output power will require a large gain to relax the drive requirements. The gain of a single stage, however, is limited by the combination of the used chip technology and the carrier frequency of the PA. When a certain amount of gain is needed the chosen chip technology will determine the number of stages required to achieve this. The gain per driving stage in function of the number of stages for a total gain of 20dB is shown in Fig.3.1.

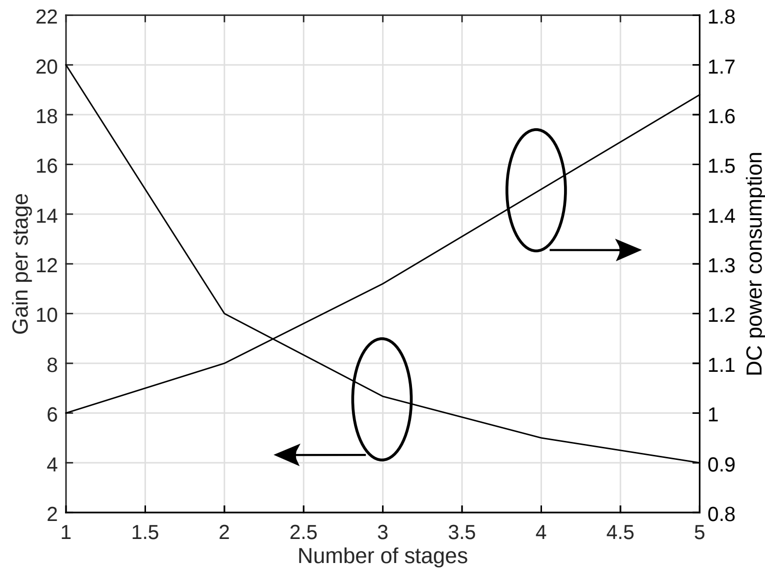

Figure 3.1: Gain required for each driving stage for a total gain of 20dB and the power consumption normalized to a one-stage amplifier in function of the number of stages.

From the definition of the efficiency η the power consumption of a multi-stage amplifier is given by equation 3.2.

$$P_{DC} = \sum_{i=1}^{n} \frac{P_{RFout}}{\eta_{stage} \cdot Gain_{stage}^{i-1}}$$

$$\text{with: n = number of stages} \tag{3.2}$$

Using this formula, the DC power consumption, normalized to a one stage amplifier, in function of the number of stages is also given in Fig.3.1. This demonstrates the direct relationship between the gain per driver stage and

the DC power consumption and subsequentially the efficiency η (is approximately equal to the PAE for a total gain of 20dB). A reasonable choice here would be two or three stages since this will alleviate the chip technology needed while the increase in DC power consumption is limited.

3.3 Amplifier class

A multitude of different amplifier classes exist which can roughly be divided into conventional mode PA's (Class-A, Class-AB, Class-B and Class-C) where the power transistor operates mainly in its linear region [3] and switch mode PA's (Class-D and Class-E) with some ambiguity about what kind of amplifier a Class-F amplifier might be. When moving to mm-wave frequencies, the realisation of switched mode PA's becomes troublesome if not impossible. Reason for this observation is that at mm-wave frequencies the transistor will not sweep fast enough through its linear region to behave like a switch [4] since the gain provided to the harmonics of the carrier frequency is minimal. At the lower side of the mm-wave spectrum Class-E amplifiers are possible if a high-speed chip technology is used ($f_t >$ 200GHz). Benefits of using a Class-E amplifier is the absorption of the parasitic output capacitance into the harmonic tuning and so called zero voltage switching (ZVS) which avoids switching losses. An extensive overview of the difficulties attributed to mm-wave Class-E amplifiers is given in [5] but one of the main issues is the peak collector voltage which goes up to 3.56 times the supply voltage V_{cc}. In fast chip technologies with low breakdown voltages this can prove to be troublesome.

For linear applications in the mm-wave domain the logical choice is a conventional mode PA. To have a better understanding of what happens when shifting from a Class-A towards Class-C, and thus decreasing the conduction angle, a plot of the harmonic current content is shown in Fig.3.2. Since the maximum output power P_{out} equals:

$$P_{out} = \frac{1}{2} \cdot V_{cc} \cdot I_{fund} \tag{3.3}$$

In equation 3.3 the factor V_{cc} is the supply voltage applied at the collector (drain) of the output transistor and I_{fund} is the fundamental of the collector (drain) current of the output transistor. From Fig.3.2 it becomes clear that the largest attainable output power will be achieved for a Class-AB amplifier. It also shows that in order to go towards Class-B and Class-C the second, third an even fourth harmonic content of the collector current needs to increase significantly. At mm-wave frequencies, the gain at these

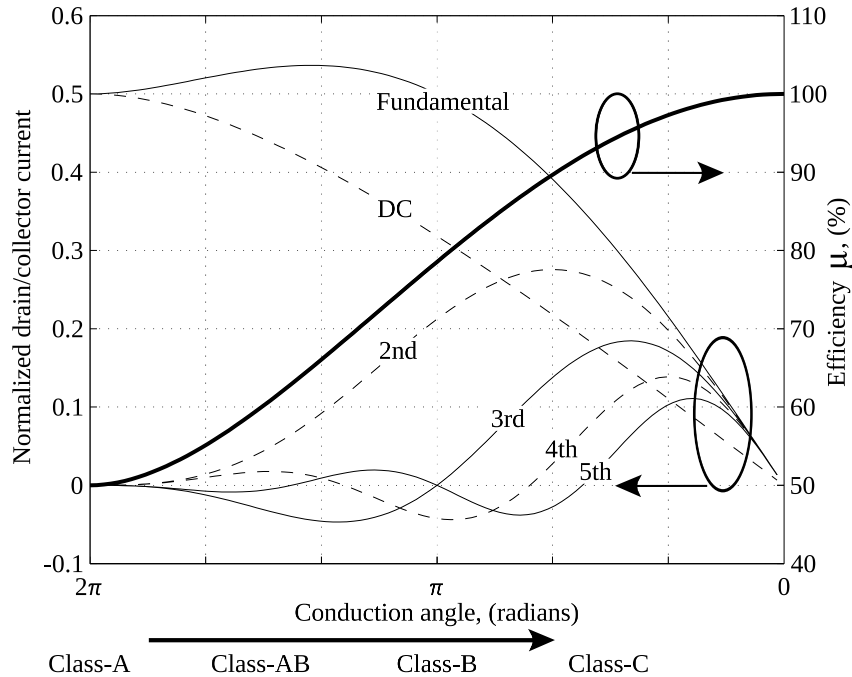

Figure 3.2: DC, fundamental and harmonic normalized drain/collector current for different conduction angles together with the efficiency (P_{out}/P_{DC}). Currents are normalized in respect to I_{max}.

harmonic frequencies is low (due to the proximity of f_t), as a result the drive level needs to increase and the gain of the output transistor drops. This will have a detrimental effect on the power added efficiency (PAE). For instance, to go from Class-A to Class-B the drive level will need to increase with 6dB [1], [4]. When taking this into account it is clear that Class-AB presents a sort of sweet spot for mm-wave amplifiers providing the largest output power with reasonable PAE and good linearity.

Between switching amplifiers and conventional mode amplifiers lies the Class-F amplifier which is actually an amplifier biased in Class-B with shorted even current harmonics and blocked odd current harmonics (except for the fundamental which is dissipated into the load). This leads to a switching behavior of the output voltage. This type of amplifier has the benefit that the highest possible output power can be achieved for a certain supply voltage namely $0.81 \cdot V_{cc}^2/R_L$ where the maximum output power of a Class-AB amplifier is approximately $0.5 \cdot V_{cc}^2/R_L$. A possible schematic to implement a mm-wave Class-F amplifier is shown in Fig.3.3.

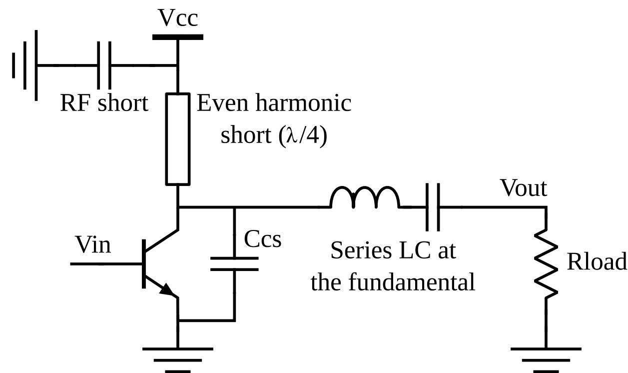

Figure 3.3: Basic circuit for implementing a Class-F power amplifier.

When implementing the circuit of a Class-F amplifier at mm-wave frequencies it becomes difficult to effectively block the odd harmonics due to the non-ideal series inductor and the parasitic output capacitance C_{CS} of the transistor. The ideal situation would be to have a combination of a Class-E and Class-F amplifier which provides [6]:

- Inclusion of the parasitic output capacitance
- ZVS to avoid current and voltage waveform overlap
- Low peak voltage (by appropriate harmonic tuning)
- Simple circuit implementation

Although it has been shown that certain of these hybrid Class PAs are possible at mm-wave frequencies by using an appropriate load network [7], the gain provided by a practical mm-wave implementation will in many cases kill the overall PAE.

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4

High power, high gain output stage

Next to creating a high output power at the output stage, it is required to have a high PAE as this will lead to lower DC power consumption and also lower chip temperature. Since the input power of an amplifier is factored into the PAE, this can only be achieved by having a high gain output stage [1]. Furthermore, higher gain also allows to go to a more efficient amplifier class like Class-B. This type of amplifier requires an increase in drive level of 6dB in comparison to a Class-A, which is only acceptable with sufficiently high gain at the PA carrier frequency, yielding the main reason why many millimeter-wave power amplifiers are biased in Class-AB [2], [3]. Moreover, a Class-A at millimeter-wave frequencies has a "soft" compressive characteristic (the output power compresses slowly with increasing input power) which leads to a back-off often larger than 10dB [4]. The cause of this phenomenon is the typically low output impedance of mm-wave PAs in silicon technologies which further decreases with increasing output voltage swings. Due to the continuous increase in f_T of SiGe BiCMOS technologies it stands to reason that it will become possible to create Class-B, Class-E, etc. type PAs for most millimeter-wave applications.

4.1 Cascode topology and transistor limitations

The output stage topology, chosen for this PA, is a differential cascode topology as shown in Fig.4.1. Although this type of topology needs more

headroom, and thus larger DC voltage, than a simple common emitter stage, it can achieve a higher output power and higher PAE. A self-shielded balun (see secton 4.5) is used for the differential to single-ended conversion.

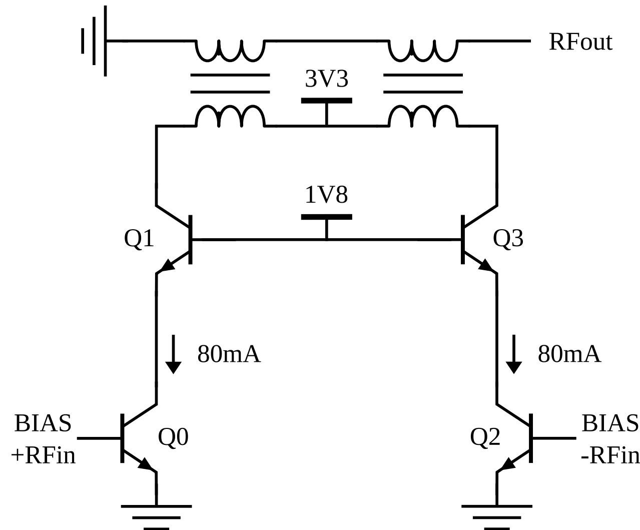

Figure 4.1: Differential cascode topology together with output balun.

Due to the common base stage and its biasing with a constant emitter current, the collector emitter voltage of this stage can be biased above BV_{CEO} as was discussed in section 2.1. This also allows to have a peak value for the time-varying collector emitter voltage that can approach the avalanche breakdown limit. The IHP 250nm SiGe BiCMOS technology used in the design of this output stage has a minimum BV_{CEO} of 2.1V and the minimum BV_{CBO} amounts to 6V. The common base output transistor is biased at a collector emitter voltage (V_{CE}) of 2.4V which is above the minimum BV_{CEO} but still safe due to the constant emitter current. Using a V_{CE} of 2.4V leads to a linear voltage swing of 3.8Vpp (with a saturation voltage of 0.5V and V_{BE} = 0.9V), while using a common emitter stage biased at a V_{CE} of 2V (considering a margin of 0.1V to be safely below BV_{CEO}) would lead to a linear swing of 3Vpp . In other words, the use of a cascode topology leads to a 2.05dB increase in linear output power while the DC power consumption goes up with a factor of 1.65 (2.17dB). It is important to note that a cascode won't be beneficial when using CMOS since their limiting factor is BV_{dg} which means that the output voltage swing won't increase in comparison to a common source stage while additional headroom needs to be created.

Although the efficiency η (P_{out}/P_{DC}) of a cascode is roughly the same as the efficiency of a common emitter stage, the PAE ((P_{out}-P_{in})/P_{DC}) is significantly better due to the larger gain of a cascoded topology which translates in a smaller required input power. In conclusion, using a cascode helps to overcome the BV_{CEO} limitation and thus achieve a higher output power. Additionally it leads to a higher gain and PAE than a simple common emitter stage.

4.2 Gain improvement using positive feedback

4.2.1 Cascode and Miller capacitance

The cascode topology is a popular option due to the suppression of the Miller capacitance at the input of the output stage and the resulting higher gain. This suppression is caused by the unity voltage gain of the common emitter transistors in a cascode configuration which leads to unity voltage gain between the collector and base of transistors Q0 and Q2 in Fig.4.1. Due to the lack of a significant voltage gain between collector and base, no feedback is present and the Miller effect is negligible.

Important to note is that the unity voltage gain comes from the input impedance of a common base transistor which is approximately 1/g_m, multiplied with the transconductance g_m of the common emitter transistor. However, it is well known that at high frequencies the input impedance of a common base transistor becomes inductive and thus will lead to a larger than one voltage gain and a return of the Miller capacitance. Hereafter it will be shown that the input impedance not only becomes inductive, but also increases with the voltage gain of the common base transistors.

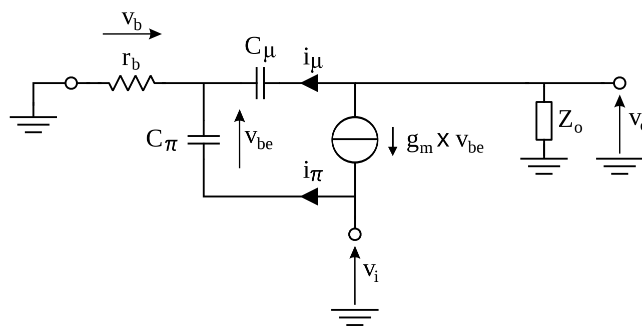

Figure 4.2: Small signal representation of the common base transistor in a cascode configuration with v_i the input voltage, v_o the output voltage and Z_o the load impedance of the cascode.

In order to calculate the input impedance of common base transistors Q1 and Q3 in Fig.4.1, the small signal model shown in Fig.4.2 is used. This is a simplified version of the complete bipolar small signal equivalent circuit [5]. The impedance Z_o is the resonant load impedance of the cascode output stage consisting of the balun inductance and the collector to substrate capacitance C_{CS}. The parasitic resistances r_μ and r_o (order of magnitude above 1kΩ) can be neglected at high frequencies in comparison to C_μ and Z_o (order of magnitude 10Ω - 100Ω). Resistances r_π, r_{ex} and r_c are left out for initial analysis but are reconsidered in the final formula describing the input impedance. The input impedance of the small signal equivalent of Fig.4.2 equals:

$$Z_{in} = \frac{v_i}{-g_m \cdot v_{be} + i_\pi}$$

With $v_{be} = -i_\pi / sC_\pi$ this leads to:

$$Z_{in} = \frac{v_i}{\dfrac{g_m \cdot i_\pi}{sC_\pi} + i_\pi} = \frac{v_i}{i_\pi \cdot \left(1 + \dfrac{g_m}{sC_\pi}\right)} \tag{4.1}$$

All that is left to do, is to solve i_π in function of v_i:

$$i_\pi = (v_i - v_b) \cdot sC_\pi \tag{4.2}$$

The term v_b in equation (4.2) can be written as:

$$\begin{aligned} v_b &= r_b \cdot (i_\pi + i_\mu) \\ &= r_b \cdot \left(i_\pi + \frac{v_o - v_b}{1/sC_\mu}\right) \\ &\dots \\ v_b &= \frac{v_o \cdot sC_\mu \cdot r_b + i_\pi \cdot r_b}{1 + sC_\mu \cdot r_b} \end{aligned} \tag{4.3}$$

When equation (4.2) and (4.3) are combined the following expression is

found for i_π:

$$
\begin{aligned}
i_\pi &= \left(v_i - \frac{v_o \cdot sC_\mu \cdot r_b}{1 + sC_\mu \cdot r_b} - \frac{i_\pi \cdot r_b}{1 + sC_\mu \cdot r_b}\right) \cdot sC_\pi \\
&\dots \\
i_\pi &= \frac{v_i \cdot sC_\pi \cdot \left(1 - \frac{v_o}{v_i} \cdot \frac{sC_\mu \cdot r_b}{1 + sC_\mu \cdot r_b}\right)}{\left(1 + \frac{sC_\pi \cdot r_b}{1 + sC_\mu \cdot r_b}\right)} \\
i_\pi &= \frac{v_i \cdot sC_\pi \cdot \left(1 - A_V \cdot \frac{sC_\mu \cdot r_b}{1 + sC_\mu \cdot r_b}\right)}{\left(1 + \frac{sC_\pi \cdot r_b}{1 + sC_\mu \cdot r_b}\right)} \qquad (4.4)
\end{aligned}
$$

In equation (4.4) the factor A_V is the voltage gain of the common base transistor. To attain a formula for the input impedance of the common base transistor equation (4.4) is put into equation (4.1) leading to the following result:

$$
Z_{in} = \frac{1 + s \cdot (C_\pi + C_\mu) \cdot r_b}{(g_m + sC_\pi) \cdot [1 + sC_\mu \cdot r_b \cdot (1 - A_V)]} \qquad (4.5)
$$

The formula for the input impedance shown in equation (4.5) is quite remarkable since it shows that the input impedance depends on the voltage gain A_V of the common base transistor and thus also on the impedance Z_o at the output of the cascode. Since this output impedance is a resonant load made up out of the balun inductance and the C_{CS} capacitance of the common base transistors, the input impedance of the common base will increase at exactly the frequency of interest for the output stage. This means that the Miller effect, and subsequentially the Miller capacitance, will be largest at the wanted frequency thus dampening the gain. Furthermore equation (4.5) shows that any parasitic resistance or inductance in series with r_b will result in a large increase in input impedance and Miller capacitance.

To get a more accurate description of the input impedance the resistances r_{ex} and r_c need to be included. With some lengthy calculus it can then be shown that the input impedance is given by:

$$
\begin{aligned}
Z_{in} = &\frac{1 + s\,(C_\pi + C_\mu) \cdot r_b + sC_\mu \cdot r_c\,[1 + r_b \cdot (g_m + sC_\pi)]}{(g_m + sC_\pi) \cdot [1 + sC_\mu \cdot r_c + sC_\mu \cdot r_b \cdot (1 - A_V)]} \\
&+ r_{ex} \cdot [1 + sC_\mu \cdot (r_b + r_c)] \qquad (4.6)
\end{aligned}
$$

To include the influence of the resistance r_π into formula (4.6), it suffices to replace the factor C_π with $(sC_\pi r_\pi + 1)/sr_\pi$. For mm-wave frequencies sC_π will typically be much higher than $1/r_\pi$ and r_π's influence can be neglected.

In DC, equation (4.6) results in the familiar result $Z_{in,DC} = 1/g_m + r_{ex}$. To prove that the previous analysis is accurate, the input impedance calculated by means of formula (4.6) is compared to the simulated input impedance of a common base in Fig.4.3 showing both the real and imaginary part of the input impedance.

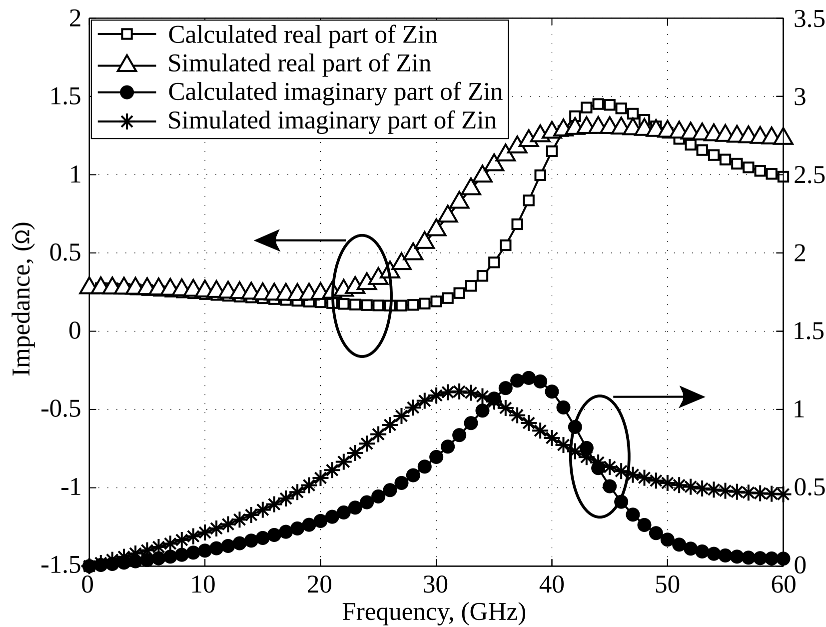

Figure 4.3: Calculated real and imaginary part of the input impedance of a common base transistor versus the simulated values.

Figure 4.3 shows that formula (4.6) is able to predict the behavior of the input impedance of a common base transistor at high frequencies. It also shows that the input impedance of a common base transistor increases at the resonant frequency of the output load and thus will have a larger input capacitance for the cascode at resonance due to the Miller effect. To counter the resulting drop in gain at resonance, positive feedback can be used as will be shown hereafter.

4.2.2 Feedback mechanism and gain improvement

By adding cross-coupled feedback capacitors C_F across the collector base junction of the common emitter transistors as shown in Fig.4.4 positive feedback is applied across the common emitter stage. The feedback in

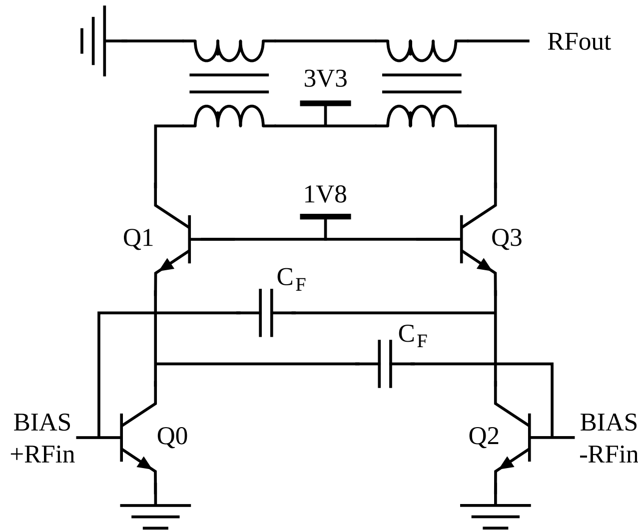

Figure 4.4: Differential cascode topology with cross-coupled feedback capacitors across the common emitter transistors.

Fig.4.4 compensates the input capacitance of the cascode with the negative capacitance provided by the cross-coupled capacitors multiplied by the voltage gain due to the Miller effect. The total capacitance at the input $C_{in,tot}$ is then given by the following formula [6]:

$$C_{in,tot} = C_{in} + (1 - |A_{V,CE}|) \cdot C_F \tag{4.7}$$

With C_{in} the input capacitance without feedback and $A_{V,CE}$ the voltage gain of the common emitter transistors. Equation (4.7) shows that the total input capacitance of the cascode can be decreased by adding the cross-coupled feedback capacitors.

By adding positive feedback an increase of 2dB in gain is achieved for the output stage biased in Class A which is shown in Fig.4.5. By choosing a larger feedback capacitor an even bigger increase in gain can be achieved, however, care has to be taken not to cause instability (negative $C_{in,tot}$ in equation (4.7)). Although an increase of a mere 2dB might not seem much, it quickly becomes significant when the output stage is biased more towards

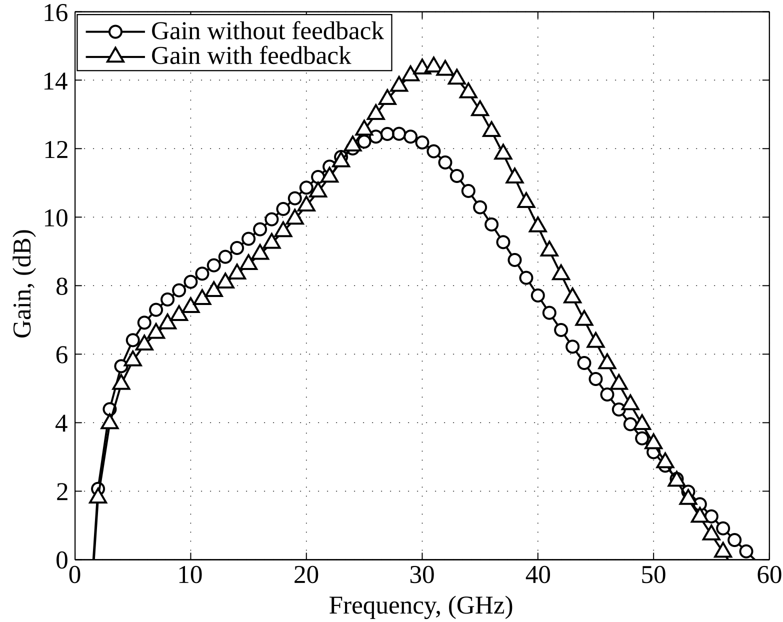

Figure 4.5: Gain of the differential cascode configuration with and without the cross-coupled feedback capacitors.

Class-B operation and the gain starts to drop. Moreover, in order to reduce the linearity and gain demands of the driving stage, a difference of 2dB will have a significant impact.

4.3 Stability considerations

Real-life transistors are potentially unstable due to feedback coming from parasitics in the small signal model (C_μ and r_μ in case of bipolar transistors in CE configuration). Operating transistors at mm-wave frequencies has the benefit that from a certain frequency onwards, depending on the configuration, the transistor will become unconditionally stable due to the limited speed of the device [7]. This frequency is known as the stability break point and defines the frequency at which the maximum stable gain (MSG) and the maximum available gain (MAG) separate. These curves and the corresponding stability break points are shown in Fig.4.6 for both a CE and cascode configuration. By using the plot shown in Fig.4.6 not only information about the stability is attained but also the possible gain at a certain frequency is given.

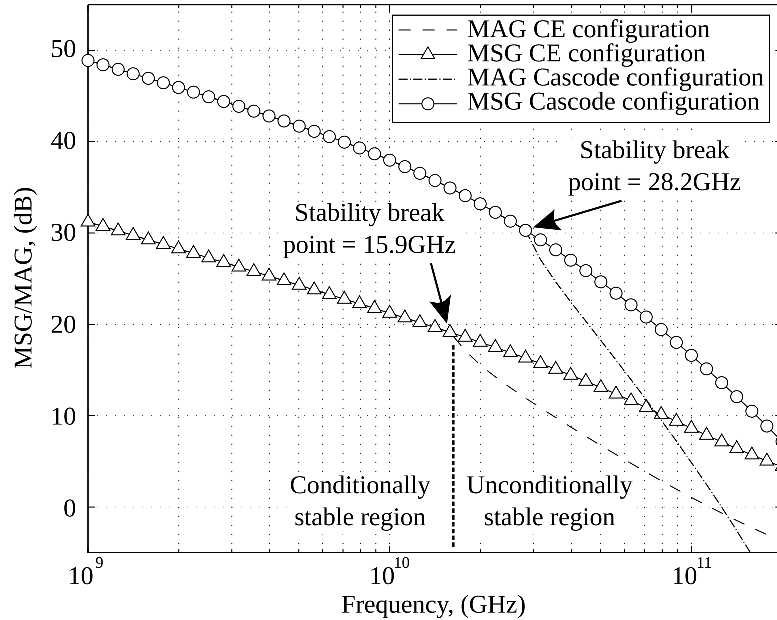

Figure 4.6: MSG and MAG curves for both a CE and cascode configuration together with their respective stability break points.

Fig.4.6 shows that using a CE configuration will pose no stability issues at Ka-band frequencies due to the limited speed of the technology used. When adapting a cascode, the output stage becomes potentially unstable for frequencies lower than 28.2GHz which is too close for comfort. Reason for this increase in stability break point lies with the addition of the CB stage which adds a second feedback path.

4.3.1 Differential stability

An important source of differential instability stems from the CB stage in the cascode topology. The transistors in this stage consist of several smaller transistors laid out as close to each other as possible to reduce inductance at the base due to the metal interconnects. This has as a result that there is a significant parasitic capacitance between the collector and emitter of the CB transistors caused by their interconnects. Since there is positive voltage amplification from emitter to collector, this capacitance provides positive feedback which can cause instability. This has been discussed in detail in [8] in which a cross-coupled capacitor is used as capacitive neutralization. However, this leads to a large shift in resonant frequency of the

output impedance Z_o. By using a series combination of a resistor R_{stab} and capacitor C_{stab}, as shown in Fig.4.7(a), stable operation is obtained with a smaller shift in resonant frequency.

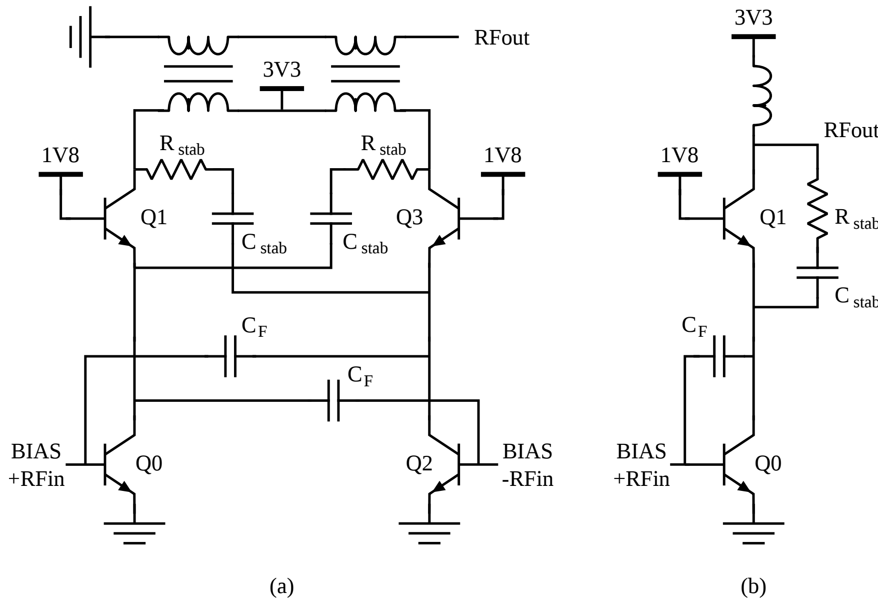

Figure 4.7: (a) Differential cascode topology with cross-coupled series resistor R_{stab} and capacitor C_{stab} across the common base transistors providing neutralization of the parasitic collector emitter capacitance. (b) Single-ended cascode topology used for analysis of common-mode stability.

Another potential source of instability is the cross-coupled capacitors C_F at the common emitter stage used to increase the gain. A too large capcacitor value will result in a negative input capacitance for the output stage (see formula (4.7)) and render the output stage instable. To verify the stability of the output stage over frequency for various C_F values the Edwards-Sinsky stability parameter μ [9] is shown in Fig.4.8. From Fig.4.8 it becomes clear that increasing the cross-coupled feedback capacitor at the common emitter stage will deteriorate stability as μ moves into a region of potential instability ($\mu < 1$) for values of C_F larger than 0.8pF. At the same time the rise in positive feedback increases gain as was discussed in 4.2.2 but it also shifts the peak gain frequency to higher frequencies. In this design a value of 620fF was used as a trade-off between gain improvement and stability. By using this value some margin is attained on the stability which allows to

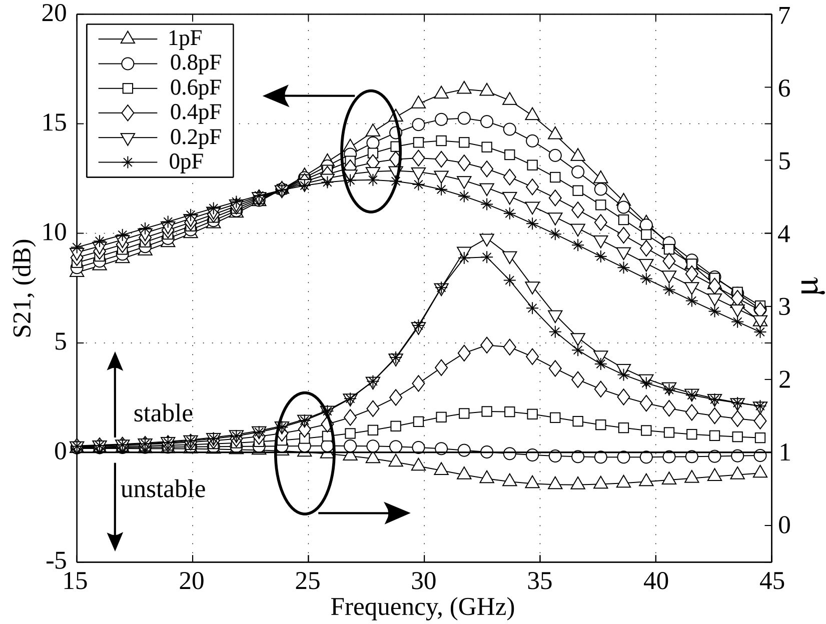

Figure 4.8: S21 and Edwards-Sinsky stability parameter μ in function of frequency for various values of C_F ranging from 0pF up to 1pF.

operate with stable behavior down to -40°C.

4.3.2 Common-mode stability

In order to reason on the common-mode stability of the output stage the output stage is converted into the single-ended topology shown in Fig.4.7(b). By adding the series resistor R_{stab} and capacitor C_{stab} between the collector and emitter of transistor Q1 the amount of positive feedback at the common base stage increases and the common-mode stability decreases. However the balun will provide a larger inductance at the CB stage collectors for common-mode signals (depending on balun coupling and symmetry) which will shift the gain peak to lower frequencies where the feedback through C_{stab} and R_{stab} has a lower impact. Additionally common-mode feedback at the CB stage is countered by capacitor C_F which will increase the stability of the cascode by supplying additional negative feedback at the common emitter stage.

4.4 Class-AB implementation and practical load line matching

4.4.1 Class-AB implementation

At the beginning of this section the choice for a Class-AB amplifier at mm-wave frequencies was explained. The textbook and practical implementation of a Class-AB amplifier is shown in Fig.(a) and (b) respectively. The explanation of Class-AB operation and calculation of the efficiency is based on the assumption that all harmonics are shorted to ground by the parallel LC tank. In the practical implementation this tank is made up out of the inductance of the DC-feed network (or balun when differential) and the device capacitance.

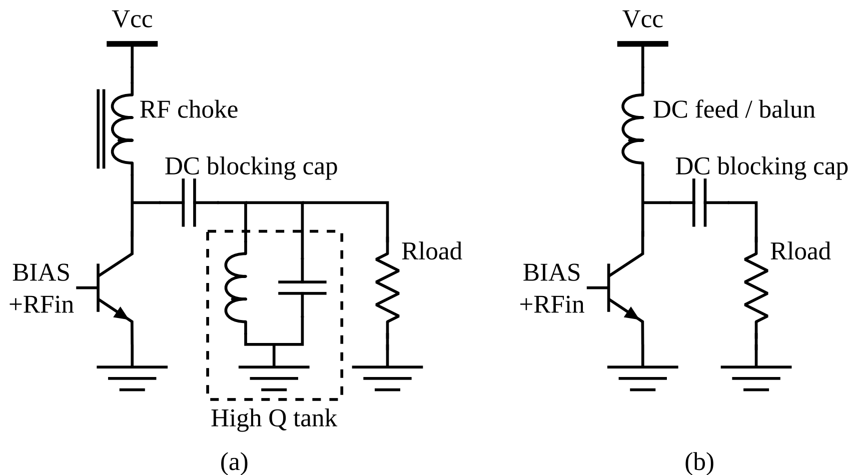

Figure 4.9: (a) Ideal (textbook) implementation of a Class-AB amplifier. (b) Practical implementation of Class-AB amplifier using transistor collector to substrate capacitance and DC feed / balun inductance to create harmonic shorting tank.

The problem when using the device capacitance to create the harmonic shorting tank is that the Q-factor of the tank is determined by the value of the device capacitance (a larger C will lead to a larger Q). A criterion for the size of this capacitance is the ratio of its capacitive reactance to the load-line resistance of the device at the fundamental frequency (X_{Ccs}/Rl). The smaller this value the easier it is to short the harmonics and to get closer to the ideal Class-AB operation. Ironically enough, when using a faster device technology at the same fundamental frequency, the breakdown volt-

ages drop (thus lowering Rl) and X_{Ccs} will increase which makes it harder to short the harmonics [10]. This can be seen in Fig.4.10 where the current and voltage waveforms for an ideal switching device with an X_{Ccs}/Rl of 0.14 and 1.4 are shown. Since the device dissipation consists of the integration of the product of collector (drain) current and voltage it is clear that the power consumption will increase with higher X_{Ccs}/Rl. The case where X_{Ccs}/Rl equals 1.4 corresponds to the output stage discussed here.

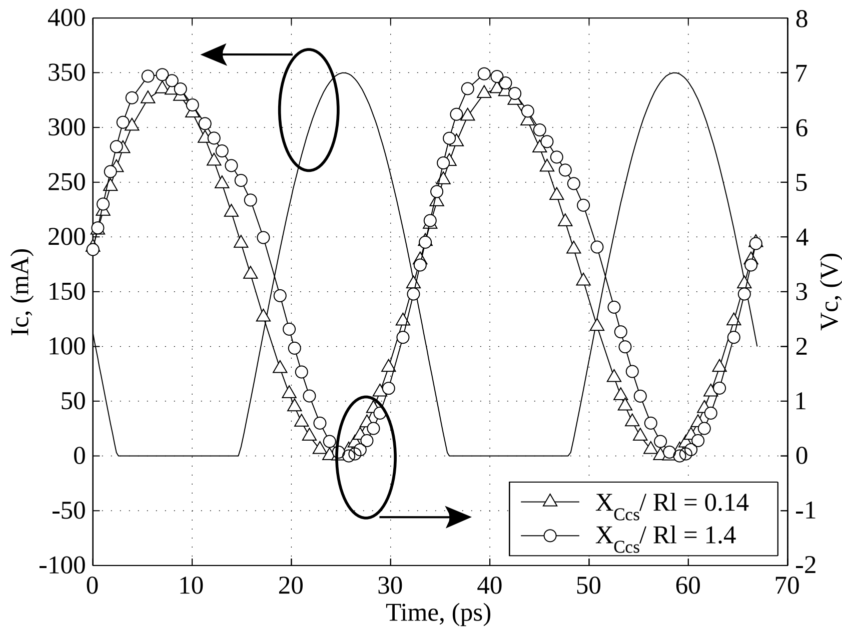

Figure 4.10: Transistor collector (drain) current and collector (drain) voltage waveforms for a Class-AB amplifier with an ideal switching device at an X_{Ccs}/Rl of 0.14 and 1.4.

It is important to remark that in the previous analysis an ideal switching device was used. An actual device will have a voltage dependent (and non-linear) output capacitance which will further lower the Q-factor of the tank which needs to short out harmonics. Moreover, it might seem from the previous analysis that using a slower technology might be beneficial. However, the ability to generate the current waveform as shown in Fig.4.10 must also be taken into account which will benefit greatly from a faster transistor. This, together with the drop in gain due to the larger input capacitance when going closer to the f_T and the lower breakdown voltages at higher nodes, means that there will be an optimal chip technology for designing a Class-AB amplifier which doesn't necessarily correspond to the fastest

available technology.

4.4.2 Load line matching

The ideal impedance to present at the output of a power transistor doesn't correspond to the conjugated output impedance of the transistor since this will in most cases not allow the maximum attainable output power and will thus lower the efficiency. Using a simplified analysis the optimal load R_l equals $(V_{DC} - V_k)/(I_{max}/2)$ with V_{DC} the supply voltage, V_k the knee voltage (output voltage at which the bipolar transistor is pinched off) and I_{max} the peak output current [3]. The output stage discussed further on has an optimal load impedance of 11.2Ω. The analysis leading to this optimal load impedance did not take into account that a bipolar is used which has an exponential I-V curve and non-linear in- and output capacitances. This leads to a strong second harmonic in the output current, however, the output voltage has a negligible second harmonic due to the self-resonance frequency of the balun primary which is located around the second harmonic.

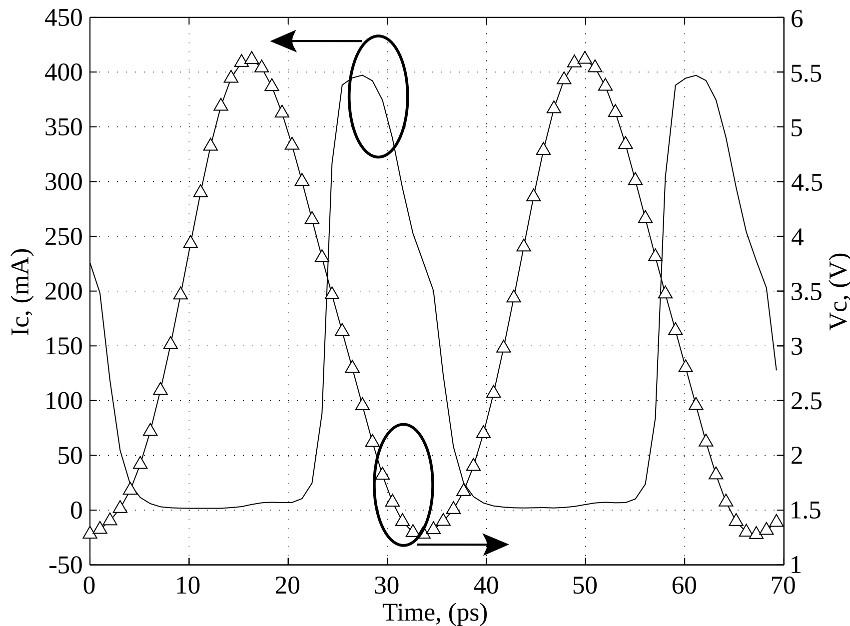

Figure 4.11: Transistor collector (drain) current and collector (drain) voltage waveform for the discussed output stage loaded with balun.

Since the output current and voltage aren't perfectly sinusoidal the optimal

load impedance will differ from the previous calculated value of 11.2Ω. The voltage and current waveform shown in Fig.4.11 resemble the waveforms found in a Class-J amplifier and similar to this type of amplifier a lower output impedance will be optimal [11]. Due to the absence of a fitting formula to determine the optimal load impedance an emperical method was used in this design. Firstly a balun with a turn ratio leading to an impedance corresponding to the classically calculated R_l was used. Subsequently the impedance at the output of the balun is altered until the maximum output power is reached. The voltage and current fundamentals at the output are then investigated and in this case led to an optimal load impedance of approximately 8.5Ω.

The area underneath the output voltage and current waveform in Fig.4.11 overlap more than the waveforms in Fig.4.10 which leads to a larger device dissipation. Since the output voltage has very little second harmonic content a capacitive harmonic termination at the output (as is done in Class-J amplifiers) won't give better results. Another option is the use of an advanced matching circuit at the input to shift the second harmonic content of the current and to decrease the DC power consumption.

Another important remark when looking at Fig.4.11 is that the knee voltage (roughly 1.3V) is already quite large in comparison to the peak output voltage attained (roughly 5.6V) which puts a severe limit on the attainable efficiency. This is caused by the use of a cascode and can be solved by using a common-base stage as was done in [2]. Using a common-base stage doesn't provide current amplification which means that a transformer will typically be used between amplifying stages which greatly increases chip size. However, when going to faster chip technologies with lower breakdown voltages, this might be the solution to get a high output power stage with good efficiency.

4.5 Self-shielded balun

In order to convert the differential output to a single-ended signal and to transform the 50Ω at the input of the power combiner to the optimum load impedance for the output stage, a self-shielded balun is used. This structure is implemented in the two thick top metal layers and is depicted in Fig.4.12.

The primary winding of this transformer is placed at the differential outputs and has a turn ratio of 0.77 and coupling factor of 0.71 which results in the desired single-ended load impedance. By using a wider primary winding, together with adding a parallel winding, not only the desired turn ratio is

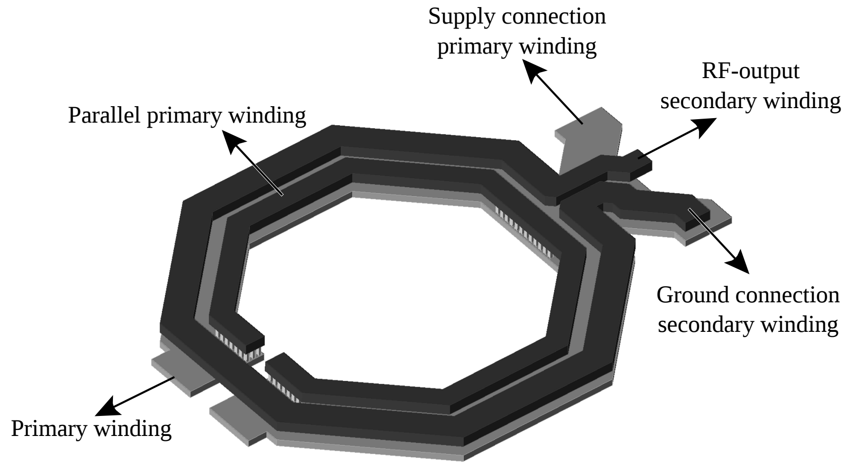

Figure 4.12: Structure of the self-shielded balun used at the output stage implemented in the top thick metal layers.

attained, the secondary is also shielded from the substrate by the primary which reduces the magnetic flux leakage [12]. Since the primary has a much lower voltage swing (simulations show a 5.5Vpp and 9Vpp signal at the primary and secondary winding respectively), it suffers less from energy coupling to the substrate. Additionally, by making the secondary winding narrower, the capacitive coupling with the primary is lowered which in turn lowers the amount of uneven voltage coupling between the primary and secondary winding and increases the symmetry of the balun. Simulation of the real part of the primary winding impedances show an impedance imbalance of 3.9% which results in the high symmetry needed to assure that both output transistors can achieve their maximum output power.

A plot of the primary and secondary inductance and their respective Q-factor in function of frequency is shown in Fig.4.13. This shows that both inductors still achieve reasonable Q-factors considering these are on-chip inductors. The Q-factor of the secondary is significantly lower than the Q-factor of the primary due to the narrower structure which increases series resistance. For both windings the maximum Q-factor is achieved around 30GHz.

Using the data of Fig.4.13 together with the coupling factor (0.71), the efficiency $\eta = P_{load}/P_{total,in}$ of the transformer can be calculated using the formula and equivalent transformer model presented in [13]:

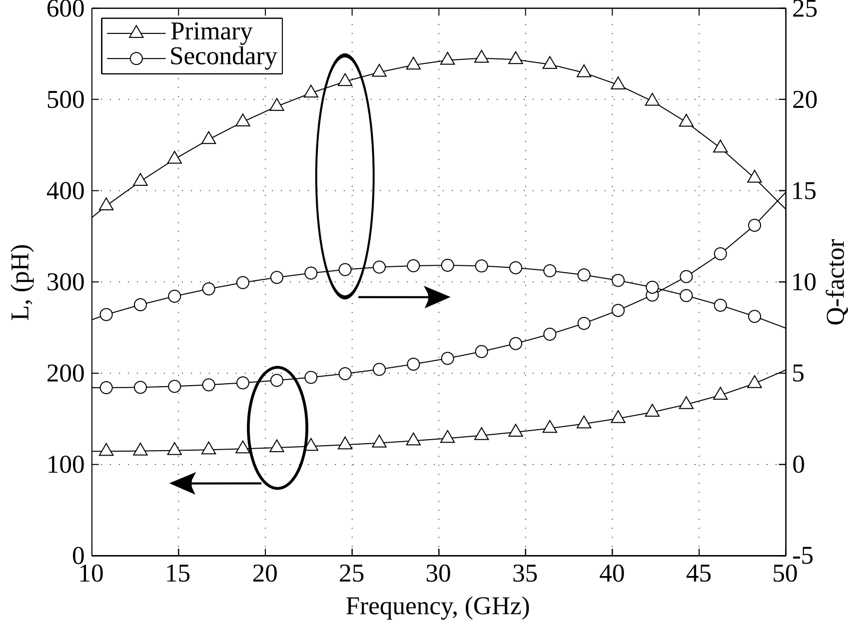

Figure 4.13: Primary and secondary inductance of the output stage balun with their respective Q-factor in function of frequency.

$$\eta = \frac{R_l/n^2}{\left(\frac{\omega L_1/Q_2 + R_l/n^2}{\omega k L_1}\right)^2 \cdot \frac{\omega L_1}{Q_1} + \frac{\omega L_1}{Q_2} + R_l/n^2} \tag{4.8}$$

Equation 4.8 calculates the efficiency to transport an input power to the load at the output in function of the load resistance R_l at the output of the balun, the winding ratio n, the primary and secondary inductance L_1, L_2 and their Q-factors Q_1, Q_2 and the coupling factor k. However, equation 4.8 assumes a series matching capacitor C_l at the secondary which resonates with the secondary inductance L_2 at the frequency of interest to attain maximal efficiency. This capacitor wasn't implemented at the balun output since an integrated series capacitor will lead to parasitic capacitance to the substrate and additional chip area needed. Reworking the original efficiency derivation found in [13] leads to the following formula excluding C_l:

$$
\begin{aligned}
\eta &= \frac{R_l'}{\left(\frac{(R_2'+R_l')^2+(\omega L_2/n^2-1/(n^2\omega C_l))^2}{(k\omega L_1)^2}\right) R_1 + R_2' + R_l'} \\
& \quad \text{with: } R_x' = \frac{R_x}{n^2} = \frac{\omega L_x}{n^2 Q_x},\ L_1 = \frac{L_2}{n^2} \text{ and } C_l = \infty \\
&= \frac{R_l/n^2}{\left(\frac{(\omega L_1/Q_2+R_l/n^2)^2+(\omega L_1)^2}{(\omega k L_1)^2}\right)\cdot \frac{\omega L_1}{Q_1} + \frac{\omega L_1}{Q_2} + R_l/n^2} \\
&= \frac{R_l/n^2}{\left(\frac{\omega L_1/Q_2+R_l/n^2}{\omega k L_1}\right)^2 \cdot \frac{\omega L_1}{Q_1} + \frac{(\omega L_1)^3}{Q_1} + \frac{\omega L_1}{Q_2} + R_l/n^2} \qquad (4.9)
\end{aligned}
$$

When comparing formula 4.9 to 4.8 an additional factor is added to the numerator when leaving out C_l which will lower the transformer efficiency. In equation 4.9 it is also shown that a high Q-factor for the primary will nullify the effect of leaving out the series matching resistor C_l at the output. In Fig.4.14 the efficiency of a balun to transfer energy from the primary winding to the secondary for both the case with and withoud series matching capacitor is shown. These efficiencies are calculated using formulas 4.9 and 4.8 with a 50Ω load and the data of the balun as shown in Fig.4.13.

By removing the series matching capacitor at the balun's secondary the efficiency at 30GHz drops from 83.3% to 78.5% (or -0.26dB). As the primary has a large Q-factor the decrease in efficiency by omitting C_l is rather small. When adding a series matching capacitor in the actual design, simulations show a negligible increase in output power of 0.09dBm. This rather small increase is due to the previously mentioned parasitic capacitances to substrate added by a series capacitor at the secondary.

4.6 Output stage layout

The layout of the output stage is depicted in Fig.4.15 and clearly shows that the largest portion of the layout area is taken by the self-shielded balun. In order to minimize the length of the traces of the output transistors (CB stage) to the balun, the output transistors are layouted close together. The transistors which constitute the CE stage can be separated more which allows to place the cross-coupled capacitors between the differential CE transistors. This also helps to lower inter transistor heat exchange (see Section: 2.4).

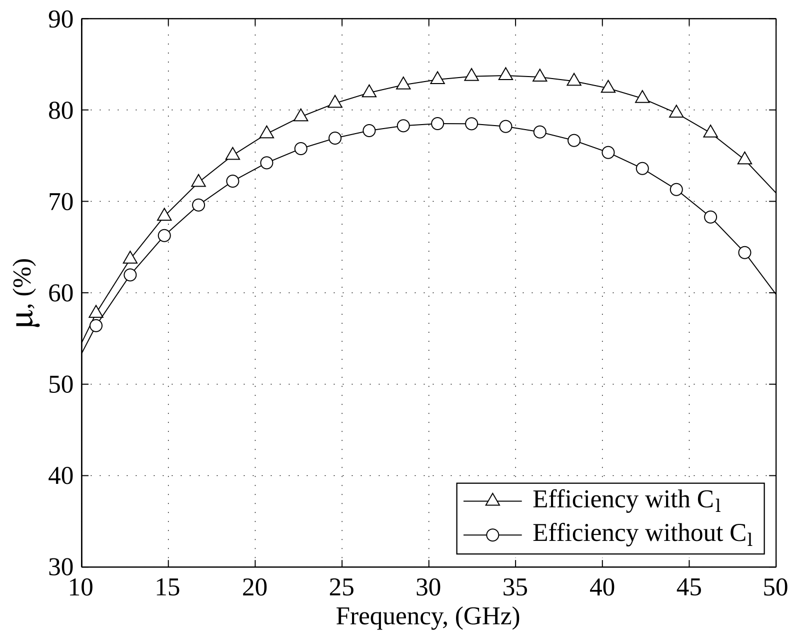

Figure 4.14: Efficiency of the output stage balun with and without series matching capacitor C_l at the load.

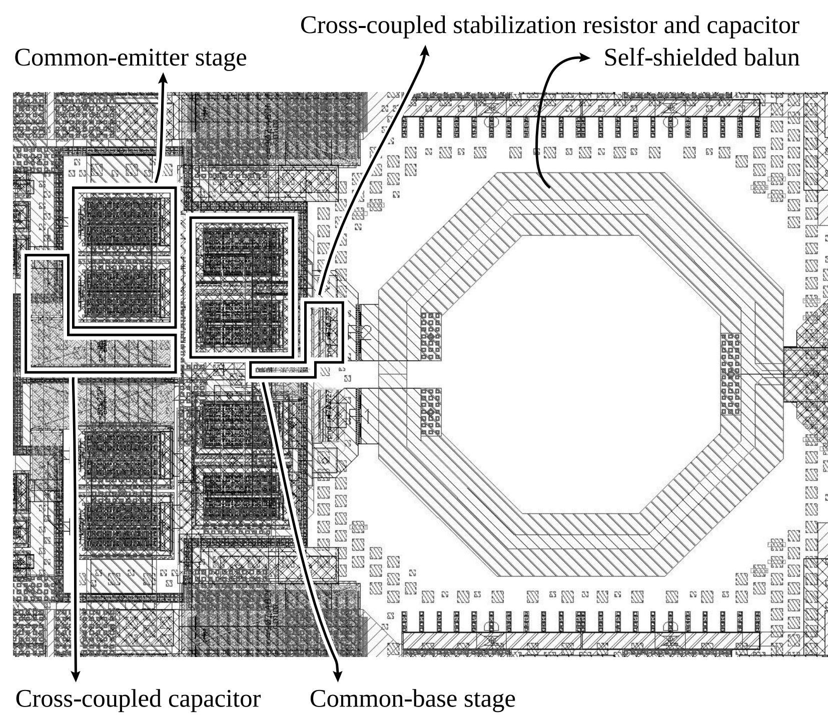

Figure 4.15: Layout of the output stage together with the self-shielded balun.

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5
Driver/biasing stage

The function of the driver/biasing stage is to provide stable and more or less temperature independent biasing while at the same time provide a drive signal to the output stage. Additionally, it needs to provide a sufficiently high drive level too push the output stage into power saturation. Moreover, to make sure that the PAE of the overall PA isn't excessively deteriorated by the driver stage, it's necessary that the driver stage provides a reasonable gain while using a fraction of the output stage DC power consumption. In this chapter a compact broadband driver stage using translinear loops, as used in this PA, is presented. The operation of translinear loops is analyzed in section 5.1 while the schematic and operation of the actually used driver stage is given in section 5.2. The stability of the driver stage during both normal operation and start-up is discussed in section 5.3.

5.1 Translinear loop biasing

The driver/biasing stage is responsible for the Class AB operation of the output stage which comes down to biasing the output stage at a certain quiescent current independent of supply voltage and temperature. At the same time it can't put a hard limit on the maximum output current of the output stage as is the case when using a tail current source to bias the output stage. A convenient way of realizing this is by means of a translinear loop [1]. By using a translinear loop it becomes possible to create a linear relationship

in the currents of different devices by using their non-linear voltage current characteristic [2]. One example of a translinear loop, which is also used in the driver/biasing stage, is shown in Fig.5.1.

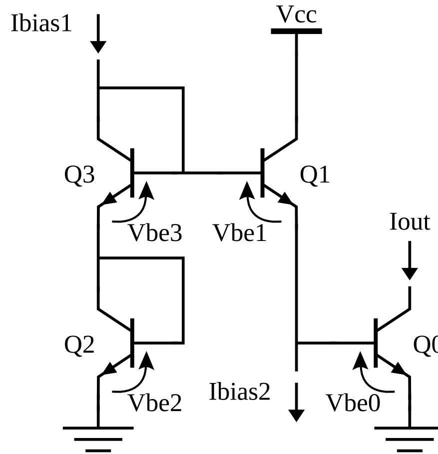

Figure 5.1: Translinear loop with bipolar transistors used to control the current of Q0.

Transistor Q0 in Fig.5.1 is the transistor of which the quiescent current Iout needs to be set and corresponds to the common emitter transistor of the output stage. By using the exponential relationship between the collector current I_C and the base-emitter voltage V_{BE} in a bipolar transistor, the relation between the different transistor collector currents can be calculated:

$$\begin{aligned} V_{BE,0} + V_{BE,1} &= V_{BE,2} + V_{BE,3} \\ &\quad \text{with: } I_C = I_S \cdot e^{\frac{V_{BE}}{V_T}} \\ V_T \cdot \left[ln\left(\frac{I_{C,0}}{I_{S,0}}\right) + ln\left(\frac{I_{C,1}}{I_{S,1}}\right) \right] &= V_T \cdot \left[ln\left(\frac{I_{C,2}}{I_{S,2}}\right) + ln\left(\frac{I_{C,3}}{I_{S,3}}\right) \right] \\ \frac{I_{C,0}}{I_{S,0}} \cdot \frac{I_{C,1}}{I_{S,1}} &= \frac{I_{C,2}}{I_{S,2}} \cdot \frac{I_{C,3}}{I_{S,3}} \end{aligned} \tag{5.1}$$

The current reverse saturation current I_S in formula 5.1 is a constant for a certain transistor and scales linearly with the transistor's size. In Fig.5.1 $I_{C,2} \approx I_{C,3} \approx I_{bias1}$ and $I_{C,1} \approx I_{bias2}$. When the same type of transistor is used for both Q_2 and Q_3 the collector current I_{out} of Q_0 can be written as:

$$I_{out} = \frac{I_{S,0} \cdot I_{S,1}}{I_{S,2} \cdot I_{S,3}} \cdot \frac{I_{bias1}^2}{I_{bias2}} \tag{5.2}$$

Often when using a translinear loop the biasing currents I_{bias1} and I_{bias2} originate from the same reference current I_{ref} which results in a linear relationship between this reference current and I_{out}.

5.1.1 Thermally stable biasing

From formula (5.2) it follows that the current relationship is temperature independent as the temperature dependence of I_S for the different transistors cancel each other out. However, the non-infinite thermal conductivity of the silicon substrate and self-heating of the transistors will lead to variations of the quiescent current. This change can lead to potentially dangerous situations. If the base-emitter voltage of Q_0 is assumed to be constant, the collector current will increase with higher temperatures [3]. An increase in collector current will in its turn lead to a higher power dissipation and temperature and will lead to thermal runaway. The reason this biasing scheme does provide stable biasing is that I_{bias2} doesn't equal $I_{C,1}$, as is assumed to get to formula (5.2), due to the presence of the base current of Q_0. The negative temperature coefficient of the current gain (β) will increase $V_{BE,1}$ for higher temperatures of Q_0 and provide negative feedback to $V_{BE,0}$. Potential thermal instability is still possible with this biasing when transistor Q_0 consists of several parallel transistors, as is the case with power amplifiers. A single hotter transistor will then be able to draw even more DC current although the total base current of transistor Q_0 is kept constant [4]. This can be avoided by making sure all parallel transistors reach similar temperatures by layouting them as close to each other as possible. Another option is to add a small series base resistance to the different parallel transistors, however, this will in many cases deteriorate RF behavior.

Another dangerous situation may arise when Q_1 is in close proximity of transistor Q_0. An increase in temperature of Q_0 will then lead to heating of Q_1 which will lead to Q_1 delivering additional current to the base of Q_0 and thus nullifying the earlier discussed negative feedback due to the negative temperature coefficient of β. This is avoided in the designed driver/biasing stage by placing Q_2 and Q_3 closer to Q_0 than Q_1. A second measure is to place the bipolar transistor Q_4 which supplies I_{bias2} close to Q_0 which will lower the base current in case Q_0 heats up.

5.2 Compact driver stage

The driver/biasing stage of this PA is based on the linearizing bias circuit proposed in [5]. Possible implementations of this driver/biasing stage are shown in Fig.5.2(a) and (b). In both these versions, transistors Q_0 and Q_B constitute a single-ended (SE) version of the output stage while transistors Q_1 to Q_4 make up the actual driver/biasing stage. The biasing of the output stage is realized by means of the translinear loop consisting of transistors Q_0 to Q_3 which allows to minimize the added capacitance to the base of transistor Q_0. Gain of the driving stage is provided by transistor Q_4 which has a CE configuration. The version in Fig.5.2(b) is more compact than the original schematic on the left due to the absence of the inductance and coupling capacitor. Moreover the biasing current source that is providing I_{bias2} has been replaced by Q_4 (biasing of this transistor is discussed further on).

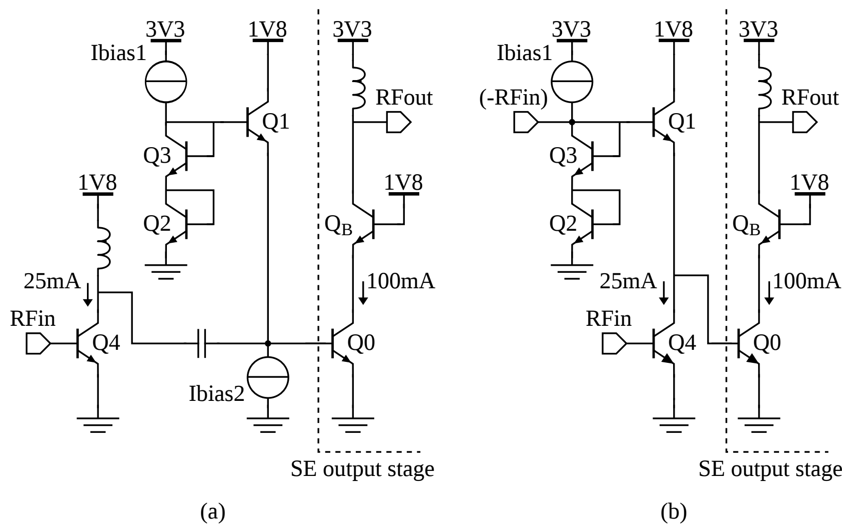

Figure 5.2: Biasing and driving of a single-ended (SE) output stage by means of a translinear loop (Q_0 to Q_3) using a coupled CE drive stage (a) and a compact version where the CE drive stage replaces I_{bias2} (b).

By removing the inductance not only a lot of chip area opens up, the driver stage also becomes broadband which helps to avoid a drop in gain due to difference in resonance frequency between the driver and output stage. However, the gain of transistor Q_4 is lower in this configuration due to the lower collector-emitter voltage. This drop in gain can be solved by applying a negative version of the input signal at the base of Q_1. The simulated

power gain and output power of the different versions of the driver stage are shown in Fig.5.3. Compact driver stage A and B in Fig.5.3 correspond to the compact driver stage without and with the negative input signal applied to the base of Q_1 respectively. The absolute values shown in Fig.5.3 don't take into account the presence of a non-ideal balun and the gain improvement of the output stage due to the cross-coupled capacitors as was discussed in chapter 4. However, it does show that by applying a negative version of the input signal RF_{in} at the base of Q_1 roughly the same amount of gain and maximum output power can be achieved as with the initial non-compact driver stage.

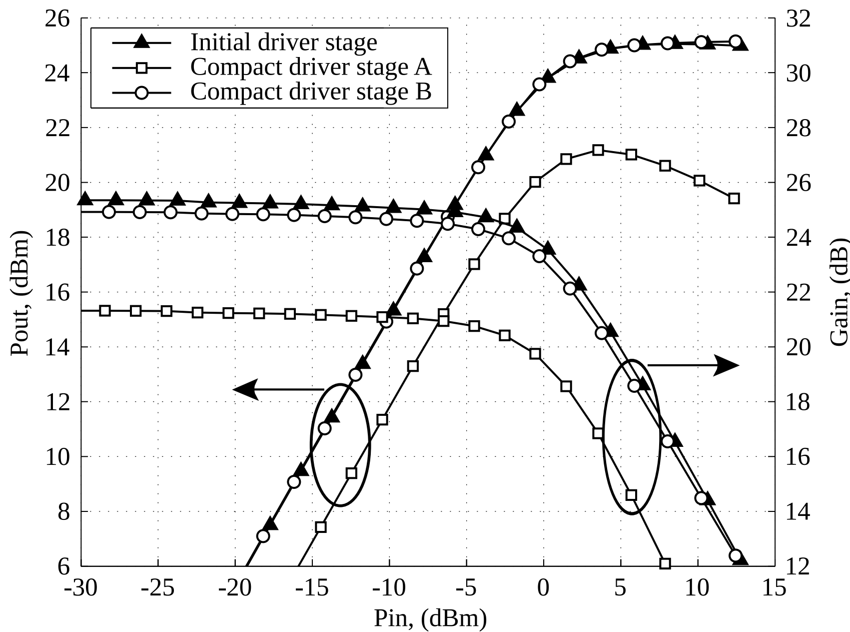

Figure 5.3: Simulated power gain and output power of the combination of the initial and compact version of the driver stage with the single-ended output stage.

When looking at the schematic shown in Fig.5.2(b) two problems arise: transistor Q_4 needs to be biased and a negative version of the signal RF_{in} needs to be supplied to the base of transistor Q_1. Both these problems are addressed by the schematic shown in Fig.5.4. A second translinear loop, consisting of transistors Q_4 to Q_7, is used in this schematic in order to bias and drive transistor Q_4. The combination of resistor R_1 and capacitor C_0 at the collector of Q_5 provides an inverted version of the signal at the input of the driver stage to the base of Q_1 which provides the increase as

previously discussed. Resistor R_0 is used to bias transistor Q_5 instead of a current source (as is normally done with a translinear loop) as a current source does not allow voltage gain from the base of Q_5 to its collector. When neglecting the biasing currents I_{bias1} and I_{bias2}, this driver/biasing stage has a power consumption amounting to 19.9% of the output stage power consumption. Furthermore the 3V3 supply used for the driver stage is completely separated from the 3V3 used for the output stage to avoid unwanted feedback through the supply lines.

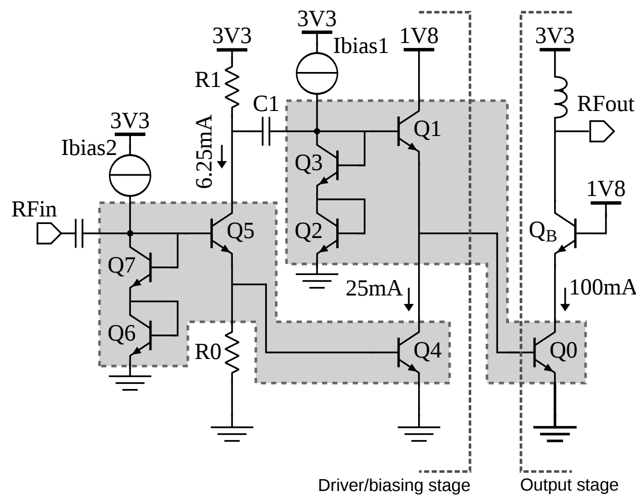

Figure 5.4: Schematic of the driver/biasing stage incorporating two translinear loops which provide biasing and drive the output stage.

5.3 Biasing and stability

Biasing of the driver stage is done by means of biasing currents I_{bias1} and I_{bias2}. Due to resistor R_0, the current through transistor Q_5 is more or less constant at 6.25mA while the current through transistors Q_1 and Q_4 varies with I_{bias2} as can be seen in Fig.5.5. The biasing of transistors Q_1 and Q_4 to Q_7 is largely independent of biasing current I_{bias1} which determines the bias current of the output stage. Since the biasing of the output stage is dependent on both biasing currents the biasing sequence is to first bias the driver stage (by increasing I_{bias2}) and secondly increase I_{bias1} until the wanted biasing point for the output stage is attained. By tuning I_{bias1} the class of the PA can be shifted from Class-A to Class-C.

Simulation showed that the driver stage is stable for all frequencies at nor-

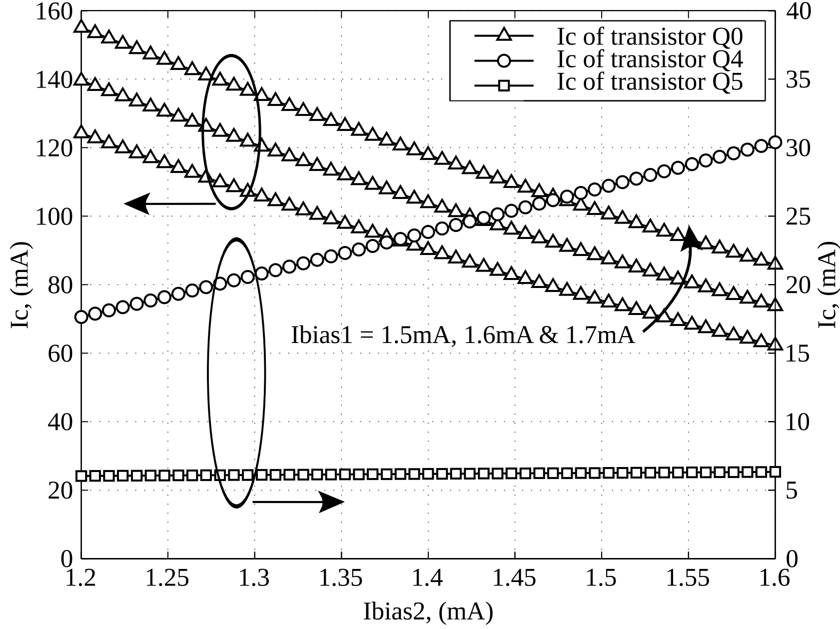

Figure 5.5: Biasing current of transistors Q_0, Q_4 and Q_5 in Fig.5.4 in function of biasing current I_{bias2} for different values of I_{bias1}.

mal biasing points (Class-A to deep Class-AB) with the most unstable behavior at roughly 30GHz. Since the driver stage is single-ended there is no need for a separate differential and common mode stability analysis as was the case for the output driver. It is also checked that the amplifier will remain stable throughout all biasing settings encountered during start-up. This is shown in Fig.5.6 where the Edwards-Sinsky stability factor μ is shown in function of biasing current I_{bias2} for various values of I_{bias1}.

As can be seen in Fig.5.6 the driver circuit is unconditionally stable for I_{bias2} current values above 0.3mA. At lower values the driver circuit is only unconditionally stable with zero I_{bias1} current. This is compatible with the start-up procedure since I_{bias2} is first increased to its nominal values which is roughly 1.4mA while I_{bias1} is kept at zero, subsequentially I_{bias1} is increased to bias the output stage.

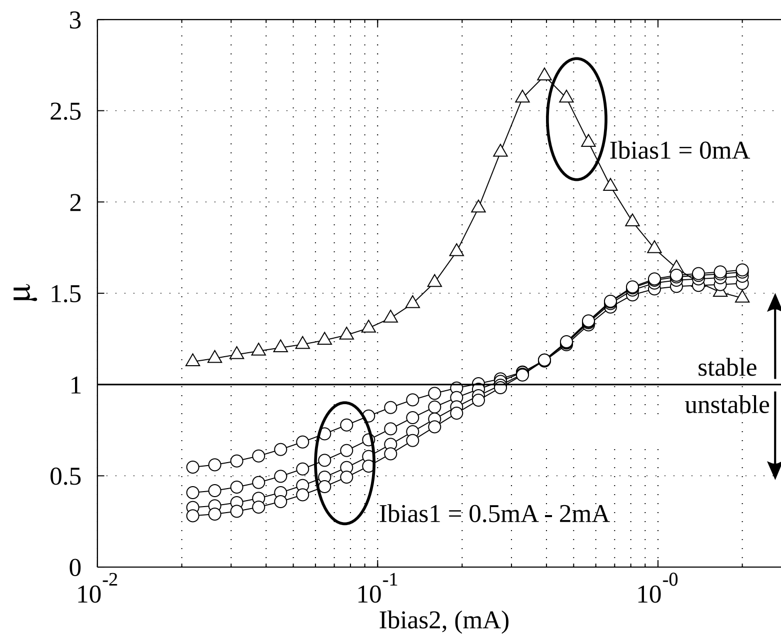

Figure 5.6: Simulated stability factor μ (Edwards-Sinsky stability factor) at 30GHz in function of biasing current I_{bias2} for various values of I_{bias1}.

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6 Pre-driver stage and power combination/distribution

In order to create an output power that is many times larger than the power available from a single transistor, power combination is needed. Furthermore, from a single RF input pin the input signal must be distributed to the different amplifiers of the PA. This PA is designed to be compatible with commercial amplifiers and thus has a single-ended input which means that a single-ended to differential circuit needs to be added.

6.1 Power combination/distribution

A distributed active-transformer (DAT) of which it has been shown that high output power levels can be achieved is a popular configuration to combine different amplifiers. A DAT performs the function of both power combiner and balun and a large amount of power transistors can have their power effectively combined [1], [2]. In a DAT the secondary winding is shared with all other amplifiers while each amplifier has two primary windings connected to the opposite output of the neighbouring amplifiers as shown in Fig.6.1.

While the circular DAT is able to realize low loss impedance transformation and power combination, the circular structure also poses some problems. The first one has to do with the distribution of the input signal to the

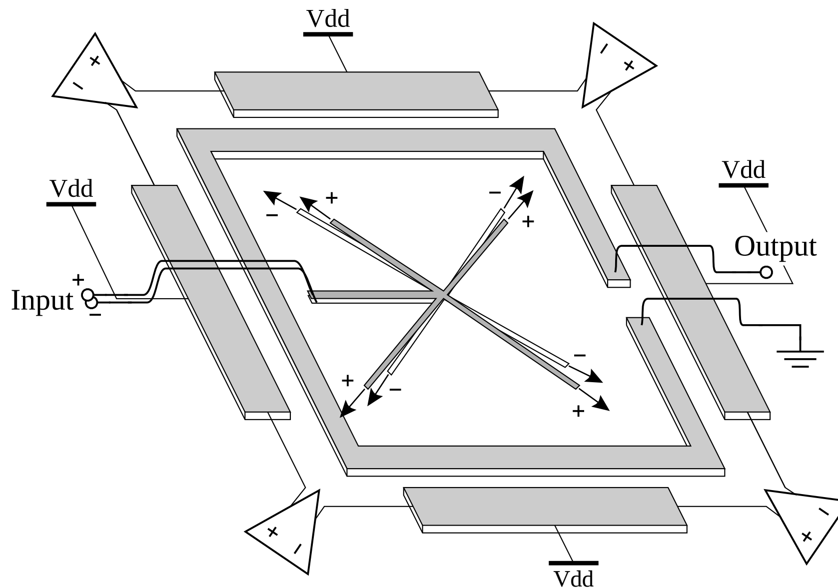

Figure 6.1: Distributed active-transformer with four amplifiers. A star-type interconnection in the middle of the PA provides distribution of the amplifier input signals.

differential amplifiers which is done from the middle of the DAT. This has the disadvantage that the input feed-lines will cross the actual DAT which, due to feed-line coupling, can lead to asymmetry of the inputs and even amplifier instability caused by positive feedback [3]. The circular structure of a DAT also has the disadvantage that the gates of the power transistors used for the differential pairs have a different direction which leads to poor immunity to process variations. By using a tournament-shaped power-combiner as shown in [4] these problems can be addressed. However, both these solutions have the disadvantage that the impedance transformation is fixed to a certain discrete value dictated by the number of amplifiers which may not correspond to the optimum impedance-transformation for a single amplifier. By using the four-way self-shielded power combining balun as described in [5] and [6], both a large number of amplifiers can have their output power combined and the impedance transformation can be changed by adapting the winding ratio. However, this solution becomes hard to route when using more than two amplifiers due to the differential inputs and output of the power combining transformer.

In this PA design, the strategy of divide and conquer is used with the balun tackling the problem of the impedance-transformation and differential to

single-ended conversion and the power combiner (with 50Ω in- and outputs) providing on-chip power combination. This also makes it easy to scale the PA when a higher output power is needed by simply doubling the number of amplifiers and adding an additional power combination stage. On the other hand, as each power-combiner adds a certain amount of loss and chip area, the viability of this solution depends strongly on the design of a low-loss compact on-chip power combiner. An overview of the power combination and distribution in the designed PA is shown in Fig.6.2.

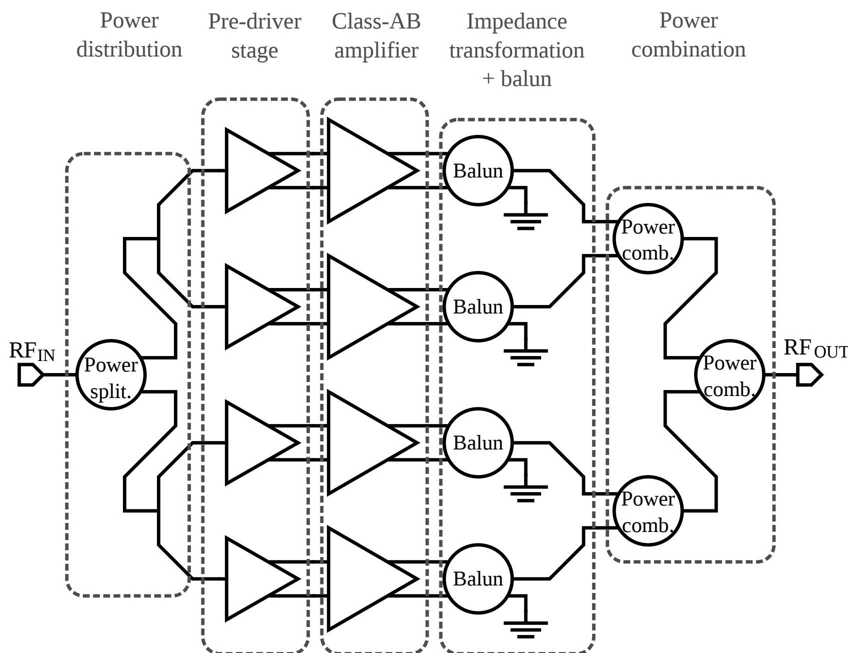

Figure 6.2: Overview of the power distribution and power combination network used in this PA.

As shown in Fig.6.2 the single-ended to differential conversion of each separate amplifier is done by the pre-driver stage. Additionally there is only one power splitter stage at the input to save chip area. The 50Ω transmission line coming from the initial power splitter is divided into two 100Ω transmission lines which are connected to the high-impedant pre-driver stage inputs.

6.2 Pre-driver stage

The pre-driver stage has two functions, namely providing single-ended to differential conversion and adding some extra gain. Since this stage is added at the very beginning of the amplifier, care needs to be taken that this stage has a better linearity than the following stages to prevent early compression of the PA. Furthermore, the ground and supply connection of this stage are separate from the rest of the PA to avoid positive feedback from the output and driver stage to the pre-driver stage. The used schematic is a degenerated common-emitter stage with differential outputs taken from the collector and emitter as shown in Fig.6.3.

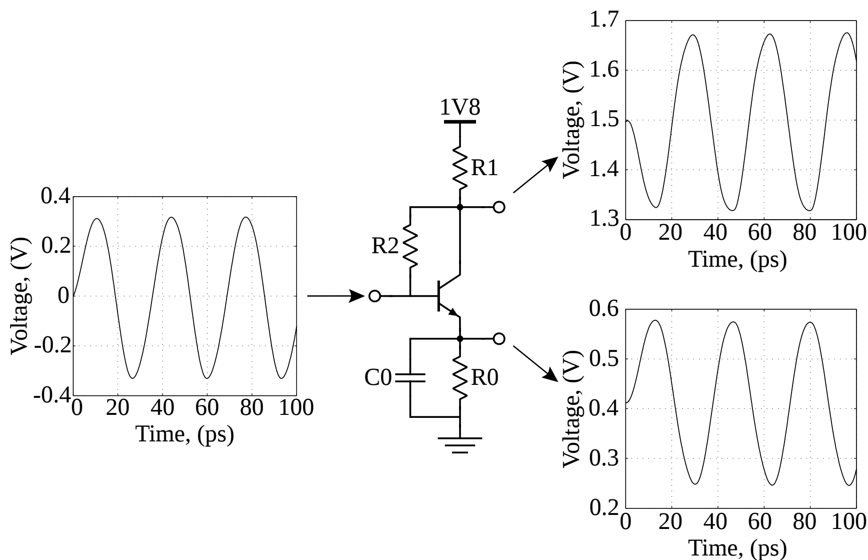

Figure 6.3: Pre-driver stage circuit used to convert the single-ended input to two differential output signals together with the corresponding simulated in- and output voltage waveforms.

In comparison to the degenerated common-emitter stage described in [7], this version uses resistive loads instead of inductors to save chip area. Additionally the use of resistors makes it easier to predict the gain at both the collector and emitter. Resistor R_2 is used to bias the transistor while capacitor C_0 will tune the phase difference between collector and emitter to exactly 180 degrees. Although the peak-to-peak voltage of the output waveforms is smaller than the peak-to-peak voltage at the input, power gain is provided since the input is high-impedant, while the input of the driver

stage is low-impedant.

Since the different junction capacitances of a transistor are voltage dependent, the phase and magnitude difference between the differential outputs of the pre-driver stage will change with increasing input voltages. As a result a pre-driver stage with perfectly balanced differential outputs at small input levels will have significant magnitude and phase imbalance at the high input levels associated with the saturated output power. In this design the resistors and capacitors in Fig.6.3 were chosen to optimize the saturated output power. This can be seen in Fig.6.4 which shows that the magnitude and phase imbalance come close to zero at saturation of the output stage output power.

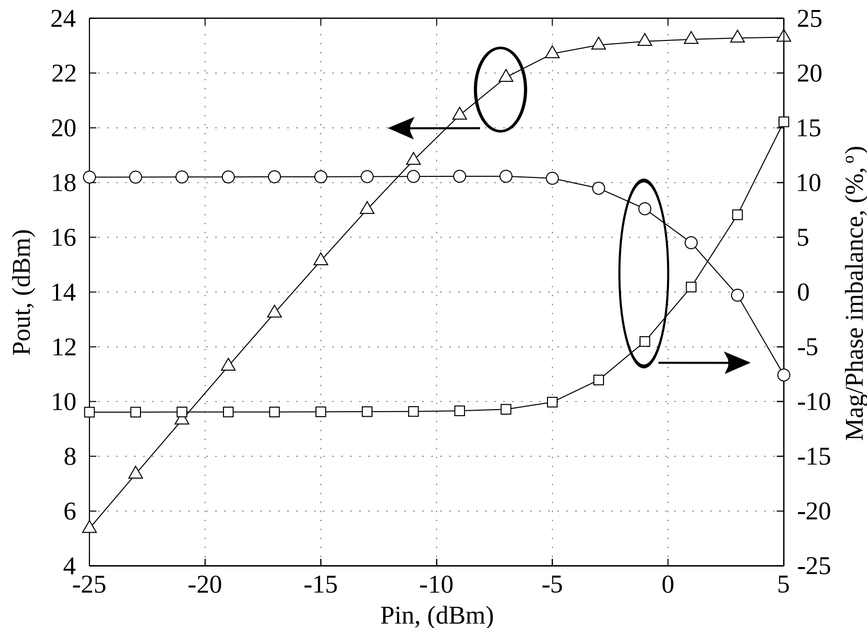

Figure 6.4: Output power at the output stage and voltage magnitude and phase imbalance at the output of the pre-driver stage as a function of the pre-driver stage input power.

6.3 On-chip power combiner/splitter

An ideal on-chip power combiner is broadband in order not to add bandwidth limitations, is compact to minimize the chip area and has high iso-

lation and low loss. In this work a transformer-type Wilkinson combiner previously used for CATV power splitters [8] is integrated on-chip to cope with these requirements. The power combiner circuit is shown in Figure 6.5 together with the matching section needed for this type of combiner.

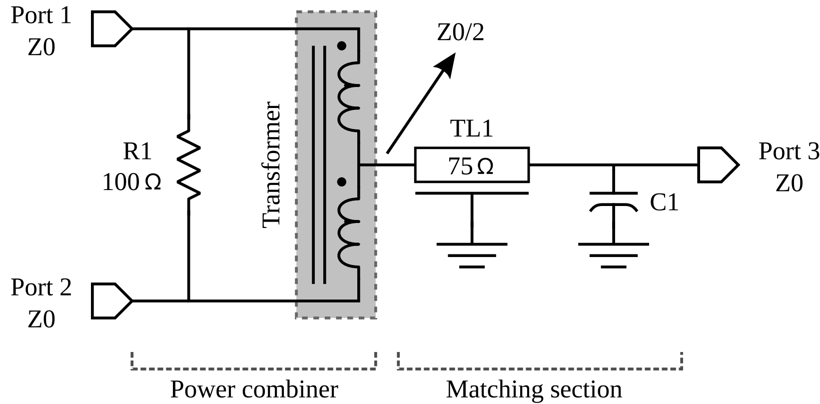

Figure 6.5: Schematic of the implemented power combiner together with matching circuit.

6.3.1 Impedances and isolation

The impedances expected at the different ports of this type of power combiner can be calculated based on Figure 6.6. Following equations apply for the voltages:

$$\begin{aligned} V3 &= V1 - Vt \\ V3 &= V2 + Vt \\ &\text{If } V1 = V2 \text{ then } Vt = 0 \\ V3 &= V1 = V2 \end{aligned} \tag{6.1}$$

When the inputs are in-phase, no current flows through resistor R1 and logically current I3 amounts to the sum of current I1 and current I2. This together with the equal voltages at all ports means that the impedance at port 3 equals half the impedance at ports 1 and 2.

Due to the half impedance at port 3 a matching section is necessary. In comparison to [9] a matching section consisting of a transmission line TL_1, with characteristic impedance of 75Ω and 80μm long (corresponding to 0.051 wavelength at 30GHz), and a capacitor C_1 with a value of 80fF is

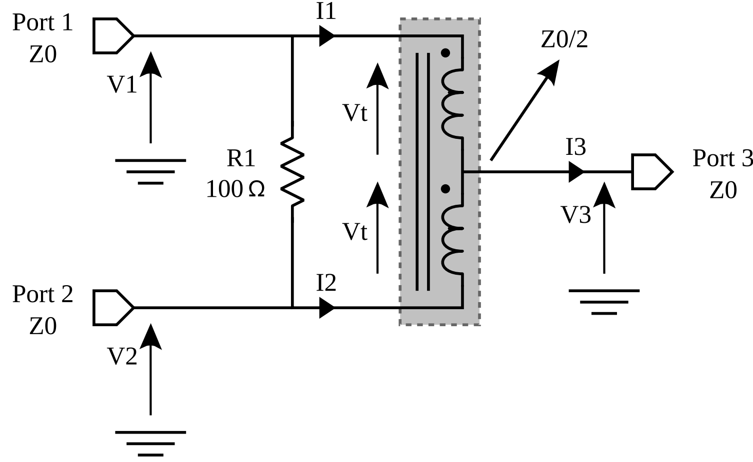

Figure 6.6: Core circuit of the implemented power combiner with associated voltages and currents.

used instead of a second transformer in order to reduce power loss. The length of the transmission line is short enough to incorporate in the RF interconnections between the different on-chip power combiners while the capacitor used for matching can be replaced partially or completely by the bondpad and ESD capacitance, allowing to compensate for their detrimental effect on RF performance. This power combiner is designed for a characteristic impedance Z_0 of 50Ω which means that resistor R_1 needs a value of 100Ω to maximize isolation. This can be seen by considering Figure 6.7.

When applying an error voltage Ve between input ports 1 and 2 in Figure 6.7 the current through isolation resistor R1 amounts to Ve/100. Due to the transformer action and in case of perfect coupling the following applies:

$$\begin{aligned} I2 &= I1 \\ &= \frac{V1 + \frac{Ve}{2}}{50} \\ &= \frac{V1}{50} + \frac{Ve}{100} \end{aligned} \tag{6.2}$$

The error current through resistor R1 will not flow towards port 2 due to the transformer action and the resulting current I2 (see equation 6.2) which results in perfect isolation. It should be noted that this is only valid in case of perfect coupling. So, in order to achieve good isolation and cancel out asymmetrical currents, the used transformer will need good coupling at the

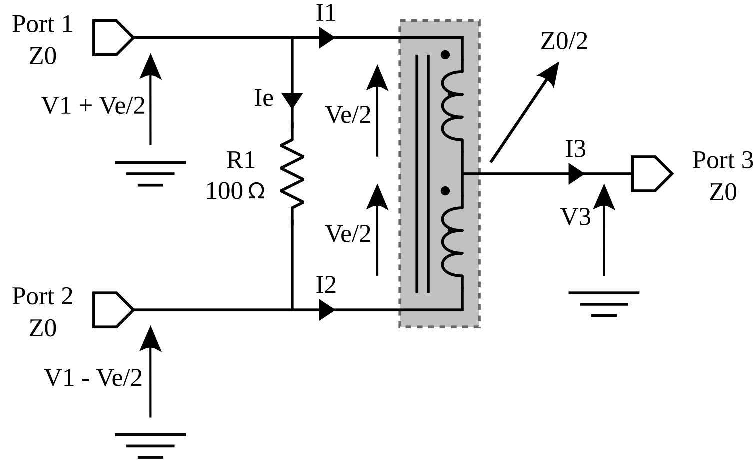

Figure 6.7: Core circuit of the implemented power combiner with associated voltages and currents in case of an error voltage Ve between ports 1 and 2.

frequencies of interest. On the other hand, the bandwidth of this circuit is not limited by a resonance so this is an inherently broadband device [10].

6.3.2 Layout and simulation

The power combiner layout is shown in Fig.6.8 and is almost completely symmetrical with the transformer occupying most of the area.

At the input ports the transformer starts on top metal 2 going down to top metal 1 and metal 3 to go back up again to top metal 2 at the combiner output leading to one-and-a-half turn. The half turn on top metal 1 is wider than the half turns on top metal 2 and metal 3 in order to reduce interwinding capacitance. EM-simulation of this transformer reveal a primary and secondary inductance of 141pH with a coupling coefficient k of 0.71. The 100Ω resistor placed in between the inputs needs to be wide enough to withstand considerable currents through this resistor due to possible voltage imbalance at the inputs (e.g. 1V imbalance will cause a current of 10mA flowing through this resistor) but small enough to limit parasitic capacitance added to the input ports. The outer metal structure shown in Fig.6.8 consists of metals 1 up to 3 and provides ground interconnection between the power combiner in- and output transmission lines.

The simulated S-parameters of the designed on-chip power combiner are shown in Fig.6.9. This demonstrates broadband behavior with the reflection

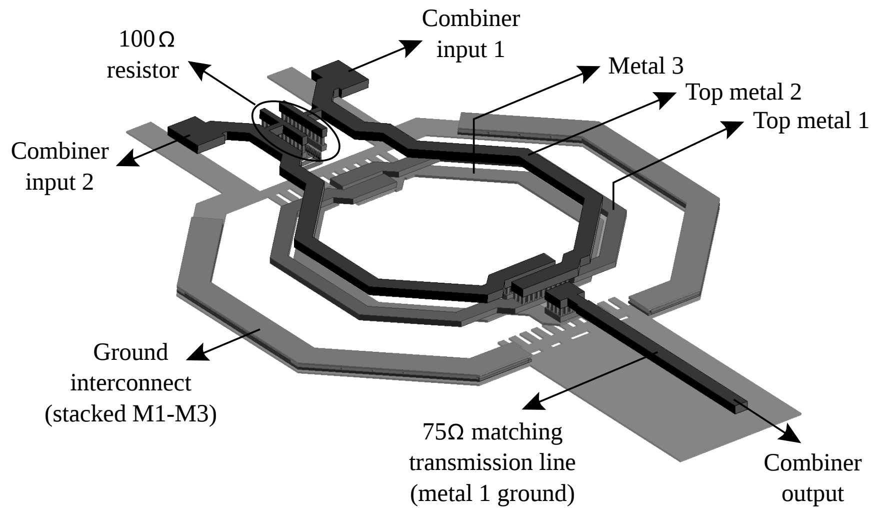

Figure 6.8: 3D structure of the power combiner implemented on the metal 3, top metal 1 and top metal 2 layer together with the 75Ω transmission line needed for matching.

coefficient of all ports below -10dB for frequencies up to roughly 47GHz. Also the transfer characteristics, S31 and S32, are very broadband with a bandwidth up to approximately 65GHz. The design of the transformer used in the power combiner has been optimized to deliver the largest isolation around the Ka-band with a dip around 33GHz.

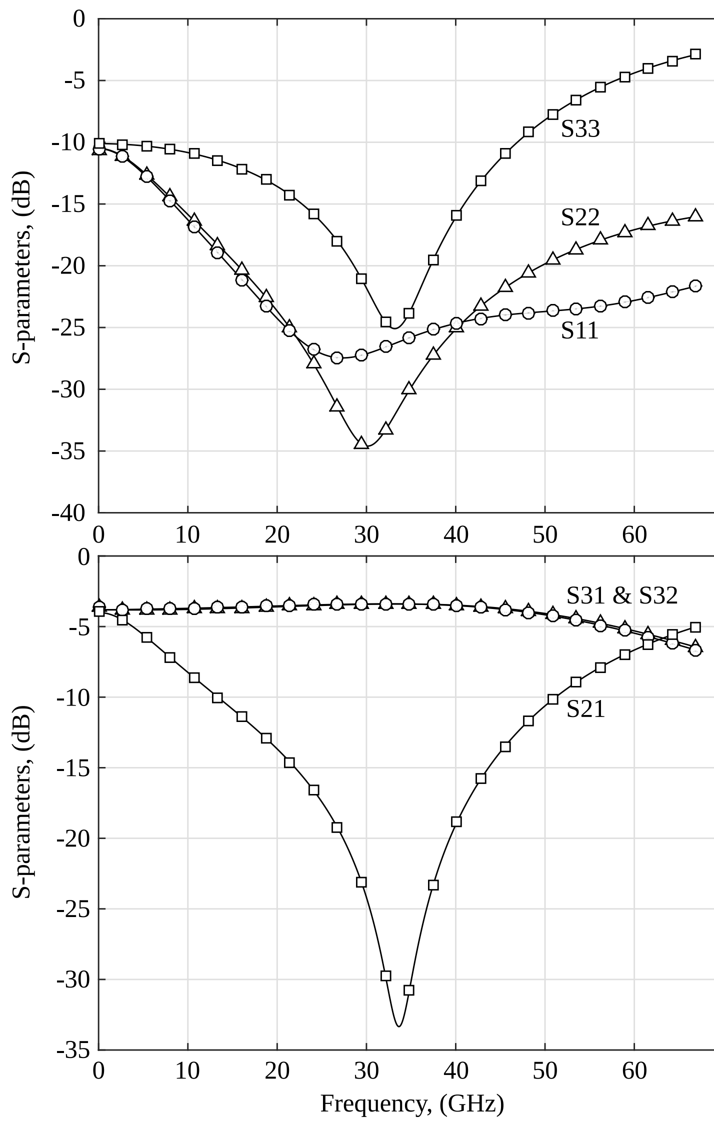

Figure 6.9: Simulated S-parameters up to 67GHz for the on-chip power combiner.

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7

Top-level chip considerations and board layout

Next to the considerations made regarding the design of the different power amplifier stages and the power combination and distribution network, some thought also needs to be spent on the chip top-level. This includes the organization of the power supply as well as the integration of an appropriate ESD solution. Together with the four-way power combining PA additional teststructures are placed on the die to verify the correct operation of certain subblocks, e.g., the on-chip power combiner. Once the chip produced, a testboard is designed which allows to measure the performance of the chip while taking into account the optimal thermal connection of the chip to a heatsink.

7.1 Power supply organization

The PA has two different supply voltages: 1.8V and 3.3V. Both these voltages are used at the output and driver stage and 1.8V is also used as a supply for the pre-driver stage. To avoid unwanted feedback loops through the supply and ground lines which might cause instability, a differential amplifier topology is adopted [1]. Additionally some supply/ground domains are split up and provided with separate bond pads. Following measures have been taken to avert supply/ground feedback:

- The power supply of the output stage is provided through the balun and is connected to a separate 3.3V supply line.
- The 1.8V for the output stage is connected to the 1.8V supply line by means of a series resistor (20Ω) with extra decoupling capacitors (≈12pF) at the output stage. This acts as a low-pass filter which suppresses feedback originating from the double carrier frequency (the carrier frequency isn't present due to the differential output stage).
- The ground and supply of the pre-driver stage are supplied separately from the rest of the chip circuitry since feedback at this stage is most likely to cause instability due to the high gain from the pre-driver stage to the output stage.

An overview of the power and ground domains and their connection to the different PA amplifying stages is depicted in Fig.7.1. All power domains remain separate on the chip and thus need separate bondpads and ESD power clamps. The 3V3_1, 3V3_2 and 1V8_1 supply are individually decoupled to GND_1 at each amplifier stage and at the corresponding bondpad while the 1V8_2 supply is decoupled to GND_2. Since ground GND_1 is shared by both the driver and output stage this ground is implemented as a ground plane on the metal 1, metal 3 and top metal 2 layer. Although GND_2 is depicted as a separate ground in Fig.7.1, which means that it has a separate interconnection, it is still connected to GND_1 through the chip substrate.

7.2 ESD solution

ESD protection devices are added to the PA supply, bias and ground lines to safely discard electrostatic discharges during handling and testing of the PA. Due to the presence of a balun at the different amplifier outputs and a coupling capacitor at the pre-driver stage input, the RF pads of the chip don't need ESD protection. This presents a large advantage since designing robust ESD devices with low added capacitance (high impedance in comparison to 50Ω at mm-wave frequencies) is challenging [2].

An overview of the implemented ESD protection is shown in Fig.7.2. It is important to note here is that the two different grounds are connected together through the silicon substrate (and are also shorted on the testboard) which allows to leave out ESD diodes connecting the ground planes. All power supplies have a power clamp to ground with input ESD diodes protecting the biasing pins.

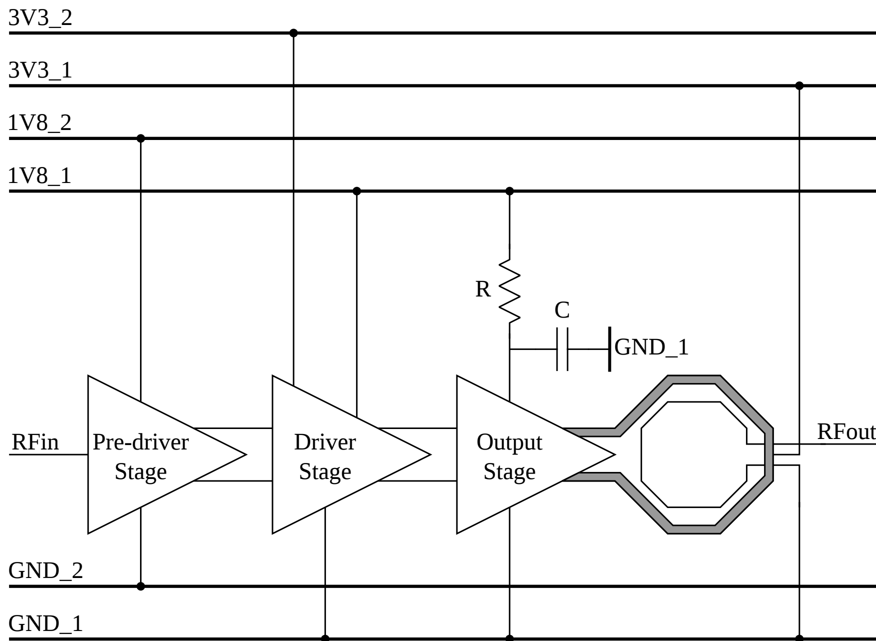

Figure 7.1: Different power and ground domains with their connections to the different PA amplifier stages.

7.3 Chip layout

Next to the four-way power combining PA, test structures are placed on the chip. These allow to measure the performance of separate components. Both a single amplifier and a power combiner test structure are added to the die. The PA with test structures amounts to a chip area of 1670μm times 1490μm or 2.49mm^2 of which a photomicrograph is shown in Fig.7.3.

Clearly visible in Fig.7.3 are the four parallel amplifiers with their respective balun and the power combination and distribution network. Biasing of the chip is done by means of an external bias resistor (to avoid change in bias due to temperature change) and an externally generated bias voltage. Since the PA is biased by means of two bias currents (see Chapter 5) a total of four biasing bondpads is needed. For the 3V3_1 supply four bondpads are used (two on each side of the four-way power combined PA) to maximize the number of parallel bondwires since the largest current will be drawn from this power domain. All the other power supplies have two bondpads to their disposal. To create a low impedant on-chip ground,

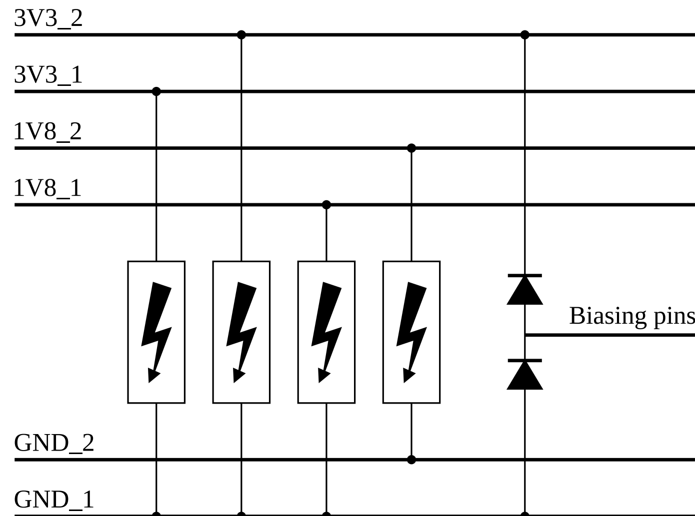

Figure 7.2: Different power and ground domains together with the power clamps protecting the power supplies and the input diodes protecting the biasing pins.

multiple ground bondpads are provided (14 are bonded when the chip was mounted for probing).

Two teststructures were added to the chip namely a single amplifier (shown in the top right corner of Fig.7.3) and a single power combiner (bottom right corner of Fig.7.3). The single amplifier can be separately biased and gets its supply from the same supply pins as the four-way power combined PA. The power combiner can be probed by means of a ground-signal-ground-signal-ground (GSGSG) probe at the input and a GSG probe at the output both with a 125μm pitch.

7.4 Board layout and PA wirebonding

Testing of the designed PA requires a testboard of which the layout is shown in Fig.7.4. Underneath the testboard a brass pedestal is placed which acts as a heatsink as was shown in Fig. 2.6(a). At the position of the PA die a cavity is foreseen in the board which allows the die to be soldered directly to the brass heatsink for optimal thermal performance. Since the board and chip have approximately the same thickness ($\approx$300μm), the bondwires connecting the chip to the board can be made short (less than 500μm). A picture of the complete testboard, including heatsink and soldered PA is

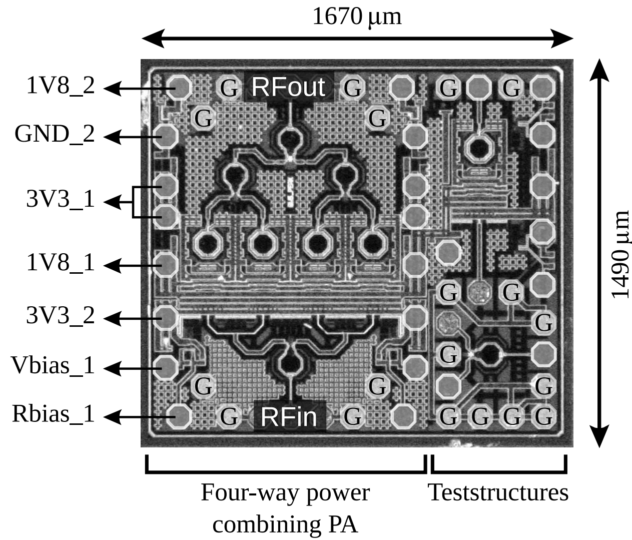

Figure 7.3: Photomicrograph of the four-way power combining PA together with teststructures. The GND_1 bondpads are denoted with the letter G.

shown in Fig.7.5. This testboard allows both testing of the performance by mounting connectors to the left and right of the board or by directly probing the PA.

The decoupling capacitors are placed as close as possible to the chip as can be seen in Fig.7.4 as are the biasing resistors. Two biasing resistors are needed to choose the two currents which determine the power consumption in the output and driving stage.

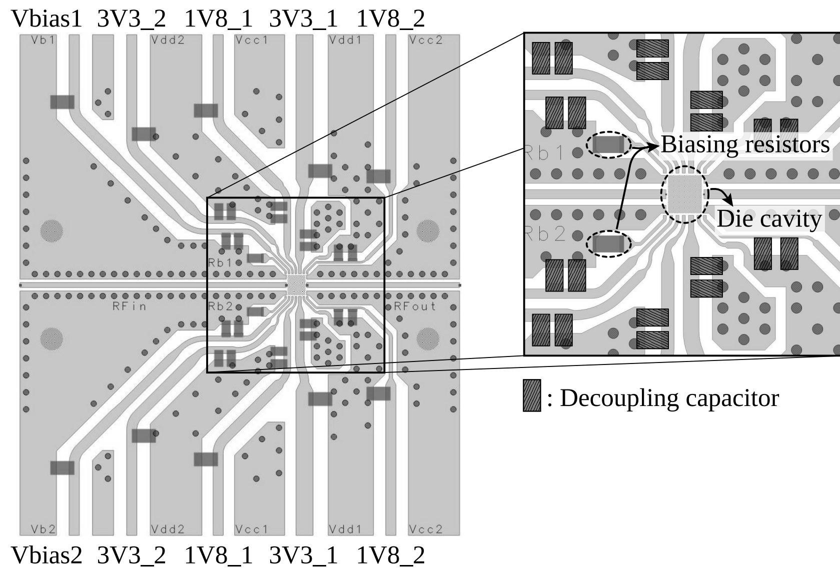

Figure 7.4: Layout of the PA testboard and annotation of the different supply/biasing voltages. The zoomed-in section shows the die cavity and the location of the biasing resistors and decoupling capacitors.

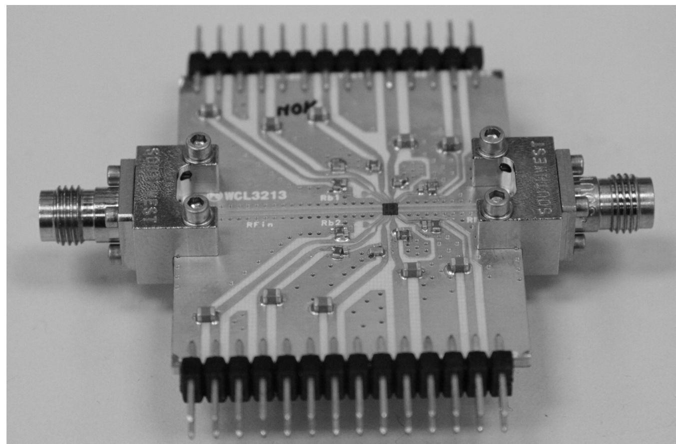

Figure 7.5: Board with mounted PA die (globtopped)and brass heatsink underneath.

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8

Measurement setup and results

8.1 Introduction

Determination of the relevant PA characteristics is far from trivial due to the combination of small and large signal measurements. This chapter starts by explaining the used probe setup and power calibration. Afterwards the measured relevant PA parameters are discussed and a simulation of the spectral regrowth in case of a complex modulated input signal (16QAM) is shown.

8.2 Characterization of the power amplifier

A probing setup is used to accurately characterize the performance of the power amplifier. Two types of measurements, namely small signal and large signal measurements, have been performed both using a network analyzer. The setup used, is shown in Fig.8.1 and includes a power attenuator of 10dB after the probe at the PA output to protect the input of the PNA-X. Because of this an accurate measurement of the S22-parameter during operation is not possible. The measured S22-parameter, shown further on, is taken with a 50Ω at the input.

Small signal calibration of the probe setup is done by using a calibration substrate, however, to do a large signal measurement (P_{out} and PAE as a function of P_{in}) a power calibration is needed. This is done by calibrating

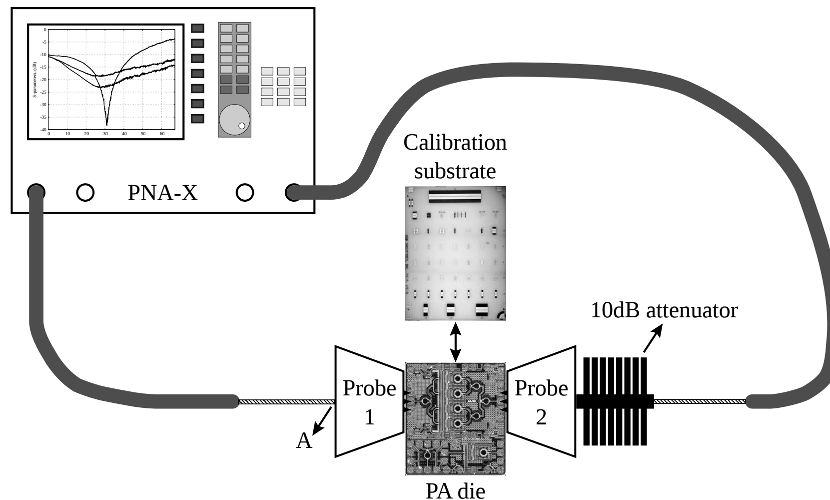

Figure 8.1: Used probing setup for characterization. Position A is connected to ECal and power sensor to allow de-embedding of the input probe and calibrate the input power at position A.

the setup at node A in Fig.8.1 and using the small signal calibration data to de-embed probe 1. By calibrating the input power at node A and taking into account the loss through the input probe, an accurate input power for the PA is attained.

8.2.1 S-parameters

The measured S-parameters of the PA are shown in Fig.8.2 and reveal a maximum gain of 25.5dB with a bandwidth of 2.65GHz [1]. Both input and output show reasonable matching, however, the input could be better matched by using a balun to create the single-ended to differential conversion. Isolation is minimum 40dB for the entire useful frequency range.

8.2.2 Gain and PAE

The output power and resulting PAE of the PA as a function of the input power are shown in Fig.8.3 at a frequency of 31.5GHz and 32GHz (corresponds to the maximum gain). A maximum power and PAE of 24.1dBm and 7.2% are achieved at 32GHz, respectively. The 1dB compression point at 32GHz occurs for an output power of 22.7dBm which is 1.4dB below the saturated output power. At the saturated output power the PA draws 982mA from the 3V3 supply and 174mA from the 1V8 supply.

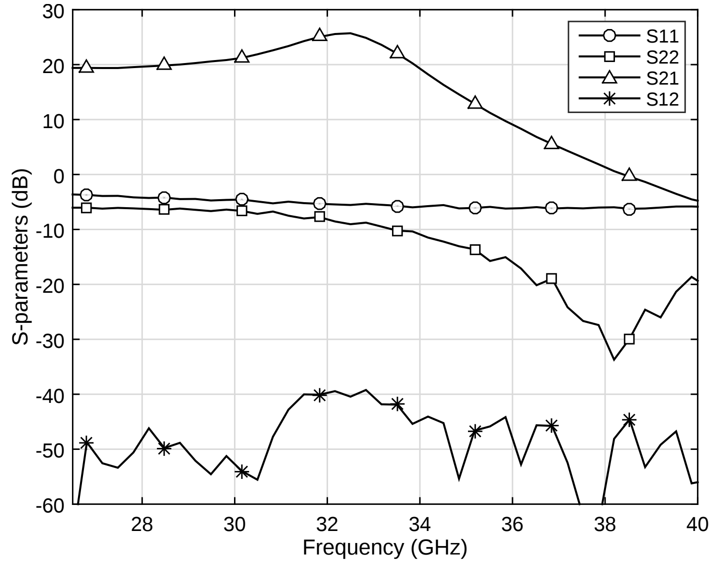

Figure 8.2: Measured S-parameters for an input power of -10dBm.

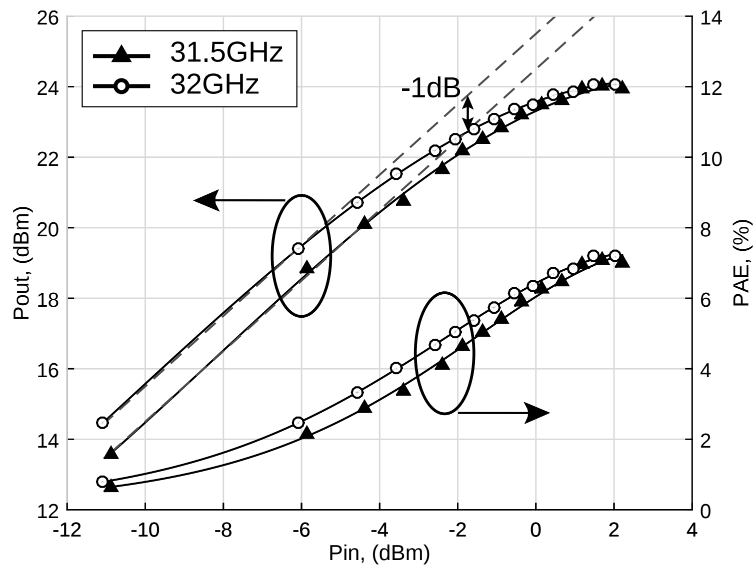

Figure 8.3: Measured output power and PAE as a function of the input power at 31.5GHz and 32GHz.

8.2.3 AM-AM, AM-PM and ACPR

The typical application for the designed amplifier is a Ka-band satellite uplink in which several adjacent data-channels are used. Important in this case is the amount of spectral regrowth introduced by the power amplifier since this will cause power of a certain channel to interfere with the adjacent channels. This is expressed by the adjacent channel power ratio (ACPR) which is the power in the main channel divided by the power in the lower plus upper adjacent channel. An accurate estimate of the ACPR can be done with a two-tone test and the third-order intermodulation product (IP3) in case of simple frequency or phase modulation. However in the case of a complex modulation (QAM, APSK) the adjacent channel distortion has little relationship to intermodulation in a two-tone test [2, 3] and will depend on the spectral regrowth coming from the AM-AM and AM-PM distortion.

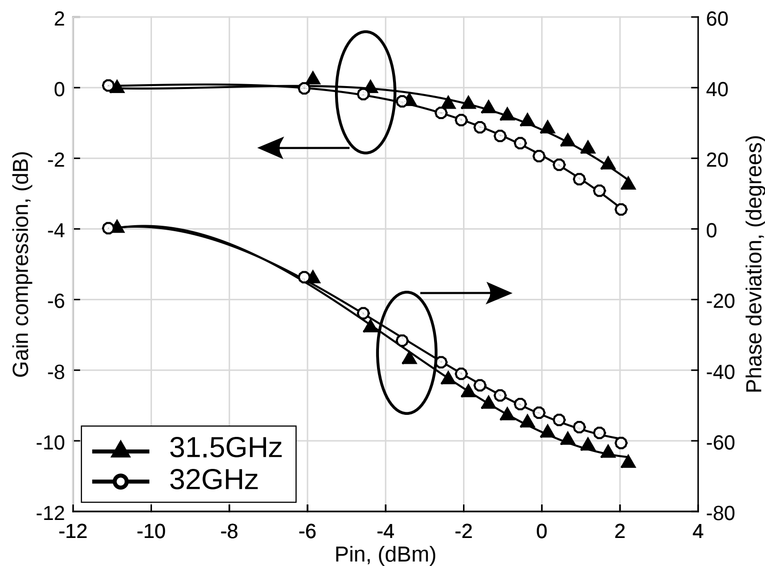

Figure 8.4: Measured gain compression and phase deviation as a function of the input power at 31.5GHz and 32GHz.

To get an accurate prediction of the spectral regrowth a behavioral model of the amplifier is needed, based on measurements of the gain compression (AM-AM distortion) and phase distortion due to amplitude variation (AM-PM distortion) [4]. Measurement results for these two parameters at frequencies 31.5GHz and 32GHz are shown in Fig.8.4. These curves can be used in Keysight's ADS simulator to create an amplifier model which can

then be subjected to a complex modulation scheme at the input. As long as the bandwidth of the complex modulated input signal is small in comparison to the bandwidth of the amplifier the influence of PM-AM and PM-PM distortion can be neglected [5]. The performance of the designed PA in terms of spectral regrowth is evaluated by means of a comparison with two commercial GaAs amplifiers (Triquint TGA4539, UMS PA) and is shown in Fig.8.5. At the input a 16QAM input signal is generated at 2MBaud with a raised cosine filter with a 0.35 roll-off factor and 10dB back-off (average input power 10dB lower than the input power which corresponds to the saturated output power). This shows a smaller spectral regrowth for the designed PA in comparison to the two commercial GaAs PA's tested.

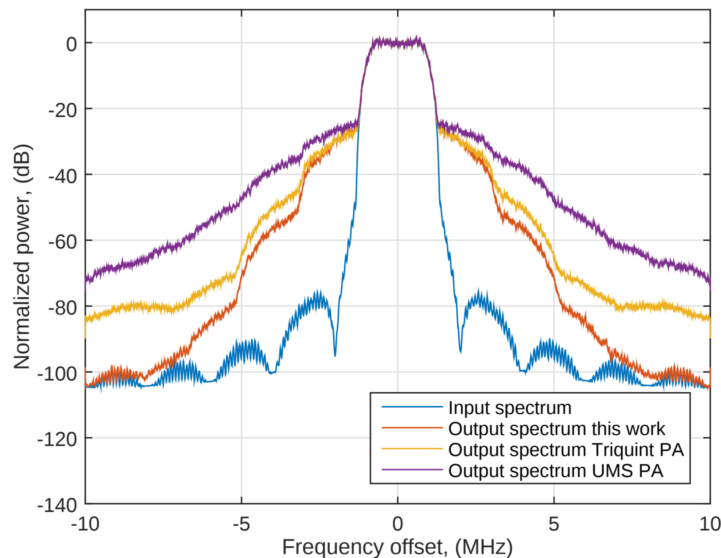

Figure 8.5: Simulated spectral regrowth for a 2MBaud 16QAM signal, put through a raised cosine filter with a 0.35 roll-off factor, and applied at the input of the amplifier subject of this work and two commercial GaAs PA's (Triquint and UMS).

8.3 Characterization of the on-chip power combiner

This structure was put separately onto the same die used for the PA in order to provide testing of the power combiner independently from the rest of the PA. Probing of the power combiner was done using a 50GHz GSGSG (ground-signal-ground-signal-ground) probe at the input and a 50GHz GSG

probe at the output, both with a 125μm pitch. The measurement results for the on-chip power combiner, with the capacitance of the input pads de-embedded, are shown in Fig.8.6.

The S-parameters depicted in Fig.8.6 demonstrate the broadband behavior of the designed power combiner (-3dB bandwidth of approximately 55GHz). Also a high isolation of 30dB between the input ports (S21-parameter) is measured at the PA carrier frequency together with excellent matching (S11-, S22- and S33-parameter lower than -15dB for the entire Ka-band). From the input to output transfer characteristics (S31- and S32-parameter) it can be seen that the power combiner is highly symmetrical. The measured phase characteristic for the S31- and S32-parameter showed a linear response with a difference of 4.7 degrees at 30GHz. However, measurements revealed a higher than expected loss of approximately 1.5dB in the transfer characteristics of the power combiner in comparison to the simulated loss of 0.55dB. Re-simulation of the power combiner showed that the difference between measurements and simulations can be explained by higher substrate losses. This leads to believe that the use of a floating ground shield might provide better results. Due to this higher loss in the actual PA, the saturated output power will already be 2dB lower than expected since 2 stages of power combination are used.

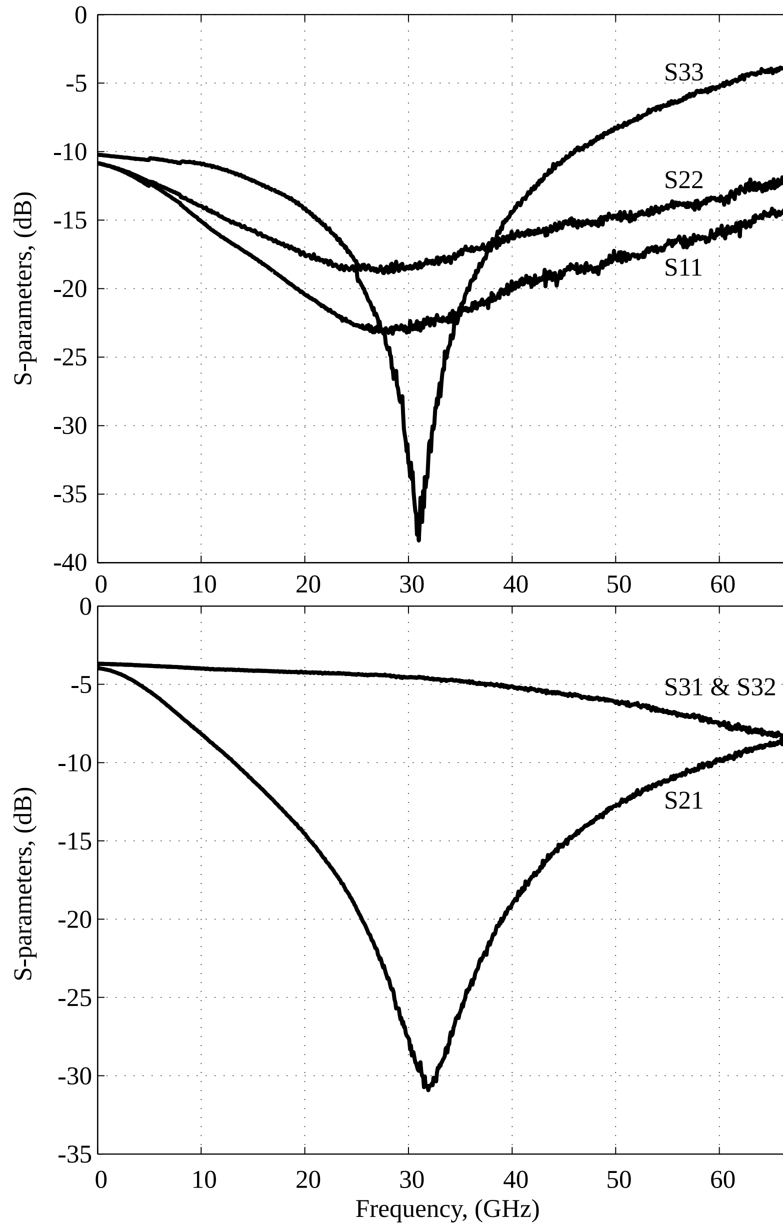

Figure 8.6: Measured S-parameters up to 67GHz (probing) with de-embedding of the input pads for the on-chip power combiner.

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9 Conclusion and further research

9.1 Results summary

In this chapter, the results from the research described in this dissertation are summarized. The design of a Ka-band power amplifier in a 250nm SiGe BiCMOS technology with more than 24dBm of output power is quite a challenge and this PA subsequently led to two publications [1, 2]. In this thesis the difficulties attributed to RF high power PA design are systematically discussed. These, amongst others, are: lossy passives, limited transistor breakdown voltages, on-chip power combination and efficient heat extraction.

Since the performance and maximum output power hinges on the design of the PA output stage, this has been discussed in-depth and a formula for the input impedance of a CB-stage in case of a resonant load was deducted. This revealed that the Miller effect returns when using a cascode configuration at RF-frequencies and a solution was implemented by means of a feedback capacitance. Due to the influence of this solution on stability, an analysis of the differential and common-mode stability was performed.

A single SiGe BiCMOS amplifier is typically not enough to achieve more than 20dBm saturated output power at millimeter wave frequencies [3, 4], which means that several power amplifiers will need to be combined. Different ways of achieving on-chip power combination have been discussed in chapter 6 together with the power combiner proposed in this work. This is

based on a transformer-type Wilkinson combiner previously used for CATV power splitters [5] and achieves broadband power combination (return loss at all ports lower than -14dB for the entire Ka-band) and high isolation between the input ports (30dB at 32GHz). However, the loss of the power combiner turned out to be larger than expected due to high substrate losses which caused the saturated output power and efficiency, to be 2dB lower than intended.

The final chip consists of the discussed amplifier together with biasing circuits and ESD protection. Adding ESD devices to RF pads without adding too much capacitance is a challenging task [6] and constitutes a specialized research field on its own. However the topology of this PA makes it possible to omit the ESD protection at the input and output RF pads due to a balun at the output stage (which shorts ESD pulses to ground) and a coupling capacitor at the input stage (which is a high-impedance for the ESD pulse).

9.1.1 Comparison

The main characteristics of the designed PA and the on-chip power combiner have been discussed in chapter 8 and chapter 6 respectively. A comparison to other state-of-the-art PAs implemented in a SiGe BiCMOS technology with a center frequency which is part of, or close to the Ka-band is given in Table 9.1.

Reference	Technology (nm)	Freq. (GHz)	P_{sat} (dBm)	P_{-1dB} (dBm)	PAE (%)	Die area (mm^2)
This work	250	32	24.1	22.7	7.2	1.7
[7]	200	24	21	18.8	13	6
[8]	130	30	19.4	15.4	6.18	14
[9]	120	33	19.4	≈16.4	11.2	1.82
[3]	120	38	23	/	10.7	1.04
[4]	130	42	28.5	/	10	5.55

Table 9.1: Performance summary for the presented PA in comparison to state-of-the-art PAs implemented in a SiGe BiCMOS technology

A high output power, in comparison to the state-of-the-art, is achieved in this work as can be seen in Table 9.1. When comparing PAs with center

frequency in the Ka-band, this work attains the highest saturated output power. Due to the technology node used, the PAE is lower than most PAs, however, this is also largely caused by the higher than expected loss in the power combination. An output power of 22.7dBm at 1dB compression is attained which is the closest to the saturated output power of the compared amplifiers. This leads to the low amount of spectral regrowth as was demonstrated in chapter 8.

9.2 Future research

9.2.1 Possible improvements

In this dissertation a PA was designed which achieves an output power of 24.1dBm. This is 2 to 3dB lower than the goal of this design which was to create a power amplifier with half a watt of saturated output power. However, the analysis provided on the different blocks should make it possible to attain this initial goal if following improvements are made:

- Apply a floating shield to the power combiner transformer to lower the combiner losses. Resimulate taking into account a factor ten higher substrate losses.
- Use a technology which has a high-ohmic substrate (e.g., ST9MW of STMicroelectronics).
- Increase the distance between output transistors to reduce the self-heating of these transistors and increase the saturated output power.
- Go to an eight-way power combination to have some margin on the saturated output power.

Next to the previously mentioned measures to increase the saturated output power there are a number of alterations that can be made to increase the PAE:

- Provide the single-ended to differential conversion at the input by means of a balun which lowers the power consumption.
- Implement a matching circuit at the input of the output stage to shift the second harmonic in the output current to reduce the power consumption of the output stage (see chapter 4).

- Port the design to a 130nm SiGe BiCMOS node which allows to achieve higher gain in the output stage and lower the power consumption of the driver stage(s).

- Use alternative output stage (discussed in 9.2.1.1)

9.2.1.1 Alternative output stage

When choosing a 130nm or 55nm SiGe BiCMOS technology to implement a Ka-band power amplifier the output stage can be altered since a cascode output stage is no longer required to achieve the necessary amount of gain. One possibility is to use a CB output stage as was done in [7] but with biasing provided by a current source as shown in Fig.9.1.

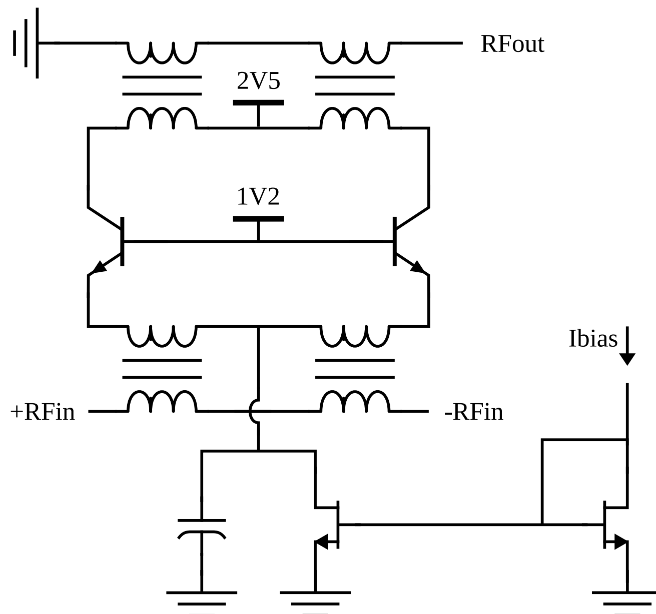

Figure 9.1: Alternative CB output stage with current source biasing.

By biasing the CB output stage with a current source the DC collector-emitter voltage is allowed to exceed BV_{CEO} [10] as was the case in the cascode configuration. In this topology, however, the required supply voltage is significantly lower since the CE stage in a cascode requires a certain collector emitter voltage to be able to provide current amplification. In this case there is less than approximately 0.2V needed at the emitters of the CB stage which allows to lower the supply voltage and increase the PAE. Im-

portant to remark is that the chosen technology node needs to have enough gain for a CB stage at the carrier frequency (order of magnitude: 10dB).

9.2.2 Higher frequencies

By porting the design described in this dissertation to a faster technology node, new applications like WiGig and WirelessHD can be addressed. These operate in the unlicensed bands at 57-64 GHz, however published SiGe BiCMOS and CMOS PAs for these applications rarely provide saturated output powers above 20dBm [11]. Since in multiple regions an equivalent isotropically radiated power (EIRP) of 40dBm is allowed, beamsteering is used to increase performance. However, published beamsteering antenna arrays haven't demonstrated much more than 15dBi antenna gain [12, 13] which means that a PA for this type of application would need to produce 25dBm to reach full potential. This hasn't yet been achieved, furthermore, the complex modulation schemes (16QAM, 64QAM) used in many standards require a large back-off which leads to a desired output power around 27 - 28dBm.

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