Dark Current Analysis in High-speed Germanium p-i-n Waveguide Photodetectors

H. Chen,[1,2,a)] P. Verheyen,[1] P. De Heyn,[1] G. Lepage,[1] J. De Coster,[1] S. Balakrishnan,[1] P. Absil,[1] G. Roelkens,[2] and J. Van Campenhout[1]

[1]*imec, Kapeldreef 75, Leuven B-3001, Belgium*

[2]*Photonics Research Group, Department of Information Technology, Ghent University—imec, B-9000 Ghent, Belgium*

We present a dark current analysis in waveguide-coupled germanium vertical p-i-n photodetectors. In the analysis, surface leakage current and bulk leakage current were separated, and their activation energies were extracted. Surface leakage current originating from the minority carrier generation on the Ge layer sidewalls, governed by the Shockley-Read-Hall process and enhanced by the trap-assisted-tunneling process, was identified as the main contribution to the dark current of vertical p-i-n photodiodes at room temperature. The behavior of this surface leakage current as a function of temperature and (reverse bias) voltage is well reproduced by using the Hurckx model for trap-assisted-tunneling.

I. INTRODUCTION

A germanium-on-silicon waveguide photodetector is a key building block for silicon photonics optical interconnects and optical sensors. Low dark current is desirable to improve the performance and reliability in these applications [1,2]. A vertical p+(Ge)-i(Ge)-n+(Si) hetero-junction, as seen in Fig. 1, is widely adopted to construct such a photodetector [3-9], showing promising device performance. This is referred to as a VPIN GePD hereafter. We have demonstrated such VPIN GePDs exhibiting high opto-electrical bandwidth (beyond 50 GHz), high responsivity (0.9 A/W) and low dark current (~15 nA) [8,9] at -1 V bias. There are several sources for the dark current of such VPIN GePDs. The diffusion current of the reverse biased p-i-n junction is the intrinsic dark current of a VPIN GePD. Another dark current source is the generation of minority carriers in the depletion region of the VPIN GePD, governed by the Shockley-Read-Hall process (SRH). This leakage current component is enhanced by misfit dislocations and threading dislocations created in the Ge epitaxy due to the 4% Ge/Si lattice mismatch. These dislocations acts as effective electrical traps and generation centers in the depletion region [10,11]. In addition, the generation of minority carriers on the Ge layer surface due to the poor passivation quality of silicon dioxide is another important dark current source [12,13], especially for the small-size Ge ($< 10 \times 10\ \mu m^2$) VPIN GePDs, which have a large perimeter to surface area ratio. In order to further reduce the dark current of a VPIN GePD, it is important to know the dark current generation mechanisms, such that specific process and/or epitaxy development can be done to optimize the corresponding aspect of the material quality.

a) Email: hongtao.chen@imec.be

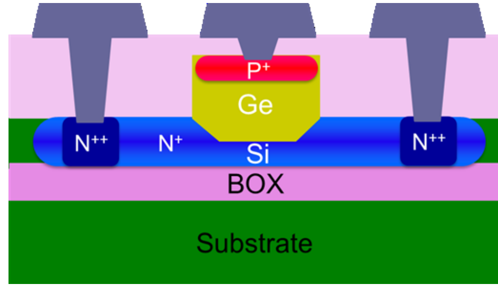

FIG. 1. Schematic of a vertical p-i-n junction Ge-on-Si photodetector.

In this paper, we report the analysis of dark current in VPIN GePDs in a design of experiment (DoE) using devices with varying Ge layer area to perimeter ratio. The surface leakage current and bulk leakage current were separated through the analysis. The activation energy of both the surface leakage current and the bulk leakage current were extracted. This analysis reveals that, for a 1.8 × 15 μm^2 VPIN GePD at room temperature, it is the surface leakage current originating from the minority carrier generation on the Ge layer sidewall, governed by the Shockley-Read-Hall process and enhanced by the trap-assisted-tunneling process, that dominates the dark current.

This paper is organized as follows. Background on germanium p-i-n photodiodes and the VPIN GePD dark current analysis is given in Section I. In section II, we introduce the VPIN GePDs and the physical model used in the dark current analysis. In section III, the dark current measurement data and dark current modeling are presented. The dark current is separated into 2 components, i.e. a surface leakage current and bulk leakage current. In section IV, the activation energy of both surface leakage current and bulk leakage current were extracted. A physical interpretation of the extracted activation energy is presented. In section V, the dark current analysis results are presented and the dominant leakage current source is determined for a baseline VPIN GePD device (1.8 × 15 μm^2). Finally, in section VI, the conclusions are formulated.

II. VPIN GERMANIUM PHOTODETECTORS AND DARK CURRENT ANALYSIS

A. VPIN Ge photodetectors

VPIN GePDs were fabricated in imec's fully integrated Si photonics platform along with Si modulators and various passive devices, going through a process flow described in [8]. The baseline VPIN GePD has a 1.8 μm wide Ge waveguide, which is nominally 400 nm thick. With phosphorus ion implantation in silicon before Ge epitaxy and boron ion implantation in the planarized Ge layer, a vertical p-i-n diode is formed. The doping profile in the Ge layer measured by secondary ion mass spectrometry (SIMS) in VPIN GePDs is shown in Fig. 2(a). It can be seen that the doping concentration drops to ~2×10^{17} cm^{-3} 100 nm away from the Ge/Si interface, as a result of the ion implantation tail. The simulated doping distribution using

Sentaurus Process (Monte Carlo ion implantation simulation calibrated by the SIMS data) in the VPIN GePD is shown in Fig. 2(b). The doping profile along the A-A' cut in Fig. 2(b) is also shown in Fig. 2(a).

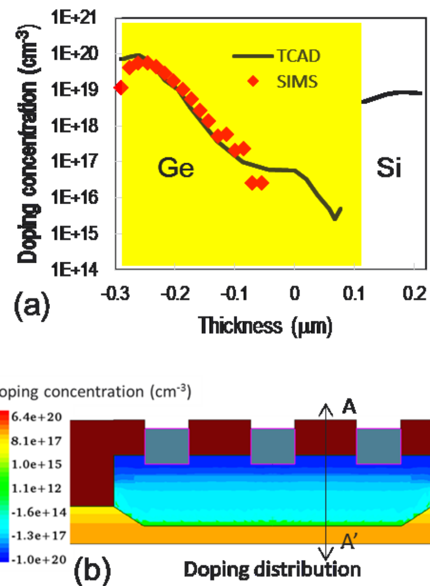

FIG. 2. (a) Boron doping profile in the Ge layer in VPIN GePDs measured by SIMS, and the doping profile from TCAD simulation along the A-A' cut. (b) Doping distribution in the baseline VPIN GePD with a 1.8 μm wide Ge layer generated from a Monte-Carlo ion implantation simulation.

The electric field distribution at -1 V bias in the VPIN GePD, simulated with *Sentaurus Device*, is shown in Fig. 3(a), and the electric filed profile along the A-A' cut is shown Fig. 3(b) for different bias voltages. This heterogeneous Ge/Si VPIN diode configuration confines the electric field in the lower part of the Ge layer. At -1 V bias, the electric field is as strong as 8.5×10^4 V/cm in the bottom 100 nm of the Ge layer. The energy-band diagram of the VPIN GePD along the A-A' cut at 0 V and -1 V are shown in Fig. 3(c). It can be seen that when a 1 V reverse bias is applied on the VPIN GePD, the depletion region mainly extends into the Ge layer. The depletion region is ~200 nm wide.

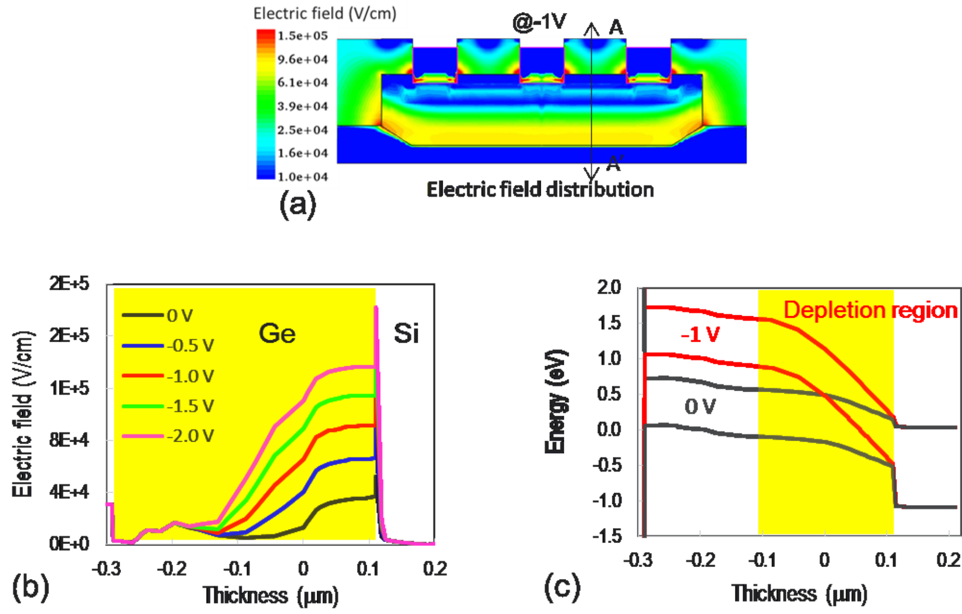

FIG. 3. (a) Simulated electric field distribution in the VPIN GePD at -1 V bias. (b) Electric field profile extracted along the A-A' cut [see Fig. 2(b)] at various bias voltages. (c) Simulated energy-band diagram along the A-A' cut at 0 V and -1 V bias.

B. Dark current analysis

A schematic diagram illustrating and simplifying the dark current analysis of VPIN GePDs is shown in Fig. 4. The dark current (I_{dark}) is divided into 2 parts, i.e. the surface leakage current and the bulk leakage current. The surface leakage current (I_{surf}) originates from the generation of minority carriers on the Ge layer surface due to the poor passivation quality of silicon dioxide. The non-passivated dangling bonds introduce a high interface-state density at Ge/SiO2 interfaces [14]. Since the top part of the Ge layer is implanted with Boron, the interfacial defects at the Ge top surface/SiO2 interface are not electrically active, and only the interfacial defects on the Ge layer sidewall are considered for the surface leakage current in the analysis. The bulk leakage current (I_{bulk}) originates from the generation of minority carriers in the depletion region in the Ge layer along with the intrinsic bulk diffusion current. The surface leakage current is governed by the Shockley-Read-Hall (SRH) process ($J_{SRH,surf}$). It is proportional to the structure perimeter P, ($2\times(L+W)$), with L the length of the structure and W the width of the structure. The bulk leakage current has contributions from both the SRH process ($J_{SRH,bulk}$) and the diffusion process (J_{diff}). Both of them are proportional to the area of the device S, ($L\times W$) under the assumption that the Ge layer is wide enough to ignore corner effects, as seen in Fig. 3(a).

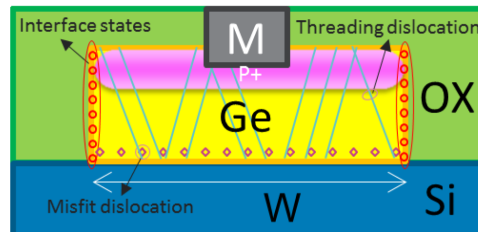

FIG. 4. Schematic diagram illustrating the dark current modeling of VPIN GePDs.

The expression for the dark current (Eq. 1) can be reformulated as in Eq. 2. This reveals that the dark current to perimeter (I_{dark}/P) ratio scales linearly proportional to the area to perimeter ratio (S/P). The bulk leakage current density (J_{bulk}) can be determined by extracting the slope of this linear relationship. By dividing by the structure area (S), Eq. 1 can be reformulated as in Eq. 3. The dark current to area ratio (I_{dark}/S) scales linearly proportional to the perimeter to area ratio (P/S), the slope of which is the surface leakage current density (J_{surf}).

$$I_{dark} = I_{surf} + I_{bulk} = P * J_{surf} + S * J_{bulk} = P * J_{SRH,surf} + S * (J_{SRH,bulk} + J_{diff}) \quad (1)$$

$$\frac{I_{dark}}{P} = \frac{S}{P} * J_{bulk} + J_{surf} \quad (2)$$

$$\frac{I_{dark}}{S} = \frac{P}{S} * J_{surf} + J_{bulk} \quad (3)$$

III. DARK CURRENT MEASUREMENT DATA AND DARK CURRENT MODELING

Six VPIN GePD test structures, numbered from 1 to 6, in the design of experiment (DoE) have a Ge layer width of [0.6, 1.8, 4.2, 9.0, 16.2, 29.4] µm (exponentially scaling) and are 15 µm long, with a nominal Ge layer thickness of 400 nm. Temperature dependent current-voltage measurements were carried out on the VPIN GePD structures in the DoE at 200 mm wafer scale from 25°C to 125°C with a step of 25°C. Wafer-scale dark current data measured at 25°C for the 0.6 µm and 29.4 µm wide VPIN GePDs at various bias voltages are shown in Fig. 5 (a). The 0.6 µm wide Ge structure exhibits a mean dark current value of 8.8 nA and 53 nA at -1 V and -2 V, respectively. It increases to a mean value of 92 nA and 542 nA as the Ge layer is scaled to 29.4 µm wide. It can be seen that there are some outlier dark current data points for the 29.4 µm wide Ge device, which is attributed to the inferior material quality in the large area Ge devices [15-17]. These outlier data points were removed from the dark current modeling. Fig. 5(b) shows the wafer-scale dark current data at -1 V for the 0.6 µm and 29.4 µm wide VPIN GePDs at various measurement temperatures. The mean dark current value of a 0.6 µm wide Ge structure is 8.8 nA and 179 nA measured at 25°C and 125°C. It rises to 92 nA and 2453 nA as the Ge layer is scaled to 29.4 µm width. Fig. 5(c) shows the wafer-scale dark current data at -1 V measured at 25°C and 125°C for the devices with varying Ge layer width. It should be mentioned that the different data point colors corresponding to VPIN GePDs at the different dies of the measured wafer. This convention applies to the following wafer-scale data in this paper.

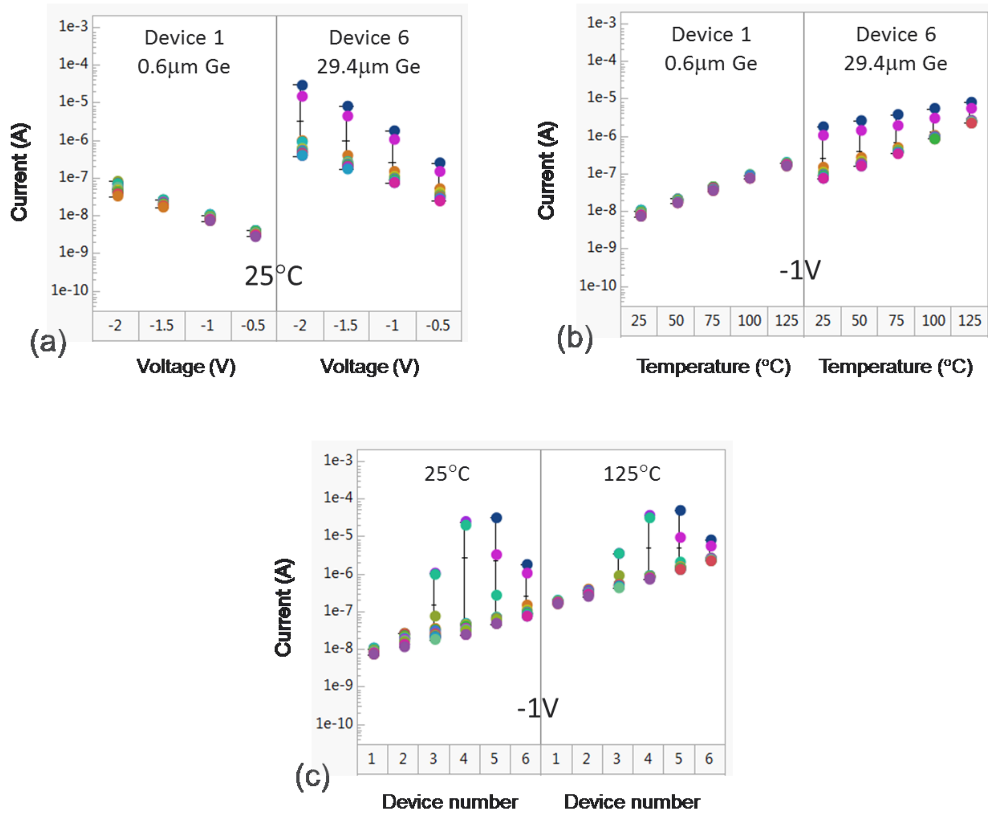

FIG. 5. (a) Wafer-scale dark current data measured at 25°C at various bias voltages for the 0.6 μm and 29.4 μm wide VPIN GePDs. (b) Wafer-scale dark current data at -1 V at various measurement temperatures for the 0.6 μm and 29.4 μm wide VPIN GePDs. (c) Wafer-scale dark current data at -1 V for the devices with various Ge layer width measured at 25°C and 125°C.

The dark current to perimeter ratio (I_{dark}/P) as a function of area to perimeter (S/P) ratio, measured at 25°C and 125°C is shown in Fig. 6(a) and Fig. 6(b), respectively. The area to perimeter ratio is [0.3, 0.8, 1.6, 2.8, 3.9, 5.0] μm for device 1 to 6, respectively. As mentioned in Section II, the linear relationship between them is valid under the assumption that the Ge layer is wide enough. In this paper, the linear fitting was done on the data of the devices with a Ge layer width of [4.2, 9.0, 16.2, 29.4] μm.

It can be seen that there is a larger spread in the data points measured at 25°C than those measured at 125°C. Considering the different temperature dependence of the SRH process related leakage current and diffusion current, as discussed below, the larger spread at 25°C indicates that there is a larger spread in the SRH process related leakage current at low temperature. This may result from the spread in the interface-state density on the Ge layer sidewall or the misfit/threading dislocations density inside the Ge layer at wafer scale.

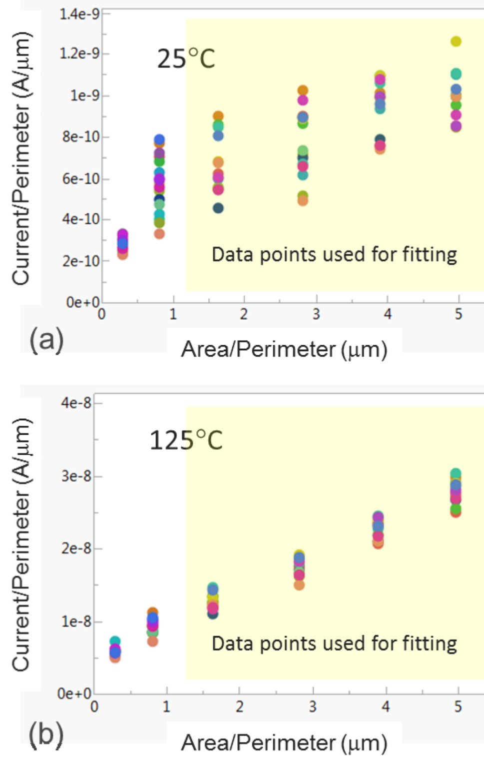

FIG. 6. Wafer-scale data of dark current to perimeter ratio as a function of the area to perimeter ratio measured at (a) 25°C and (b) 125°C.

The dark current to area ratio (I_{dark}/S) as a function of perimeter to area (P/S) ratio, measured at 25°C and 125°C is shown in Fig. 7(a) and Fig. 7(b), respectively. The perimeter to area ratio is [3.47, 1.24, 0.61, 0.35, 0.26, 0.20] μm^{-1} for device 1 to 6, respectively. Similar to extracting bulk leakage current density, the linear fitting was done on the data of the devices with a Ge layer width of [4.2, 9.0, 16.2, 29.4] μm.

Extracting the slope of the linear relationship in Eq. 2 and Eq. 3 using data of the VPIN GePD devices die by die generates surface leakage current density (J_{surf}) data and bulk leakage current density (J_{bulk}) data at wafer scale, as shown in Fig. 8(a) and 8(b). At 25°C, the mean value of surface leakage current density and bulk leakage current density is 0.5 nA/μm and 0.1 nA/μm^2, respectively. It rises to 5.5 nA/μm and 4.5 nA/μm^2 as the temperature is increased to 125°C.

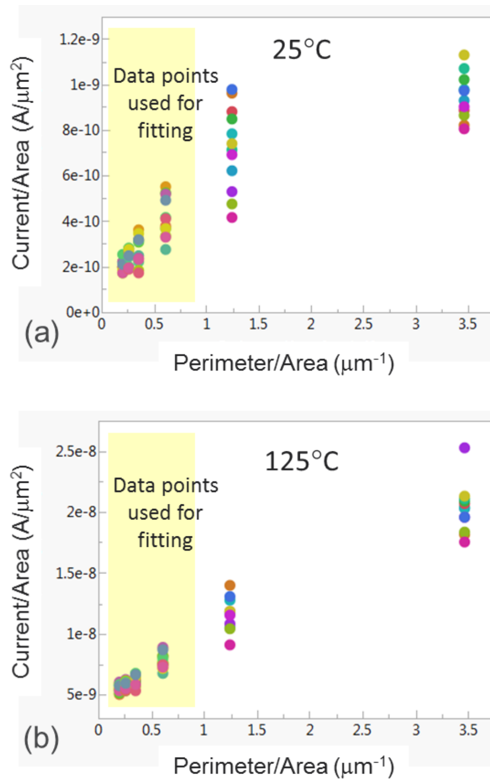

FIG. 7. Wafer-scale data of dark current to area ratio as a function of the perimeter to area ratio measured at (a) 25°C and (b) 125°C.

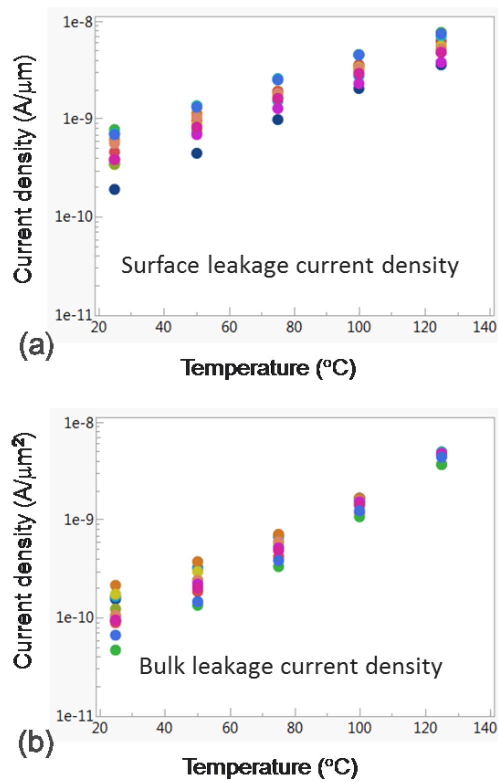

FIG. 8. Wafer-scale (a) surface leakage current density data extracted from the slope of Eq. 3 and (b) bulk leakage current density data extracted from the slope of Eq. 2 using data of the devices die by die as a function of measurement temperature.

IV. ACTIVATION ENERGY EXTRACTION

A. p-i-n diode leakage current theory

The diffusion current density can be expressed as in Eq. 4 for a reverse biased VPIN GePD. In the equation, q is the elementary charge, $n_{i,Ge}$ and $n_{i,Si}$ is the intrinsic carrier concentration in Ge and Si, N_D and N_A is the donor and acceptor doping concentration, D_n and D_p is the electron and hole diffusion coefficient, L_n and L_p is the electron and hole diffusion length, $E_{bg,Ge}$ is the Ge bandgap. As seen in Fig. 2(a), the n-type doping concentration in Si underneath the Ge layer is 5×10^{18} cm^{-3} and quite uniform. As seen in Fig. 3(c), at -1 V bias, the depletion region extends 200 nm from the Ge/Si interface into the Ge layer, up to where the p-type doping concentration reaches ~1×10^{17} cm^{-3}. Therefore, the diffusion current in the vertical p-i-n junction is dominated by the (minority) electron diffusion current in the quasi-neutral region in the Ge.

The generation of minority carriers on the Ge layer sidewall can be expressed as in Eq. 5 for a reverse biased VPIN GePD. In the equation, q is the elementary charge, $n_{i,Ge}$ is the intrinsic carrier concentration in Ge, S is the surface recombination velocity on the Ge layer sidewall and t is the thickness of the depletion region. The generation of minority carriers in the depletion region (in Ge) can be expressed as in Eq. 6 for a reverse biased VPIN GePD. In the equation, q is the elementary charge, $n_{i,Ge}$ is the intrinsic carrier concentration in Ge, τ_G is the minority carrier lifetime in the depletion region and t is the thickness of the depletion region.

$$j_{diff} = \frac{q*D_p*n_{i,Si}^2}{L_p N_D} + \frac{q*D_n*n_{i,Ge}^2}{L_n N_A} \approx \frac{q*D_n*n_{i,Ge}^2}{L_n N_A} \sim e^{\frac{-E_{bg,Ge}}{k*T}} \tag{4}$$

$$j_{SRH,surf} = q*S*n_{i,Ge}*t \sim e^{\frac{-E_{bg,Ge}}{2*k*T}} \tag{5}$$

$$j_{SRH,bulk} = q*\frac{n_{i,Ge}}{\tau_G}*t \sim e^{\frac{-E_{bg,Ge}}{2*k*T}} \tag{6}$$

The trap-assisted-tunneling (TAT) process, occurring along with the SRH process where there is a strong electric field, is considered as an enhancement to the SRH-related minority carrier generation for both the Ge layer sidewall leakage current ($J_{SRH,surf}$) and bulk leakage current ($J_{SRH,bulk}$). It can be described by the Hurkx model [18,19], as given in Eq. 7 and 8. In Eq.7, τ_{SRH} is the Shockley-Read-Hall carrier lifetime in the depletion region or the inverse of the surface recombination velocity on the Ge layer sidewall. $\tau_{SRH,TAT}$ is the equivalent carrier lifetime taking the enhancement from the TAT process into consideration. In Eq.8, kT is the thermal energy, q is the elementary charge, $\hbar$ is the reduced Planck constant, and m^* is the tunneling effective mass of the carriers. ΔE_T is related to the trap level and equals $E_{bg,Ge}/2$ for midgap states. E is the local electric field.

$$\tau_{SRH,TAT} = \frac{\tau_{SRH}}{(1+\Gamma)} \tag{7}$$

$$\Gamma = \frac{\Delta E_T}{kT} \int_0^1 exp\left[\frac{\Delta E_T}{kT} u - \frac{4}{3} \frac{\sqrt{2m^*}(\Delta E_T)^{3/2}}{q\hbar|E|} u^{3/2}\right] du \tag{8}$$

The natural logarithm of j_{diff}, $j_{SRH,surf}$ and $j_{SRH,bulk}$ scales linearly proportional to the natural logarithm of the intrinsic carrier concentration in Ge ($n_{i,Ge}$) and therefore scales linearly proportional to the reciprocal of temperature ($1/T$), without considering the enhancement of the TAT process. The activation energy can be extracted from the slope of this linear relationship. It is the Ge bandgap ($E_{bg,Ge}$) and half of the Ge bandgap ($E_{bg,Ge}/2$) for the diffusion current density and the SRH process related current density respectively. With the TAT process taken into consideration, the temperature dependence of the TAT enhancement factor Γ also contributes to the activation energy of the SRH-related leakage current density. Since TAT has a negative activation energy [20], it will lower the overall activation energy below half of Ge bandgap.

B. Activation energy data

Fig. 9(a) and Fig. 9(b) show the wafer-scale data in an Arrhenius plot for the surface leakage current density and bulk leakage current density, respectively. It can be seen that, while there is a linear relationship for the surface leakage current density, the data for the bulk leakage current density largely deviates from a linear relationship. This is because both the SRH process related leakage current and diffusion current contribute comparably to the bulk leakage current and they have different activation energy, while only the SRH related leakage current contributes to surface leakage current.

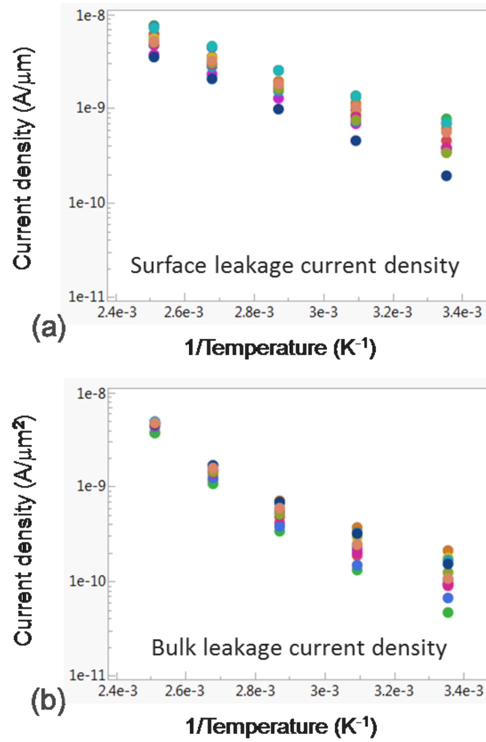

FIG. 9. Arrhenius plot of wafer-scale (a) surface leakage current density data and (b) bulk leakage current density data at -1.0 V bias as a function of the inverse of the measurement temperature.

In order to differentiate the contribution of the SRH process related leakage current and diffusion current in the bulk leakage current over the measured temperature range, the activation energy is extracted as a function of temperature using data at 2 adjacent temperature points, as shown Fig. 10(b). The same exercise is done for surface leakage current for reference, as shown in Fig. 10(a). The surface leakage current shows an activation energy between 0.2~0.3 eV. This value is below half of the Ge bandgap ($E_{bg,Ge}/2$), which is attributed to the influence of trap-assisted-tunneling (TAT) occurring under relatively strong electric field [20-22]. The bulk leakage current activation energy increases from 0.2-0.3 eV to about 0.6 eV as the temperature is increased from 25°C to 125°C. This is because at low temperature, the SRH-related minority carrier generation in the depletion region in Ge dominates over the diffusion current density, exhibiting an activation energy value similar to that of the surface leakage current. As the measurement temperature is increased, there is a larger contribution from the diffusion current to the bulk dark current, resulting in a higher activation energy, close to the Ge bandgap ($E_{bg,Ge}$).

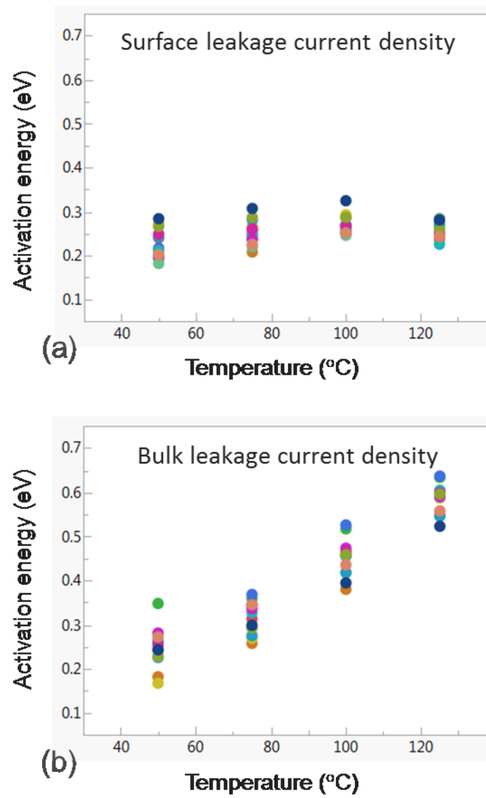

FIG. 10. Wafer-scale activation energy data of (a) surface leakage current density and (b) bulk leakage current density as a function of measurement temperature.

V. DISCUSSON AND OUTLOOK

The dark current and its 2 contributing components, surface leakage current and bulk leakage current, of the 1.8 µm wide VPIN GePD in the DoE are shown in Fig. 11, as a function of the measurement temperature (at -1 V bias). These dimensions are close to that in a baseline VPIN GePD device. At 25°C, surface leakage current contributes much more than bulk leakage current to the dark current of the VPIN GePD device. As the temperature is increased, the relative contribution of the bulk leakage current increases. This increase in the bulk leakage current mainly comes from the intrinsic diffusion current, as seen from the activation energy in Fig. 10(b). The fact that, for a baseline VPIN GePD device at room temperature, surface leakage current is contributing much more than bulk leakage current indicates that improving the Ge layer sidewall passivation quality to reduce the interface-state density on the Ge layer sidewall should be able to effectively reduce dark current of the VPIN GePD device. Since surface leakage current contributes much more than bulk leakage current to the dark current of the VPIN GePD device at low temperature, the large spread in the data points measured at 25°C in Fig. 6 (a) can be attributed to the large spread in the interface-state density on the Ge layer sidewall at wafer scale.

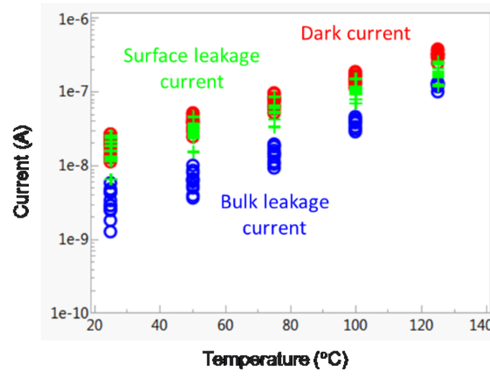

FIG. 11. Wafer-scale dark current data and its 2 contributing components, surface leakage current and bulk leakage current, of a 1.8 μm wide VPIN GePD device at -1 V bias as a function of measurement temperature.

It can be seen from Fig. 5(a) that the dark current increases exponentially as a function of the applied bias for the 0.6 μm wide Ge at 25°C. This indicates that the surface leakage current increases exponentially with applied bias, which cannot be explained by the SRH process. We attribute this to the enhancement of the TAT process at increasing reverse bias. In order to support this, the activation energy of the surface leakage current density at -0.5 V, -1 V, -1.5 V and -2 V bias were extracted, as shown in Fig. 12 (at 50°C). It can be seen that the activation energy decreases as the bias voltage is increased. The activation energy of the surface leakage current density generated by numerically evaluating Eq. 5, Eq. 7 and Eq. 8 is also shown in Fig. 12. In the numerical evaluation, $E_{bg,Ge}$ (Eq. 5) was chosen to be 0.66 eV, ΔE_T (Eq. 8) was chosen to be $E_{bg,Ge}/2$ and thus 0.33 eV [20-22], m^* (Eq. 8) was chosen to be $0.02 \times m_0$ [22]. The electric field magnitude $|E|$ (Eq.8) was chosen to be 6.57×10^4 V/cm, 9.11×10^4 V/cm, 1.14×10^4 V/cm and 1.36×10^4 V/cm at -0.5 V, -1.0 V, -1.5 V, and -2.0 V, respectively, as seen in Fig. 3(b). The extension of the depletion region in the Ge layer with increasing bias voltage was not considered. This numerical evaluation predicts well how does the surface leakage current density activation energy drop as a function of the applied bias. The deviation at higher bias voltage can be partly attributed to the neglect of the depletion region extension. A higher bias voltage generates a stronger electric field in the VPIN GePD. It further pulls the activation energy of the surface leakage current density, through the second term of the integrand in Eq. 8, from the activation energy of SRH process related surface leakage current density, that is around half of the Ge bandgap.

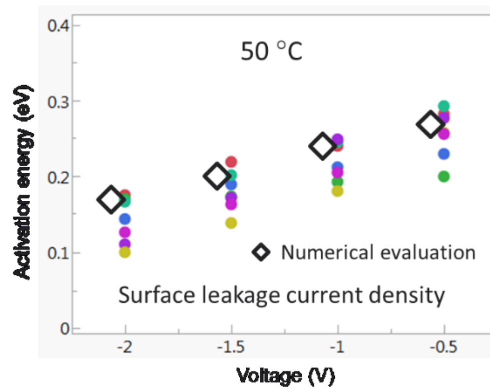

FIG. 12. Wafer-scale activation energy data of the surface leakage current density as a function of bias voltage at 50°C, along with the activation energy generated from a numerical evaluation.

The carrier generation enhancement rate ($1+\Gamma$) due to trap-assisted tunneling obtained by numerical evaluation is plotted together with the wafer-scale dark current data measured at 25°C for the 0.6 µm wide VPIN GePD, as shown in Fig. 13. In the plot, the value at -0.5 V was scaled to be 3.5×10^{-9} A and the ($1+\Gamma$) values at the other voltage points were scaled accordingly. It can be seen that this numerical evaluation also predicts well the current-voltage characteristic of the VPIN GePD at 25°C. The deviation at higher bias voltage can be partly attributed to neglecting the depletion region extension.

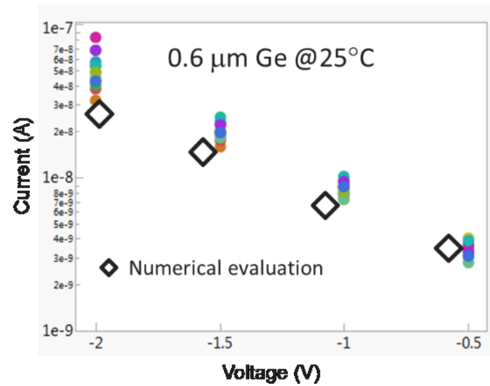

FIG. 13. Wafer-scale dark current data measured at 25°C at various bias voltages for the 0.6 µm wide VPIN GePDs, along with that from a numerical evaluation.

VI. CONCLUSION

The dark current analysis of Ge VPIN photodetectors implemented on imec silicon photonics platform is reported. Surface leakage current and bulk leakage current were separated, and their activation energies were extracted. Surface leakage current, governed by the SRH process enhanced by the TAT process, was identified as the main contribution at room temperature to the dark current of a baseline VPIN GePD device (1.8 × 5 µm^2). The behavior of the dark current as a function of reverse bias and temperature is well reproduced by using the Hurckx model for trap-assisted-tunneling. Improving the Ge layer sidewall passivation quality is therefore proposed to effectively further reduce the Ge VPIN photodetector dark current.

ACKNOWLEDGEMENTS

This work was carried out as part of imec's industry affiliation program on Optical I/O. The device simulations were performed in *Sentaurus* TCAD, provided by *Synopsys*. The device layout was performed in *IPKISS* provided by *Luceda Photonics*. We acknowledge imec's mask preparation team and process line for their contributions.

REFERENCES

[1]J. Michel, J. Liu and L. C. Kimerling, "High-performance Ge-on-Si photodetectors," Nat. Photonics 4, 527 (2010).

[2]I. Aberg, B. Ackland, J. V. Beach, C. Godek, R. Johnson, C. A. King, A. Lattes, J. O'Neill, S. Pappas, T. S. Sriram, and C. S. Rafferty, "A low dark current and high quantum efficiency monolithic germanium-on-silicon CMOS imager technology for day and night imaging applications," Tech. Dig.-Int. Electron Devices Meet.14.4.1 (2010).

[3]J. Liu, D. Pan, S. Jongthammanurak, K. Wada, L. C. Kimerling, and J. Michel, "Design of monolithically integrated GeSi electro-absorption modulators and photodetectors on an SOI platform," Opt. Express 15, 623 (2007)

[4]T. Yin, R. Cohen, M. M. Morse, G. Sarid, Y. Chetrit,D. Rubin, and M. J. Paniccia, "31 GHz Ge n-i-p waveguide photodetectors on Silicon on-Insulator substrate," Opt. Exp., 15, 13965 (2007).

[5] L. Vivien, J. Osmond, J. M. F´ed´eli, D. Marris-Morini, P. Crozat, J. F. Damlencourt, E. Cassan, Y. Lecunff, and S. Laval, "42 GHz p.i.n Germanium photodetector integrated in a silicon-on-insulator waveguide," Opt. Exp., 17, 6252 (2009).

[6]S. Liao, N.-N. Feng, D. Feng, P. Dong, R. Shafiiha, C.-C. Kung, H. Liang, W. Qian, Y. Liu, J. Fong, J. E. Cunningham, Y. Luo, and M. Asghari, "36 GHz submicron silicon waveguide germanium photodetector," Opt. Exp., 19, 10967 (2011).

[7]C. T. DeRose, D. C. Trotter, W. A. Zortman, A. L. Starbuck, M. Fisher, M. R. Watts, and P. S. Davids, "Ultra-compact 45 GHz CMOS compatible Germanium waveguide photodiode with low dark current," Opt. Exp., 19, 24897 (2011).

[8]P. Verheyen, M. Pantouvaki, J. Van Campenhout, P. Absil, H. Chen, P. De Heyn, G. Lepage, J. De Coster, P. Dumon, A. Masood, D. Van Thourhout, R. Baets, and W. Bogaerts, "Highly uniform 25 Gb/s Si photonics platform for high-density, low-power WDM optical interconnects," presented at the Integr. Photon. Res., Silicon Nanophoton. Conf., 2014, Paper IW3A.4.

[9]P. Absil, P. Verheyen, P. De Heyn, M. Pantouvaki, G. Lepage, J. De Coster, and J. Van Campenhout, "Silicon photonics integrated circuits: a manufacturing platform for high density, low power optical I/O's," Opt. Express 23, 9369-9378 (2015)

[10]G. Eneman, E. Simoen, R. Yang, B. De Jaeger, G. Wang, J. Mitard, G. Hellings, D. P. Brunco, R. Loo, K. De Meyer, M. Caymax , C. Claeys, M. Meuris, and M.M. Heyns, "Defects, Junction Leakage and Electrical Performance of Ge pFET Devices," ECS Trans. 19, 195 (2009).

[11]G. Eneman, R. Yang, G. Wang, B. De Jaeger, R. Loo, C. Claeys, M. Caymax, M. Meuris, M.M. Heyns and E. Simoen, "P+/n junction leakage in thin selectively grown Ge-in-STI substrates," Thin Solid Films 518, 2489 (2010).

[12]N. A. DiLello and J. L. Hoyt, "Impact of post-metallization annealing on Ge-on-Si photodiodes passivated with silicon dioxide," Appl. Phys. Lett. 99, 033508 (2011).

[13]N. A. DiLello, D. K. Johnstone and J. L. Hoyt, "Characterization of dark current in Ge-on-Si photodiodes," J. Appl. Phys. 112, 054506 (2012).

[14]J. R. Weber, A. Janotti, P. Rinke and C. G. Van de Walle, "Dangling-bond defects and hydrogen passivation in germanium," Appl. Phys. Lett. 91, 142101 (2007).

[15]H.-C. Luan, D. R. Lim, K. K. Lee, K. M. Chen, J. G. Sandland, K. Wada, and L. C. Kimerling, "High quality Ge epilayers on Si with low threading-dislocation densities," Appl. Phys. Lett. 75, 2909 (1999).

[16]J. Liu, J. Michel, W. Giziewicz, D. Pan, K. Wada, D. D. Cannon, S. Jongthammanurak, D. T. Danielson, and L. C. Kimerling, "High-performance, tensile-strained Ge p-i-n photodetectors on a Si platform,"Appl. Phys. Lett. 87, 103501 (2005).

[17]T. H. Loh, H. S. Nguyen, R. Murthy, M. B. Yu, W. Y. Loh, G. Q. Lo, N. Balasubramanian, D. L. Kwong, J. Wang, and S. J. Lee, "Selective epitaxial germanium on silicon-on-insulator high speed photodetectors using low-temperature ultrathin Si0.8Ge0.2 buffer," Appl. Phys. Lett. 91, 073503 (2007).

[18]G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, "A new recombination model for device simulation including tunneling," IEEE Trans. Electron Devices 39, 331 (1992).

[19]G. A. M. Hurkx, H. C. de Graaff, W. J. Kloosterman, and M. P. G. Knuvers, "A new analytical diode model including tunneling and avalanche breakdown," IEEE Trans. Electron Devices 39, 2090 (1992).

[20]E. Simoen, F. De Stefano, G. Eneman, B. De Jaeger, C. Claeys, and F. Crupi, “On the Temperature and Field Dependence of Trap-Assisted Tunneling Current in Ge p+n Junctions, ” IEEE Electron Device Lett. 30, 562 (2009).

[21]M. B. Gonzalez, G. Eneman, G. Wang, B. De Jaeger, E. Simoen, and C. Claeys, “Analysis of the Temperature Dependence of Trap-Assisted-Tunneling in Ge pFET Junctions, ” J. Electrochem. Soc. 158, H955 (2011).

[22]G. Eneman, M. B. Gonzalez, G. Hellings, B. De Jaeger, G. Wang, J. Mitard, K. De Meyer, C. Claeys, M. Meuris, M. Heyns, T. Hoffmann, and E. Simoen, “Trap-Assisted Tunneling in Deep-Submicron Ge pFET Junctions,” ECS Trans. 28, 143 (2010).