Quad configuration for improved thermal design of a cascode current mirror

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Quad configuration for improved thermal design of a cascode current mirror

M. Jabłoński, G. De Mey and A. Kos

Abstract

In this paper, the influence of a temperature gradient on the performance of a current mirror will be investigated. It will be proved that a new design based on a quad layout can make the current mirror almost insensitive to a temperature gradient.

I. Introduction

A current mirror is on the one hand based on the fact that the transistors should have identical characteristics and on the other hand their output characteristic should be horizontal in order to provide constant current. As a consequence the transistors should also have the same temperature. Any temperature difference will inevitably give rise to non matching characteristics and a non proper operating current mirror. Just one report could be found related to this problem [1].

A cascode current mirror layout (fig. 1(a)) is often used for its high output impedance [2][3]. It will be proved by numerical simulation and also theoretically that a temperature change of either transistor 1 or 2 has a much higher influence on the output current than a similar temperature variation of transistor 3 or 4.

If the temperatures of all transistors are changed equally, their characteristic remain identical and there will be no influence on the circuit performance. A problem arises if a temperature distribution is created due to other heat dissipating transistors on the same chip. A temperature gradient is then built up across the current mirror. The temperature differences will then cause a malfunctioning of the circuit especially when the transistors 1 or 2 have different temperatures. A solution to this problem will be proposed. Both transistors 1 and 2 have to be split in two equal ones in parallel and the resulting four have to be placed geometrically in a so called quad layout. It will be shown by numerical simulation and theoretically that this configuration is almost insensitive to any temperature gradient.

II. Numerical simulation of the cascode layout

The numerical simulations have been carried out using the software package TI-TINA made availaible by Texas Instruments [5]. It is a Spice like program but it allows to give every component a different temperature. Simulations have been carried out for an input current $I_{in} = 500\mu A$ and 4 identical, N-Type, wide channel, MOSFET transistor models (SPICE level-2) with $W/L = 150$. The model is based on a real device [4].

If all four transistors (fig.1(a)) were held at $25°C$ the output current was found to be $I_{out} = 500\mu A$ for an output voltage $V_{out} = 4.7V$ or a relative deviation $|I_{out} - I_{in}|/I_{in} = 0\%$. By varying the output voltage, the output resistance R_{out} could be determined. One got $R_{out} = 7M\Omega$. Heating up any single transistor to $35°C$ at a time led to no significant current error $|I_{out} - I_{in}|/I_{in} < 0.03\%$ when applied to transistor 3 or 4. Only when either transistors 1 or 2 were heated up the output current error would become significant (2.3% and 2.4% respectively). Hence one came to the conclusion that a temperature variation of one of the two bottom transistors (T_1, T_2) has a much more pronounced influence on the behaviour of the current mirror. It should be noted that influence on the output resistance was limited ranging from $6.77M\Omega$ to $7.25M\Omega$.

Similar results have been found for other values of the input current I_{in}. At higher temperatures (one transistor at $85°C$, the other at $75°C$) the same conclusions still hold.

It should be noted here that the results are proportional to the temperature difference. For a temperature difference of only $1°C$ instead of $10°C$ the above mentioned values for $|I_{out} - I_{in}|/I_{in}$ have to be 10 times smaller. Moreover when dealing with a thermal gradient it is assumed that the self heating of the transistors has a negligible influence on the temperature distribution.

If the current mirror is under the thermal influence of other components integrated in the same chip, it is quite obvious to approximate the spatial temperature distribution as a superposition of a uniform temperature rise and a thermal gradient field. It is also assumed that the four transistors are located on the corners of a square. Some results obtained with temperature gradients in 8 different directions are shown in table 1.

The first result is that the output resistance of a cascode mirror is not significantly affected by temperature distribution. The influence on the output current however is much more pronounced. Only the case 1 and 5, where the transistors on the left have the same temperature as the transistors on the right, the output current equals the input one. This result is quite obvious, because the circuit remains symmetrical under the influence of a temperature gradient oriented

vertically. For all other cases, the relative error is in the range of a few percent.

III. Numerical simulation of the quad layout

The idea of the quad layout originates from one of the first designs of the input stage of an operational amplifier [6]. Each of the two transistors 1 and 2 in fig.1(a) is replaced by two equal transistors in parallel: 1-1' and 2-2' giving rise to the new circuit shown in fig.1(b).

The four transistors 1, 1', 2 and 2' must be placed on the corners of a square as depicted in fig.1(b) as well. Whatever the orientation of the thermal gradient might be, a "colder" transistor is always connected in parallel with a "warmer" one so that the difference in their characteristics will be compensated.

The transistors 3 and 4 were not replaced by equivalent parallel combinations as it was clearly demonstrated their temperature mismatch has a minor influence on current mirror performance. During the simulations, $T_3 = T_4 = 25°C$ was used for simplicity.

The simulation results are shown in table 2. First of all, one observes that the output resistance is almost the same as for the cascode mirror. The error $|I_{out} - I_{in}|/I_{in}$ is now two orders of magnitude less which can be regarded as a considerable improvement. This circuit can be considered as insensitive to any temperature gradient. The price one has to pay is that the layout is a bit more complicated (4 bottom transistors instead of 2 and more interconnections).

IV. Analytical model

In this section it will be proved theoretically that the transistors 3 and 4 of the typical cascode mirror (fig.1(a)) have a minor influence on the error $|I_{out} - I_{in}|/I_{in}$ compared to the bottom transistors 1 and 2.

An incremental model of the cascode current mirror of fig.1(a) is drawn in fig.2. A MOS transistor is represented by a transconductance g_m and an output resistance r_0 [7]. In order to take into account the temperature effects, (incremental) voltages $-\alpha\Delta T$ have to be added to the gate voltages ΔV_G in order to provide the drain current $g_m(\Delta V_G - \alpha\Delta T)$.

Without going into the mathematical details, the final result is found to be:

$$\Delta V_{out} = r_0(2 + g_m r_0)\Delta I_{out} + \frac{g_m^2 r_0^2 \alpha}{1 + g_m r_0}[(1 + g_m r_0)\Delta T_1 + \Delta T_3] - g_m r_0 \alpha[(1 + g_m r_0)\Delta T_2 + \Delta T_4] \quad (1)$$

For a MOS transistor $g_m r_0 >> 1$ so that (1) can be simplified to:

$$\Delta V_{out} = g_m r_0^2 \Delta I_{out} + g_m^2 r_0^2 \alpha[\Delta T_1 - \Delta T_2] - g_m r_0 \alpha[\Delta T_3 - \Delta T_4] \quad (2)$$

The first term of (1) and (2) gives the output resistance R_{out} of the current mirror:

$$R_{out} = r_0(2 + g_m r_0) \approx g_m r_0^2 \tag{3}$$

The other terms provide the influence of the temperature. Obviously if

$$\Delta T_1 = \Delta T_2 = \Delta T_3 = \Delta T_4 \tag{4}$$

, it is proved by (2) that there is no influence on the output current. Even when

$$\Delta T_1 = \Delta T_2 \neq \Delta T_3 = \Delta T_4 \tag{5}$$

the output current is not influenced. From (2) it is also clear that the coefficient of $\Delta T_1 - \Delta T_2$ is much greater than the coefficient of $\Delta T_3 - \Delta T_4$ which proves that a temperature variation of the bottom transistors has a major influence on the overall behaviour of the current mirror. This result agrees with the numerical simulation outline above.

In case of the quad configuration fig.1(b) each transistor 1 and 2 was replaced by a parallel connection 1-1' and 2-2'. These transistors having the half width of the original one, so that their transconductance is $g_m/2$, their output resistance $2R_0$ and the temperature dependence is $\alpha/2$. The second term of the right hand member of (2) becomes now:

$$\frac{1}{2} g_m^2 r_0^2 \alpha [\Delta T_1 + \Delta T_{1'} - \Delta T_2 - \Delta T_{2'}] \tag{6}$$

Due to the fact that the four transistors 1, 1', 2 and 2' are located on the corners of a square (fig.1(b)), one has:

$$\Delta T_1 + \Delta T_{1'} - \Delta T_2 - \Delta T_{2'} = 0 \tag{7}$$

for any possible direction of the thermal gradient. This explains why the quad configuration is much less sensitive to the thermal gradient as compared to the classical cascode layout of fig.1(a).

V. Conclusion

The influence of a temperature gradient on a cascode current mirror has been analysed. A possible solution based on the quad layout of the two bottom transistors turned out to be almost insensitive to any temperature gradient. The results were obtained using numerical simulations (SPICE) and analytical calculations.

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TABLE I

case		T_3	T_4	cascode mirror	
		T_1	T_2	$\lvert I_{out} - I_{in}\rvert / I_{in}$	R_{out} MΩ
0		25	25	0.00%	6.99
		25	25		
1	↑	35	35	<0.01%	6.82
		25	25		
2	↗	30	35	1.21%	6.94
		25	30		
3	→	25	35	2.37%	7.07
		25	35		
4	↘	25	30	1.18%	7.03
		30	35		
5	↓	25	25	<0.01%	6.99
		35	35		
6	↙	30	25	1.20%	6.87
		35	30		
7	←	35	25	2.45%	6.74
		35	25		
8	↖	35	30	1.23%	6.78
		30	25		

TABLE II

case		T_1	T_2	quad cascode mirror	
		T_2'	T_1'	$\lvert I_{out} - I_{in}\rvert / I_{in}$	R_{out} MΩ
		25	25		
0		25	25	0.00%	7.012
		35	35		
1	↑	25	25	<0.01%	7.011
		30	35		
2	↗	25	30	0.03%	7.008
		25	35		
3	→	25	35	<0.01%	7.011
		25	30		
4	↘	30	35	0.03%	7.014
		25	25		
5	↓	35	35	<0.01%	7.011
		30	25		
6	↙	35	30	0.03%	7.008
		35	25		
7	←	35	25	<0.01%	7.011
		35	30		
8	↖	30	25	0.03%	7.014

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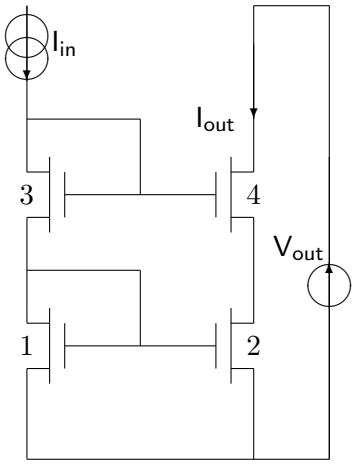
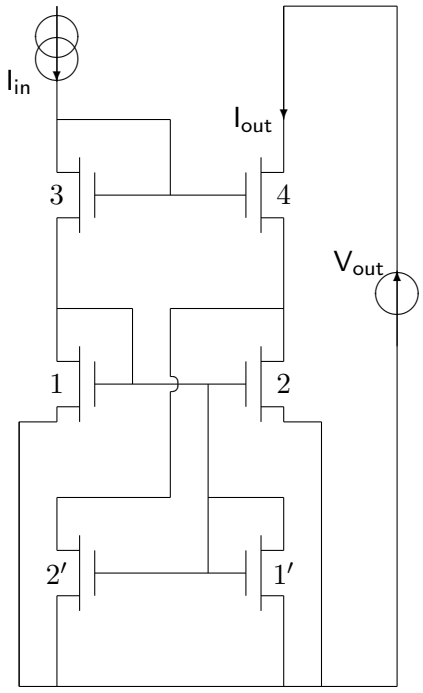


(a)



(b)

Fig. 1.

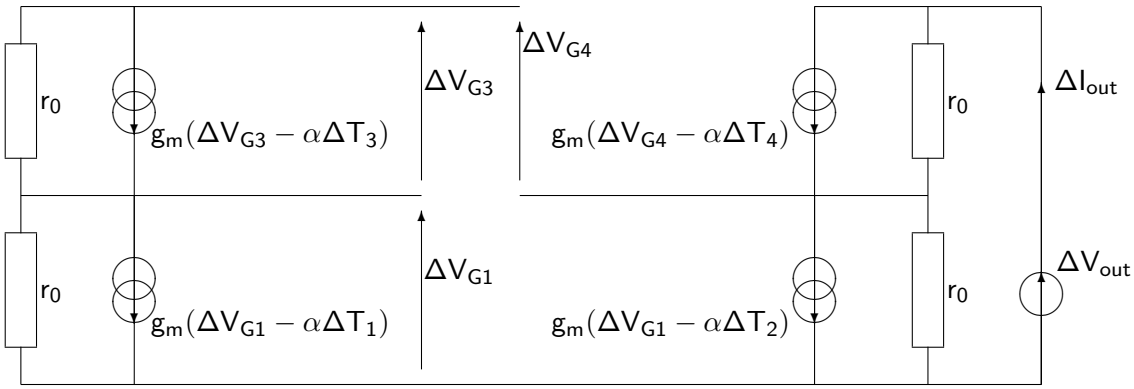

r_0
$g_m(\Delta V_{G3} - \alpha \Delta T_3)$
ΔV_{G3}
ΔV_{G4}
$g_m(\Delta V_{G4} - \alpha \Delta T_4)$
r_0
ΔI_{out}
r_0
$g_m(\Delta V_{G1} - \alpha \Delta T_1)$
ΔV_{G1}
$g_m(\Delta V_{G1} - \alpha \Delta T_2)$
r_0
ΔV_{out}

Fig. 2.