A Model- Based Approach to Automatic Diagnosis Using General Purpose Circuit Simulators

E. N. Dimitrova*, E. D. Gadjeva**, A. Van den Bossche*** and V. C. Valchev*

* Technical University of Varna / Department of Electronics, Varna, Bulgaria
** Technical University of Sofia/Department of Electronics, Sofia, Bulgaria
*** Ghent University / Department of Electrical Energy, Systems and Automation, Ghent, Belgium

Abstract: **An approach is proposed to automatic testing of analog electronic circuits using *PSpice*-like general purpose circuit simulators based on parameterized models of the faulty elements. Using time domain response parameters that well characterize the faults, the set of typical faulty variants of the circuit is simulated. Using post-processing of the obtained results and macro-definitions in the graphical analyzer *Probe*, a diagnosis of parametric faults in the circuit is performed. The models of the faulty elements are defined in the form of parameterized library components for the *Cadence PSpice* simulator. Examples are given illustrating the proposed approach.**
Keywords: Fault Modeling/ Circuit Simulation/PSpice

I. INTRODUCTION

A very important stage in the realization of electronic circuit consists of testing the product. The testing phase is aimed at the verification that the circuit meets all the design specifications. Besides the final tests, intermediate tests are normally executed to verify the behavior of single parts of the circuit and identify possible causes of fault or malfunctioning.

Recently, due to the exploding telecommunications market, as well as markets for consumer and automotive electronics, more and more mixed-signal devices are being designed, integrating digital and analog components on a single chip in order to improve performance and reduce board size and cost. In the production of these circuits, testing can be a limiting factor, contributing significantly to manufacturing cost [1]. A typical strategy for testing a mixed-signal chip involves, when possible, first testing the digital and analog components, followed by some system tests to check the at-speed interaction among components. The digital parts will be tested with standard methods, aided by software for automatic test pattern generation, scan chains, and built-in self test (BIST), which has become mature and cost effective. Yet, diverse design styles and a multitude of response parameters make analog circuit testing difficult and expensive. This motivates research in structured fault-based approaches [2]-[5]. In such approaches, fault models capture the effect of physical defects on circuit behavior, fault simulation evaluates the detection capabilities of a test set on a set of faults (and measures fault coverage), and test generation derives a minimal test set to detect those faults.

In this paper a model-based approach to automatic diagnosis of parametric (soft) faults in analog circuits using general purpose circuit simulators is proposed. The advantage of *PSpice*-like circuit simulators is the universal working interface combined with flexible and fast program tools [8, 9, 10]. The large possibilities of the input language, the wide range libraries of adequate component models, as well as the possibilities of post-processing in the graphical analyzer *Probe* allow the realization of effective diagnosis algorithms.

Parameterized faulty models for generation of parametric faults in the circuit elements are developed and the computer realization in the form of parameterized library elements for the *Cadence PSpice* simulator is presented in Section II. The diagnosis approach is given in Section III. The feasibility of this approach is demonstrated by diagnosis of a benchmark circuit and a PID regulator circuits in Section IV.

II. PARAMETERIZED FAULT MODELS

The parametric faults are deviations of component values, resulting in a failure of some circuit specifications. The proposed faults are deviations of ±20% and ±50% from the nominal values of the passive components. These faults seem to be distributed well enough in order to cover a possible set of typical faults [6, 7].

Each of the passive elements is characterized by the attributes M20, P20, M50 and P50, defining a deviation from the nominal value of -20%, +20%, -50% and +50% correspondingly. A fault number F_i, $i = 1, 2, \ldots, m$ is assigned to each of the attributes M20, P20, M50, P50, where m is the total number of the faults modeled.

A parametric analysis is used for the fault generation, whose parameter is the number of the fault.

A. Model of Faulty Resistor

The model of a faulty resistor R_f is shown in Fig.1a, where the element ΔR models the deviation from the nominal value R_{nom} in the case of a fault. The simulation model of ΔR is shown in Fig.1b, using voltage controlled current source (VCCS). The value of the controlling parameter g is represented in Table 1 in respect to the deviation from the nominal value.

TABLE I.

VALUES OF THE CONTROLLING PARAMETER IN THE RESISTOR MODEL

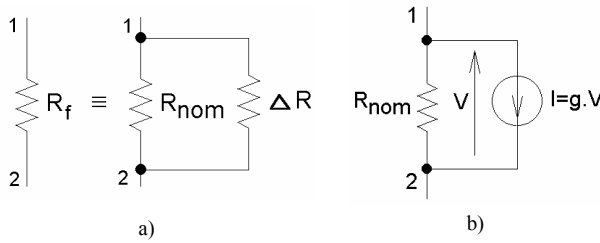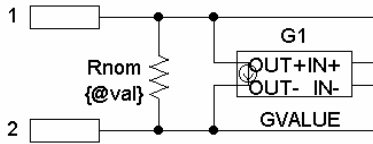| g	R_f
$0.25/R_{nom}$	R_{nom}–20% R_{nom}
$1/R_{nom}$	R_{nom}–50% R_{nom}
$-1/(6R_{nom})$	R_{nom}+20% R_{nom}
$-1/(3R_{nom})$	R_{nom}+50% R_{nom}
0	R_{nom}

Figure 1. Model of faulty resistor

Figure 2. Computer realization of the faulty resistor model

The computer realization of the faulty resistor model is performed in the graphical editor *Cadence Capture* using a block definition as shown in Fig. 2.

A voltage controlled current source of GVALUE type is used to define the controlling parameter g modeling the fault (Table I). This source type allows the inclusion of the IF_THEN_ELSE statement in the expression for the controlling parameter g in order to define the corresponding deviation. The current of the source VCCS has the form:

V (%IN+, %IN-)* if(@M20==@par,0.25/@val,
         if(@M50==@par,1/@val,
         if(@P20==@par,-1/(6*@val),
         if(@P50==@par,-1/(3*@val),0))))

Where *val* is the nominal value of the element and *par* = 1,2,…,*m* is the number of the modeled fault.

B. Model of Faulty Capacitor

The model of a faulty capacitor Cf is shown in Fig. 3a, where the element ΔC models the deviation from the nominal value in case of a fault. The model of ΔC is shown in Fig. 3b. The current controlled current source (CCCS) I1=1.I_C and the voltage controlled voltage source (VCVS) $V_1=k.V$ model the component equation of the element ΔC :

$$i_1(t) = 1.i_c(t) = k\frac{dv(t)}{dt} \qquad (1)$$
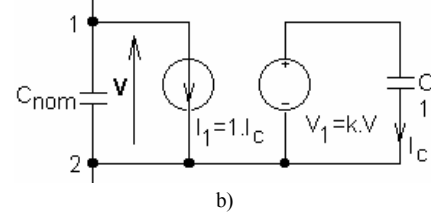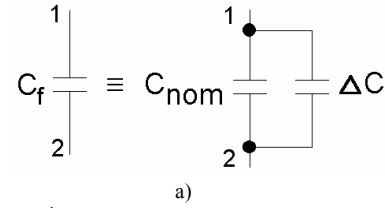

a)
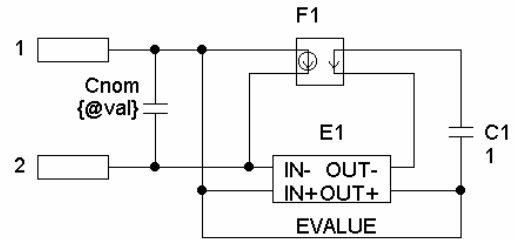

b)

Figure 3. Model of faulty capacitor

Figure 4. Computer realization of the faulty capacitor model

TABLE II.

VALUES OF THE CONTROLLING PARAMETER IN THE CAPACITOR MODEL

κ	C_f
$-0.2C_{nom}$	C_{nom}–20% C_{nom}
$-0.5C_{nom}$	C_{nom}–50% C_{nom}
$0.2C_{nom}$	C_{nom}+20% C_{nom}
$0.5C_{nom}$	C_{nom}+50% C_{nom}
0	C_{nom}

The computer realization of the faulty capacitor model is performed in the graphical editor *Cadence Capture* using a block definition as shown in Fig. 4.

The voltage controlled voltage source of *EVALUE* type is used to define the controlling parameter k modeling the fault. The value of the parameter k depends on the deviation. It is shown in Table II.

This source type allows the inclusion of the IF_THEN_ELSE statement in the expression in order to define the corresponding deviation. The voltage of the source VCCS has the form:

V(%IN+, %IN-)*if(@M20==@par,-0.2*@val,
        if(@M50==@par,-0.5*@val,
        if(@P20==@par, 0.2*@val,
        if(@P50==@par,0.5*@val,0))))

C. Model of Faulty Inductor

The model of a faulty inductor L_f is shown in Fig. 5a, where the element ΔL models the deviation from the nominal value in case of a fault. The model of ΔL is shown in Fig. 5b.
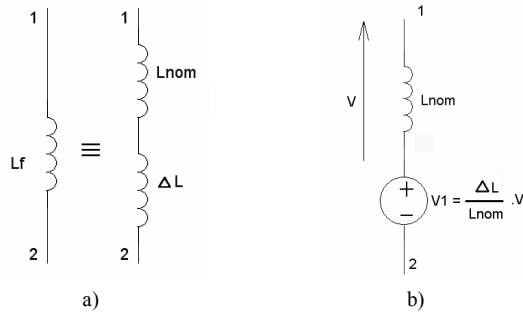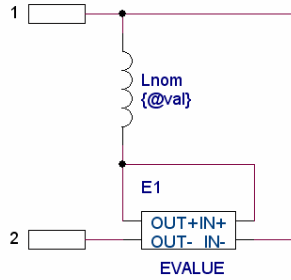
Figure 5.   Model of faulty inductor

Figure 6.   Computer realization of the faulty inductor model

The voltage controlled voltage source (VCVS) $V_1=k.V$ models the component equation of the element ΔL:

$$v_1(t) = \Delta L \frac{di_L(t)}{dt} = \frac{\Delta L}{L_{nom}} v(t) \qquad (2)$$

The computer realization of the faulty inductor model is performed in the graphical editor *Cadence Capture* using a block definition as shown in Fig. 6.

The voltage controlled voltage source of *EVALUE* type is used to define the controlling parameter $k = \Delta L / L_{nom}$ modeling the fault (Table III). The voltage of the source VCCS has the form:

V(%IN-, %IN+)*if(@M20==@par,-0.2,
        if(@M50==@par,-0.5, if(@P20==@par,0.2,
        if(@P50==@par,0.5,0))))

Based on computer models of the faulty elements, shown in Fig. 2, Fig. 4 and Fig. 6, parameterized library elements for the fault generation are created in the powerful graphical editor *Capture*. Based on these elements, automatic diagnosis can be performed by the user.

III.   AN AUTOMATIC FAULT DIAGNOSIS APPROACH

The proposed diagnosis approach of parametric faults in analog circuits is a model-based method. The developed faulty models of the passive components are used. The proposed faults to be detected are deviations of ±20% and ±50% from the nominal values of the passive components.

The dimensioning of the input stimulus and the observed and measured output signal by which the faults are best characterized is in accordance with the methodology presented in [7]. The test input signal is a saturated ramp.

TABLE III.

VALUES OF THE CONTROLLING PARAMETER IN THE INDUCTANCE MODEL

κ	L_f
-0.2	L_{nom}–20% L_{nom}
-0.5	L_{nom}–50% L_{nom}
0.2	L_{nom}+20% L_{nom}
0.5	L_{nom}+50% L_{nom}
0	L_{nom}

Since the ramp is a compressed test waveform that consists of many frequency components, the transient response depends on the system poles and zeros. Therefore, the movement of poles and zeros under a fault will potentially affect the transient and steady-state characteristics. The goal is to stimulate the fault circuit with the input that maximizes the error in the response. Under a fault–production condition, the time response parameters that vary widely from the fault-free values are "steady state", "delay", "rise time" and "overshoot". The target is to obtain as much different time response output parameters of the faulty variants of the circuit as possible, and that imposes the dimensioning of the parameter "rise time" and the amplitude of the input test signal.

Let the parameters of the circuit response used to characterize the faults be denoted as follows:

1. Steady state voltage V_{st} : ST;

2. Overshoot: OV;

$$OV = \frac{V_{\max} - V_{st}}{V_{st}}.100 \qquad (3)$$

3. Rise time TR;
4. Delay time TD.

These parameters can be calculated in the graphical analyzer *Probe*. The determination is facilitated using the available macro-definitions included in *Probe*.

After having completed parametric analysis, where the fault number F_i is defined as a parameter ($i = 1,…,m$), the calculated parameters are used for creating a fault dictionary and for detecting faults in the circuit under test.

The fault identification is based on the calculation of the relative difference of the measured parameters and the parameters corresponding to the fault F_i.

The measured time response parameters of the circuit under test *ST, OV, TR, TD* are available. After the parametric time domain simulations, the parameters ST_i OV_i , TR_i and TD_i corresponding to the fault F_i ($i = 1,2,…,m$), are calculated. The relative difference of the measured   parameter   *ST*   and   the   parameter ST_i corresponding to the fault F_i is:

$$ST_{ri} = \frac{ST - ST_i}{ST_i} \qquad (4)$$

Similarly, the relative differences OV_{ri} , Tr_{ri} and TD_{ri} are obtained.

In the case where the fault of the circuit under test and the simulated defect coincide, the relative difference will be minimal (in the ideal case this value is zero). The complex indicator of a defect is the total mean square difference (distance) S_i:

$$S_i = \sqrt{ST_{ri}^2 + OV_{ri}^2 + TR_{ri}^2 + TD_{ri}^2} \qquad (5)$$

The value of S_i (i) equals zero when $\boldsymbol{i}$ is the number of the modeled defect, which coincides with the defect in the circuit under test. In this way, automatic diagnosis of the faulty component is performed and the faulty element is identified in the circuit under test. Because of the design tolerances, the fault is selected when the function $S_i(i)$ has its minimum.

The distance S_i is automatically calculated using post-processing by corresponding macro-definitions in the graphical analyzer *Probe*. The syntax of the macros for the given example is presented in Section IV).

The basic steps of the proposed diagnosis approach are shown in Table IV.

TABLE IV.

BASIC STEPS FOR THE PROPOSED DIAGNOSIS APPROACH

1.Draw a circuit with faulty models of passive elements in *Cadence Capture*;
2.Make Ramp Test Generation and Find the best ramp or collection of ramps;
3.Insert measured values for ST, OV, TR, and TD of the circuit under control by including DC voltage sources in the modeled faulty circuit;
4.Using the selected stimulus; execute parametric simulations in the time domain;
5.Calculate in *Probe* each of time response parameters ST_I, OV_i, TR_i, TD_i, and the distance S_i using the created macro- definitions;
6.Create a fault dictionary for every saturated ramp input;
7.Determine the ambiguity groups;   Find the faulty elements.

This approach can be applied when the deviation of the passive component in the circuit under test does not coincide with the determined faults (±20%, ±50%). In this case the diagnostic procedure detects the fault classifying it within the closest modeled fault of the element or ambiguity group in which it is included.

In comparison with the existing standard methods using time response parameters the advantage of the diagnostic method proposed is the usage of a standard circuit simulator instead of specialized software. The approach allows automation of the diagnostic process by using parametric analysis. Moreover, the exact models of electronic devices existing in the standard circuit simulators allow precise modeling of the circuit characteristics under test, which in turn leads to adequate diagnostics.

IV.   EXAMPLES

Two examples for the feasibility of the proposed diagnosis approach are given for the fault identification in a benchmark circuit and in a PID regulator.

A. *Diagnosis of benchmark circuit of biquadratic filter*

The schematic diagram of biquadrate filter is shown in Fig. 7. It is used as a benchmark circuit in [6,7]. The input signal is a ramp function. A ramp input with a saturation value of 1V and a rise time of $100\mu s$ has been chosen.

The proposed faults to detect are deviations of ±20% and ±50% from the nominal values of the passive components (a set of 32 faults).

Taking the case R_2-20% , for example, while other components stay at their nominal value, the measured parameters are:

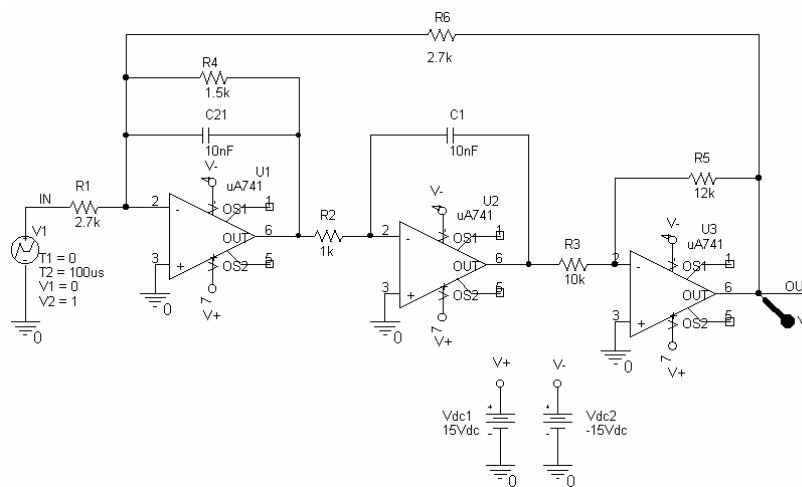$ST = -0.99V$, $OV = 5,31\%$, $TR = 79.4\mu s$, $TD = 12.5\mu s$

Figure 7.   Benchmark example circuit

The measured values of the characteristics *ST, OV, TR* and *TD* are introduced in the diagnosis model using independent sources of *VDC* type. In this way, they are represented in the model by the corresponding node voltages *V(ST), V(OV), V(TR)* and *V(TD)*.

The following built in *Probe* functions are used: **Risetime**; **Overshoot**; **AVGX(1,X_value)** – for definition of the average value in the defined time interval to determine "steady state", and **XatNthY** (Value of X corresponding to the nth occurrence of the given Y_value, for the specified waveform) – to determine "delay".

The determination of the parameters TR_{ri}, OV_{ri}, ST_{ri}, TD_{ri}, according to (4), and S_i, according to (5), is automatically performed using post-processing in the graphical analyzer *Probe*. The macro-definitions TRr, OVr, STr and TDr are created and used for this purpose.

Using function **Rise time** *(the time for which the output signal rises from 10% to 90% of its max value),* the macro for the relative difference of the measured parameter V(TR) and the parameter Risetime(-V(OUT)) of the diagnostic model is:

TRr = abs(max(V(TR))-Risetime(-V(OUT)))/
    Risetime(-V(OUT))

By analogy, using **Overshoot** function**:**
OVr = abs(max(V(OVSH))-Overshoot(-V(OUT)))/
    Overshoot(-V(OUT))

Using **AVGX** function for **steady state** *(value at the end of the measuring window)*:
STr = abs(max(V(ST))-max(AVGX(-V(OUT),1ms)))/
    max(AVGX(-V(OUT),1ms))

Using functions *AVGX* and *XatNthY* for the parameter **delay** *(Interval of time between input and output signals at 50% of their max. value)*:
*output signal delay DOp
Diff = 0.5*max(AVGX(-V(OUT),1ms))+V(OUT)
DOp=XatNthY(Diff,0,1)
*input signal delay DIp
DIp = XatNthY(V(IN),0.5,1)
DO1p=max(V(DO))
DEL = DOp-DIp
DEL1 = DO1p-Disp
*relative difference of the delay time
DELr = abs(DEL-DEL1)/DEL

The macro for the distance S_i according to (5) is:
SUMrms = sqrt(TRr* TRr +STr* STr +OVr* OVr +
    DELr* DELr)

The obtained results are presented in Table V. It is seen that faults R₂-20%, R₃-20% and C₁-20% have the same attributes and it is impossible to distinguish between them using the measures (1÷4). Hence, the corresponding faults (F5, F9, F25) form an ambiguity group. In the same way, ambiguity groups [R₂+20%, R₃+20%, C₁+20%]

(faults F6, F10, F26), [R₂-50%, R₃-50%, C₁-50%] (faults F7, F11, F27) and [R₂+50%, R₃+50%, C₁+50%] (faults F8, F12, F28) are formed. The results for the ambiguity groups determination correspond to the obtained in [6].

The results of the fault modeling using parametric analysis are presented in Fig. 8. The output response is shown in Fig. 8b and the distance *SUMrms = f(par)* is represented in Fig. 8a, where *par* is the fault number.

The minimal value of SUMrms is for *par*=5, corresponding to the fault F5 (R2-20%). The obtained result is in a good agreement with the diagnosis results for this benchmark circuit obtained in [6].

TABLE V.
DIAGNOSIS RESULTS FOR THE BENCHMARK CIRCUIT

| F_i	value	S_i	F_i	Value	S_i
0	nom	0.2416	17	R₅-20%	0.4242
1	R₁-20%	0.3136	18	R₅+20%	0.0472
2	R₁+20%	0.3137	19	R₅-50%	1.2043
3	R₁-50%	0.5569	20	R₅+50%	0.3144
4	R₁+50%	0.5547	21	R₆-20%	0.2500
5	R₂-20%	**2.93e-7**	22	R₆+20%	0.4412
6	R₂+20%	0.3928	23	R₆-50%	1.4992
7	R₂-50%	1.0279	24	R₆+50%	0.6644
8	R₂+50%	0.5685	25	C₁-20%	**5.48e-4**
9	R₃-20%	**7.79e-3**	26	C₁+20%	0.3927
10	R₃+20%	0.3942	27	C₁-50%	1.0519
11	R₃-50%	1.1365	28	C₁+50%	0.5682
12	R₃+50%	0.5733	29	C₂-20%	0.4526
13	R₄-20%	0.8661	30	C₂+20%	0.3218
14	R₄+20%	0.1684	31	C₂-50%	2.4186
15	R₄-50%	1.18e5	32	C₂+50%	0.5252
16	R₄+50%	0.2990			
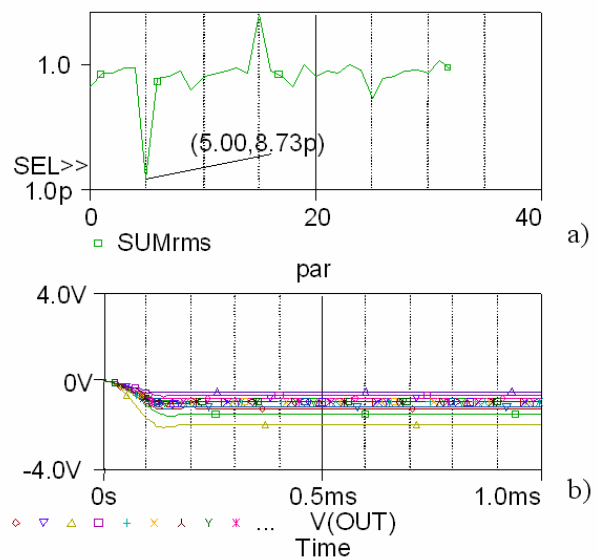
Figure 8.   Diagnosis results of the fault F5 in the benchmark circuit

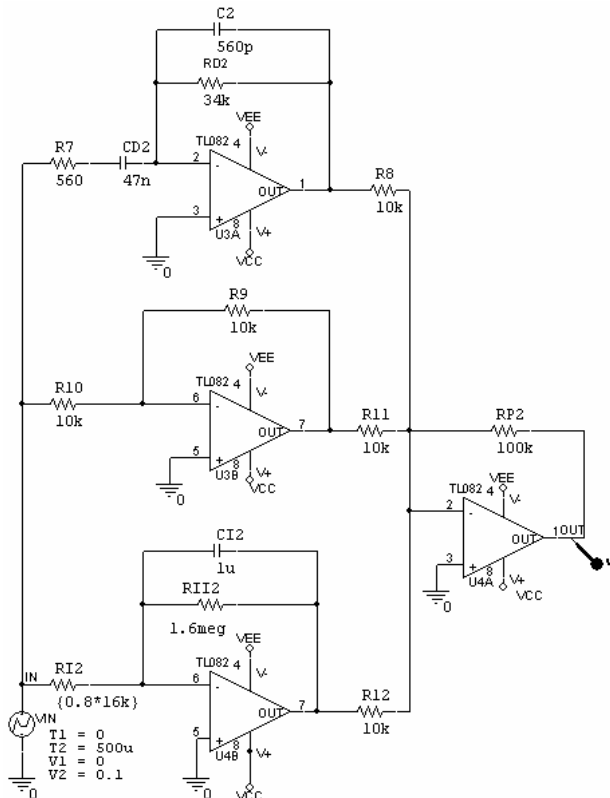Figure 9. PID regulator circuit under test

Figure 10. Diagnosis results for the fault F33 in the PID regulator

B. PID regulator diagnosis

The schematic diagram of the PID regulator under test is shown in Fig. 9. The proposed faults to detect are deviations of $\pm 20\%$ and $\pm 50\%$ from the nominal values of the passive components (a set of 52 faults).

Having completed preliminary simulations the most informative parameters of the input test signals are defined. The input signal is a saturated ramp with rise time TR=0.4 ms and amplitude of 0.1V.

A fault RI2-20% (par=33) is set. The obtained graphical results are shown in Fig. 10. The minimal value of the distance function SUMrms is at par =33. To detect RI2 without an ambiguity, the input ramp should be slower one (in the range of seconds). Several ramps could be necessary for a complex system (step 6 in the basic steps).

V.   CONCLUSIONS

A model-based approach to automatic diagnosis of electronic circuits using *Cadence PSpice* has been proposed. Parameterized computer models of the faulty elements have been developed. The fault generation is reduced to a parametric analysis of the circuit. The results of the fault detection and the ambiguity groups determination of the benchmark circuit confirm the possibilities and applicability of the proposed diagnosis approach.
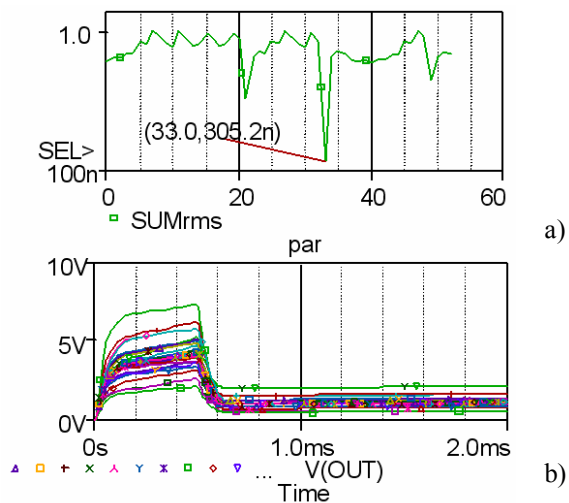
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