Harmonic Balance Surrogate-Based Immunity Modeling of a Nonlinear Analog Circuit

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***Abstract*—Electromagnetic compatibility-aware design of microelectronic circuits is a challenging task as it involves fulfilling strict requirements concerning conducted and radiated emission and immunity levels. Therefore, the need for fast and accurate behavioral models predicting, in the early design stage, the circuit performance during emission or immunity tests, arises rapidly. Hence, in this paper, a new harmonic balance surrogate-based technique to create immunity models of a nonlinear analog circuit is proposed, which hide the real netlist, reduce the simulation time and avoid expensive and time-consuming measurements after tape-out, while still providing high accuracy. The resulting immunity model can be easily integrated into a circuit simulator together with additional subcircuits, e.g. board and package models, as such allowing to efficiently reproduce complete immunity test set-ups during the early design stage and without disclosing any intellectual property. The novel method is validated by means of application to an industrial case study, being an automotive voltage regulator, clearly showing the technique's capabilities and practical advantages.**

***Index Terms*—Immunity model, surrogate modeling, harmonic balance, direct power injection (DPI) test, voltage regulator.**

I. Introduction

ADVANCED miniaturization and increasing complexity of integrated circuits (ICs) pose many electromagnetic compatibility (EMC) challenges for designers of modern microelectronic circuits. As radiated and conducted emission and immunity properties of microelectronic components must be precisely controlled, international EMC standards have been developed and are still evolving. For example, starting in 2002 the International Electrotechnical Commission (IEC) has been publishing families of standards for ICs, specifying measurement methods from 150 kHz to 1 GHz for emission [1] and immunity [2].

Furthermore, EMC-aware application designers more and more demand emission and immunity models from their application-specific integrated circuit (ASIC) vendors. Such models enable them to make EMC assessments during the design phase, i.e. at a stage when modifications can be applied in limited time and with relatively small costs. Hence, recent research has been devoted to creating such models, in particular focusing on modeling the immunity of ICs to radio frequency (RF) noise during the direct power injection (DPI) test [3]. In [4], the authors suggest to mimic the results of a DPI test of the manufactured IC by modeling the printed circuit board (PCB) using measured scattering parameters and concatenating them with a simplified circuit model of the IC. This allows to approximately predict the performance of the circuit, provided it is not too complex. A second approach relies on performing DPI measurements and fitting a mathematical model to the collected data, using Neural Networks (NN) [5]–[7]. The obtained model hides the original netlist of the circuit, allowing the ASIC vendor to provide this model to the customers without disclosing any intellectual property (IP). The main drawback of this method is, however, that it requires manufacturing and measuring the IC to generate the model. Moreover, the model represents the behavior of the IC including the effect of the PCB and package. Hence, as there is no model available for the bare IC (die), the model is only valid for this particular DPI configuration. Another technique [8], [9] proposes to use simulations that include the netlist of the IC and equivalent circuit models for the DPI test set-up (signal generator, PCB, package, etc.) to predict measurement results. Since the model is based on simulated data, this method does not require manufacturing and measuring the IC, which speeds up the process and reduces the costs. The disadvantage lies in the usage of the original netlist of the IC, as for this reason, the method can only be used by the IC manufacturer himself, who does not want to share his IP.

In this paper we propose a new technique to create an accurate immunity model of an analog IC, which can then be used within a complete immunity test setup. The novelty of our approach is twofold. First, the model relies on surrogates, constructed using Artificial Neural Networks (ANN), which replace the real netlist, as such concealing the IP of the manufacturer. Second, the data are collected by means of Harmonic Balance (HB) simulations [10], allowing to model both the functional and the noisy behavior of the nonlinear circuit in the frequency domain, as such making it ideally suited for efficient immunity simulations such as DPI [3], bulk current injection (BCI) [11], [12], etc. Hence, the immunity model can be used by both the ASIC designer and by the application designer. The former can use the model to make his/her IC more robust; the latter may rely on the model to take the necessary precautions, such as placing decoupling capacitors, at the board level. Moreover, since in the end the model is merely a mathematical expression, it can be evaluated very rapidly, allowing for efficient optimizations by, e.g., the

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board designer.

This paper is organized as follows. In the next section we propose the model architecture, which comprises several components (building blocks). Section III presents the construction of the surrogates for these model components, using ANNs. In Section IV, the generated surrogates are shown, as well as the complete immunity model. The model is further used in an application by integrating it into a popular circuit simulator, allowing to validate the modeling accuracy and efficiency by first considering the bare IC and by further combining it with equivalent models for a typical PCB, used during a DPI test. Conclusions are summed up in Section V.

II. Model architecture

To clearly explain our immunity modeling approach, we first briefly describe how immunity tests for ICs are typically performed. In this paper, we are not considering transient tests, such as IEC 62215-2 synchronous transient injection [13], but frequency domain tests, such as, e.g., IEC 62132-4 DPI [3] and IEC 62132-3 BCI [11]. For these EMC tests, the device-under-test (DUT), i.e. the IC, is placed on a PCB, together with all the components that are required to let this DUT function properly. Additionally, sinusoidal RF noise is injected into the DUT while its performance is being monitored. The frequency and power of this RF noise are varied, following the specific EMC standard. For example, for the IEC 62132-4 DPI test [3], the frequency is swept from 150 kHz to 1 GHz and the power is varied between 0 dBm and 30 dBm. If the examined characteristics of the DUT remain within preset specifications for the complete frequency and power range, then the DUT passes the test. If not, the maximum power levels at which the DUT still functions properly are recorded, allowing the engineers to adapt the IC's circuitry or to take other precautions, e.g., at the board level.

With the technique proposed in this paper, a behavioral immunity model of the circuitry of the IC is constructed that accurately describes both the functional and the noisy behavior. The goal is that this model can then later be used within a complete set-up of the EMC immunity test, such as DPI or BCI, and hence, specific modeling assumptions have to be made to achieve this goal (see further). To develop our technique an important test case has been chosen, i.e. an automotive voltage regulator (VR) that is being designed by Melexis Technologies N.V., Belgium. This novel DUT, which has not even been taped-out yet, is called MLXTC883 and its netlist consist integrated active and nonlinear components, i.e. 21 transistors, and 123 passive components (resistors and capacitors). This device has been especially selected because of its highly nonlinear behavior and to immediately demonstrate the accuracy and efficiency of our novel modeling method when applied to a state-of-the-art commercial product. In its intended automotive application, the VR MLXTC883 is connected to a 5V DC supply, which it converts into a stable 3.3V DC output voltage. However, it is well-known that VRs are susceptible to RF noise at their DC supply pin [14], (note, however, that in [14] a simplified linear model was constructed). In the specific case of the MLXTC883, it is observed (see Section IV) that for particular values of noise frequency and power, a significant drop of the output voltage occurs.

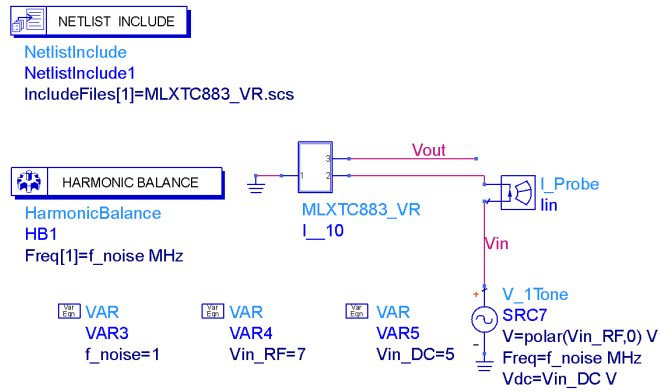


Fig. 1. Schematic used for Harmonic Balance simulation of the voltage regulator.

To start constructing the immunity model of this IC, first, all necessary data are collected. Here we opt to use Agilent's Advanced Design System (ADS) for this task, using the circuit schematic depicted in Fig. 1. The block that contains the entire netlist of the MLXTC883 VR is connected to a voltage source. This voltage source produces a waveform:

$$V_{in}(t) = V_{in,DC} + V_{in,RF}\sin(2\pi f_{noise}\, t), \qquad (1)$$

which is the superposition of (i) the 5V DC component $V_{in,DC}$ that is part of the circuitry necessary for the correct operation of the VR, and (ii) the sinusoidal RF noise, with a variable noise frequency f_{noise} and amplitude $V_{in,RF}$. This waveform (1) will allow us to construct a parameterized immunity model as described in the beginning of this section, i.e. allowing to vary f_{noise} and $V_{in,RF}$, and is thus ideally suited for our goal. For this case study and as in an actual DPI test we assume that the DC input voltage $V_{in,DC}$ is fixed as we want to concentrate on the immunity against RF noise.

Now, while sweeping f_{noise} and $V_{in,RF}$, HB simulations are performed, as this allows the full analysis of a nonlinear circuit, subject to sinusoidal RF noise. During the simulations, the voltage V_{out} at the output pin is being observed as well as the input current I_{in}. In general, apart from DC, all harmonics f_{noise}, $2f_{noise}$, $3f_{noise}$, etc, can be observed and modeled. In practice, this will not always be necessary for our goal, which is an accurate description of an immunity test. For the presented case study, the higher order harmonics ($f \geq 2f_{noise}$) of I_{in} and V_{out} can be ignored, as tests have shown that the influence of these harmonics is negligible. The results of one representative test are depicted in Fig. 2, where the DC component and harmonics up to order five are shown for the input current and output voltage, using a noise amplitude $V_{in,RF} = 7$ V and noise frequency $f_{noise} = 1$ MHz. It is demonstrated in Fig. 2(a) that all higher order harmonics of I_{in} are at least 10 dB lower than the first harmonic. Hence, we will not consider these harmonics in our model. Moreover, no significant harmonics are found at the output of the VR

(Fig. 2(b)) because of the inherent filtering characteristics of the circuit, which apparently behaves as a low-pass filter.

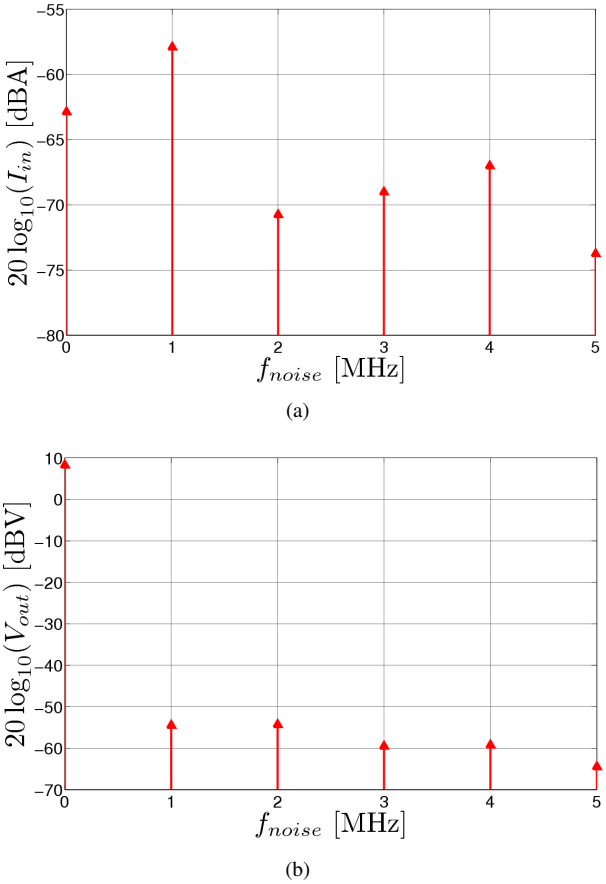


Fig. 2. Representative example of the DC component and the harmonics of (a) I_{in} and (b) V_{out}.

Therefore, for the specific case of constructing an immunity model for the MLXTC883, at the input, the DC current and the first harmonic are recorded, approximating the total input current as follows:

$$I_{in}(t) \approx I_{in,DC}(f_{noise}, V_{in,RF}) + I_{in,RF,1}(f_{noise}, V_{in,RF}) \sin(2\pi f_{noise}\, t). \quad (2)$$

Note that both the DC component $I_{in,DC}$ and the first harmonic $I_{in,RF,1}$ depend on the noise frequency and amplitude, indicating the nonlinear behavior of the VR. For a fixed $V_{in,DC}$ and a varying $V_{in,RF}$ we now define input impedances of the voltage regulator for DC and the first harmonic as follows:

$$R_{in,DC}(f_{noise}, V_{in,RF}) = \frac{V_{in,DC}}{I_{in,DC}(f_{noise}, V_{in,RF})}, \quad (3)$$

$$Z_{in,RF,1}(f_{noise}, V_{in,RF}) = \frac{V_{in,RF}}{I_{in,RF,1}(f_{noise}, V_{in,RF})}. \quad (4)$$

These input impedances constitute two essential components (building blocks) of our immunity model, because, during an immunity test (and also in its intended application), the RF noise is not delivered using a perfect voltage source nor is it directly connected to the VR. The input impedances (3) and (4) will make sure that the current I_{in} flowing into the VR remains correct, also when a $50\,\Omega$ power source is used instead of a perfect voltage source and when the VR is packaged and placed on a PCB including additional components at its input (see Section IV-C and IV-D). At the output, the DC output voltage is approximated as

$$V_{out}(t) \approx V_{out,DC}(f_{noise}, V_{in,RF}), \quad (5)$$

modeling the nonlinear response of the voltage regulator in the presence of the injected RF noise, and representing the third essential component of our model.

All this, together with the fact that the next stage — connected at the output pin— is high-impedant, both in its intended automotive application and in immunity test setups, leads to the model architecture proposed in Fig. 3. It is immediately clear that, if necessary, the model architecture can be extended by adding more components, as such taking more harmonics at the input and/or at the output into account. In order not to complicate the matter and to clearly explain and illustrate our modeling paradigm, in this paper we further focus on the architecture of Fig. 3. The validity of this architecture will be clearly demonstrated *a posteriori* in Section IV, where it is shown that it is perfectly suited to achieve our goal. In the next section, first, surrogates for the three model components $R_{in,DC}$, $Z_{in,RF,1}$ and $V_{out,DC}$ are created.

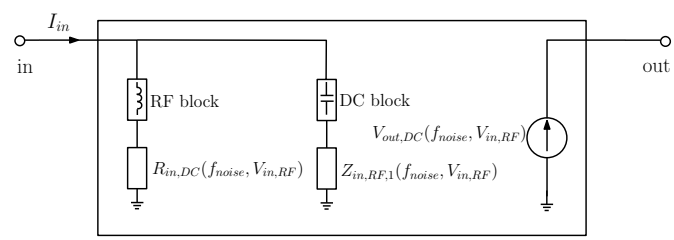


Fig. 3. Architecture of the voltage regulator's HB surrogate-based immunity model, illustrating the several components (building blocks).

III. Construction of Surrogates

It has become more and more popular among electronic engineers to substitute a real circuit by a less computationally intensive approximation, called a surrogate [15]–[17]. This is mainly done because surrogates allow to significantly expedite the simulations, compared to the time needed to analyze the original circuitry, while still providing sufficient accuracy. Construction of such surrogates is, however, not always a trivial task, as it requires the careful selection of many model parameters, such as surrogate type, measure and error function, number of samples and sampling scheme, etc.

To reliably describe the functional and immunity behavior of the VR MLXTC883, surrogates for the three components $V_{out,DC}(f_{noise}, V_{in,RF})$, $R_{in,DC}(f_{noise}, V_{in,RF})$ and $Z_{in,RF,1}(f_{noise}, V_{in,RF})$ are constructed. As a surrogate type, artificial neural networks (ANNs) are chosen, since they are very well suited to model functions with sharp nonlinearities [18]. A five-fold cross validation measure [19] is used to assess

the accuracy of the surrogates. Cross validation temporarily retrains a surrogate several times with different subsets of data (called folds) and assigns an error to each fold using an error criterion. The final accuracy error is then taken to be the mean over all folds. In this paper, the desired final accuracy error is set to $3 \cdot 10^{-3}$ for the surrogates of all components, which is sufficiently low for our needs (see Section IV). The error criterion, used to estimate the error of each fold, is calculated using the formula:

$$error_{fold} = \sum_{i=1}^{N_{fold}} w_i (s_i - s_{model,i})^2, \tag{6}$$

where w_i is the weighting factor, s_i is the value of the component for data sample i of that particular fold, obtained by means of the HB simulations described in Section II, $s_{model,i}$ is the value of the component obtained by evaluating the cross validated surrogate for the same sample, and N_{fold} is the number of samples in that fold. The weighting factor is assigned to the samples according to the rule:

$$w_i = \begin{cases} 10\,, & |3.3\text{ V} - s_i| \leq 0.15\text{ V} \\ 2\,, & 0.15\text{ V} < |3.3\text{ V} - s_i| \leq 0.5\text{ V} \\ 1\,, & 0.5\text{ V} < |3.3\text{ V} - s_i| \leq 1\text{ V} \\ 0.1\,, & 1\text{ V} < |3.3\text{ V} - s_i| \end{cases} \tag{7}$$

where 3.3 V is the desired value of $V_{out,DC}$, i.e., the proper functional behavior in the absence of RF noise. By applying this kind of weighting (7), the modeling efforts are most focused towards the critical region around 3.3 V, where the VR just passes or fails an immunity test. Less attention is paid to regions where $V_{out,DC}$ really differs from 3.3 V, i.e. where the circuit fails badly anyway. In this way, the construction time of all surrogates is kept low, while still providing enough accuracy where needed. The initial surrogates are created starting from data obtained by a Latin Hypercube Design [20]. Subsequently, the surrogates are updated with new samples selected by the highly adaptive Lola-Voronoi algorithm [21] that makes a trade-off between equally filling up the design space and selecting data points from nonlinear regions.

It will also be shown in Section IV that the components $R_{in,DC}$ and $Z_{in,RF,1}$ vary over a large range, extending several orders of magnitude. Therefore, surrogates can either be built for (i) $R_{in,DC}$, $Re(Z_{in,RF,1})$ and $Im(Z_{in,RF,1})$ or (ii) $\log_{10}(R_{in,DC})$, $\log_{10}(Re(Z_{in,RF,1}))$ and $\log_{10}(-Im(Z_{in,RF,1}))$. The former surrogates will be called "linearly scaled surrogates" in Section IV. The latter are called "logarithmically scaled surrogates", and their modeling range is obviously much reduced, thanks to the logarithmic compression. Note also that, as the imaginary part of $Z_{in,RF,1}$ is always negative for this VR, a pertinent change of sign is introduced before compressing.

IV. Results

A. Surrogates

The Lola-Voronoi sampling algorithm adaptively selected 252 samples in the $(f_{noise}, V_{in,RF})$ design space. For these samples, HB analyses are performed in ADS (see Fig. 1) and the surrogates for $R_{in,DC}$, $Z_{in,RF,1}$ and $V_{out,DC}$ are

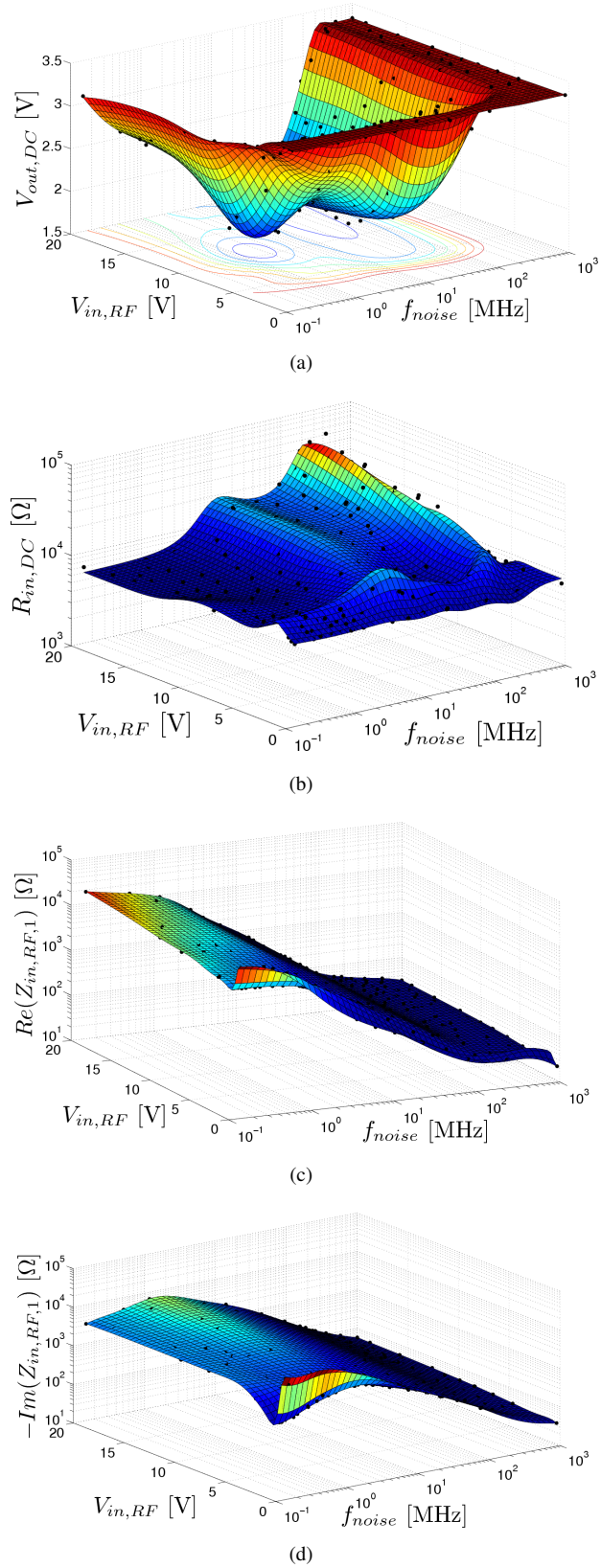


Fig. 4. ANN surrogates (colored surface plots) of the output voltage and input impedances, using 252 samples (black dots) obtained by HB simulations of the original netlist. (a) $V_{out,DC}(f_{noise}, V_{in,RF})$ (b) $R_{in,DC}(f_{noise}, V_{in,RF})$ (c) $Re(Z_{in,RF,1}(f_{noise}, V_{in,RF}))$ (d) $-Im(Z_{in,RF,1}(f_{noise}, V_{in,RF}))$

constructed, all simultaneously reaching the desired cross-validation target accuracy of $3 \cdot 10^{-3}$. This complete process took 4 h 51 min on a computer with an Intel(R) Core(TM)2 Quad Q6700 CPU @ 2.67 GHz, 8 GB of RAM, and a 64-bit Windows Vista operating system. The results of this surrogate modeling process are shown in Fig. 4, where the black dots indicate the samples obtained by ADS using the original netlist of the MLXTC883 and the colored surface plots represent the ANN surrogates. As observed from Fig. 4(a), at lower frequencies, $V_{out,DC}$ rapidly decreases when the magnitude of the RF noise increases above 5 V. For frequencies higher than 100 MHz, the VR exhibits better immunity characteristics. Indeed, in that region $V_{out,DC}$ remains stable despite the presence of the noise. Note that for clarity of the figures, in Figs. 4(b), 4(c) and 4(d), the values are displayed in a logarithmic scale. Hence, as already stated in Section III, the DC input impedance (Fig. 4(b)) varies over quite a large range, but always remaining rather high. From Figs. 4(c) and 4(d), depicting the real and minus the imaginary part of $Z_{in,RF,1}$, respectively, it becomes apparent that this impedance also varies over a very large range, going from very high to very low values with increasing frequency.

B. Model verification - bare voltage regulator

We now integrate the model architecture of Fig. 3, where the components $R_{in,DC}$, $Z_{in,RF,1}$ and $V_{out,DC}$ are replaced by their ANN surrogates, into the circuit simulator ADS (Fig. 5), using the frequency-domain defined device (FDD) block (in contrast to [22] and [23], where a time-domain suited Symbolically Defined Device (SDD) block is used). It is important to mention here that this FDD block allows to describe current and voltage spectral values for nonlinear circuits defined by the user, as such making it ideal for the very efficient implementation of frequency domain immunity models, as envisaged in this paper and often required in industry.

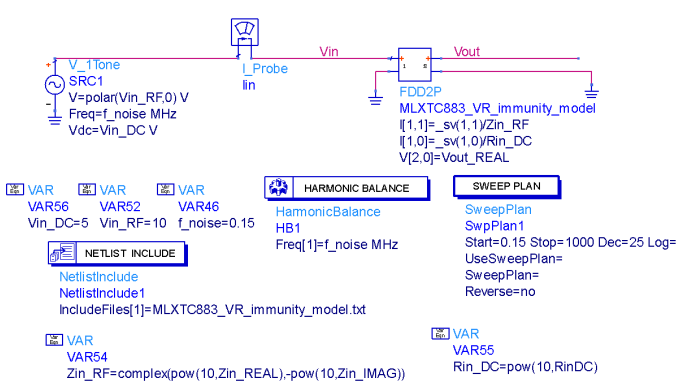


Fig. 5. Implementation of the surrogate-based model in the circuit simulator.

Several immunity models, using different settings for the construction of the surrogates, were tested and an exemplary comparison of the $V_{out,DC}$ characteristics is presented in Fig. 6. In this case, the magnitude of the RF noise is fixed to 10 V and the frequency f_{noise} is swept from 150 kHz to 1 GHz (as prescribed in, e.g., [3] and [11] for the DPI and

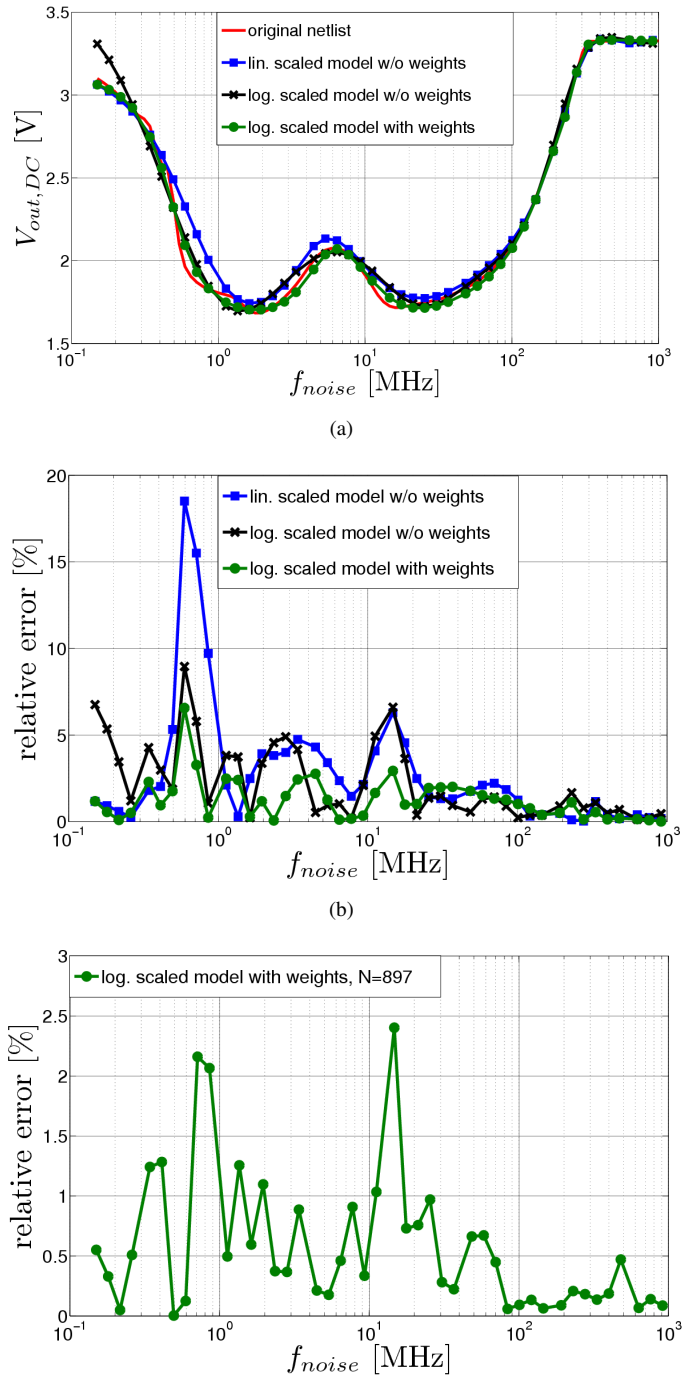
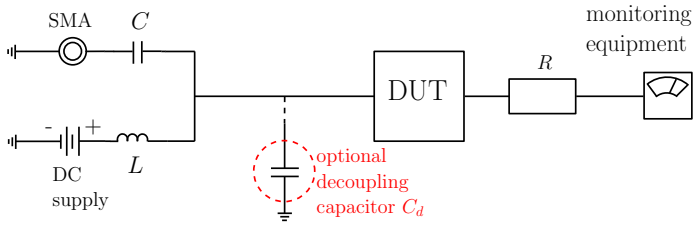
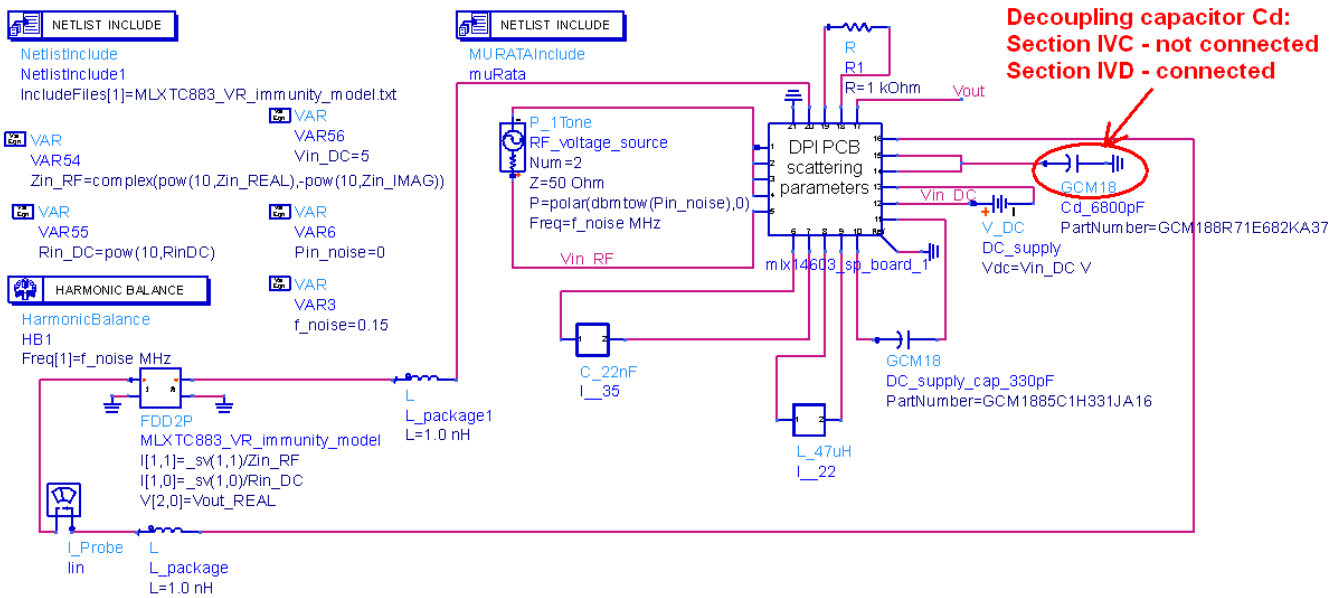


Fig. 6. Validation of the immunity modeling approach, using several settings for the construction of the surrogates. (a) $V_{out,DC}(f_{noise}, V_{in,RF})$ for $V_{in,RF} = 10$ V (b) relative errors for $N = 252$ (c) relative error for the best model constructed using $N = 897$ samples



(a)



(b)

Fig. 7. DPI setup (a) schematic configuration (b) implementation in ADS of the DUT (here the immunity model is shown), together with a model for the package, the PCB, and the lumped components.

BCI test, respectively). The red line in Fig. 6(a) represents the data obtained using the original MLXTC883 netlist. The blue line with squares (□) shows the scenario where the immunity model consists of ANN surrogates that were created without applying additional weighting factors (7), i.e. $w_i = 1$ in (6) for all i, and where the input impedances are modeled on a linear scale. The black line with crosses (X) depicts the immunity model case where the surrogates for the input impedances were constructed on a logarithmic scale, as such hugely compressing the modeling range, but still all samples are weighted equally ($w_i = 1$). The green line with circles (○) presents the immunity model when applying logarithmic compression for the input impedances and the additional weighting factors (7). As observed from Fig. 6(b), where the relative error between the three models and the results from the original netlist are shown, compressing the modeling range of the impedances reduces the maximal relative error from about 18.5% (blue line with □) to 9% (black line with X). Moreover, focusing the sample selector on the critical areas by adopting the weights (7), additionally reduces the maximal relative error to 6.5% (green line with ○), and, more importantly, at the lowest and at the highest frequencies, where the VR (almost) exhibits the desired 3.3 V output behavior, the relative error decreases to 1%. Therefore, the model represented by the green line, with logarithmic compression and additional weighting, is considered to be the best one. For illustration purposes, we also show in Fig. 6(c) a model that is constructed using logarithmically compressed surrogates with weights (7), but based on a larger number of samples $N = 897$. This leads to a further reduction in maximal relative error down to 2.5% and the error value at higher frequencies decreases below 0.5%. However, for our purposes, the model based on 252 samples provides satisfactory accuracy and therefore it is further used in the examples given in Sections IV-C and IV-D.

As a first indication of the efficiency, we mention here that the total time needed to obtain these results from Fig. 6 using the original netlist equals 50.2 s, whereas it only takes 1.5 s when using the surrogate-based immunity model. So, for this small example, a speed-up factor of more than 30 is obtained. Of course, the surrogates need to be created first, but this can happen off-line, and once available they can be reused many times for evaluation and optimization purposes (see below).

C. Application example 1 - VR within a DPI test

As an application example, the original netlist of the VR MLXTC883 and its surrogate-based immunity model are used within a setup mimicking a DPI test. A schematic of such a DPI setup is shown in Fig. 7(a). As also prescribed in [3],

in essence it consists of the DUT itself, placed on a PCB, a bias tee allowing to provide the DC supply and to inject the RF noise via a subminiature version-A (SMA) connector, and a decoupling network, here represented by a large resistor R, for monitoring the DUT's behavior. Additionally, although not a part of the DPI setup, decoupling capacitors at the input can be leveraged to improve the immunity behavior, as will be demonstrated in Section IV-D. In Fig. 7(b) it is shown how such a DPI setup is implemented in ADS. In this paper, for illustration purposes, the VR is connected to a simplified package model, consisting of 1 nH inductors. More elaborate package models can of course also be used. To accurately incorporate the influence of the typical DPI PCB on which the packaged VR is placed, an advanced model is used, by adopting the EM/circuit co-simulation technique described in [24]. Thereto, first the unpopulated PCB is analyzed in terms of its pertinent scattering parameters by means of a full-wave simulation in ADS -Momentum. Next, these scattering parameters are imported into the circuit simulator and combined with dedicated models for the lumped components, and also with the packaged DUT. The bias tee consists here of a DC blocking capacitor AVX Z5U 08055E223MAT2A with nominal value $C = 22$ nF and a DC feeding inductor (Ferroperm Type 1583 RF choke) with nominal value $L = 47$ μH. These real lumped components that also include parasitic effects were selected according to the suggestions given in [24], as they lead to compliance with the requirements described in [3] concerning the RF power injection path. Finally, an RF voltage source provides the RF noise and a DC voltage source, together with its capacitor (GCM1885C1H331JA16) of 330pF, biases the IC with 5V. The behavior of the IC is monitored, specifically its DC output voltage, using a resistor of $1k\Omega$ as decoupling network.

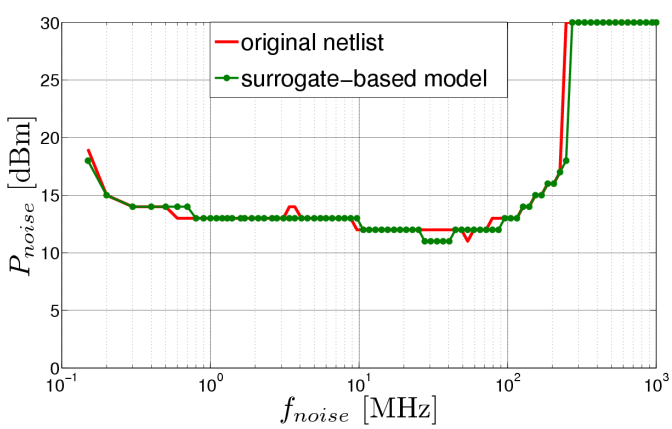


Fig. 8. Comparison of the DPI test results of the original circuit (red line) and the surrogate-based immunity model (green line with circles).

In Fig. 8, the typical test results from such a classic DPI test are shown, presenting the maximum value of the RF noise power (in dBm) that the IC can withstand without going out of spec. Here, this specification is as follows: the VR is considered to behave appropriately, if the DC output voltage remains within the range $[3.2\text{V}, 3.4\text{V}]$, so i.e. no more than 100 mV difference from the desired 3.3 V value is allowed (which now also explains the choices of the weighting factors (7)). The results of this simulated DPI test show excellent agreement between the data obtained by using the original VR netlist and the surrogate-based immunity model. At 150 kHz, according to the original netlist, the IC withstands 19 dBm and still operates correctly, while the surrogate-based model returns 18 dBm as a maximal acceptable value of the RF noise power. For the large frequency range from 500 kHz till 100 MHz this value decreases to less than 14 dBm, according to both setups. For frequencies higher than 300 MHz, the IC fully passes the DPI test, as it withstands 30 dBm of RF noise. To obtain the results of this test, the simulation time, using the set-up with the original netlist, is 2913.8 s, whereas the simulation time when using the surrogate-based model equals only 32.6 s. Hence, a considerable speed-up factor of 90 is obtained.

D. Application example 2 - VR within a DPI test setup with additional decoupling capacitor at its input

The surrogate-based models can now also be used to rapidly verify the effect of EMC precautions taken at the board level. To demonstrate this, in this example, an additional decoupling capacitor GCM188R71E682KA37 of 6.8 nF is placed at the input pin, as shown in Fig. 7, leading unwanted RF noise to ground. The simulation of the DPI test is repeated for the original netlist and the behavioral immunity model, and the results are presented in Fig. 9. Again, a very good agreement between both results is achieved. It is clearly observed that the decoupling capacitor significantly improves the immunity. The DPI test is passed starting from 3 MHz up to 1 GHz. However, the circuit with this decoupling capacitor still cannot fulfill the standard requirements of 30 dBm within the 150 KHz - 3 MHz range. To fully pass the DPI test, additional capacitors with optimal values need to be added, or additional expensive components such as ferrite beads need to be placed on the board, or the VR circuitry itself needs to be adapted in order to decrease its susceptibility. The surrogate-based immunity model can help, already during this early design phase, to explore the best and most cost-efficient options for both the ASIC manufacturer, who is responsible for the ASIC, and the customer, who uses this device at the board and system level within its intended application.

V. Conclusion

A novel technique to generate reliable immunity models of nonlinear analog circuits has been presented. The method leverages Harmonic Balance analysis and surrogate modeling to create a behavioral immunity model of the IC, as such hiding the IP and significantly speeding up the simulation process, while maintaining high accuracy. A representative test case of an analog, highly nonlinear VR for automotive purposes was selected, for which the model construction parameters have been carefully investigated and optimal settings have been selected ensuring high precision and efficiency. The model was readily integrated into a circuit simulator, which allowed its validation and application. Since the surrogates are created merely by means of simulated data, the proposed

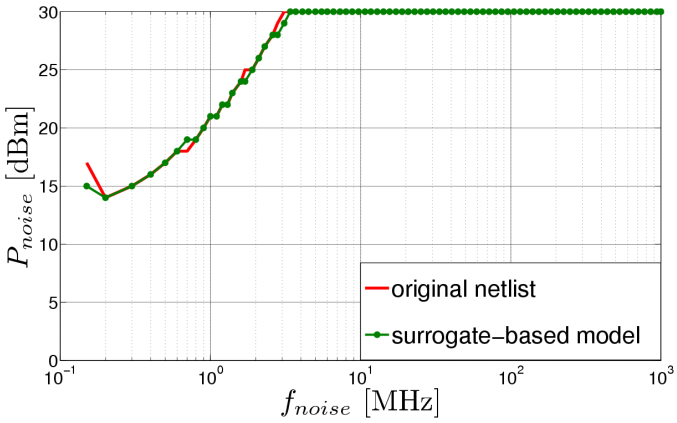


Fig. 9. Comparison of the DPI test results of the original circuit (red line) and the surrogate-based immunity model (green line with circles) with additional decoupling capacitor.

approach allows to use the model in the early design phase of the circuit, without performing expensive and time-consuming measurements. Indeed, it was shown that implementation of the model of the VR within a IEC62132-4 DPI setup, with and without additional decoupling capacitor, returns accurate and meaningful results in a very efficient way, compared to using the full original netlist. This confirms the usefulness of the proposed technique for industrial applications.

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