Planar Concave Grating Demultiplexer on a Nanophotonic Silicon-on-Insulator Platform

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***Abstract*—We present measurement results of a 4-channel silicon-on-insulator grating demultiplexer fabricated in a CMOS line. It has an ultra-small footprint of 280x150μm^2, 20nm channel spacing, on-chip loss of 7.5dB and crosstalk of better than -30dB.**

I. Introduction

THE two main technologies available today for implementing (de-)multiplexer functionality based on planar spectrograph type designs are Arrayed Waveguide Gratings (AWGs) [1] and etched Planar Concave Gratings (PCGs) [2]. Compared with AWGs, PCGs offer potentially smaller chip sizes and higher integration density for devices with a large number of output channels. However, insertion losses reported to date are higher as compared to AWGs. Grating profile imperfections and particularly the verticality of these deeply etched grating facets remain a critical issue. In this paper, we show that the insertion loss caused by these factors can be reduced by fabricating the PCGs on a nano-photonic silicon-on-insulator (SOI) platform.

We present for the first time a planar concave grating demultiplexer fabricated on SOI using standard wafer scale CMOS processing techniques including deep-UV lithography. This opens the way for low cost components that can be mass fabricated. The devices are fabricated on a 200 mm SOI wafer with a silicon top layer of 220 nm and a buried oxide of 1 μm. The high refraction index contrast between core and cladding allows the creation of very compact and high density waveguide circuits including so-called 'photonic wires' with core sizes of only 0.1 μm^2 and bend radii as small as 1 μm.

II. Design and fabrication

The layout of the PCG is shown in Figure 1. The footprint of the device including photonic wire access waveguides is 280 x 150 μm^2. The design is based on the Rowland geometry: the input and output waveguides are positioned on a circle with a radius of 188 μm and the curved grating sits on a 375 μm radius circle. The order of diffraction is 10 and the tapered entrance and exit waveguides are 2 μm wide with a spacing of 5 μm between the centers of the output waveguides

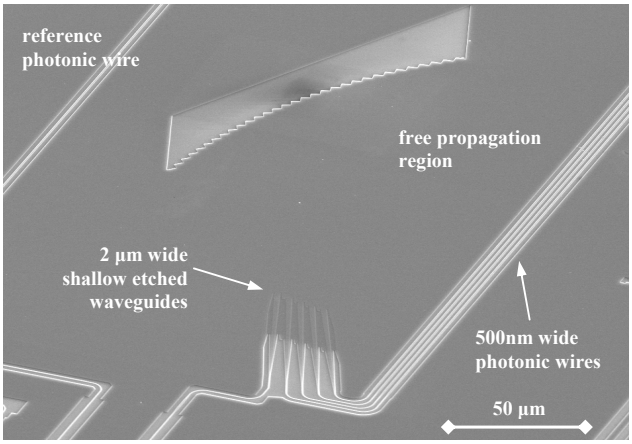

Fig. 1. SEM picture of 1x4 demultiplexer.

along the Rowland circle. The angle between the input waveguide and the grating pole is 41°. This configuration results in a linear dispersion of 0.25 μm/nm. The 31 facets are individually blazed to maximize the transmission of the two central output channels and the projected grating period is 4.35 μm. Simulations are based on scalar diffraction theory and predict a free spectral range of 115 nm around a central wavelength of 1550 nm. The four output channels are separated by 20 nm, making the device suitable for coarse WDM applications.

Structures were defined with 248nm deep-UV lithography, and transferred into the silicon using ICP-RIE etching. The fabrication process is described in detail in [3]. The lithography is a two step process which combines deep- and shallow etching. For the definition of the grating and the photonic wires, the 220 nm thick Si layer is etched through. A more shallow etch (70 nm) is used for the definition of the fiber couplers and the 2 μm entrance- and exit waveguides on the Rowland circle. The fiber couplers are gratings that convert the mode between a broad access waveguide and the fiber to allow characterization of the component [4].

III. Measurement results

The measured transmission spectrum (TE polarization) of the 1x4 demultiplexer is shown in Figure 2. This transmission spectrum is normalized to a reference photonic wire

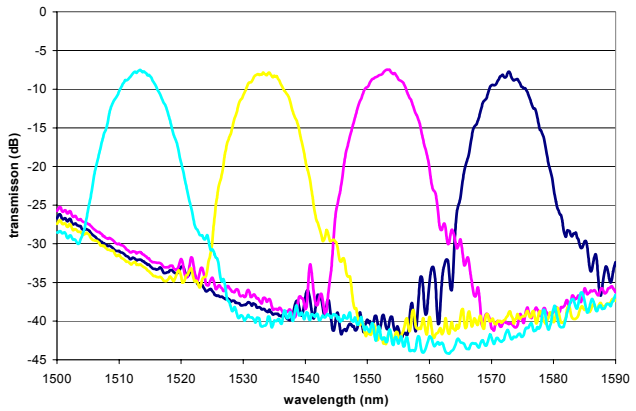

Fig. 2. Transmission spectrum of 1x4 demultiplexer.

waveguide (Figure 1). The on-chip loss is about 7.5 dB and the crosstalk is better then -30 dB. The loss variation over the channels is 0.5 dB. Measurement results are slightly disturbed by the low noise floor of the measurement setup.

The main loss source is the reflection loss of the etched facets since no measures were taken to enhance the reflectivity. The effective index of the slab waveguide mode is 2.83 at λ = 1.55 µm. This results in a reflection loss in the order of 5.5 dB as derived from a plane wave approximation and taking into account the non-verticality of the facets. A second contribution is caused by the non-verticality of the grating facets. As mentioned before, standard deep-UV lithography in combination with ICP-RIE dry etching is used for the definition of the structures, including the grating facets. This fabrication process is not optimized to create perfect vertical etching and results in a rather large non-verticality of 10.5°. However, this only gives rise to an additional loss of 0.4 dB, calculated with eigenmode expansion. PCGs reported up to date including PCGs on SOI [5] have a several micrometer thick free propagation region with deeply etched grating facets. Sidewall non-verticalities as reported in this paper would completely destroy the transmission characteristics of these devices. A third contribution, which is inherent to the design, is the diffraction loss of 0.7 dB for the central channels. This means that only 0.9 dB of loss is caused by other effects, mainly grating profile imperfections like facet corner rounding and surface roughness. This low value, as compared to previous reported SOI PCGs [5], is due to the fact that the grating only needs to be etched 220 nm deep, making it possible to obtain a high quality grating profile making use of standard dry etching techniques as can be seen in Figure 3. If precautions are taken to reduce the reflection loss at the facets like coating the backside of the grating with a metal film, we believe that on-chip losses of less than 4 dB can be achieved.

The measured value of channel crosstalk of the demultiplexer is 5 to 10 dB worse as compared to simulation results. This rather small deviation is mainly caused by small grating profile imperfections as discussed earlier. AWGs fabricated on the same nanophotonic SOI platform [1] still have significant crosstalk due to phase noise caused by small

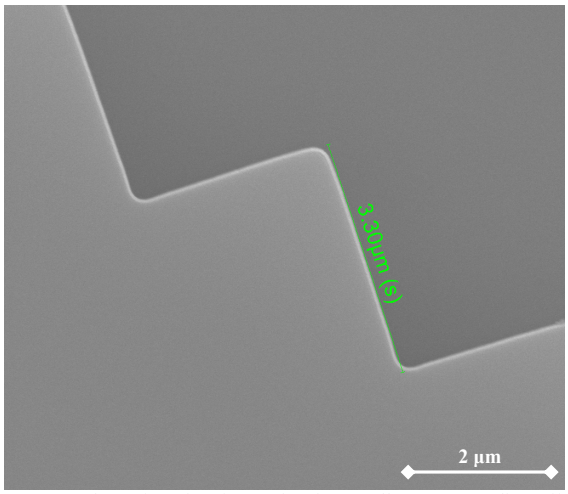

Fig. 3. Top view of grating facets showing small corner rounding effects. Only 0.9 dB of the on-chip loss is caused by grating profile imperfections.

length deviations of the photonic wires. This problem is not present in the PCG presented here.

IV. Conclusions

We showed for the first time that the fabrication - making use of standard CMOS wafer scale processing techniques - of PCGs on a nanophotonic silicon-on-insulator platform can lead to compact devices with high performances. This is a consequence of the fact that the grating facets only need to be etched 220 nm deep. First of all this reduces the strict fabrication tolerances of grating verticality. Secondly, a more perfect grating profile can be fabricated (corner rounding, roughness) without the need of dedicated deep etching techniques and thirdly, since the free propagation region (FPR) only supports one guided mode there is no deterioration of insertion loss and channel crosstalk caused by multimode propagation in the FPR. We believe that by coating the backside of the grating with a metal film, the on-chip loss can be further reduced to less than 4 dB. The standard CMOS fabrication techniques open the way for the realization of low cost (de-)multiplexers that can be mass fabricated.

Acknowledgment

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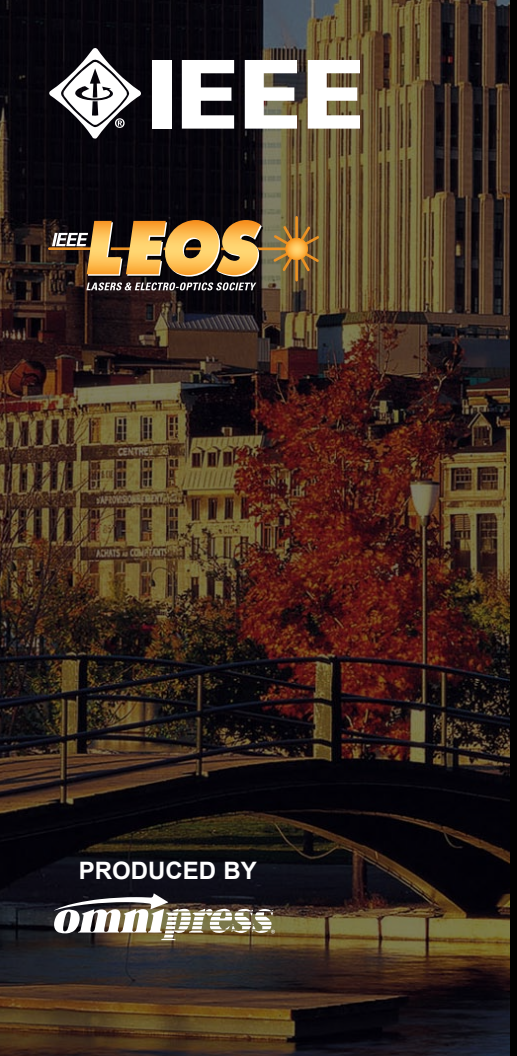

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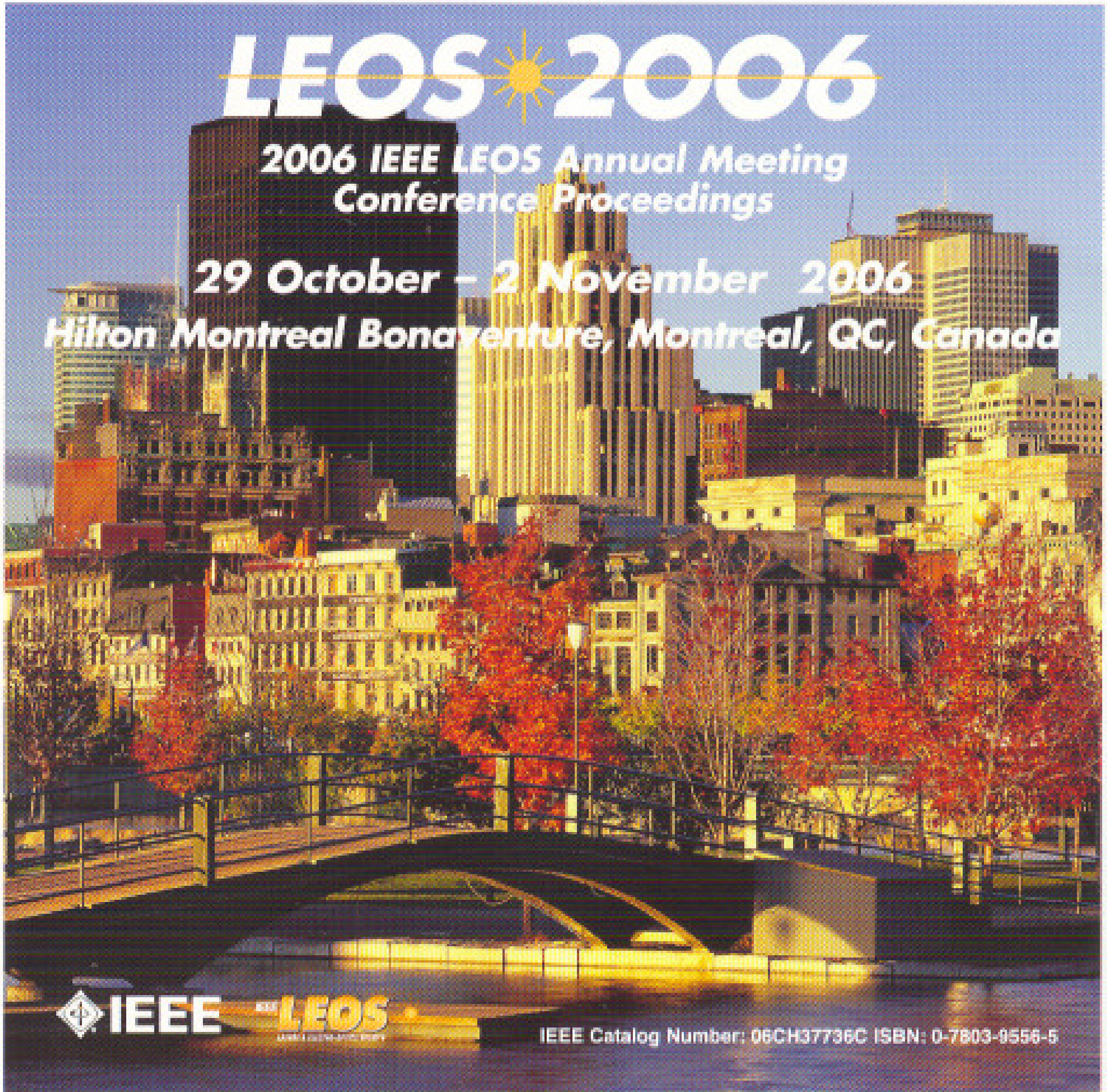

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