2006

INTERNATIONAL SYMPOSIUM ON VLSI DESIGN, AUTOMATION, AND TEST (VLSI-DAT)

PROCEEDINGS OF TECHNICAL PAPERS

April 26-28, 2006

AMBASSADOR HOTEL

HSINCHU,TAIWAN

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Industrial Technology Research Institute

IEEE

A Fully Integrated Ultra-Low-Power High-Voltage Driver for Bistable LCDs

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ABSTRACT

A complete ultra-low-power high-voltage driver for a 80 x 104 passive-matrix bistable LCD is integrated in a 0.7µm CMOS smart-power technology. It features 100V driving capability on all row and column outputs and comprises all necessary digitally programmable high-voltage generators and multiplexers to synthesize the required complex high-voltage waveforms from a 3V battery. An original level-shifter design for the high-voltage multiplexers yields an extremely low internal power consumption below 10mW for the entire driver chip.

INTRODUCTION

Bistable flat panel displays, such as cholesteric texture LCDs or bistable nematic LCDs, are very well suited for portable battery-powered applications (PDA, E-book, etc.). Their bistability makes them very power-efficient as they don't need continuous refreshing to maintain an image on the screen. Unfortunately, the bistable LCDs require very high voltages (from 20V to 100V) to switch the pixels from one stable state to the other. Hence, special high-voltage driver chips with on-chip high-voltage generators have to be developed. As the bistable displays aim at portable battery-powered applications, very strong constraints regarding internal power consumption are also put on these high-voltage drivers. In order to meet this stringent requirement, very special care has to be taken during the design of the on-chip programmable high-voltage generators to make them as power-efficient as possible. Also the design of the level-shifters in the high-voltage analog output multiplexers is a very challenging task if one wants to achieve very low internal power dissipation. During the design phase of the presented bistable LCD driver, these problems were tackled by introducing new circuit concepts and architectures, and the resulting driver chip successfully combines full 100V driving capability on all outputs and a very low internal power consumption below 10mW during line scanning.

DRIVER ARCHITECTURE

The internal architecture of the presented driver is depicted in Fig. 1. The row driver, responsible for scanning the row electrodes in consecutive order, consists of an 80-stage shift-register plus latch, a logical control unit, and 80 low-power high-voltage analog multiplexers capable of connecting each row electrode to 1 out of 3 high-voltage levels or ground. The column driver, responsible for putting the gray scale data on the column electrodes, has a similar structure, but it consists of 104 stages and it also contains a 4-bit PWM modulator for producing the gray shades. The high-voltage analog switches in the output multiplexers employ the 'dynamic charge control' technique to reduce the power consumption in the level-shifters to an absolute minimum (see the section on level-shifter design). The different high-voltage levels, needed by the output multiplexers, are generated on-chip by means of a set of 5 high-efficiency high-voltage generators. Each generator is digitally programmable and produces an output voltage in the range 0 – 100V with 8-bit resolution from the 3V battery power supply. The charge-pump in each high-voltage generator requires a small external low-loss inductor as an energy transfer element from the low-voltage to the high-voltage side, and preferably also a small external capacitor to minimize the ripple on the output voltage and to act as a charge buffer capable of supplying sudden peak currents to the display electrodes. All functions of the chip are controlled by 7 internal

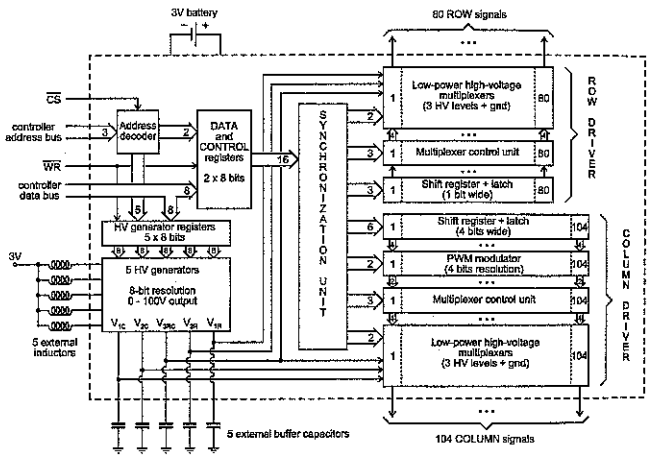

FIGURE 1. BLOCK DIAGRAM OF THE ULTRA-LOW-POWER HIGH-VOLTAGE BISTABLE LCD DRIVER 'AKIRA'.

registers (5 for the generators and 2 for the row and column drivers). Communication between these internal registers and an external microprocessor or microcontroller is established through a standard data and address bus architecture. As a consequence, the driver chip can be addressed by the system's processor as if it were a standard memory device.

The chip was designed and manufactured in the Intelligent Interface Technology (I^2T) from AMI Semiconductor, which is a 100V smart-power technology based on a standard 0.7µm CMOS process. Fig. 2 shows a photograph of the complete silicon die, identifying the most important building blocks of the driver. The die measures 13 x 10mm^2 and contains approximately 120k transistors, 10k of which are high-voltage devices such as 100V lateral DMOS transistors (Drain-extended or Double-diffused MOS). The size, pitch and distribution of the IO pads have been chosen to accommodate wire-bonding or flip-chip assembly.

PROGRAMMABLE HIGH-VOLTAGE GENERATORS

In order to convert the 3V battery power supply into very stable, reproducible and well-defined voltage levels up to 100V, a dedicated architecture for the on-chip high-voltage generators was designed

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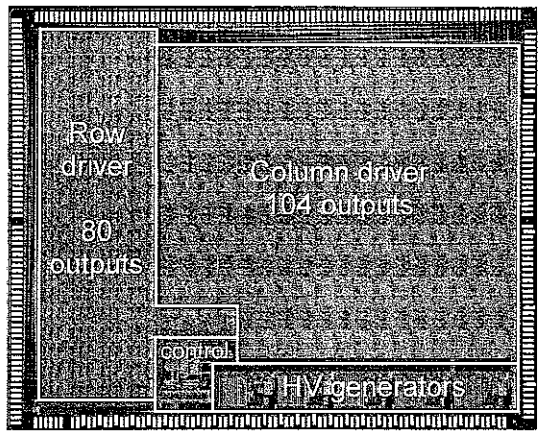

FIGURE 2. DIE PHOTOGRAPH OF THE ULTRA-LOW-POWER HIGH-VOLTAGE BISTABLE LCD DRIVER 'AKIRA'.

and optimized [1]. The block diagram of these fully programmable high-voltage generators is shown in Fig 3. A set of 8 digital input bits, coming from one of the chip's internal registers, transform an internal reference voltage into 1 out of 256 linearly distributed current levels. This current level is then compared to a second current level that is proportional to the generator's output voltage. Depending on which of the 2 currents is the largest, the clock signal of a high-efficiency charge-pump is enabled or disabled, thereby causing the generator's output voltage to rise or drop. By means of the negative feedback, a situation is reached where the 2 internal current levels become nearly equal, and the output voltage will start to oscillate around a certain mean value with a very small amount of ripple. In this way, 256 linearly distributed voltage levels can be generated according to the formula:

$$V_{out} = V_{ref} \times \left(1 + \frac{R_{FB}}{256\,R_{ref}} \times \left(\sum_{i=0}^{7} B_i \cdot 2^i\right)\right)$$

In this equation, V_{out} represents the output voltage, V_{ref} the internal reference voltage, B_i the 8 digital input bits, R_{ref} an internal reference resistor in the voltage-to-current converter connected to the voltage reference, and R_{FB} an internal feedback resistor in the voltage-to-current converter connected to the generator's output. As the ratio R_{FB}/R_{ref} is determined by geometrical layout parameters

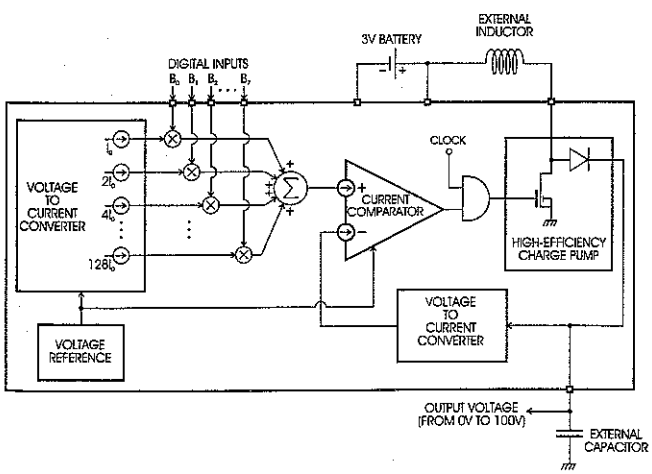

FIGURE 3. BLOCK DIAGRAM OF A FULLY PROGRAMMABLE 100V GENERATOR WITH 8-BIT RESOLUTION.

only, the generator's output voltage becomes highly reproducible and insensitive to process parameter variations. By choosing R_{ref} and R_{FB} appropriately, the output voltage range was set to 100V. Optimum performance in terms of output current driving capability and power efficiency was achieved by setting the charge-pump's clock frequency to 128kHz with a duty ratio of 75% for a 220µH external inductor.

LEVEL-SHIFTER DESIGN

A major problem in the development of high-voltage driver chips is the design of the level-shifter circuits for converting the 3V digital signals into appropriate high-voltage signals for controlling the DMOS transistors in the high-voltage switches of the output multiplexers. The level-shifters in standard high-voltage display driver chips exhibit continuous power dissipation, which is of course an important drawback for battery-powered applications. Therefore, a completely new level-shifter architecture with no static power consumption at all was designed [2]. Fig. 4 shows the schematics of a high-voltage analog switch, as used in the output multiplexers of the presented driver chip, employing this new type of low-power level-shifter.

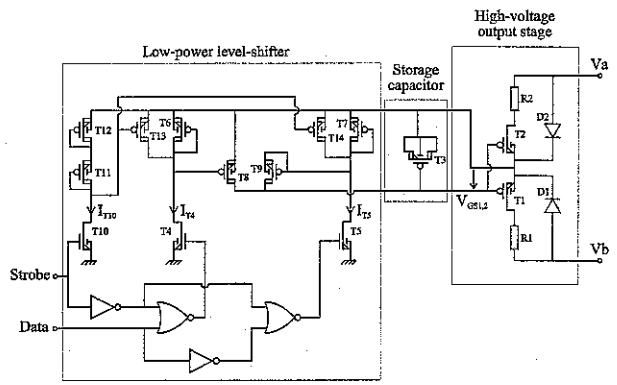

FIGURE 4. CIRCUIT SCHEMATICS OF A HIGH-VOLTAGE ANALOG SWITCH BASED ON A DYNAMICALLY CONTROLLED LEVEL-SHIFTER WITHOUT STATIC POWER CONSUMPTION.

The operation of this low-power level-shifter is controlled by a special *Strobe* signal. When *Strobe* goes high, one of the 2 transistors T4 or T5 (according to the logical value of the *Data* signal) will carry a 30µA drain current (see the simulated waveforms in Fig. 5), causing a voltage drop of approximately 4.7V over the p-type load transistor T6 or T7. For a "0" bit at the *Data* input, the 4.7V drop across T6 turns on transistor T8, and consequently, the source-gate capacitance of the p-type DMOS transistors T1 and T2 is totally discharged (i.e. $V_{GS1,2}$ = 0V), meaning that T1 and T2 will be switched off and that the high-voltage switch between the nodes *Va* and *Vb* will go into the insulating state. For a "1" bit at the *Data* input, on the other hand, the 4.7V drop across T7 will pull down the gate potential of T1 and T2 through transistor T9 (used as a p-n diode between its drain and bulk), yielding a source-gate voltage $V_{GS1,2}$ of approximately –4V for the T1 and T2 output transistors, and hence, T1 and T2 will be turned on, resulting in a bi-directional conductive path between the nodes *Va* and *Vb*. When the *Strobe* signal goes low, T4 and T5 are switched off, and as a consequence, T8 will also be turned off (if the *Data* input was a logical "0" during the *Strobe* pulse) or the 'diode' T9 will be reverse biased (if the *Data* input was "1"). In both cases, the gate electrodes of the p-type DMOS transistors T1 and T2 become electrically isolated from the rest of the level-shifter circuit, and hence, the charge that was previously stored on their gate capacitance during the *Strobe* pulse (i.e. $V_{GS1,2}$ equal to

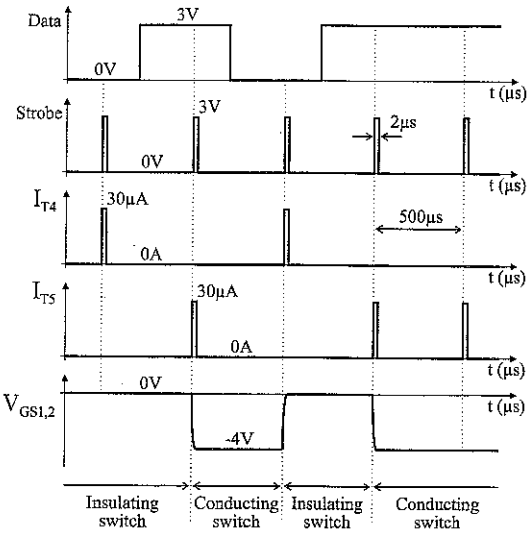

FIGURE 5. WAVEFORMS IN THE DYNAMICALLY CONTROLLED LEVEL-SHIFTER.

0V or –4V, according to the *Data* signal) will remain unchanged until the next *Strobe* pulse is applied.

This unique 'dynamic charge control' approach, where the gate capacitance of the DMOS output transistors is used as a kind of dynamic memory cell whose charge is updated at the rhythm of a strobe signal that is synchronized to the data flow, yields an enormous reduction in power dissipation if the duration of one strobe pulse can be kept very short compared to the duration of one bit of input data (since power is consumed only during the strobe pulses!). This is definitely the case for bistable LCD drivers as these bistable LCDs usually require very low image frame rates.

To improve the performance of this low-power level-shifter even more, some extra features have been added in the schematics of Fig. 4. Transistors T10 till T14, activated directly by the *Strobe* signal, were added to ensure that the active loads T6 and T7 are completely discharged after each *Strobe* pulse. Without this feature, sub-threshold currents in T8 might cause charge leaking from the gate capacitance of T1 and T2 in between consecutive *Strobe* pulses. The effect of parasitic charge leaking can be reduced even further by adding transistor T3, acting as a storage capacitor in parallel to the gate capacitance of T1 and T2. Finally, diodes D1 and D2 together with the resistors R1 and R2 prevent the triggering of substrate currents in T1 and T2 due to reverse conduction under certain operating conditions.

EXPERIMENTAL RESULTS

The accuracy of the high-voltage generator's programming capability can be observed in Fig. 6. In the whole range up to 100V, the absolute non-linearity error of the output voltage is less than ±1 LSB at all times. The output current driving capability of the generator for different programmed output voltages is illustrated in Fig. 7. At an output voltage of 100V, the generator is capable of delivering 180µA into the load, which is enough for most bistable LCD applications. At lower output voltages, the maximum output current increases rapidly (e.g. 750µA at 50V). Another important figure of merit of the high-voltage generator is its power efficiency. In Fig. 8, the measured power efficiency is plotted against the output current for different values of the programmed output voltage. At

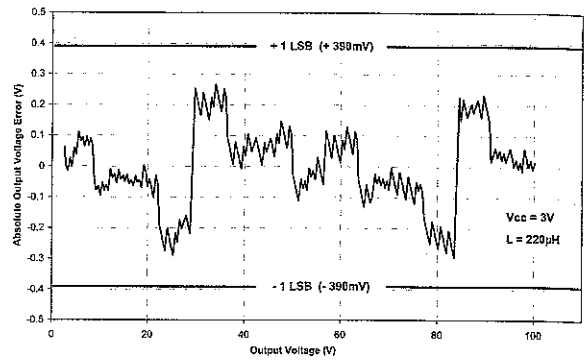

FIGURE 6. MEASURED ABSOLUTE NON-LINEARITY ERROR VS. OUTPUT VOLTAGE OF A PROGRAMMABLE HIGH-VOLTAGE GENERATOR.

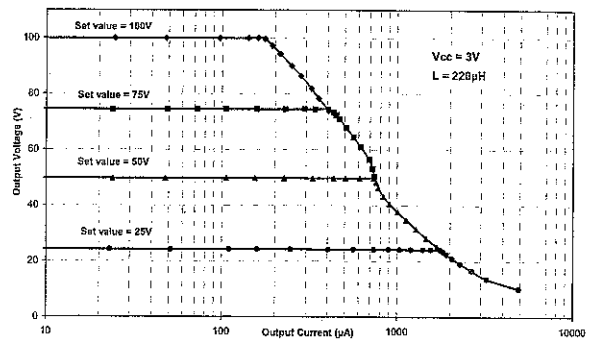

FIGURE 7. MEASURED OUTPUT VOLTAGE VS. OUTPUT CURRENT OF A PROGRAMMABLE HIGH-VOLTAGE GENERATOR.

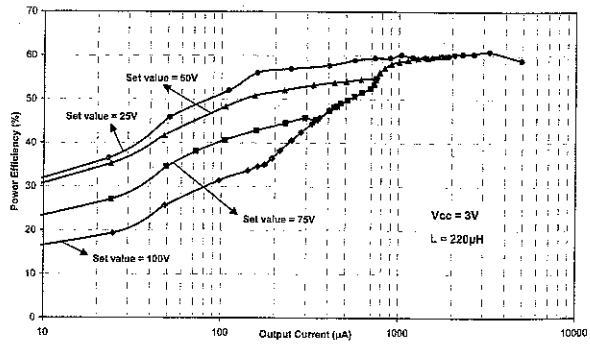

FIGURE 8. MEASURED POWER EFFICIENCY VS. OUTPUT CURRENT OF A PROGRAMMABLE HIGH-VOLTAGE GENERATOR.

100µA output current, a power efficiency of 48% is achieved at 50V output voltage, and still 32% at 100V.

A measured current-vs.-voltage characteristic of a conducting dynamically controlled high-voltage analog switch is given in Fig. 9. Symmetrical curves are obtained, meaning that the circuit behaves like a real bi-directional switch. This is necessary because during display driving, the high-voltage generators have to be able not only to source current through the switches in order to charge the display electrodes, but also to sink current through the same switches in order to discharge the display electrodes. Note that the curves in Fig. 9 were measured after putting the high-voltage switch into the

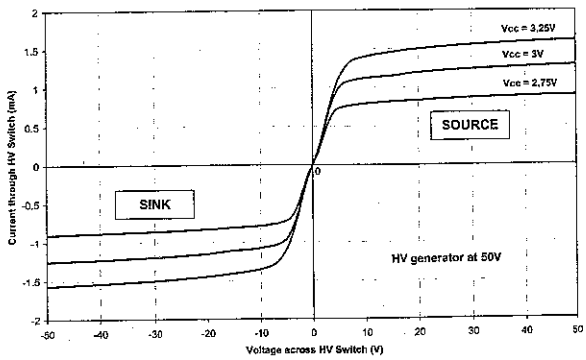

FIGURE 9. MEASURED CURRENT-VS.-VOLTAGE CHARACTERISTIC OF A CONDUCTING HIGH-VOLTAGE ANALOG SWITCH.

conducting state by means of a single 2µs strobe pulse in the corresponding level-shifter.

Fig. 10 shows the row, column and pixel waveforms at the output of the chip for addressing a bistable cholesteric texture LCD. The presence of a double reset sequence, the line scanning and the PWM gray scale modulation are clearly visible. These graphs demonstrate that the chip is indeed capable of synthesizing the high-complexity high-voltage waveforms from a 3V battery for driving a bistable LCD. Fig. 10 also shows how the high-voltage generators can be reprogrammed to obtain independent voltage levels during the different phases of a given driving scheme.

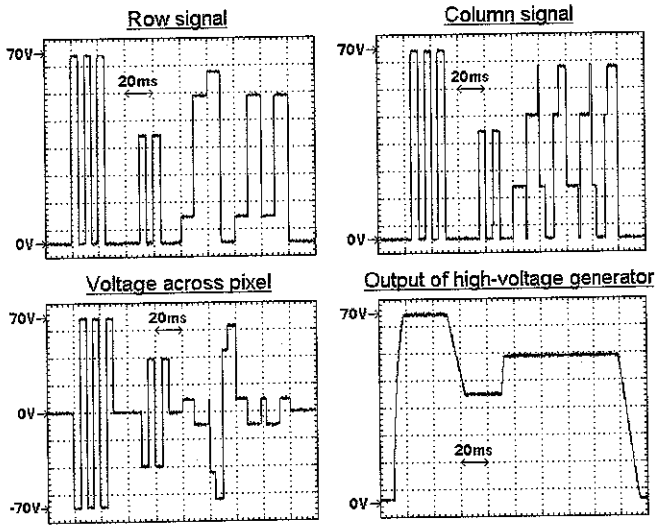

FIGURE 10. MEASURED WAVEFORMS FOR DRIVING A CHOLESTERIC TEXTURE LCD.

The total power dissipation inside the driver chip was measured while addressing a 80 x 104 cholesteric texture LCD with a display area of 250mm^2 and using the voltage levels and waveforms of Fig. 10. For a line addressing time of 5ms, the average power dissipation in the entire chip was 9.7mW. Increasing the line addressing time to 20ms resulted in an average power dissipation of only 2.5mW. This extremely low value makes the driver ideally suited for various portable applications. As a matter of fact, this driver chip was originally designed for addressing a 80 x 104 cholesteric texture LCD embedded in a sophisticated wrist-watch to allow a preview of pictures taken by a built-in camera. Fig. 11 shows a fully functional prototype of this sophisticated wrist-watch "IRIS" from the Swatch-Asulab company, in which the presented driver chip is successfully addressing the cholesteric texture LCD. As this watch is powered by a tiny battery that is meant to last for many months, reaching an extremely low level of power consumption was indeed an absolute necessity. Note, however, that this chip can also be used very easily to drive other types of bistable displays because of its pronounced flexibility and programmability.

FIGURE 11. SOPHISTICATED WRIST-WATCH "IRIS" FROM SWATCH-ASULAB, CONTAINING THE PRESENTED DRIVER CHIP ADDRESSING A 80 X 104 CHOLESTERIC TEXTURE LCD.

CONCLUSION

A versatile ultra-low-power 100V bistable LCD driver was presented. New architectures and design concepts for the digitally programmable high-voltage generators and level-shifters yield an exceptionally low internal power consumption below 10mW for the entire chip during display addressing. Although the chip was originally developed for addressing a cholesteric texture LCD in a watch application, its pronounced flexibility and programmability make it also suitable for driving a variety of other bistable flat panel display types.

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