Analog Front-End ASIC Requirements for a FDM Broadband Powerline System Enabling Co-Existence

J. Bauwelinck, E. De Backer, C. Mélange, X.Z. Qiu, J. Vandewege*
C. Thornton, A. Boss, S. Horvath†, S. Rao‡

*Department of Information Technology, INTEC/IMEC, Ghent University
41 Sint-Pietersnieuwstraat, 9000 Gent, Belgium

†Advanced Communications Networks SA, ACN
8A Rue Du Puits-Godet, 2000 Neuchatel, Switzerland

‡Telscom A.G.
20 Aarwilweg 20, 3074 Muri Bei Bern, Switzerland

***Abstract*— This paper presents a feasible set of analog ASIC requirements optimized to achieve co-existence in a broadband Power Line Communications (PLC) system based on Frequency Division Multiplexing (FDM). FDM is the most straightforward way to achieve co-existence between different systems, however, this involves many design challenges at the circuit level. First, a short description will be given of the PLC system, which is under development in the EU funded IST POWERNET project. It will be shown that conventional receiver architectures, typically designed for Time Division Multiple Access (TDMA) schemes, are not well suited for FDM systems e.g. due to challenges arising from near/far situations. Solutions to improve the performance will be discussed and simulation results will be presented of the proposed architecture, based on parameters extracted from circuit designs, to show the feasibility of high bit rates in FDM transceivers.**

***Keywords*— Analog front-end, Co-existence, Frequency division multiplexing, Peer-to-peer, Powerline communications**

I. Introduction

POWERLINE communication systems are becoming more and more widespread. Many different systems and standards are developed, however, as more and more systems will be deployed co-existence becomes increasingly important. This research is part of the EU funded IST POWERNET project [1]. The goal of this project is to validate the "cognitive broadband over powerline (CBPL)" technology in the field. The CBPL technology employs asynchronous, peer to peer communications, instead of the commonly used master-slave communications, between the users in order to keep the required transmit power spectral density as low as possible to comply with the regulatory requirements [2]. The different asynchronous channels are allocated in a flexible way to different frequency bands, the bandwidth of which depends on the service requirements.

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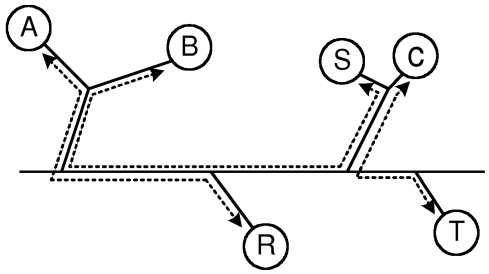

Fig. 1. Peer-to-peer powerline system.

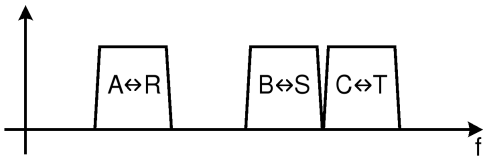

Fig. 2. Spectrum containing several asynchronous channels.

A. Peer-to-Peer Frequency Division Multiplexing

Fig. 1 together with Fig. 2 shows a peer-to-peer PLC network in which different asynchronous channels are communicating at the same time in different frequency bands. In order to achieve high data rates, through a higher number of channels, the system bandwidth is specified up to 60 MHz so that emerging multimedia services such as IPTV, HDTV, etc. can be supported. PLC systems face many challenges. This paper focuses on the analog front-end ASIC. It is clear that the Analog Front-End (AFE) requires low noise and low distortion; however, clear figures are often missing in publications [3].

B. Analog Front-End Design Challenges

FDM is often criticized because it would require more complex front-ends to address the near/far problem that would affect the dynamic range [4]. On the other hand, FDM is undoubtedly the most straightforward way to achieve co-existence between PLC different systems, even Homeplug AV includes the possibility to use FDM for coexistence [4]. However, if the system and the front-ends are not optimized to support FDM, a significant performance penalty cannot be avoided. In a CBPL system, peer-to-peer communication is used, instead of master-slave communication. In this way, the distance between the communicating nodes is reduced and the transmit (TX) level can be lowered. As a consequence, the near/far problem is somewhat relaxed. On the other hand, FDM will always pose significant design challenges in the analog front-end. This paper mainly focuses on the receiver (RX) part of the AFE, since this is the most critical part. Especially because it captures the complete used spectrum and the properties of the received signal spectrum depend on many (poorly known) factors. The purpose of this paper is to show the feasibility, of the ASIC integration of the AFE, based on parameters extracted from ongoing circuit design of the most important building blocks. The remainder of this paper is organized as follows. Section II will show that conventional AFE architectures, designed for TDMA schemes, are not really suited to support FDM. Section III presents the design trade-offs for an AFE architecture optimized to support FDM. Section IV presents simulation results, based on parameters extracted from circuit designs, to show the feasibility of the proposed AFE ASIC. Finally, conclusions are given in Section V.

II. Conventional Analog Front-Ends

Conventional PLC transceivers, such as described in [5][6][7][8][9], employ a straightforward architecture in the RX path mainly consisting of a low-noise amplifier (LNA), a low-pass filter (LPF), a variable gain amplifier (VGA) and a high speed analog-to-digital converter (ADC) as shown in Fig. 3. This is a very good architecture for TDMA based communication, in which the available bandwidth is assigned to a single user in a certain timeslot.

However in a FDM system, the spectrum is shared by a number of users resulting in simultaneous communication channels, each having different properties. As a consequence, AD conversion of the entire band is not a robust solution in an FDM system for several reasons:

1) A high number of bits (in fact signal-to-noise and distortion ratio, SINAD) would be required for disadvantageous cases:
   a) Only a small part of the spectrum (e.g. 1 to 16 MHz out of 60 MHz) could be used so most of the AD dynamic range could be occupied by unwanted channels.
   b) The power density of the wanted channel can be significantly (e.g. 30 dB) weaker than the other channels.
   c) The peak-to-average ratio becomes worse: e.g. for 20 channels using 128 carriers, the RX effectively receives 2560 carriers.
2) Higher bandwidths (e.g. 60 or even 100 MHz) are considered for next generation PLC systems, requiring advanced AD converters (conversion rate e.g. 3 times the bandwidth (BW) depending on the analog anti-aliasing filter), which cost tens of dollars. Moreover, at high conversion rates the signal-to-noise ratio (SNR) does not improve as much as the number of bits ideally predict (e.g. the state-of-the art AD9461 130 Msps 16-bit ADC provides 12.5 effective bits [10]).

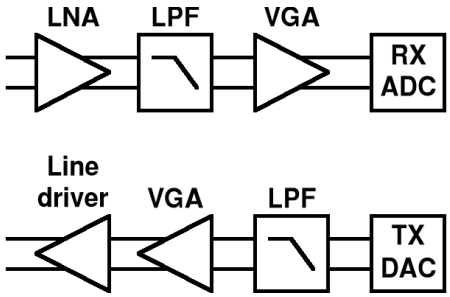

Fig. 3. Conventional AFE architecture.

As a consequence, taking into account the powerline uncertainties and a FDM scheme, the requirements on AD converters are huge if a minimum SNR is required in bad conditions, especially for the next generation PLC systems up to 100 MHz (as considered in the IEEE P1901 working group). Another important aspect is that in an asynchronous peer-to-peer FDM system, channels can be added or removed from the spectrum at any time. This would require a more complex automatic gain control (AGC), compared to the proposed architecture in Section III. Robustness against interferences or blockers is one of the main advantages of the proposed FDM system, because signals in other frequency bands will be filtered in the AFE.

So in order to design a transceiver, optimized for a FDM system, we propose to use a frequency conversion scheme in the analog domain so that analog filtering can be used prior to AD conversion, thus relaxing the AD requirements. Moreover, making the on-chip filtering tunable (2 to 16 MHz in our proposed design) provides a flexible way to allocate a certain amount of bandwidth to specific users or services. Furthermore, the guard bands between channels can be made relatively small by combining analog and very selective digital filters in the RX path. Another advantage is that our frequency conversion based architecture (designed for up to 60 MHz) can be easily upgraded to higher frequencies (e.g. 100 MHz as considered in the IEEE P1901 working group) because the AD performance and implementation cost is not the limiting factor in our architecture.

III. PROPOSED ANALOG FRONT-END

A. Transmitter

The discussion in Section II focused on the RX path because it is more critical than the TX path. However, the TX design is also critical in a FDM system. Care must be taken to limit spectral regrowth due to the non-linearity of the transmitter, especially of the line driver (because it handles the largest voltage/current signals). These intermodulation (IM) products could enter other (weak) channels. 30 dB notches as used in Homeplug AV at licensed frequency bands is not sufficient to protect other frequency bands because the signal one would like to receive could be attenuated by e.g. 40 dB. As the frequency channel is not fixed, no fixed filter can be used after the line driver so that optimizing the linearity of the line driver is very important, in combination with a predistortor in the digital domain to pre-compensate the non-linear line driver characteristic. The trade-offs concerning TX architecture are a bit different from the reasoning we did for the RX part. This is because digital-to-analog converters (DAC) with high conversion rate and high SINAD are commercially available at relatively low cost or much easier to implement. Moreover, the TX has to process only one channel, in contrast to the RX section. As a consequence, the TX path design can be based on a high-speed DAC, combined with digital mixers to upconvert the baseband signal into a particular frequency band.

B. Receiver

In the RX path it is key to achieve a high dynamic range. First of all, the input referred noise should be below the noise floor of the powerline system. Secondly, a high linearity is very important to avoid that other frequency bands or blockers reduce the SINAD of the desired channel due to IM. Several techniques are considered to reduce the IM distortion. The first priority should be to suppress undesired frequency bands, before the signal is amplified to a high swing. Up to the point where the signal is filtered, the non-linearity should be sufficiently high. In case of a very strong input signal (compared to the input-reffered 1 dB compression point), it is even desirable to attenuate the signal before mixing (trading of an increased AFE noise floor against a reduction of the IM products). After frequency conversion, fixed passive and/or active filters can attenuate the undesired channels before further amplification towards the ADC. In the following section it will be shown that sufficient dynamic range and SINAD can be achieved in a frequency conversion RX based on an architectural model using parameters extracted from circuit level designs. This chip is under development and will be tested in the field in 2007.

C. Receiver Model

A model was developed for the RX path to estimate the SINAD in a realistic frequency conversion scheme. For every building block, the noise and 3rd order IM distortion contribution is calculated depending on the gain, the input-referred noise and the 1dB compression point (CP) of the block. Estimating the signal level is straightforward for every carrier, the voltage at the output of stage i is given by:

$$v_{out,i} = \alpha_{1,i}\, v_{in,i} \tag{1}$$

where $v_{out,i}$ is the output voltage, $v_{in,i}$ is the input voltage and $\alpha_{1,i}$ is the voltage gain. The noise at the output of stage i is given by:

$$v_{nout,i} = A_V \sqrt{v_{nout,i-1}^2 + v_{nin,i}^2} \tag{2}$$

where $v_{nout,i}$ is the rms output noise voltage of stage i, $v_{nout,i-1}$ is the rms output noise voltage of the previous stage $(i-1)$ and $v_{nin,i}$ is the rms input referred noise voltage generated by stage i.

Estimating the distortion due to 3rd order non-linearity (a fully differential design is assumed) is more complex. Due to the multicarrier modulation many terms should be taken into account. The non-linear transfer characteristic of the stages is approximated as:

$$v_{out,i} = \alpha_{1,i}\, v_{in,i} + \alpha_{3,i}\, v_{in,i}^3 \tag{3}$$

where $\alpha_{1,i}$ is the voltage gain of stage i, and $\alpha_{3,i}$ models the 3rd order non-linearity of stage i. $\alpha_{3,i}$ is related to the 1 dB compression point (V_{1dB}, in V):

$$\alpha_{3,i} = (0.38)^2\, \frac{\alpha_{1,i}}{V_{1dB}^2} \tag{4}$$

The worst-case 3rd order IM product can be calculated analytically by:

$$\frac{3\,\alpha_3\, v^3}{2} \left\{ \begin{array}{l} \frac{N}{2}\left(\frac{N}{2}-1\right) + \frac{1}{4}\left(\frac{N-(N \bmod 4-2)}{2}-1\right)^2 \\ \ldots + \frac{1}{2}\left(2N-1\right) + \frac{1}{2}\left(\frac{N}{2}-1\right) \\ \ldots + \frac{1}{4}\left(N \bmod 4-2\right)\left(\frac{N-(N \bmod 4-2)}{2}-1\right) \\ \ldots + \frac{N}{8}\left(\frac{N}{2}-3\right) - \frac{1}{4}\left(\frac{N}{2}-3+\frac{N \bmod 4-2}{2}\right) \end{array} \right\} \tag{5}$$

where N is an even number of carriers, and v is the amplitude of each carrier. This formula was derived using extensive enumeration of the 3rd order IM products. It is valid for the middle carriers, which experience more IM than the carriers at the edges of the channel. No coding, or predistortion was assumed to reduce the peak-to-average ratio. Based on this IM level that each of the N carriers experiences, the 3rd order distortion after a certain block can be approximated as:

$$IM_{3,i} = \alpha_{1,i}\, IM_{3,i-1} + im_{3,1} \tag{6}$$

where $im_{3,i}$ is the 3rd order IM generated in stage i, $IM_{3,i}$ is the total IM at the output of stage i, which also includes the (amplified) IM of the previous stage. Now that the IM distortion is estimated at every carrier, the total IM distortion can be calculated, and consequently also the SINAD.

IV. SIMULATION RESULTS

In the receiver model, the gain of the different blocks can be optimized automatically to maximize the SINAD. Since the maximum SINAD is a trade-off between noise and IM, this is not a trivial job to do manually. Especially because the IM depends on the signal level. The stronger the signal the higher the SNR, but the lower the signal to distortion ratio. Fig. 4 shows a simplified block diagram, corresponding parameters and a simulation result as an example.

The parameters taken for the non-linearity and the noise are derived from an ongoing circuit design. Several effects are not included in this model e.g. phase noise, rejection of the image frequencies due to the frequency conversion, rejection of the aliasing frequencies due to the ADC, etc. because it would make the simulation unnecessarily complex. Each of these factors can be kept well below the resulting SINAD by a proper choice of the frequency conversion scheme, the AFE architecture and the circuit design. The details of the analog design will be presented when measurement results become available; the purpose of this paper is to show the feasibility and potential of an integrated frequency conversion front end. Table 1 summarizes the simulation results as a function of the attenuation between the TX and the RX taking into account optimum gain settings at the different stages and a BW of 1 MHz, a TX level of -60 dBm/Hz, 128 carriers, and a powerline noise floor of -140 dBm/Hz. The simulation model also learns what range of gain settings is required at every step. This SINAD computer simulation did not include interferences, however, this architecture is more robust against the conventional architectures. The effect of peak-to-average-power ratio (PAPR) reduction techniques was not yet taken into account. Moreover, the 3rd order polynomial approximation based on the 1 dB compression point often

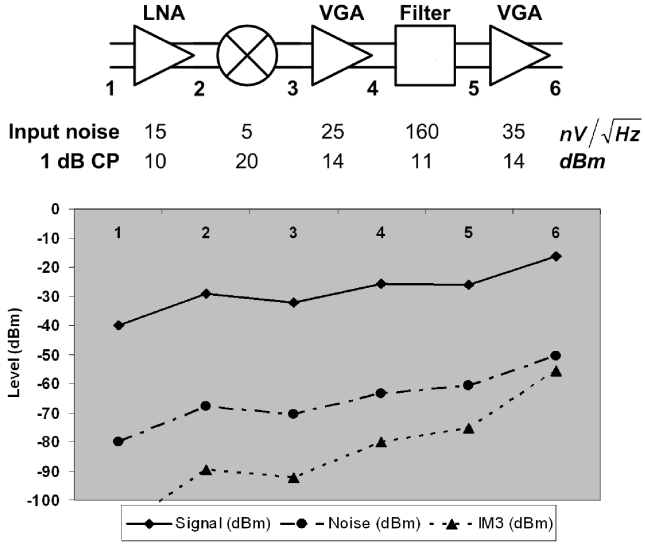

Fig. 4. Simplified receiver block diagram including main parameters. A simulation result shows the signal level, the noise and the 3rd order IM at the output of the different stages.

Attenuation [dB]	SINAD [dB]	Modulation scheme
0-40	>34	1024 QAM
41-49	>28	256 QAM
50-55	>23	64 QAM
56-61	>17	16 QAM
62-68	>10	4 QAM

Fig. 5. Summary of the applicable modulation scheme

overestimates the distortion for signals well below the 1dB compression point because the 1 dB compression point is often determined by clipping. Below the clipping point the IM is better compared to what is predicted based on the 1 dB compression point.

Several conclusions can be drawn from the results presented in Fig. 5. First of all, sufficient SINAD can be achieved over a wide attenuation range. This enables high aggregate data rates in a system optimized for FDM. Secondly, peer-to-peer operation can effectively increase the throughput in the system. Assume for example the attenuation between two nodes is 70 dB, and that an intermediate node is available. The communication to the intermediate node can ideally use a modulation scheme of 1024 QAM.

V. CONCLUSION

An analog front-end ASIC, based on a frequency conversion architecture, has been proposed. It is shown that such schemes overcome the disadvantages of conventional architectures in PLC systems based on FDM enabling co-existence. A model is presented to estimate the SINAD in a multi-carrier modulation scheme. Simulation results, based on parameters extracted from integrated circuits in development, show that high aggregate data rates can be achieved over a wide range of attenuation.

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