The ePIXnet Silicon Photonics Platform

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Abstract— **The ePIXnet Silicon Photonics Platform provides a facility access programme for research and prototyping of silicon-on-insulator nanophotonic devices and circuits, based on cost sharing and CMOS fabrication facilities.**

I. Introduction

The silicon photonics platform is an initiative of the EU ePIXnet Network of Excellence. The main activity of the platform is its facility access programme. This programme is briefly introduced in section II. However, the platform's activities extend beyond this programme, as described in section III. More information is available through the website at **http://www.siliconphotonics.eu**.

II. Facility Access Programme

The silicon photonics platform offers access to the CMOS research facilities of IMEC (Belgium) and CEA-LETI (France) for fabrication of silicon photonic circuits with stable processes. Through cost sharing, a large reduction in the cost per user can be obtained, to levels that are affordable for research labs and start-up companies. The platform is ideal for fabricating a lot of different structures, design variations of one component, or large and dense photonic integrated circuits on one chip. Moreover, a user of the platform gets a full wafer of chips, and an automatic parameter variation can be obtained over the wafer if desired.

A. Cost sharing

The users signing in to a fabrication run share the mask cost, the actual processing cost, and the cost of the mask checking and integration and post-processing such as thinning and dicing. In this way, a large cost reduction is obtained. To reach this, the platform re-uses the strengths of the CMOS fabrication environments.

For instance, without cost sharing a design with a 10-step fabrication process and a 10mm by 10mm mask area would cost over 15000 euro to get designed and fabricated on a single wafer. Through cost sharing, this can typically be reduced to 5000 to 7000 euro or even better. For designs with less processing steps, which are very relevant today for research on silicon photonic integrated circuits, a user can get a full wafer, with an automatic parameter space variation, for typical cost of 2000 to 5000 euro. The more users join a fabrication run, the lower the cost for each user. The platform offers a limited but still diverse set of processes, and to a certain extent standardizes on mask design, allow for further cost reduction.

The cost paid by the user reflects the actual cost, including mask, mask checking and integration, processing and post-processing. A cost model is elaborated on the website. As the cost of coordination of the silicon photonics platform is covered by the EU ePIXnet Network of Excellence, users that are not an ePIXnet partner pay an overhead cost.

B. Work flow and Confidentiality

The platform issues calls for participation 2 to 3 times a year, to which users can sign in. The users deliver their mask designs and the platform returns the users one or a few wafers each. The facility access programme is basically open to research labs and commercial users, from Europe and world-wide. The facility access programme currently runs at best effort, no guarantees are given. More details can be found on the website.

As cost reduction is obtained through sharing, the platform works with a multi-project wafer approach, where most users will get a wafer not only containing their own design but also the designs of others. Therefore, a simple NDA needs to be signed by the fabricating partner and the users. If a user desires not to disclose in any way designs to other users, this can be agreed upon. Of course, the cost reduction is smaller in that case.

C. Offered technology

Both IMEC and CEA-LETI open up their CMOS pilot line through the silicon photonics platform. All technology is wafer-scale on 200mm SOI wafers. Only processes that are stable and known are offered. Process development is not a part of the platform.

a) Passive waveguide circuits: The platform offers passive waveguides and photonic crystals in SOI at both IMEC [1] and CEA-LETI [2]. IMEC focusses on a Si film thickness of 220nm and maximizes cost sharing in this way, while LETI offers a more flexible film thickness between 50nm and 400nm. At both locations, 193nm and 248nm deep UV lithography is used. Figure illustrates the typical kind of structures based on this technology.

b) Multiple etch steps: Beyond the processing of simple waveguide structures and photonic crystals, IMEC offers a standard grating coupler module for interfacing to fibre, again maximizing cost sharing. These grating couplers have great alignment tolerances and therefore allow for much easier and faster alignment than with end-fire coupling, saving precious

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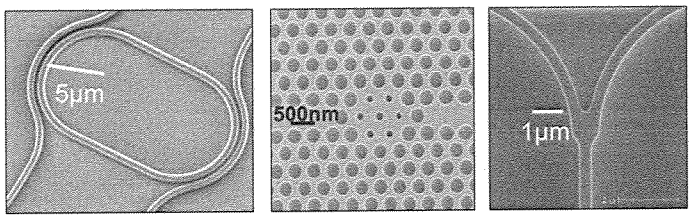

Fig. 1. Examples of structures based on Silicon-on-insulator photonic wires and photonic crystals.

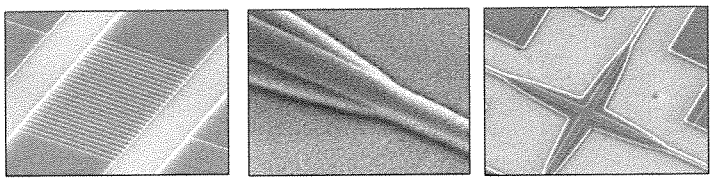

Fig. 2. Examples of structures based on a double shallow and deep etch in Silicon-on-insulator: grating coupler and low-loss crossing

time in characterisation. A guideline for creating a measurement setup is available on the website. The shallow etch used for this fibre couplers is also available to create double-etch structures, as illustrated in figure 2, and more advanced fibre couplers. The alignment tolerance between both lithography steps is about 50nm with the right alignment markers. The platform takes care of integrating the right alignment markers on the mask designs.

Like IMEC, CEA-LETI can etch shallow or completely through the Silicon film. The etch depth can be chosen flexibly.

c) Epitaxy and amorphous SOI: CEA-LETI also offers epitaxy of Si, SiGe and Ge films onto SOI. These processes can be used as a basis for advanced devices such as detectors and for complex structures with a varying Silicon film thickness. Additionaly, waveguides can be defined in amorphous Silicon-on-insulator in addition to the standard crystalline SOI [2]. To obtain planar surfaces, CMP (chemical mechanical polishing) steps can be included.

d) Post-processing: After fabrication, wafers can be diced if desired. At IMEC, wafers can be thinned to allow for an easy cleaving of facets. On the other hand, polished facets for end-fire coupling to (high NA or lensed) fibre can be obtained through the ePIXnet network packaging platform.

III. About the platform

The silicon photonics platform is created by the EU FP6 ePIXnet network of excellence. While the platform has grown from the facility access offered by IMEC in earlier projects and ePIXnet, it's mission is broader. The platform wants to help build a future for silicon photonics in Europe through the development of a fabless model for the fabrication of silicon photonic circuits. The whole rationale is to re-use as much as possible the processes, tools and methods of CMOS labs and foundries, and focus on the problems to be tackled for fabricating general silicon photonic circuits in a CMOS environment.

The platform is advancing beyond just offering the facility access programme and wants to foster roadmapping activities and explore commercial manufacturing routes for general silicon photonic circuits. While research and development is not a task of the platform, the platform wants to foster and help set out routes for the development of missing links in the design and fabrication toolchain, the definition of the various interfaces in this chain. Also, new processes that come available, implemented in a CMOS fabrication environment, can gradually be integrated in the facility access programme's offering.

Through all its activities, the platform wants to ease the transition of silicon photonic components from research to the market.

A newsletter is issued a few times a year with announcements and updates on the fabrication runs, new processes made available, news from the platform and research results from silicon photonic research groups. One can sign-in on this newsletter through the website.

IV. Contact

A lot of information is made public on the website http://www.siliconphotonics.eu. You can also contact the co-ordinator through e-mail (pieter.dumon@imec.be).

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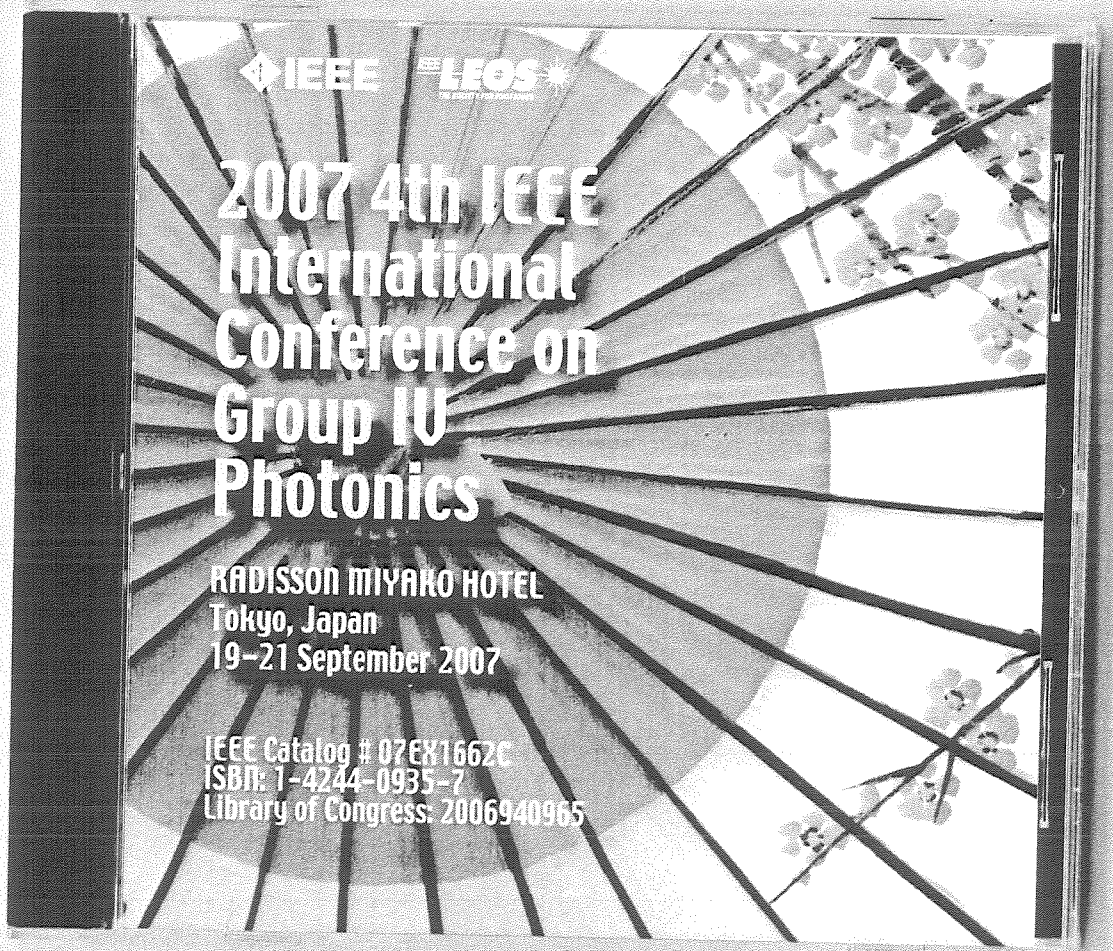
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