An Immunity Modeling Technique to Predict the Influence of Continuous Wave and Amplitude Modulated Noise on Nonlinear Analog Circuits

Celina Gazda, Dries Vande Ginste, Hendrik Rogier, Ivo Couckuyt and Tom Dhaene Department of Information Technology Ghent University Gent, Belgium Email: celina.gazda@intec.UGent.be Kristof Stijnen and Hugo Pues Melexis Technologies N.V. Tessenderlo, Belgium

Abstract—An innovative method to model, in the early design stage, the behavior of nonlinear analog circuits in the presence of noise is presented. The technique relies on Harmonic Balance analysis and the obtained model does not only efficiently predict the influence of a continuous wave disturbance, it may also be used to quickly estimate the device's behavior while being subjected to amplitude modulated noise. The method leverages surrogate models, as such reducing the simulation time and concealing the intellectual property of the circuit manufacturer. Moreover, the model can be easily integrated into a circuit simulator. An industrial case study of a voltage regulator for automotive applications is described in this contribution and it clearly confirms the capabilities of the method.

I. INTRODUCTION

The design of electronic circuits intended for the automotive industry is a challenging task, as these devices must be able to work in a noisy environment without suffering from electromagnetic compatibility (EMC) issues. Obviously, it is of utmost importance to guarantee proper EMC behavior of electronic circuits before they reach the market. To unify the validation methods, international EMC standards have been developed, providing clear definitions, exact testing procedures and limitations to the allowed levels of disturbance and susceptibility. However, the typical approach to verify a circuit's compliance with the EMC standards in its test or even production phase, often results in expensive redesigns and significantly lengthens the total time-to-market. To avoid this, efficient modeling techniques are needed that help engineers to mimic the EMC behavior of the circuit in its early design stage, giving the possibility to efficiently remedy the problems.

In this contribution we propose a novel method to construct a behavioral model, which allows to predict the performance of the electronic circuit subjected to a standardized immunity tests, such as the direct power injection (DPI) test. Using an industrial case study of a nonlinear analog voltage regulator, it is shown that the newly developed Harmonic Balance surrogatebased model is perfectly suited for modeling the impact of the continuous wave (CW) testing signals. Moreover, it also allows to quickly estimate the circuit's behavior when amplitude modulated (AM) noise is injected. As the constructed immunity model consists of surrogates, it provides a very short simulation time, while maintaining high accuracy and, very importantly, it hides the original netlist of the modeled circuit. The complete methodology was first detailed in [1] for CW noise only. This contribution demonstrates how to employ the obtained behavioral model to also predict the influence of AM noise on the behavior of the device.

In the next section we briefly describe how the DPI test is performed, using CW and AM testing signals. Section III presents the developed modeling technique. Section IV shows the CW DPI test results obtained using the proposed behavioral model and explains how to apply the model to also predict the AM DPI test. The last section summarizes our work.

II. DIRECT POWER INJECTION TEST



Fig. 1. Schematic configuration of the DPI test set-up

Fig. 1 depicts a schematic set-up of a DPI test, which is a popular immunity test that allows to validate the EMC behavior of an electronic circuit subjected to conducted radio frequency (RF) noise. To perform it under standardized conditions, we follow the 62132-4 standard of the International Technical Commission (IEC) [2]. Therefore, the device-undertest (DUT), i.e. the IC, is placed on a printed circuit board (PCB), together with all the necessary components required for the proper functioning of the DUT. Via a bias tee, a testing signal, i.e. RF noise, is injected into the DUT and its



Fig. 2. Peak preservation rule between continuous wave (CW) and amplitude modulated (AM) signal.

performance is being monitored, using a decoupling network with a very high impedance, represented in Fig. 1 by R. The frequency of the RF noise is swept from 150 kHz to 1 GHz and its power is varied between 0 dBm and 30 dBm. The maximal power levels at which the observed characteristics of the DUT remain within preset specifications are recorded. It is assumed that the DUT passes the test only if it can withstand 30 dBm of RF noise over the complete frequency range. Otherwise, the circuitry of the DUT must be adapted or extra precautions, such as for example ferrite beads or decoupling capacitors C_d , must be added to improve the EMC behavior.

The IEC 62132-4 DPI test specification states that the injected RF noise can be in the form of a continuous wave (CW)signal or that it can be amplitude modulated (AM). However, if the AM signal is applied, the peak power P_{AMpeak} , and thus also the corresponding peak voltage V_{AMpeak} (Fig. 2), should remain the same as in case of CW:

$$P_{AMpeak} = P_{CWpeak},\tag{1}$$

$$V_{AMpeak} = V_{CWpeak}.$$
 (2)

Therefore, the correlation between the mean power of the CW and the AM RF noise used in the DPI test, as shown in Annex B of the ISO11452-1 standard concerning road vehicles [3], can be expressed as:

$$\langle P_{AM} \rangle = \langle P_{CW} \rangle \cdot \frac{2+m^2}{2(1+m)^2},\tag{3}$$

where *m* is the modulation index and $\langle \cdot \rangle$ indicates the mean. By default it is recommended to perform the modulation using a modulating signal with frequency $f_{mod} = 1$ kHz and with m = 0.8. Substituting these values into (3), yields $\langle P_{AM} \rangle =$ $0.407 \langle P_{CW} \rangle$.

III. IMMUNITY MODELING - CASE STUDY

Since the CW DPI test is more severe for the DUT in terms of average injected power, we first focused on developing a modeling technique that allows a reliable prediction of the results of this test. As a case study, we used a nonlinear voltage regulator (VR), called MLXTC883, designed by Melexis Technologies N.V., Belgium, which consists of integrated active nonlinear components, i.e. 21 transistors, and 123 passive components (resistors and capacitors). In its intended automotive application, the VR MLXTC883 receives 5V DC on its supply pin, which it converts into a stable 3.3V DC on its output. However, it is found that, for a large range of noise frequencies and for sufficiently high noise amplitude, the desired 3.3 V output voltage drops significantly.



Fig. 3. Schematic used for Harmonic Balance simulation of the voltage regulator.

To effectively model this nonlinear behavior, first, we collect all necessary data by means of Harmonic Balance (HB) simulations of the VR's original netlist. We use this simulation method, because it yields frequency-domain data by directly calculating the steady-state spectral content of voltages and currents in the circuit, thus it is perfectly suited to analyze nonlinear analog circuits. Moreover, HB simulation is much faster than transient tests, hence we can significantly reduce the total modeling time. We perform the simulations in Agilent's Advanced Design System (ADS), using the circuit schematic presented in Fig. 3. The custom-created block, containing the complete netlist of the investigated VR, is connected to a voltage source, which produces a waveform:

$$V_{in}(t) = V_{in,CW}(t) \equiv V_{in,DC} + V_{in,CW} \sin(2\pi f_{noise} t).$$
(4)

This signal consists of the 5V DC component $V_{in,DC}$ that represents the DC supply of the MLXTC883 VR, and the RF component, being the CW RF noise at frequency f_{noise} and amplitude $V_{in,CW}$. As our research goal is to investigate the influence of RF noise on the performance of this VR, the DC input voltage $V_{in,DC}$ is fixed. By varying f_{noise} and $V_{in,CW}$, a complete analysis of the circuit's immunity behavior is obtained, and a parameterized model can be constructed.

To generate an accurate immunity model of the MLXTC883 VR, the DC current and the first harmonic at the input are recorded (tests proved that higher order harmonics are negligible, for further details see [1]), approximating the total input current as:

$$I_{in}(t) \approx I_{in,DC}(f_{noise}, V_{in,CW}) + I_{in,CW,1}(f_{noise}, V_{in,CW}) \sin(2\pi f_{noise} t).$$
(5)

The nonlinear behavior of the VR is characterized in (5) by the dependance of the DC component $I_{in,DC}$ and the first harmonic $I_{in,CW,1}$ on the CW noise frequency and amplitude. From the input voltage and the input current, for both the DC and the first harmonic, we define the corresponding input impedances as follows:

$$R_{in,DC}(f_{noise}, V_{in,CW}) = \frac{V_{in,DC}}{I_{in,DC}(f_{noise}, V_{in,CW})},$$
 (6)

$$Z_{in,CW,1}(f_{noise}, V_{in,CW}) = \frac{V_{in,CW}}{I_{in,CW,1}(f_{noise}, V_{in,CW})}.$$
 (7)

These two impedances can make sure that for a given input signal (9), the current I_{in} flowing into the VR remains correct, accurately mimicking the circuit's behavior during DPI test conditions. Therefore, these impedances constitute two essential building blocks of the developed immunity model. The third and last component of the model represents the DC output voltage, approximated as:

$$V_{out}(t) \approx V_{out,DC}(f_{noise}, V_{in,CW}),\tag{8}$$

and it models the nonlinear response of the voltage regulator in the presence of the injected CW RF noise. It is sufficient to consider only the DC voltage at the output of the VR, as the circuit, thanks to its low-pass filtering characteristics, suppresses the RF signals at its output [1]. Additionally, we consider the output pin as being open, because in its typical automotive application, as well as during the DPI test, this pin is loaded with a very high impedance. Thus, the output impedance, does not have an impact on the behavior of the VR and therefore it is not included in the model. All the parameters and assumptions explained above lead to the equivalent model architecture depicted in Fig. 4. To speed-up the simulation process and to hide the intellectual property of the circuit's manufacturer, while still maintaining high accuracy, we represent these three crucial model components $R_{in,DC}$, $Z_{in,CW,1}$ and $V_{out,DC}$ by surrogates [4], more specifically by artificial neural networks (ANNs) [5], [6]. A detailed description of how the surrogates were created is given in [1].



Fig. 4. Architecture of the voltage regulator's behavioral model, illustrating the three pertinent components (building blocks).

IV. RESULTS

A. CW testing signal

We now integrate the model of Fig. 4 back into Agilent's ADS circuit simulator. This is a straightforward operation, as all three components are ANNs, which are merely mathematical functions. An exemplary comparison of the $V_{out,DC}$ characteristics obtained from the HB simulations using the

original VR netlist (red line) on the one hand and from the surrogate model (green line with squares) on the other hand, is presented in Fig. 5. In this case, the frequency f_{noise} is fixed to 30 MHz and the amplitude of the CW RF noise $V_{in,CW}$ is swept from 0.32 to 10 V, which corresponds to an injection of CW RF noise with power increasing from 0 to 30 dBm in a 50 Ω load system, as required by the specifications given in [2]. Very good agreement between both results is obtained, which proves that our surrogate-based model can accurately predict the influence of the CW RF noise on the investigated VR. The total time needed to obtain results from Fig. 5 by employing the circuit's original netlist equals 70.15 s, whereas for the immunity model it only takes 1.8 s, resulting in a speed-up factor of 39. This clearly indicates the efficiency of our method.



Fig. 5. Validation of the immunity modeling approach: $V_{out,DC}(f_{noise}, V_{in,CW})$ at $f_{noise} = 30$ MHz.

To further test our immunity model, we integrate it into a complete setup of the DPI test, specified in [2], which principle schematic was presented in Fig. 1. The block representing the VR (its original netlist or the behavioral model) is now first connected to 1 nH inductors that mimic the role of the VR's package. Next, by adopting the EM/circuit co-simulation technique described in [7], the effect of the PCB is included. Thereto, using full-wave simulation obtained with ADS-Momentum, the pertinent scattering parameters of the unpopulated PCB are imported into the circuit solver, where they are combined with the other components, i.e. the packaged VR and the necessary lumped elements. A DC blocking capacitor capacitor AVX Z5U 08055E223MAT2A with a nominal value C = 22 nF, together with DC feeding inductor (Ferroperm Type 1583 RF choke) with a nominal value $L = 47 \ \mu \text{H}$ constitute the bias tee. The choice of these lumped components, including their parasitic effects, is carefully made, as advised in [7], so that the requirements concerning the pertinent RF injection path given in [2] are fulfilled. The 5V DC supply is provided from a DC voltage source with a DC supply capacitor GCM1885C1H331JA16 of 330pF, and the RF noise is generated by an RF power generator. The behavior of the VR, i.e. its output DC voltage, is monitored using a resistor of $R = 1 k\Omega$ as decoupling network.



Fig. 6. Comparison of the CW DPI test results of the original circuit and the surrogate-based behavioral model.

Fig. 6 shows the results of the simulated DPI test using both the original netlist (red line) and the surrogate-based model (green line with circles). These curves represent the maximum value of the CW RF noise power P_{noise} (in dBm) that the investigated VR can withstand while Vout, DC still remains within an acceptable ± 100 mV margin from its desired value, i.e. $V_{out,DC} \in [3.2V, 3.4V]$. Over the complete frequency range of the simulated DPI test, very good agreement between both results is observed. At 150 kHz, according to the original netlist, the IC withstands 19 dBm and still functions correctly, whereas the immunity model returns a value of 18 dBm. For the broad frequency range from 500 kHz till 100 MHz, the VR cannot withstands more than 14 dBm of CW RF noise. For frequencies higher than 300 MHz, the IC fully passes the DPI test, as it is capable to withstand 30 dBm of CW RF noise. The simulation time for this test using the original netlist equals 2913.8 s, whereas for the same test performed by relying on the surrogate-based model only 32.6 s are needed. Therefore, by applying the proposed behavioral model, a significant speed-up factor of 90 is obtained.

B. AM testing signal

Now we demonstrate how the developed immunity model allows to quickly estimate the influence of an AM testing signal on the circuit. As an example of the injected AM RF noise, we use the signal presented in Fig. 7(a) (detailed view in Fig. 7(b)), which has the waveform:

$$V_{in}(t) = V_{in,AM}(t) \equiv V_{in,DC}$$
(9)
+ $\frac{V_{in,CW}}{(1+m)} (1+m\cos(2\pi f_{mod} t))\cos(2\pi f_{noise} t),$

where $V_{in,DC}$ is the 5 V DC supply, the modulating index m = 0.8, the modulating frequency $f_{mod} = 1$ kHz, the noise frequency f_{noise} is equal to 30 MHz, and the peak amplitude of the AM RF noise is equal to 10V. This peak amplitude corresponds to the requirement put forward in Section II, and it is equivalent to the maximum CW RF noise of 30 dBm. Note also, from Fig. 6, that the VR performs the worst at this noise frequency of 30 MHz. First, a transient simulation



Fig. 7. AM RF noise injection (a) $V_{in}(t)$ (b) zoomed view of $V_{in}(t)$ (c) $V_{out}(t)$.

was leveraged to analyze the influence of this AM RF signal on the output voltage. This simulation took 84 min 32 s. This very long simulation time can be attributed to the multi-scale problem we are dealing with. Indeed, the rapidly oscillating carrier signal requires many testing samples (using classical simulation techniques, the sampling frequency should be at least twice the frequency of the sampled signal) and the slowly varying modulating signal requires a long signal duration.

To expedite the simulations we propose to use the surrogatebased immunity model again, but this time to reconstruct the time-domain waveform. Thereto, first, we collect n samples from the envelope $V_{env}(t)$ of the AM RF noise. This envelope is marked with a black line in Fig. 7(a) and the collected samples are indicated by the black squares. Second, each envelope sample, denoted $V_{env}(t_n)$, is translated into an output sample $V_{out,DC}(t_n)$. This is done by using $V_{env}(t_n)$, i.e. the amplitude of the modulation, and the frequency f_{noise} of the carrier (here 30 MHz) as input for our immunity model of Fig. 5. By collecting all the $V_{out,DC}(t_n)$ values, marked in Fig. 7(c) with black squares, we can quickly reconstruct the $V_{out}(t)$ signal. A good agreement with the results from the transient simulation of the original netlist (red line) is obtained. Furthermore, the total simulation time of the novel approach is of the order of seconds (depending on the number of samples). In future work we will investigate to what extent this method to efficiently reproduce these kind of time-domain waveforms can be extended to general analog circuits.

V. CONCLUSION

A surrogate-based immunity modeling technique, which allows to predict the behavior of electronic devices during immunity testing, has been proposed. The model is constructed starting from Harmonic Balance simulations and a proper model architecture was put forward. By replacing the pertinent components of the developed model with surrogates, the model hides the original netlist of the circuit and it is easily integrated into commercial software. Moreover, the simulation time becomes very short.

In this contribution, an industrial case study, being a nonlinear analog voltage regulator for automotive applications, was selected. First, the immunity model was validated by mimicking the DPI test (IEC62132-4), during which a CW RF noise signal is injected into the DUT. Very good agreement between the results obtained with the original netlist and with the novel immunity model were presented. Second, it was shown that the model can also be leveraged to mimic the behavior of the VR whilst being subjected to an AM RF noise signal. Apart from the good agreement, compared to the transient simulations of the original netlist, a considerable speed-up was obtained.

REFERENCES

- C. Gazda, D. Vande Ginste, H. Rogier, I. Couckuyt, T. Dhaene, K. Stijnen, and H. Pues, "Harmonic Balance surrogate-based immunity modeling of a nonlinear analog circuit," *accepted for publication in IEEE Transactions* on Electromagnetic Compatibility, vol. -, pp. –, 2013.
- [2] Integrated Circuits Measurement of Electromagnetic Immunity, 150 kHz to 1 GHz - part 4: Measurement of Conducted Immunity - direct RF power injection method., International Electrotechnical Commission, IEC 62132-4 Std., 2006.
- [3] Road Vehicles Component Test Methods for Electrical Disturbances from Narrowband Radiated Electromagnetic Energy Part 1: General Principles and Terminology, International Organization for Standardization, ISO 11452-1 Std., 2005.
- [4] M. Yelten, T. Zhu, S. Koziel, P. Franzon, and M. Steer, "Demystifying surrogate modeling for circuits and systems," *IEEE Circuits and Systems Magazine*, vol. 12, no. 1, pp. 45–63, Feb. 2012.

- [5] J. Lawrence, Introduction to Neural Networks, 5th Edition. California Scientific, Nevada City, 1993.
- [6] D. Gorissen, L. De Tommasi, K. Crombecq, and T. Dhaene, "Sequential modeling of a low noise amplifier with neural networks and active learning," *Neural Comput. Appl.*, vol. 18, no. 5, pp. 485–494, Jun. 2009.
- [7] D. Vande Ginste, H. Rogier, D. De Zutter, and H. Pues, "Efficient analysis and design strategies for radio frequency boards dedicated to integrity monitoring of integrated circuits using an electromagnetic/circuit codesign technique," *IET Science, Measurement Technology*, vol. 4, no. 5, pp. 268–277, Sep. 2010.