

# Assembly of Optoelectronics for Efficient Chip-to-Waveguide Coupling

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## Abstract

This paper presents two solutions to achieve efficient optical coupling between vertical cavity surface emitting lasers and planar optical waveguides, by minimizing the free space optical path length. One approach is based on embedding of optoelectronic chips in polymer layers, and the other approach on flip-chip assembly using micro-bumps. These micro-bumps are defined by laser-induced-forward-transfer (LIFT), a technique in which the bumping material can be transferred from a donor carrier to the waveguiding substrate. In both cases, out-of-plane bending of the light is accomplished by using a 45 degrees micro-mirror interface.

## Rationale

Light as a transmission medium for data communication has proven its success for many years. Over long distances like intercontinental and intercity links, optical interconnects have been the obvious choice due to the low propagation losses and high bandwidth. Over short distances, optical interconnections have only found their way into supercomputers and some niche applications, since higher cost and a sometimes drastic change in system architecture are still jeopardizing the transition from electrical to optical interconnections. These drawbacks are however slowly fading away owing to recent progress in commercially available optoelectronic components, optical waveguide materials and new process techniques. In the meantime, the channel speeds in current communication systems have past the point of 10 Gbit/s and is currently in a research context scaling up to 25 Gbit/s and more, at which electromagnetic interference is limiting the use and the density of electrical interconnections [1].

The need for the transition from electrical to optical interconnections is thus fastly approaching for systems where data speeds are continuously growing. Since materials, active devices and fabrication tools are improving due to this trend, one must also tackle the high costs related to optical coupling. Unlike electronic coupling, which is quite straightforward, optical coupling is more complicated and therefore more costly because light is directional and has to be directed, reflected, confined and focused in the aim to prevent excessive losses over the propagation path of the light. Waveguiding structures like planar polymer waveguides or discrete polymer or silica fibers can confine the light during propagation by making use of total internal reflection on the interface between waveguide core and cladding, and bends in the waveguide can steer the light to the desired direction. However, one must couple the light from a light source into this waveguiding structure at one side and at the other side, the light exiting the waveguides needs to be coupled into a

photodetector in view of realizing a complete optical communication link. This coupling results for many systems in a significant addition of complexity and thus cost.

The main reason for the complexity is the way the optoelectronic device is packaged. Standard flip chip and wirebonding assembly processes of optoelectronic (OE) components result in quite bulky OE-packages, making it very difficult to couple the light from the OE to optical waveguiding structures because of the long free space path length before the entry of the waveguide. Consequently there is a need for active alignment or for lens arrays to focus the light into the waveguide when a passive alignment method is envisioned [2].

In this paper, we present two advanced OE assembly processes, which limit the free space optical propagation distance from the OE to the waveguide to 100  $\mu\text{m}$ , eliminating the need for microlenses. The resulting coupling schemes approach the theoretical optimal situation of butt-coupling. The presented assembly processes focus on enabling the co-integration of OE-assembly and optical coupling in a miniaturized coupling scheme.

## Polymer embedding of optoelectronic components

The first OE assembly approach is based on the face-up embedding of ultra-thin VCSELs and photodiodes in thin polymer layers. The basic embedding process has been described in detail in the past [3]. In view of a clear understanding of the presented coupling schemes in this paper, we briefly describe the abovementioned chip embedding technique.

Before embedding, the commercially available optoelectronic components are thinned down by lapping and polishing to 20  $\mu\text{m}$ , allowing for a thin polymer embedding layer to minimize the stress in the package. The resulting ultra-thin OE's have a high yield, no change in optical or electrical performance and have a very low backside roughness below 10 nm. This OE thinning can be performed on wafer-level as to upscale the process. A complete planar package is obtained by laser ablating a cavity in a spin-on polymer layer, followed by mounting of the OE in the cavity, using adhesive. Consecutively, a final spin-on polymer covers the chip, levels out the irregular surface underneath and acts as a dielectric for the interconnection of the embedded chip. This galvanic interconnection is realized by laser ablation of micro-via's towards the contact pads of the embedded chip (via resistance = 16,5 m $\Omega$ ), followed by metallization, photolithography and etching of the electrical fan-out. The complete process flow is illustrated in Figure 1. Figure 2 shows the top view of a VCSEL embedded in SU8 polymer (MicroChem

Corporation) on top of an FR-4 PCB-substrate. This packaging approach results in a fully contacted OE, covered

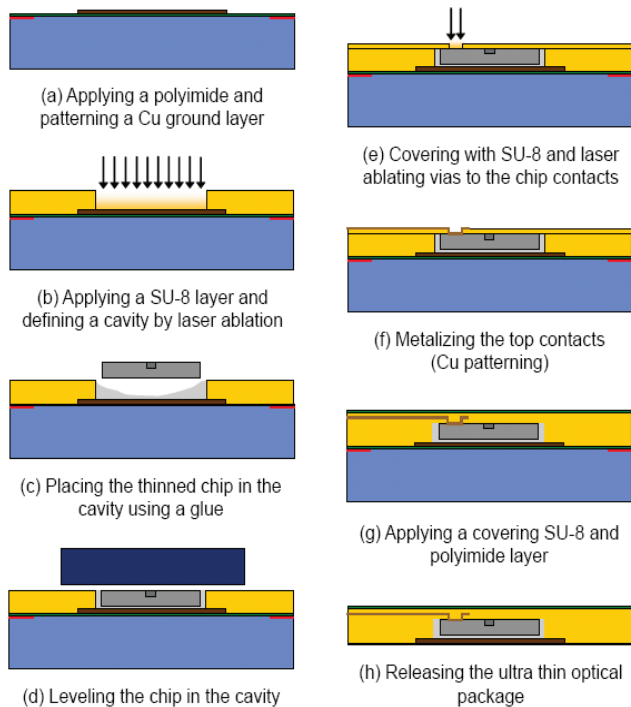


Figure 1: Process flow for the polymer embedding and release of ultra- thin optoelectronic components.

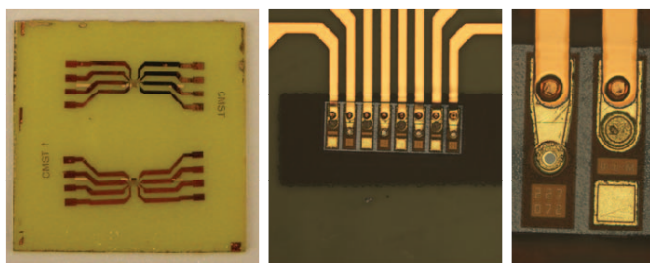


Figure 2: The top view of a VCSEL embedded in SU8 polymer (MicroChem Corporation) on top of an FR-4 PCB-substrate.

by an optically transparent layer of only 10  $\mu\text{m}$ . The heat dissipated in the chip can be spread out by a heat sink, patterned on the substrate before application of the first polymer layer. When the polymer layers are processed on top of a polyimide layer (deposited on a glass carrier), release of the complete polymer stack from the substrate can be achieved, resulting in a 50  $\mu\text{m}$  thin, flexible OE package. The package has a minimum bending radius of 2.5 mm and can endure 1000 bending cycles at this radius. The electrical VI-curve, optical LI curve, and modal behavior of the embedded dies are preserved after the packaging. The heat spreading has been monitored by measuring the red-shift, showing very good thermal behavior, depending on the substrate where the package will finally be mounted on.

## Optical coupling of embedded optoelectronics

The planarity of the above presented OE assembly allows for any waveguiding structure to be brought into close contact to the optical active area of the chip without e.g. the obstruction of wirebonds. Different coupling scenarios were investigated all schematically shown in Figure 3.

### A. Butt coupling of optical fibers or waveguide foil vertical positioned on top the package

The 10  $\mu\text{m}$  transparent polymer layer in between the waveguiding structure and the OE results in negligible losses. The use of index-matching gel can eliminate possible reflection losses at the interface. The vertical mounting however nullifies the advantages of the planar approach of the OE embedding concerning the compactness, the scalability of the mounting process and the reliability of the connection.

### B. Coupling into planar waveguides, positioned in a horizontal way on top of the planar embedded OE

This approach minimizes the thickness of the complete assembly. However, 90 degree out-of-plane light bending has to be introduced. This is accomplished by the use of 45 degree coupling plug. The plug consists of a 100  $\mu\text{m}$  thin polymer foil with a gold coated 45 degree end facet [4]. Figure 4 shows an image of the mirror plug after gold evaporation (left) and a closer angled view (center) and cross-section (right). The plug can be mounted with standard pick and place assembly tools on the embedded OE. The light from the OE will be deflected into the horizontal plane by the mirror. Consecutively, a flexible waveguide foil can be mounted next to the mirror to confine the light, limiting the free optical path to the thickness of the waveguide foil. The fabrication of a flexible waveguide foil can be realized by structuring flexible optical waveguide materials and releasing them from their temporary rigid process carrier. Even stretchable materials like PDMS can be used to achieve deformable waveguide foils. Figure 5 shows the coupling of a PDMS multimode waveguide foil with an embedded 1x4 circular photodiode-array [5].

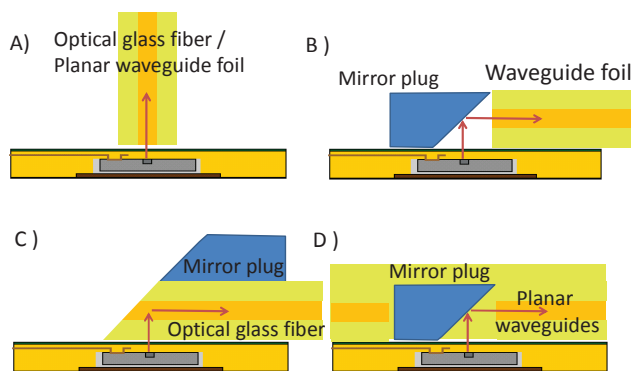


Figure 3: Schematic overview of four coupling approaches of the embedded optoelectronic components from and to a waveguiding medium.

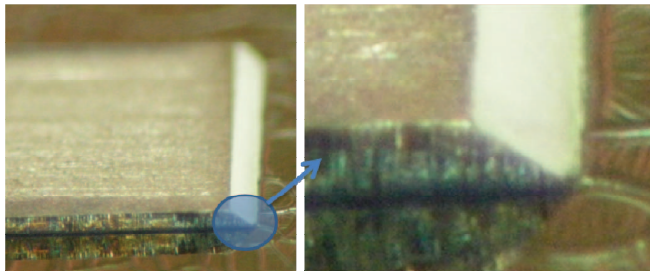


Figure 4: 45 degree mirror plug (2000 x 1000 x 100  $\mu\text{m}$ ), after gold evaporation

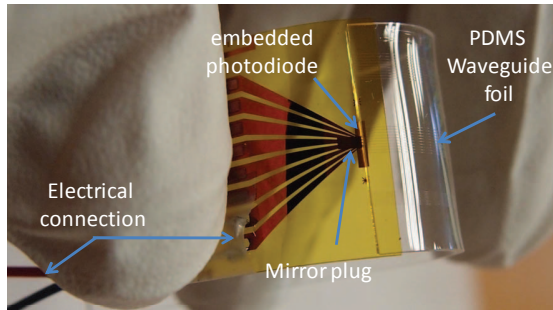


Figure 5: Coupling of a PDMS multimode waveguide foil with an embedded 100  $\mu\text{m}$  1x4 circular photodiode-array.

As an alternative for the few commercially available flexible waveguide materials, we developed a waveguide foil fabrication process in which rigid materials are used. The flexibility of the waveguide stack is enhanced by sandwiching the stack between two spin-on polyimide layers, which act as bending stress distribution layers, resulting in a minimum foil bending radius of 4.5 mm without any increase in the propagation losses after 1000 bending cycles. The optical bending losses at 850 nm at this radius are below 0.03 dB/cm.

#### C. Coupling into optical silica fibers, positioned in a horizontal way on top of the planar embedded OE

The mounting of fibers requires a fiber confining V-groove structure for passive alignment and fixation of the fiber. To further push the integration in this field, the mirror facet can be fabricated at the end of this V-groove structure. The V-grooves are fabricated in a 500  $\mu\text{m}$  thin PMMA ferrule by laser ablation, followed by UV adhesive mounting of the silica fibers in the grooves. After fiber mounting, the whole PMMA piece, containing the fiber, is polished at 45 degree resulting in a smooth end facet to the fiber with an rms roughness below 25 nm.

In a final step, a 100 nm thin gold layer is evaporated, which is required because the UV adhesive impedes total internal reflection. The PMMA piece is then actively aligned by driving current through the embedded VCSEL and measuring the light intensity at the fiber pigtail. When aligned, the PMMA piece is glued to the chip package using an UV curable adhesive. The coupling loss between an embedded VCSEL and a multimode optical fiber is 2,8 dB [6].

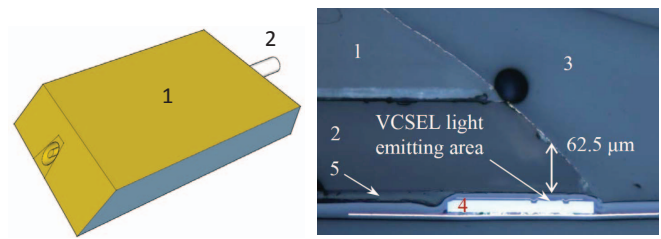


Figure 6: Design of the mirror plug (1) with integrated silica fiber (2) and polished 45 degree end facet (left), together with a cross-section of the UV-adhesive (3 and 5) mounted mirror plug on top of an embedded VCSEL chip (4) (right).

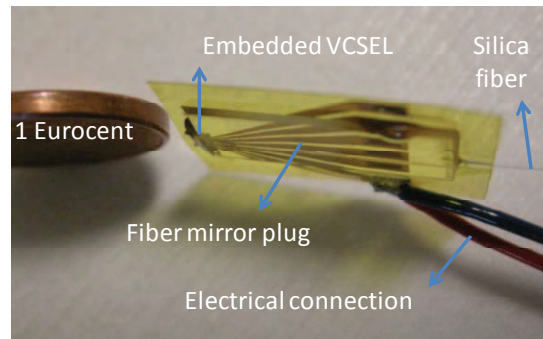


Figure 7: Image of a flexible VCSEL package with electrical interconnections and mounted mirror plug with silica fiber.

Figure 6 shows the design of the mirror plug with integrated silica fiber and polished 45 degree end facet (left), together with a cross-section of the mounted mirror plug on top of an embedded VCSEL chip (right). The cross-section provides a clear view on the free optical path length, which is 72.5  $\mu\text{m}$  (= silica fiber half width 62.5  $\mu\text{m}$  + 10  $\mu\text{m}$  VCSEL embedding polymer). Figure 7 shows a released flexible VCSEL package with electrical interconnections and mounted mirror plug with silica fiber.

#### D. Fabrication of planar polymer waveguides on top of the embedded OE

This approach results in the highest level of integration. The cladding-core-cladding build-up for waveguide formation can be fabricated directly on top of the package considering the high planarity of the package. Before fabricating the waveguide layer stack, a metal island is deposited and patterned on top of the embedded OE, which acts as a laser stop later on in the process to remove the waveguide layers locally on top the OE. This metal island assures the correct height of the mirror plug placement after the removal of the metal islands by chemical etching. The total stack of OE package and waveguide layers together is only 150  $\mu\text{m}$  thick. Figure 8 and 9 show the fully integrated optical link in a cross-sectional view and photograph view respectively. As demonstrator, a 1x4 multimode VCSEL array and a 1x4 photodiode array were embedded and optically interconnected through a 2 cm long 1x4 waveguide array, fabricated on top of the embedded devices. As depicted above, the coupling from and to the devices is performed by embedded mirror



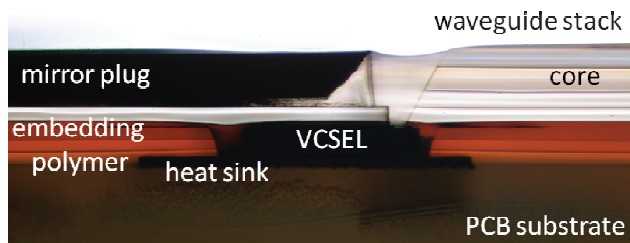


Figure 8: Cross-sectional view on the fully integrated VCSEL-to-waveguide coupling.

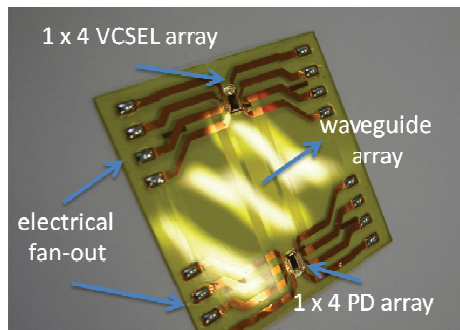


Figure 9: Image of the full integration of 4 parallel VCSEL to PD links in a 150 μm thin polymer stack.

plugs. As such, a complete parallel VCSEL-to-PD connection is realized. The total optical loss over the complete link is  $6,5 \pm 2$  dB, measured over multiple samples and links. The links also show good reliability in accelerated aging tests. The functionality of the optical links is not influenced by humidity exposure for 500 hours at 85 °C and at 85% r.h. or by 100 thermal cycles from -40 °C to 125 °C. More details can be found in [4].

### Flip-chip assembly of optoelectronic devices based on microbumps

The second approach is based on a flip chip assembly process, in which the electrical connection is achieved using micro-bumps. These structures are defined through laser-induced forward transfer (LIFT) of metal inks [7-9]. In LIFT, a donor substrate coated with a material to be transferred is brought in proximity with the receiver substrate. A focused pulsed laser beam induces the local release of the donor material from the donor substrate and transfers a pixel of material towards the receiver substrate. This technique is very versatile and flexible and is able to produce very small and thin micro-bumps in the order of microns for flip-chip assembly. The latter is a requirement to reduce the chip-to-waveguide distance after mounting of the OE. The coupling to planar waveguides is similarly achieved by a mirror plug which is mounted prior to the OE assembly as depicted in Figure 10. This work is ongoing.

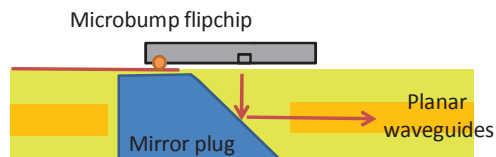


Figure 10: Schematic representation of the compact OE-to-waveguide coupling by flipchip using LIFT microbumps.

#### A. LIFT of AgNP bumps

Thin films of donors were prepared by spin coating (1000 rpm, 20 s) a silver nano-particle (AgNP) based ink (particle size: 100 nm; 20 wt% Ag content; viscosity: 10-14 mPas, curing temperature: 150 °C) from SunChemical onto a UV-transparent quartz carrier substrate (2.5 cm x 2.5 cm x 0.07 cm).

The samples were then kept for ~ 4 hours under ambient conditions to achieve an optimum AgNP concentration and viscosity for the donor film that enabled LIFTing of well-defined droplets (as reported in [9]). Glass substrates with pre-patterned Ni-Au plated bond-pads ( $80 \mu\text{m} \times 80 \mu\text{m} \times 4.5 \mu\text{m}$ ) were used as the receiver substrates. The donor-receiver assembly was mounted on a computer-controlled 2D translation stage and a spacing of 50 μm was maintained between the donor and the receiver by means of metallic spacers. Single laser pulses from an excimer laser (248 nm, 7 ns) were then focused at the carrier-donor interface thereby providing the force required to forward-transfer micro-dots of the AgNP ink onto the receiver substrate at the precise location of the Ni-Au-bond pads. All the experiments were performed in air and at room temperature.

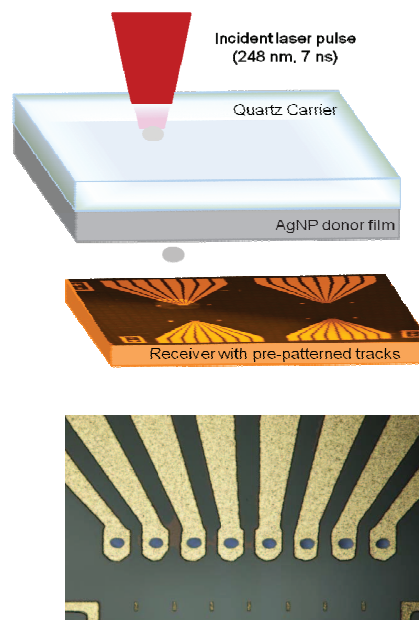


Figure 11: Schematic depicting the principle of the LIFT technique (top) and an optical micrograph of LIFTed AgNP ink micro-bumps (bottom). The line-pitch on the image is 125 μm.

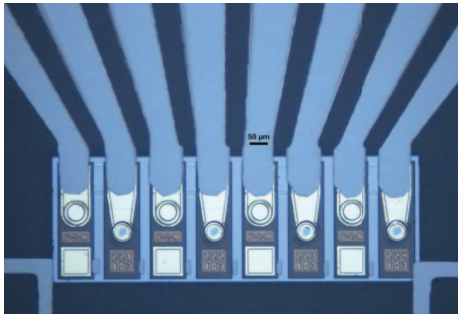


Figure 12: Single VCSEL array chip post-FC bonding to the bumped substrate.

Figure 11 (top) and 11 (bottom) show the schematic of the LIFT technique and the AgNP dots printed onto the receiver pads respectively. The LIFTed dots were measured to be  $\sim 30 \mu\text{m}$  in diameter and  $\sim 4 \mu\text{m}$  in thickness and were transferred at a laser fluence of  $4.2 \text{ J/cm}^2$ .

### B. Flip-chip assembly

Single VCSEL array (1x4) chips from ULM ( $1000 \mu\text{m}$ ,  $350 \mu\text{m} \times 150 \mu\text{m}$ ; 5 Gbps, 850 nm) were then bonded to these bumped substrates. A semi-automatic flip chip bonder (T 320-X) from Tresky was used to achieve thermo-compression bonding of the VCSEL chips to the substrates. The pressure used for bonding was 12.5 gf/bump and a temperature of  $150 \text{ }^\circ\text{C}$  was maintained between the pick-up tool and the chip.

The bonding time was set to 10 min to semi-cure the ink-bumps after which the assembly was transferred to a convection oven for  $\sim 60 \text{ min}$  @  $150 \text{ }^\circ\text{C}$  to evaporate the remaining solvent (ethanol, ethanediol, glycerine and 2-isopropoxyethanol). This ensured complete curing of the ink micro-bumps, and establishing an electrical and mechanical interconnection between the VCSEL chip and the substrate. Figure 12 shows a flip-chip bonded VCSEL as observed under an optical microscope from the backside of the receiver glass substrate.

### C. Characterization of the bonded assembly

The FC bonded VCSELs were subsequently characterized both electrically and optically. Figure 13 depicts the LIV curves recorded from a FC bonded VCSEL chip. The recorded curves were in good agreement with those from a bare die indicating the successful functioning of the VCSEL arrays post-bonding.

### Conclusions

Two optoelectronic device assembly approaches to achieve efficient optical coupling from these devices towards different optical waveguiding structures were proposed, fabricated and characterized. In one approach, the optoelectronics were embedded in polymer layers enabling the waveguiding structure to be brought into close contact to the OE. Multiple degrees of co-integration of the OEs and the coupling features were put forward, all resulting in low coupling losses and showing an increasing degree of miniaturization.

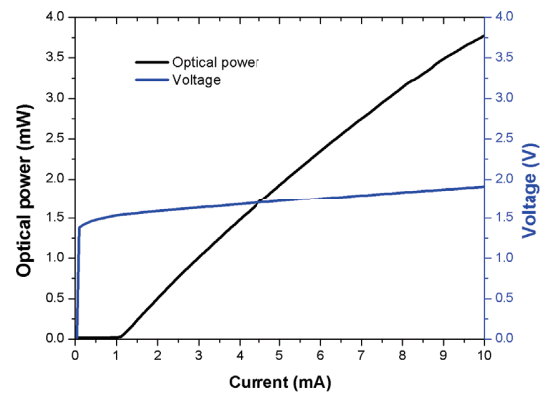


Figure 13: LIV curve recorded for a LIFT-assisted flip-chip bonded VCSEL array chip.

In another approach, the OEs were successfully flip-chip mounted using LIFT assisted microbumps, resulting in a very small distance between OE output and waveguide entry.

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