

A Programmable, Multi-Format Photonic Transceiver Platform Enabling Flexible Optical Networks

S. Dris^{1*}, M. Vanhovecke², A. Aimone³, D. Apostolopoulos¹, I. Lazarou¹, P. Demeester², J. Bauwelinck²,
G. Gotz⁴, T. Wahlbrink⁴, R. Magri⁵, I. Papafili⁶, G. Agapiou⁶, H. Avramopoulos¹

¹ National Technical University of Athens, 15780 Zografou, Greece

² Ghent University – iMinds – IMEC, Dep. INTEC, 9000 Ghent, Belgium

³ Fraunhofer Heinrich Hertz-Inst., 10587 Berlin, Germany

⁴ AMO GmbH, 52074 Aachen, Germany

⁵ Ericsson Telecomunicazioni, Pisa, Italy

⁶ Hellenic Telecommunications Organization S.A. (OTE), Maroussi, Greece

* e-mail: sdris@mail.ntua.gr

ABSTRACT

Development of programmable photonic devices for future flexible optical networks is ongoing. To this end, an innovative, multi-format QAM transmitter design is presented. It comprises a segmented-electrode InP IQ-MZM to be fabricated in InP, which can be directly driven by low-power CMOS logic. Arbitrary optical QAM format generation is made possible using only binary electrical signals, without the need for high-performance DACs and high-swing linear drivers. The concept enables a host of Tx-side DSP functionality, including the spectral shaping needed for Nyquist-WDM system concepts. In addition, we report on the development of an optical channel MUX/DEMUX, based on arrays of microresonator filters with reconfigurable bandwidths and center wavelengths. The device is intended for operation with multi-format flexible transceivers, enabling Dense (D)WDM superchannel aggregation and arbitrary spectral slicing in the context of a flexible grid environment.

Keywords: coherent optical systems, flexible optical networks, flexible transceiver, MUX/DEMUX

1. INTRODUCTION

The coherent revolution that has shaped modern telecom networks began roughly 10 years ago, when it became apparent that state-of-the-art CMOS technology could deliver cost- and energy-efficient real-time digital signal processing (DSP) for demodulation and impairment mitigation at the Gbaud-rates required by telecom optical systems. After more than a decade of hibernation, coherent intradyne detection suddenly re-emerged as a prominent topic of research in the field of telecoms, promising a significant boost in both capacity and reach over legacy systems based on simple modulation formats and direct detection. It was only a matter of time before optical transport network (OTN) 100G technology became standardized, with subsequent commercial adoption arriving in 2010. Today's core optical networks are starting to be dominated by 100G optical channels, based on Dual-Polarization (DP) Quadrature Phase Shift Keying (QPSK) at 28/32 Gbaud, definitively proving the commercial viability of the technology.

Scaling next-generation optical networks to higher capacities will necessitate further innovations: The insatiable demand for bandwidth is stretching physical layer capacity and dictating the migration towards flexible optical network architectures. Moreover the changing nature of data traffic, which is becoming more volatile and unpredictable, has prompted system designers to think about introducing flexibility in both modulation format and elasticity in spectrum utilization, by abandoning the fixed grid and allowing dynamic adjustment of throughput and wavelength allocation. The foundations for this fundamental paradigm shift were laid by the ITU-T as early as 2012: Recommendation G.694.1 [1] defines the Flexible Dense Wavelength Division Multiplexing (DWDM) grid, designed to accommodate optical lightpaths with mixed-bitrates and modulation formats, in slots that can be adjusted to any spectral width with 12.5 GHz granularity. Several elastic optical networking concepts based on software-defined networking (SDN) have since emerged, but complementary innovations at the physical layer are also required: Fully-programmable optical components supporting rate- and format-adaptation are also necessary to reap the benefits of flexible operation.

SPIRIT, a project funded by the EC's FP7 program, is developing a digitally-programmable photonic transceiver platform that, together with DSP-based impairment monitoring functionality, represents a promising approach toward enabling operational flexibility in optical metro and core networks. The envisaged photonic integrated circuit (PIC) leverages mature photonic and electronic technologies, to produce an energy-efficient solution: IQ Mach-Zehnder Modulators (MZM) in Indium Phosphide (InP) utilize a segmented-electrode design, and are driven directly by binary signals from low-power CMOS digital electronics. Moreover, the novel transmitter structure allows for the creation of multi-level optical signals with 5-bit resolution per I/Q arm without the use of DACs and linear drivers. A multitude of QAM formats are therefore supported at 28/32 Gbaud. WDM superchannel operation is supported by the inclusion of a Si microring resonator (MRR)-based multiplexer-demultiplexer (MUX/DEMUX). The innovative design of the MRR filters allows tuning of both the center wavelength, as well as the bandwidth of each optical channel. The proposed MUX/DEMUX

structure is therefore ideal for use in superchannel-based flexible grid (or even gridless) environments that enable a gain of up to 25% in net fiber capacity through more efficient spectrum use [2].

2. THE SPIRIT TRANSMITTER

2.1 Segmented-Electrode InP IQ-MZM with Direct Digital Drive using CMOS Inverters

A periodically-driven segmented-electrode modulator design is proposed, constituting a promising approach for overcoming the stringent trade-off between driving voltage and electro-optic (EO) bandwidth imposed by current state-of-the-art Travelling Wave Electrode (TWE) designs. In addition, it paves the way for greatly reducing driving voltage requirements, obviating the need for high-power amplifiers which are necessary to drive conventional modulators, and enabling direct digital drive with low voltage swings from CMOS logic instead.

Modulation efficiency is determined by the half-wave voltage \times length product ($V_\pi L$), which is constant for a given modulator technology. It is therefore possible to reduce the voltage (V_π) needed to induce a π phase shift in one arm of an MZM (and therefore the output swing required from the electronic drivers), by elongation of the waveguide interaction length (L). However, in TWE modulators, the phase velocity mismatch between the travelling electrical and optical signals, results in reduced EO modulation bandwidth, a problem that is exacerbated the further the length is increased. The proposed design solves this by employing multiple, high-bandwidth electrode segments at each MZM arm, that are individually driven by an amplifier array (Figure 1(a)). The input RF signal is applied sequentially at each driver with a delay from one segment to the next, in order to match the speed of the optical signal in the modulator chip. For this purpose, on-chip retiming circuits and programmable delay cells are included. Since the precise value of the required inter-segment delay depends upon process variations, the electronic delay circuits are made user-adjustable. The interaction length can therefore be longer, opening the way for low V_π design without sacrificing the EO bandwidth.

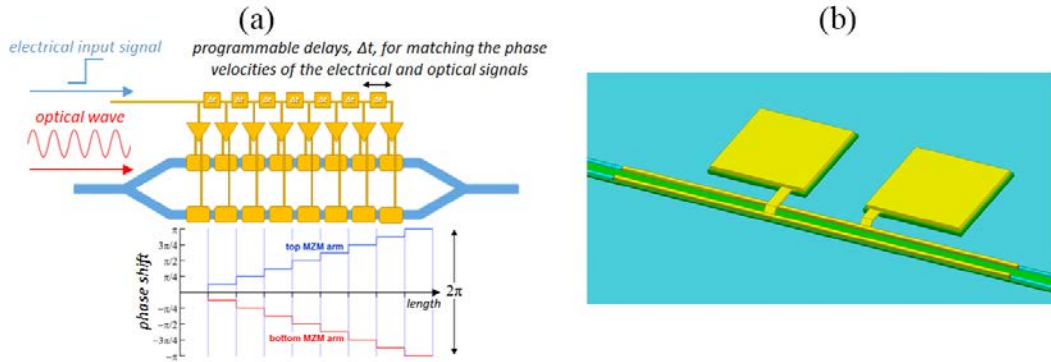


Figure 1. (a) Illustrating electro-optical phase velocity matching with the segmented-electrode MZM concept. (b) Model of a single electrode segment used to evaluate the design.

Challenges of a segmented modulator design include the single sections layout, their placement, and everything that concerns the optical level. Input and output spot size converters and multi-mode interferometers as splitters and couplers are included along the optical path. Dedicated phase sections are included in each modulator branch to allow the choice of modulator working point, which needs to be biased at the zero transmission point for IQ configuration. The segment design involves the consideration of several parameters such as segment length, waveguide width and intrinsic region thickness. These parameters affect the load that the CMOS electronics are required to drive, changing the achievable speed and modulation depth. In the SPIRIT modulator, the waveguide width is kept constant along the whole active area in order to minimize optical losses. In addition to the electrodes themselves, the air bridges and the contact pads need to be properly sized as well, as the parasitics they introduce need to be minimized. In particular, any additional parasitic capacitance that limits system bandwidth has to be avoided. Figure 1(b) shows the 3D model of a single segment that was used to evaluate the best design choices. As no TWE is present, there is no need for passive areas between the segments, and the different sections can be placed close to each other. However, due to the cross-talk through the shared biasing mesa and the technology limitations, a minimum spacing of some tenths of microns is required between the several sections.

The low voltage swing requirement, as well as the binary nature of the driving signals, makes low-power CMOS inverters in a deep submicron technology node the ideal circuit to drive the modulator segments. Since the segments are sufficiently small to be considered lumped capacitances, there is no need for power-hungry 50 Ω terminated drivers. In contrast to current-mode logic (CML) drivers, CMOS logic has negligible static power consumption, while providing a fast rail-to-rail output swing, allowing the design of a low-power output driver with less than 1pJ/bit power consumption. SPIRIT's modulators will be used in a nested I/Q configuration, in which an MZM is commonly biased at its zero transmission point and a peak-to-peak

modulation voltage of $2 V_\pi$ is required to completely switch the field transfer function of the modulator. With a supply voltage of 1.1 V, a complementary tapered inverter chain delivers a 2.2 V differential driving voltage.

2.2 Flexible, Multi-Format Functionality with Optical Arbitrary Waveform Generation

Multi-level optical signals are commonly generated by an electrical Digital-to-Analog Converter (DAC) followed by a linear driver. The proposed transmitter structure does away with these expensive, power-hungry components: Rather than change the drive voltage with a DAC, the effective interaction length is varied in a programmable fashion. By altering the number of segments contributing to the modulation, different optical levels can be generated, while the CMOS inverters keep on delivering a rail-to-rail output swing.

Each driver is controlled individually by CMOS logic functioning as an encoder that maps input binary words to the driver outputs; thus multiple optical levels at each MZM can be produced, and multi-level QAM can be generated with only binary signals driving a dual-nested IQ-MZM. SPIRIT's transmitter essentially functions as a digital-to-analog optical arbitrary waveform generator: It will be fully programmable by the digital lines of an external FPGA or ASIC with 5 bits of resolution per I/Q arm, allowing Tx-side DSP functionality such as static pre-compensation for linearization of the EO modulator response, digital filtering for chromatic dispersion pre-compensation, spectrum shaping (e.g. Raised Cosine pulse-shaping), and multi-carrier (OFDM) generation.

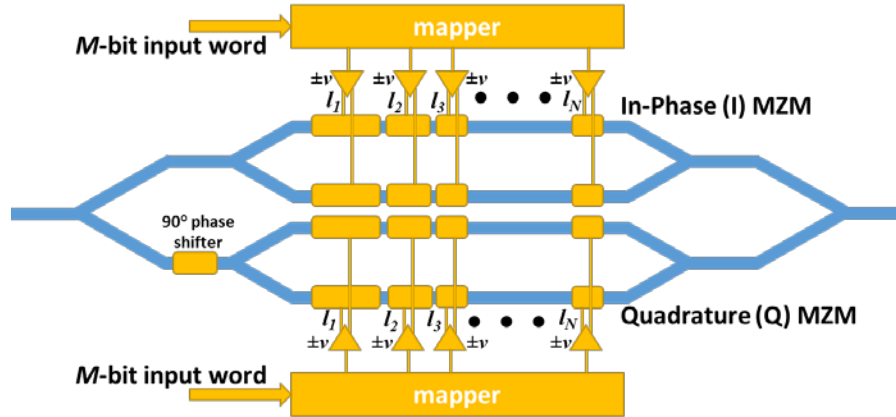


Figure 2. Showing the SPIRIT IQ-MZM with variable-length segmented electrodes (l_1, l_2, \dots, l_N), driven by binary amplifiers. A logic circuit maps M -bit input words to appropriate logic levels of the drivers, producing any desired multi-level optical signal at the output.

The principle of operation is illustrated in Figure 2, with an IQ-MZM whose in-phase (I) and quadrature (Q) electrodes are split in an identical fashion into N segments, with individual lengths l_j (where $j = 1 \dots N$). Each segment is driven in push-pull configuration, and receives a voltage level which can take one of two values ($\pm v$), corresponding to logical '0' and '1'. For each IQ-MZM input arm, and at discrete intervals in time, a digital logic circuit receives an input binary word of length M bits, and maps it onto one of 2^M unique combinations of voltage levels driving the segments, corresponding to a specific point on the I or Q axis of the output complex optical field. The mapper at each arm can be described by a $2^M \times N$ matrix denoted by \mathbf{B} . Each M -bit binary input indexes a specific row, \mathbf{B}_i , containing the respective binary voltages ($\pm v$) applied to the N electrode segments (in other words, for the i^{th} input word, matrix entry B_{ij} contains the voltage that must be applied to the j^{th} electrode segment). Given an input binary word \mathbf{X}_i , the output field transfer function is then given by:

$$\frac{E_{out}}{E_{in}}(X_i) = \frac{1}{2} \cos \left(\frac{\pi}{2V_\pi L} \sum_{j=1}^N B_{ij}^{(I)} l_j^{(I)} \right) + j \frac{1}{2} \cos \left(\frac{\pi}{2V_\pi L} \sum_{j=1}^N B_{ij}^{(Q)} l_j^{(Q)} \right) \quad (1)$$

Note that for proper IQ operation, each MZM structure must be set to its zero transmission point, by applying the appropriate DC bias voltage ($V_{bias} = -V_\pi L$). For clarity in equation (1) the bias voltage is not explicitly shown, but implicitly contained as a DC offset in the binary RF signals applied to the segments (that is, $B_{ij} = \pm v + V_{bias}$). In its simplest form, the segment lengths can be kept equal. The drawback is that with such a configuration, the number of segments needed grows exponentially with the desired output resolution ($N=2^M$). This results in increased power consumption, but also complicates integration and introduces signal integrity issues, due to the large number of RF lines needed to interface the drivers with the InP chip. Alternatively, the number of segments can be minimized by employing binary coded lengths (i.e. $l_1=x, l_2=2x, \dots, l_N=2^{M-1}x$), as in the theoretically proposed scheme of [3]. In practice, however, this is impractical; for sufficiently high resolution, the lengths vary enormously from segment to segment, thus presenting wildly different load conditions for the electronic drivers, rendering direct digital drive impossible. SPIRIT's design is an optimized trade-off that achieves 5-bit resolution, with only 10 segments whose variable lengths remain within a reasonable range for the drivers.

3. FLEXIBLE MUX/DEMUX

Reconfigurable multiplexers/demultiplexers (MUX/DEMUX) for Tx-side aggregation, and Rx-side slicing of Terabit/s DWDM superchannels, are key ingredients enabling next-generation flexible optical networks. A complete and integrable solution is being developed by SPIRIT researchers, with tunable filters fabricated in Si that address both the wavelength- and bandwidth-selectivity needed for flexible grid applications. The proposed structure is based on twin arrays of 8 2nd order micro-racetrack (MR) filters, attached to two joint bus waveguides feeding a polarization beam combiner; the structure is therefore able to shape, multiplex, and demultiplex 8- λ dual-polarization (DP) DWDM superchannel signals, with reconfigurable spectral widths, center wavelengths and channel spacings (Figure 3). The MRs are enhanced with a symmetric Mach Zehnder Interferometer (MZI) as a variable splitting-ratio coupler between the cross section of their sub-MRs, and are designed for bandwidth- and wavelength-resonance reconfigurability through thermal tuning with microheaters.

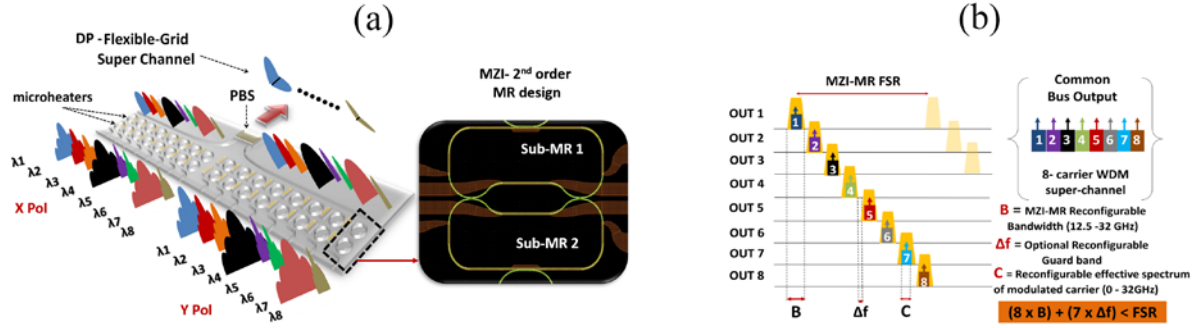


Figure 3. (a) Conceptual illustration of the flexible MUX operation. The inset shows an actual design of a single 2nd order MZI-MR. (b) MUX principle of a WDM superchannel in one polarization tributary.

Proof-of-concept simulations on a single MZI-assisted 2nd order MR (MZI-MR) show the suitability of the proposed approach for flexible grid applications, exhibiting minimum spectral degradation in the filter response, as well as spectral slot tunability between 12.4-32.5 GHz (Figure 4). MZI-MR test structures have also been recently fabricated in silicon on insulator (SOI) technology, with initial experimental results showing good agreement with the simulations, as well as on-the-fly reconfigurability (first results will be reported in [4]).

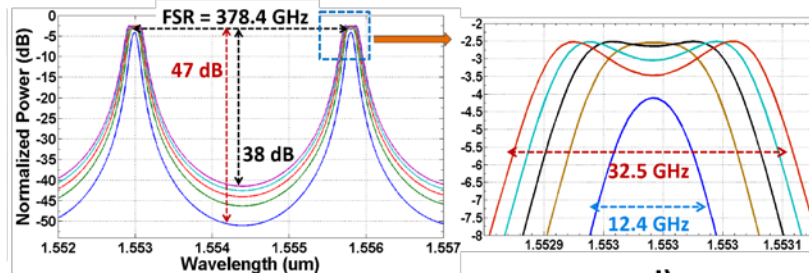


Figure 4. Simulated DROP spectral response (left) and close-up of the MZI-MR filter's 3 dB bandwidth evolution (right) for various MZI splitting ratios.

4. CONCLUSION

We have presented a concept for a CMOS-driven IQ-MZM transmitter, capable of programmable QAM format generation without the use of DACs and linear drivers. Operated together with a flexible MUX/DEMUX based on fabricated MZI-assisted MR filters, support for aggregation/slicing of DWDM superchannels in a flexible grid environment is enabled.

ACKNOWLEDGEMENTS

This work has been supported by EC FP7 project ICT-SPIRIT.

REFERENCES

- [1] ITU-T Recommendation G.694.1: Spectral grids for WDM applications: DWDM frequency grid (2012)
- [2] "Super-Channels: DWDM Transmission at 100Gb/s and Beyond," Infinera White Paper
- [3] Y. Ehrlichman et al., "A Method for Generating Arbitrary Optical Signal Constellations Using Direct Digital Drive," J. Lightw. Technol., Vol. 29, No. 17, September 2011
- [4] I. Lazarou et al., "Bandwidth and Wavelength-Selective MUX/DEMUX Microresonator Elements for Flexible-Grid Applications," to be presented at Advanced Photonics Conference, Boston, USA, July 2015