Numerical and Experimental Study of III-V on SOI Microdisk Lasers with p-i-n Junction

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Continuous wave lasing has been demonstrated in electrically driven InP-based microdisk lasers coupled to an underlying sub-micron silicon wire waveguide, fabricated through heterogeneous integration of InP on silicon-on-insulator (SOI)[1]. A tunnel junction was incorporated in the epitaxy to efficiently contact the p-side of the p-n junction. Our approach focuses on a similarly heterogeneously integrated structure where the tunnel junction has been replaced by a p-type InP top contact layer, which makes the epitaxy easier to grow. We have performed a numerical analysis of the electrical and optical properties of this new microdisk laser, and we have developed a process to reduce the optical losses induced by the p-type top contact layer. Samples demonstrate so far good electrical injection, and further lasing characterization will be investigated on a new set of processed samples.

Introduction

The silicon-on-insulator (SOI) material platform, with its high refractive index contrast, makes it possible to fabricate very compact passive optical waveguide circuits. Heterogeneously integrating III-V on the SOI platform provides dense, large-scale integration of high speed, low-power and compact active devices. Continuous-wave operation of compact, electrically pumped microdisk lasers with diameters as small as 5µm has been demonstrated[1]. These microdisk structures support whispering-gallery modes (WGMs) that enable ultracompact and low-threshold laser operation. The resonant modes propagate at the edge of the disk without the need for a guiding structure.

The III-V membrane used to fabricate these microdisk lasers includes a tunnel junction for a low loss p-contact. This tunnel junction requires a heavy development process at the epitaxial level : achieving an abrupt transition between the heavily p-doped region and the heavily n-doped region makes the growth of this epitaxy a real challenge. The doping of the layers also induces optical losses at the edge of the microdisk where the mode propagates.[2]

The alternative lies in processing microdisks in a p-i-n junction epitaxial stack, easier to grow, and where a heavily p-doped region replaces the tunnel junction. The whole challenge is then to reduce the optical losses induced by this p-type top contact, without jeopardizing the optical confinement of the mode and the electrical characteristics of the device.

Device design

The diameter of the considered microdisks is 10µm. The devices are bonded on top of an SOI circuit. The optical confinement is provided by the InP-membrane structure. The emitted light from the active regions is evanescently coupled to two underlying waveguides that are ended on both sides by fiber grating couplers. A schematic 3D view of the microdisk is depicted in Figure 1.

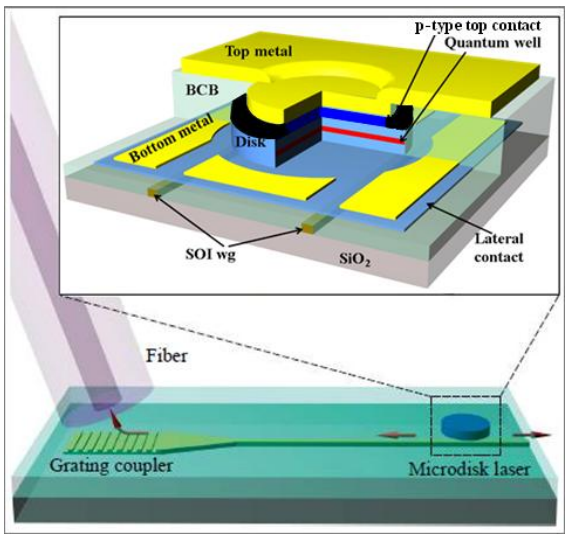

Figure 1: Schematic structure of the circuit (only one waveguide and a grating coupler on one side are depicted on the SOI) and the microdisk laser etched at its edge (in black)

The III-V membrane has a total thickness of 1.075µm and includes 3 compressively strained InGaAs quantum wells that provide the TE mode gain. The bottom contact consists in heavily Si-doped InP layers, and the top contact is made of heavily Zn-doped InP layers and a heavily Zn-doped InGaAs layer on which the metallic contact is deposited. As mentioned before, it is important to reduce the optical losses induced by the heavily doped p-type top contact. This can be performed by etching the microdisk on its edge, as indicated on Figure 1. However, optical simulations have to be performed to quantify the impact of such etching process on light confinement. Also, the simulations must demonstrate an efficient electrical injection in the devices.

Optical and electrical simulations

The simulations using ATLAS-Silvaco consider half of a 7.5µm disk embedded in silica, and rely on the cylindrical symmetry and mesh available in the module. Six designs have been considered in total, but we will focus on the best options as shown on Figure 2. Design A is the reference structure. For this implementation, the lower part of the structure consists of a 335nm-thick n-doped InP bottom contact layer. In addition, this design has no etching at its edge. In design B, the bottom contact consists of 335nm-thick n-doped InP layers and the structure is etched for 250nm at its edge. The simulation parameters are optimized to obtain a reliable band diagram of the complete epitaxial stack. Regarding optical losses, an imaginary refractive index has been considered to simulate the losses induced by the top metal contact (Au) and by the heavily doped p-type and n-type layers.[3]

As can be seen on Figure 2, the fundamental mode is confined at the edge of the disk and overlaps well with the quantum wells, even in the structure with the etching on the side. The mode is pushed down as the side etching depth increases. We demonstrate a much better mode confinement, with better overlap of the mode and the quantum wells. The light confinement of the fundamental mode is 27% higher in the etched structure than in the reference one. The two structures demonstrate the same electrical I-V characteristic, with a threshold voltage of 0.85V. Etching the structure results in higher hole concentration, i.e. larger radiative recombination rate, in the quantum wells.

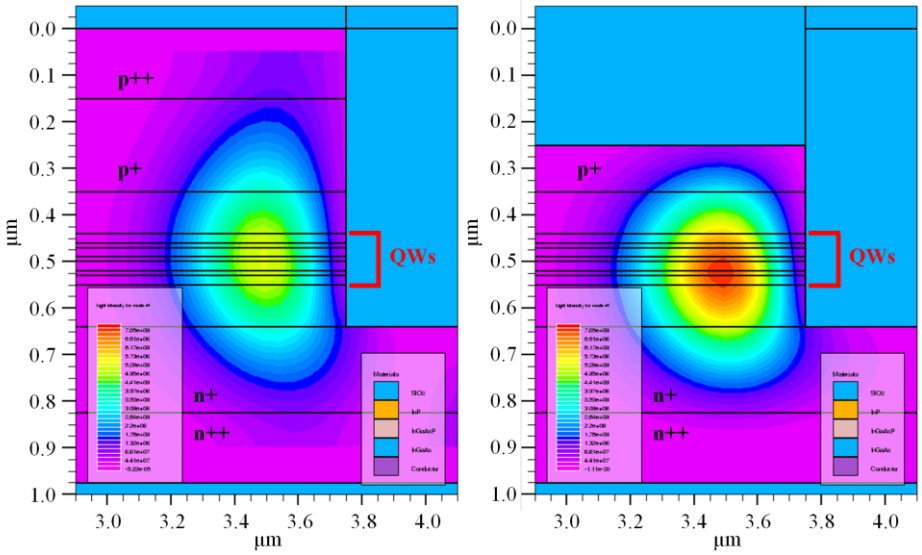

Figure 2 : Improvement of the fundamental mode confinement in design B (right) compared to the reference design A (left)

In conclusion, the best simulated structure is obtained when 250nm is etched at the edge of the microdisk. There is no significant electrical difference in simulation between a thin and a thick bottom contact. However, the mode in the structure with a thick bottom contact expands more in the layer, which will make the evanescent coupling to the underlying waveguides more efficient. In addition, from a thermal point of view, a thicker bottom contact allows a more efficient heat distribution in the disk.

Device fabrication

The SOI circuit, consisting of 500nm wide and 220nm high straight silicon waveguides on top of a 2µm buried oxide, is fabricated with 193nm DUV lithography through the ePIXfab silicon photonic platform. After etching the sacrificial layers, a thin silica layer (100nm) is deposited on top of the epitaxial stack. The unpatterned III-V die is attached to the SOI using adhesive die-to-wafer bonding with a DVS-BCB (divinylsiloxane-benzocyclobutene) polymer bonding agent. After removing the InP substrate, a pattern of 7.5µm diameter top contact Ti layer is lifted-off with a negative contact lithography. The III-V is etched down in the ICP using the Ti pattern as a mask. The total etching depth coincides with the value which provided the best results in the simulations (350nm total etching depth). The etching process has been optimized to reduce the micro-masking due to the sputtering of the Ti layer. After depositing a 300nm-thick SiN_x layer, a pattern of 10µm diameter disks is defined with contact lithography on top of the previously etched structures in order to align the disks with respect to the underlying straight waveguides. The III-V layers are etched by inductively coupled

plasma-reactive ion etching (ICP-RIE) until the thin bottom contact layer is reached (n-doped InP layer). The bottom contact is deposited on a slab around the disk without inducing optical losses and consists of titanium/platinum/gold layers. To isolate one disk from another, the InP contact layer is then removed on unwanted areas. The whole structure is then covered with BCB in order to isolate the optical waveguides from the absorptive metal contacts. Via's are opened in the BCB to reach the bottom contact and to open the top of the disks. The top contact is then deposited using evaporation on the center of the microdisks. The gold layer is 800nm thick and acts as a heat sink as it improves heat-dissipation under continuous-wave bias. Contact recipes and thicknesses have been extracted beforehand from Transmission Line Measurements results.

Characterization

Electrical pumping is performed by biasing the microdisk structure with two DC probes. Figure 3 shows the I-V characteristic of the device. The measured threshold voltage is comparable to the simulation results, at 0.8V.

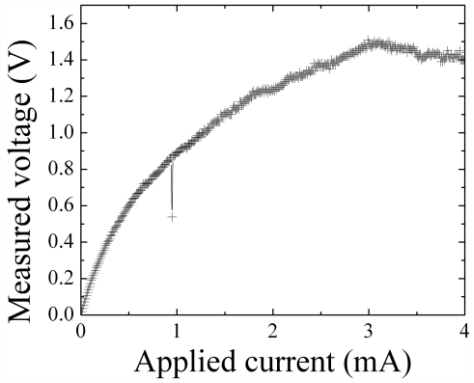

Figure 3 : I-V characteristic of a processed 10um diameter p-i-n microdisk

Lasing has not been observed on this sample. When performing transmission measurements in the waveguide through the grating couplers, no resonant cavity can be characterized. This can be due to the design of the SOI that leads to weak coupling efficiency between the waveguide and the microdisk, but also to the roughness of the microdisk sidewall after ICP etching.

Conclusion

P-i-n junction-based microdisk structures are a good alternative to the tunnel junction devices fabricated so far. A process has been developed to reduce the optical losses induced by the heavily doped p-type top contact. Simulations conclude that the electrical characteristics and the confinement of the optical mode are improved when etching the edge of the microdisk. Further processing will be performed, for which the SOI design as well as the etching quality have been optimized.

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